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Impact of Slim DC Capacitance on Floating Capacitor H-bridge Motor Drive

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Abstract—This paper discusses the impact of small DC capacitance in a motor drive using a floating capacitor H-bridge topology. Special attention is paid on investigating the 2nd order DC capacitor voltage ripples, whose influence on the induction motor as well as on the motor drive itself is of importance. This issue is addressed in this paper through rigorous mathematical formulations. It is found that by inverting 2nd order DC ripple voltage using conventional SVPWM, no harmful harmonics will be generated in the motor line voltage. This demonstrates the possibility of drastically reducing the DC capacitance of the proposed system. Induction motor as well as H-bridge performance with respect to different DC capacitance is demonstrated by experiments, which lays the foundation for cost reduction and reliability enhancement of the proposed system.

Index Terms—Floating capacitor; H-bridge; induction motor; series compensation; voltage ripple

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I. INTRODUCTION

Direct-on-line start of an induction motor usually results in a high inrush current and a large starting torque, which has a negative impact on the motor itself as well as on the electrical power system feeding the motor. Internally, large inrush current induces large magnetic forces in the stator windings to force the windings to move and distort [1]; the power dissipation associated with high levels of inrush current can produce a rapid temperature rise and may damage the winding insulation [1]. Externally, the inrush current may cause the local grid voltage to dip and circuit breakers to trip [2]. On the other hand, induction motors require also reactive power to establish a magnetic field; therefore, its input power factor is in the lagging area. In fact, induction motors are the prime contributor to the total reactive power demand of any given power system [3]. In order to reduce the start-up impact of induction motors, a number of techniques has been developed, which can be grouped as: a) electromechanical [4], b) solid-state [5]-[6], c) Variable Frequency Drive (VFD) [7]-[8], and as recently introduced d) series voltage injection topology[9]-[11].

For serial voltage injection topology [9]-[11], a power electronics device called “Magnetic Energy Recover Switch” (MERS) was proposed, in which the magnetic energy stored in the inductive load can be restored. The topology of MERS consists of four forced commutated switches and a small DC capacitor [12]. The configuration of MERS is similar to that of a single-phase full bridge, but MERS is connected in series between grid and load. Hence, different control techniques are applied. For the MERS, the capacitor is not connected to a DC power supply, which means the capacitor voltage is allowed to change dynamically and even to become zero. Therefore, the size of the capacitor is several times smaller [13]. By injecting a voltage in series with the grid voltage, induction motor voltage can be controlled in order to achieve soft start and a leading power factor operation for induction motor becomes possible.

The inherent characteristics of MERS is the use of low switching frequency where the semi-conductor switches turn ON and OFF only once in a cycle at 50/60 Hz supply frequency. However, due to its low

switching frequency, the AC voltage supplied to the motor contains low order harmonics. The self-excited AC harmonic current introduced by MERS generates torque which has different synchronous speed and therefore, may work as a braking torque [14]-[17]. This torque can cause oscillations or prevent increasing the motor speed to the rated value. The closed-loop control was found to be useful to damp out such oscillations, but it cannot be completely avoided [9]-[10].

In order to provide a more stable soft start solution, [18]-[21] present a floating capacitor H-bridge that can also provide soft start and VAR compensation, as it is shown in Fig. 1.It should be noted that the physical installation point of the proposed motor drive should be as close to motor as possible so that reflected wave phenomenon from motor cable influence can be minimized.

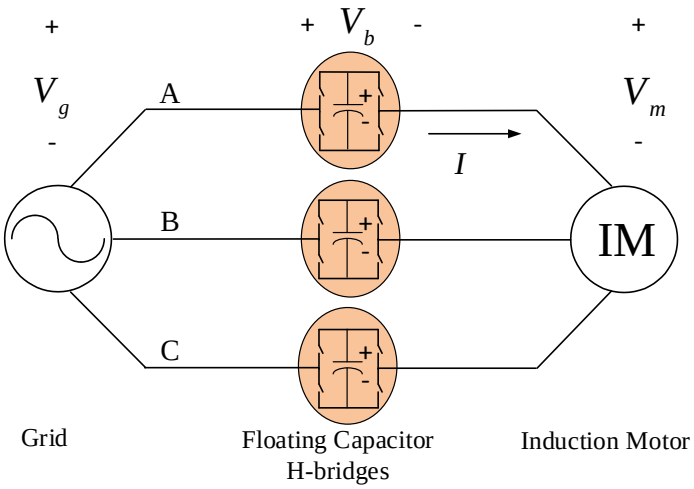


Fig. 1. Floating capacitor H-bridge induction motor drive.

The main difference between the MERS and the floating capacitor H-bridge shown in Fig. 1 is that the latter one uses SVPWM, which means the switching frequency is much higher than that of the MERS. As a result, only fundamental AC voltage component plus high-order AC harmonics around the switching frequency is injected between the grid and motor. The later ones can easily be filtered out by induction motor. Therefore, self-excited low-order AC harmonic current in the motor can be avoided, which greatly improves the system stability.

It should be noted that for the proposed topology in Fig. 1, each phase is subject to power pulsations at twice the grid fundamental frequency. To buffer the energy variations, energy storage element such as DC capacitors were used. For a 5 HP (3.725 kW) induction motor, the reported DC capacitors used in DC-link are electrolyte capacitors with a capacitance of 8 mF per phase [18]-[21]. This capacitance value is much larger than that of typical DC capacitor used in a conventional Variable Frequency Drive (VFD). The large electrolytic capacitor bank poses a lot of issues: a) high cost of large DC capacitors; b) electrolytic capacitor has relatively high equivalent series resistance (ESR), low ripple current ratings, and wear out issue due to the evaporation of electrolyte [22]-[24]. In fact, it has been pointed out in [25] that the nominal lifetime of electrolytic capacitors is not long enough for most applications; c) high cost on cell protection due to large energy that is dissipated in the event of dc-link shoot-through; d) significant weight and volume of the converter, which can make it difficult to build a high power density power electronic system [26].

Therefore, it is desirable that the capacitance of the DC capacitors be reduced for the proposed floating capacitor H-bridge system. In this paper, the impact of such DC capacitance reduction is investigated. It turns out that the 2^{nd} order DC voltage ripple does not introduce problematic harmonics in the motor current. This is because for capacitive mode of operation, the ripple waveform has the same phase-angle as the absolute value of output voltage. Although for inductive mode, such phenomenon is not true, but this condition does not occur in floating capacitor H-bridge motor drive because the proposed system always operates with a leading power factor [20]-[21].

In fact, a similar method has been utilized before for use in a Cascaded H-bridge (CHB) multilevel inverters where low DC capacitance values can be used [27]-[29]. While the conclusions are similar, the application is totally different. For the CHB systems [27]-[29], the DC capacitor voltages are regulated. However, for the proposed system shown in Fig. 1, the DC capacitor voltages are free-floating. Since no control is needed for floating DC capacitor voltage, there is no necessity for analytic filtering scheme [27]. In addition, for the proposed system shown in Fig. 1, the system is assumed to be balanced. Therefore, the

2nd order DC capacitor ripples can be easily filtered out by averaging the three capacitor voltages. Thus, no DC-link variation feed-forward compensation [28]-[29] is needed. All of these features make the proposed control algorithm very easy to be implemented.

Allowing larger DC capacitor voltage variations implies also the use of significantly lower DC capacitance values. Thus, the electrolytic capacitors can be easily replaced with Metalized Polypropylene Film (MPPF) capacitor, which has much longer life time [30]-[33]. In addition, this paper finds that when the 2nd order ripple fluctuates, the equivalent modulation index for H-bridge is boosted. Such phenomenon will be taken into account in the control algorithm so that a more accurate motor voltage control can be achieved. It should be noted that for unbalanced grid condition (e.g. in an isolated micro grid), the modulation strategy proposed in this paper will no longer be valid, mainly because: a) the presence of negative sequence component will degrade the performance of PLL used in this paper; b) the 2nd order DC ripple may not cancel each other under unbalanced condition. The method to overcome this issue is out of the scope of this paper.

This paper is organized as follows. In Section II, the basic information on motor terminal voltage control is presented. In Section III, 2nd order DC voltage ripple is modeled, which serves as the foundation for the mathematical analysis in Section IV. Section V gives details of the laboratory setup. Then, hardware experimental results are given in Section VI. Finally, conclusions are drawn in Section VII.

II. MOTOR TERMINAL VOLTAGE CONTROL

The motor terminal voltage control strategy of the proposed system can be illustrated using a voltage vector diagram representing one phase of the motor, as shown in Fig. 2.

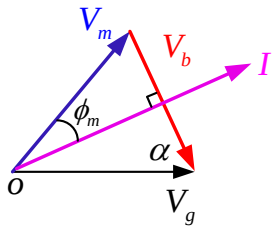


Fig. 2. Voltage vector diagram for an induction motor.

Fig. 2 is based on rotating frame using d-q transformation. V_g represents grid voltage vector, which is tracked by a Phase Locked Loop (PLL) and aligned with the d-axis. V_b represents a serial AC voltage injected by H-bridge and V_m represents the motor terminal voltage. It can be seen that by manipulating angle alpha (the angle between grid voltage vector V_g and bridge voltage vector V_b), magnitude of motor terminal voltage V_m can be changed accordingly [19]-[21].

A. Alpha Angle Control

The block diagram for alpha angle control is shown in Fig. 3.

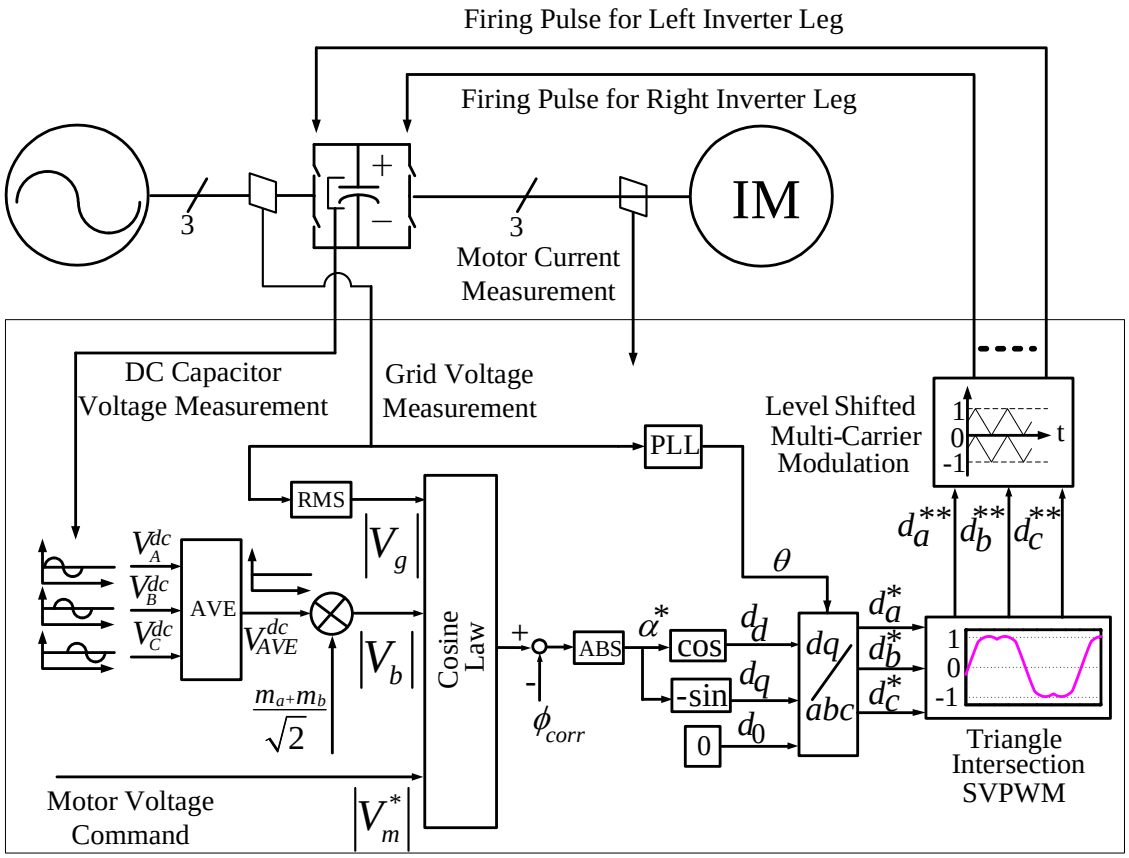


Fig. 3. Block diagram for alpha angle control.

Compared with the previously proposed control method in [19]-[21], the main difference in this paper is that drastic DC capacitance reduction will results in 2nd order DC voltage ripple. As a result, instead of constant modulation index for the H-bridge (m_a represents the constant modulation index in [19]-[21]),

the equivalent modulation index of the H-bridge is boosted in this paper (m_a+m_b represents the equivalent modulation index). This phenomenon will be taken into account in the control loop so that more accurate motor terminal voltage control can be achieved.

Assume that the grid is balanced and the 2nd order voltage ripples are also balanced. In Fig. 3, it can be seen that taking the average of three DC capacitor voltages will eliminate the 2nd order ripple component, leaving only the DC offset value as:

$$V_{AVE}^{dc} = \frac{V_A^{dc} + V_B^{dc} + V_C^{dc}}{3} \tag{1}$$

$|V_b|$in Fig. 3 is the Root-Mean-Square (RMS) for fundamental AC voltage injected by H-bridge (m_a represents the constant modulation index of the SVPWM, while m_b represents the modulation index boost caused by DC voltage ripple, which will be explained later in this paper):

$$|V_b| = \frac{V_{AVE}^{dc} \cdot (m_a + m_b)}{\sqrt{2}} \tag{2}$$

The angle α can be set by the controller, using the vector relationships shown in Fig. 2, to supply the motor at a specific desired operating voltage$|V_m^*|$such that:

$$\cos\alpha^* = \frac{|V_g|^2 + |V_b|^2 - |V_m^*|^2}{2 \cdot |V_g| \cdot |V_b|} \tag{3}$$

where $|V_g|$ represents the measured RMS of the grid phase voltage.

In Fig. 3, the reference signal for $\alpha^*$is derived from (3). A phase correction signal ϕ_{corr} is used to take into account various signal phase delays, like SVPWM signal generation delays [20]-[21]. A PLL is used to track the grid voltage angle (θ), which is used to perform the inverse Park transformation. The SVPWM modulation method uses the zero-sequence signal injection to increase the modulation index [34]-[36]. The theoretical upper limit for m_a using zero-sequence injection is 1.1547. In this work, m_a is set to be slightly lower (m_a =1.1 in this work for minimum pulse width considerations, as will be explained in the next section. For equivalent modulation index (m_a+m_b), it can be quantified, as it will be shown in Section IV. In order to generate a perfect five-level PWM line voltage waveform, the level-shifted multi-carrier waves [37] are used to generate the firing pulses for the H-bridges.

B. Minimum Pulse Width Consideration

Carrier-based PWM methods employ the "per-carrier cycle volt-second balance" principle. A modulation wave is compared with a triangular carrier wave and the intersections define the switching instants. Using zero-sequence signal injection, the peak of original modulation wave get dampened, allowing higher modulation wave to be fitted into the envelop of carrier waveform. In this way, modulation index can be increased from 1.0 to 1.1547. Should m_a=1.1547 be chosen, the peak of modulation wave will have the same magnitude as the peak of carrier wave. This means in the regions where modulation wave are near the tip of carrier waves, the PWM firing pulses will be very short. If short PWM firing pules are less than dead time and IGBT turn ON/OFF time combined, this will result in missing IGBT output. In other words, IGBT is not switching despite its firing pulse is provided simply because the pulse is too short. For the IGBT modules used in this paper (SEMiX202GB12E4s), the adaptor board (Board 2s SKYPER 32PRO R) has a dead time of 2.2 uS. Also, the turn ON and turn OFF time of IGBT is tuned at 0.4 uS and 0.7 uS, respectively. Therefore, theoretically for IGBT to respond, the duration of its firing pulse should not be less than 3.3 uS. Considering the fact that carrier period is 133 uS (7.5 kHz switching frequency, as can be seen in Section V), this means the peak of modulation wave should be no more than 95% of carrier envelop ($1-\frac{3.3}{133/2}=0.95$) to avoid generating pulses that are too short for IGBT to respond. Therefore, m_a=1.1547x0.95=1.1 is chosen for minimum pulse width considerations.

III. DC RIPPLE VOLTAGE MODELING

To quantify the DC voltage ripple, a rigorous energy analysis is carried out in this section. Assuming a balanced system with 50 Hz grid frequency, the instantaneous power flow from/to the H-bridge in phase A can be expressed as:

$$P_A = -|V_b| \cdot I_m \cdot \sin(200 \cdot \pi \cdot t) \tag{4}$$

where $|V_b|$represents the RMS for AC voltage injected by H-bridge, I_m represents the RMS for motor current. Equation (4) implies that: a) the instantaneous power flow from/to the H-bridge is fluctuating at

twice the grid frequency; b) neglecting losses in IGBT and capacitors, the average net power to the H-bridge is zero. For the proposed H-bridge topology, the DC capacitor is not connected to DC power supply and thus free floating. This means the only element that can absorb/release such fluctuating energy is the DC capacitor. Due to this fluctuating power flow, the DC capacitor is constantly being charged and discharged, causing a 2nd order DC ripple voltage, as shown in Fig. 4.

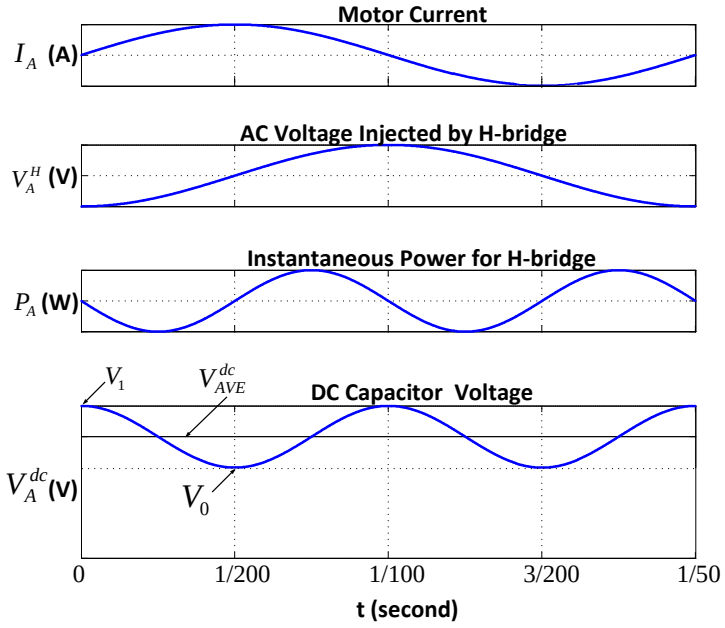


Fig. 4.Waveform of different parameters for the H-bridge system.

To quantify the magnitude of DC ripple voltage, the energy removed from the DC capacitor during the discharging period (the first ¼ cycle in Fig. 4) can be calculated as:

$$W_{discharge} = \int_0^{\frac{1}{200}} P_A \cdot dt = -\frac{|V_b| \cdot I_m}{100 \cdot \pi} \tag{5}$$

On the other hand, the energy removed from the DC capacitor during the discharging period (the first ¼ cycle in Fig. 4) can also be calculated by the voltage difference between the initial and final voltage as:

$$W_{discharge} = \frac{1}{2}\left(V_0^2 - V_1^2\right) \cdot C = -\frac{1}{2} \cdot \left(V_1 + V_0\right) \cdot \left(V_1 - V_0\right) \cdot C = -V_{AVE}^{dc} \cdot \Delta V \cdot C \tag{6}$$

where *C* represents the capacitance of DC capacitor. Combining equations (2), (5) and (6), the magnitude of DC ripple can be obtained as:

$$\Delta V = V_1 - V_0 = \frac{I_m \cdot (m_a + m_b)}{100 \cdot \sqrt{2} \cdot \pi \cdot C} \tag{7}$$

Equation (7) shows that the magnitude of the DC ripple is generally proportional to motor current and inversely proportional to the capacitance of DC capacitor. Since the motor current is determined by the motor load condition, the only factor that can reduce the DC ripple is to increase the capacitance of the DC capacitor. However, such approach requires a very large capacitance value and it is not practical. In this paper, another approach is taken and it will be shown in the next section.

IV. IMPACT OF DC RIPPLE

This section systematically explores the impact of DC ripple. First, the AC voltage injected by H-bridge in each phase is modeled in time domain (phase A and B, respectively). Then, the line voltage is revealed by calculating the difference between the two phases. Following that, IGBT voltage stress caused by ripple is discussed and ripple current of capacitor is calculated. Finally, a way to estimate the minimum DC capacitance value for the H-bridge system is proposed.

A. H-bridge Phase Voltage

From Fig. 4, it is obvious that the voltage ripple is lagging the instantaneous power by 90 degree. Therefore, in the time domain, the DC capacitor voltage in phase A of the H-bridge system can be modeled as

$$V_A^{dc} = V_{AVE}^{dc} - \frac{\Delta V}{2} \cdot \sin(200 \cdot \pi \cdot t - \frac{\pi}{2}) \tag{8}$$

If the H-bridge is injecting AC voltage using conventional SVPWM (m_a fixed, no DC link variation feedforward compensation used), the RMS of fundamental AC voltage injected by H-bridge in phase A can be modeled as:

$$V_A^{RMS} = \frac{m_a}{\sqrt{2}} \cdot V_{AVE}^{dc} - \frac{I_m \cdot m_a \cdot (m_a + m_b)}{400 \cdot \pi \cdot C} \cdot \sin(200 \cdot \pi \cdot t - \frac{\pi}{2}) \tag{9}$$

From Fig. 4 it can also be seen that the H-bridge AC voltage is 90 degree lagging the motor current. Therefore, the voltage injected by the H-bridge in time domain can be expressed as

$$V_A^H = V_A^{RMS} \cdot \sin(100 \cdot \pi \cdot t - \frac{\pi}{2}) \tag{10}$$

Combine equation (9) with (10), after simplification, the AC voltage injected by H-bridge in the time domain can be expressed as

$$V_A^H = -(\frac{m_a}{\sqrt{2}} \cdot V_{AVE}^{dc} + \frac{I_m \cdot m_a \cdot (m_a + m_b)}{800 \cdot \pi \cdot C}) \cdot \cos(100 \cdot \pi \cdot t) - \frac{I_m \cdot m_a \cdot (m_a + m_b)}{800 \cdot \pi \cdot C} \cdot \cos(300 \cdot \pi \cdot t) \tag{11}$$

From equation (11), it can be seen that the DC ripple in capacitor voltage actually introduces a third harmonic component to the voltage injected by H-bridge. This phenomenon is because multiplications of the harmonic components in the time domain are the convolutions in the frequency domain. For example, when the 1st harmonic component is multiplied by 2nd harmonic component in the time domain, both 1st and 3rd harmonic component will be generated.

Taking into account the fact that in this paper, zero-sequence signal injection is used to increase the modulation index [34]-[36]. The modification of the modulating waveform requires the addition of one-sixth of the third harmonics [38]. This means besides the third harmonic component caused by DC voltage ripple, there should be an additional third harmonic component caused by the SVPWM. Interestingly, it is found that the two third harmonic components have an opposite phase angle, which means the third harmonic created by DC ripple voltage will cancel out part of the third harmonic component generated by SVPWM.

Therefore, the AC voltage injected by H-bridge in the time domain, which takes into account the DC ripple effect as well as the third harmonic injection effect from SVPWM should be expressed as:

$$V_A^H = -(\frac{m_a}{\sqrt{2}} \cdot V_{AVE}^{dc} + \frac{I_m \cdot m_a \cdot (m_a + m_b)}{800 \cdot \pi \cdot C}) \cdot \cos(100 \cdot \pi \cdot t) + (\frac{1}{6} \cdot \frac{m_a}{\sqrt{2}} \cdot V_{AVE}^{dc} - \frac{I_m \cdot m_a \cdot (m_a + m_b)}{800 \cdot \pi \cdot C}) \cdot \cos(300 \cdot \pi \cdot t) \tag{12}$$

B. H-bridge Line Voltage

Assuming a balanced system, the current and voltage in phase B of the system is lagging phase A by 120 degree. Using similar analysis for phase A, the AC voltage injected by the H-bridge in phase B is:

$$V_B^H = -(\frac{m_a}{\sqrt{2}} \cdot V_{AVE}^{dc} + \frac{I_m \cdot m_a \cdot (m_a + m_b)}{800 \cdot \pi \cdot C}) \cdot \cos(100 \cdot \pi \cdot t - \frac{2\pi}{3}) + (\frac{1}{6} \cdot \frac{m_a}{\sqrt{2}} \cdot V_{AVE}^{dc} - \frac{I_m \cdot m_a \cdot (m_a + m_b)}{800 \cdot \pi \cdot C}) \cdot \cos(300 \cdot \pi \cdot t) \quad (13)$$

Using equations (12) and (13), the line voltage produced by the H-bridges can be modeled as:

$$V_{AB}^H = V_A^H - V_B^H = \sqrt{3} \cdot \left(\frac{m_a \cdot V_{AVE}^{dc}}{\sqrt{2}} + \frac{I_m \cdot m_a \cdot (m_a + m_b)}{800 \cdot \pi \cdot C} \right) \cdot \sin(100 \cdot \pi \cdot t - \frac{\pi}{3}) \quad (14)$$

Since the proposed H-bridge motor drive system works on the principle of series voltage injection as shown in Figs. 1-2, the actual motor line voltage is the end result between grid line voltage and line voltage produced by H-bridges. Assuming grid line voltage is sinusoidal and free of low order harmonics. Equation (14) shows that if line voltage produced by H-bridge is also free of low order harmonics, then the motor line voltage will be free of low order harmonics as well.

C. Equivalent Modulation Index

By definition, the equivalent modulation index of the H-bridge under DC ripple condition is the ratio between the injected fundamental AC voltage RMS and average DC capacitor voltage. Therefore, the following equation holds:

$$m_a + m_b = \frac{\frac{m_a \cdot V_{AVE}^{dc}}{\sqrt{2}} + \frac{I_m \cdot m_a \cdot (m_a + m_b)}{800 \cdot \pi \cdot C}}{\frac{V_{AVE}^{dc}}{\sqrt{2}}} = \frac{m_a}{1 - \frac{\sqrt{2} \cdot I_m \cdot m_a}{800 \cdot \pi \cdot C \cdot V_{AVE}^{dc}}} \quad (15)$$

Equation (15) implies that if the DC voltage ripple cannot be neglected, the equivalent modulation index (m_a+m_b) for the H-bridge will be higher than the modulation index of the conventional SVPWM (m_a).

This phenomenon can be explained by the fact that conventional SVPWM method assumes a constant DC link voltage and manipulates only the width of the pulses over each cycle. For floating capacitor H-

bridge topology with a small DC capacitance, besides the SVPWM manipulating the width of the pulses, the magnitude of the pulses are also changed due to DC ripple (pulse magnitude is reduced at the beginning and the end of each half cycle, pulse magnitude boosted around center region for each half cycle, as can be seen in section VI).Thus, the combined factors (width modulation caused by SVPWM as well as magnitude modulation naturally caused by DC ripple) sometimes can push the equivalent modulation index (m_a+m_b) above the conventional 1.1547 limit without entering the nonlinear region.

Equation (15) will be used throughout this paper in many ways: It will combine with equation (2) to improve the motor voltage control accuracy, as it is shown in Fig. 3. It will combine with equation (7) to predict IGBT voltage stress and it will also combine with equation (22) to assess the capacitor ripple current magnitude. It should be noted that the equivalent modulation index cannot be amplified infinitely above 1.1547 as there is a theoretical upper limit for it, as will be shown in equation (21).

D. IGBT Voltage Stress

Since the DC capacitor voltage for the proposed topology are free-floating, the IGBT voltage stress needs to be characterized. Combining equation (12) with (15) and only consider fundamental component injected by H-bridge, following equation can be obtained:

$$\left(V_{AVE}^{dc}\right)^2 - \frac{\sqrt{2}\cdot|V_b|}{m_a}\cdot V_{AVE}^{dc} + \frac{|V_b|\cdot I_m}{400\cdot\pi\cdot C} = 0 \tag{16}$$

Solving equation (16) yields:

$$V_{AVE}^{dc} = \frac{|V_b|}{\sqrt{2}\cdot m_a} + \sqrt{\frac{|V_b|^2}{2\cdot\left(m_a\right)^2} - \frac{|V_b|\cdot I_m}{400\cdot\pi\cdot C}} \tag{17}$$

In the meanwhile, from Fig. 2, it can be seen that $|V_b|$can be expressed as:

$$|V_b| = V_m\cdot\sin(\phi_m) + \sqrt{V_g^2 - \left(V_m\cdot\cos(\phi_m)\right)^2} \tag{18}$$

where ϕ_m represents motor power factor angle [39]. Suppose V_g is constant and V_m can be maintained by H-bridges at the rated motor voltage, equation (17)-(18) shows that average DC capacitor voltage as a function of DC capacitance can be obtained as long as ϕ_m and I_m are known. This is not difficult because ϕ_m and I_m can be deduced from motor nameplate. Upon obtaining the value of average DC capacitor voltage, the value of equivalent modulation index of the H-bridge (m_a+m_b) is known. Then, the magnitude of the DC capacitor ripple can be obtained (see equation (7)). Finally, peak DC capacitor voltage for the proposed topology will be the average DC capacitor voltage plus one-half of DC ripple voltage magnitude as:

$$V_{peak} = V_{AVE}^{dc} + \frac{\Delta V}{2} \tag{19}$$

Equation (19) will be used to predict IGBT voltage stress.

E. Maximum Equivalent Modulation Index

Equation (15) shows the possibility of increasing the equivalent modulation index of H-bridge beyond the conventional 1.1547 limit. To estimate the maximum modulation index boost, the boundary condition for the modulation index m_a+m_b is investigated. From (17), it can be seen that the boundary condition is:

$$C_{bond} = \frac{I_m \cdot (m_a)^2}{200 \cdot \pi \cdot |V_b|} \qquad V_{AVE}^{dc} = \frac{|V_b|}{\sqrt{2} \cdot m_a} \tag{20}$$

Put equation (20) into (15), the boundary condition for m_a+m_b is found to be:

$$m_a + m_b = 2 \cdot m_a \tag{21}$$

which is exactly twice of the modulation index if an infinite DC capacitance is used. ($C = \infty$, $m_a + m_b \approx m_a$ as can be seen from (15)). This means although reducing DC capacitance can boost equivalent modulation index of H-bridge, such boost has an upper limit, which is 2.0 However, such value is only a theoretical limit because in practice, such value can never be achieved due to other constrains, as will be explained in later section.

F. Capacitor Ripple Current

Due to ESR in the capacitor, the maximum permitted ripple current is set by the manufacturer so that capacitor load life specification will not be compromised. From equation (7)-(8), the RMS ripple current of the floating capacitor can be derived as:

$$I_{ripple} = \frac{1}{\sqrt{2}} \cdot C \cdot \frac{dV_A^{dc}}{dt} = -\frac{I_m \cdot (m_a + m_b)}{2} \cdot \cos(200 \cdot \pi \cdot t - \frac{\pi}{2}) \tag{22}$$

From (22), it can be seen that capacitor ripple current is oscillating 100 Hz and it is proportional with the motor current. Taking into account the upper boundary for m_a+m_b, as it is shown in (21), the theoretical maximum ripple current RMS for the capacitor is found to be:

$$I_{ripple}^{\max} = I_m \cdot m_a \tag{23}$$

Equation (23) is the worst case scenario for capacitor ripple current and in reality; such value can never be reached. Equation (23) can be used in the design phase to select the correct DC capacitors.

G. Minimum DC Capacitance

The previous analysis shows that DC capacitance of the proposed system has a theoretical lower limit (equation (20)). It can be seen from equation (20) that the minimum DC capacitance is determined when the motor is running under extreme conditions, where I_m reaches its maximum value and magnitude of V_b reaches its minimum value. For I_m to reach its maximum value, this happens during the soft start phase, where the upper limit for the motor current is controlled around 3-4 p.u. for the proposed system [20]. For the magnitude of V_b to reach its minimum value, such condition happens under full load condition [21]. Combining these two factors, in practice, the minimum DC capacitance should be 3-4 times (k_a= 3-4) of the theoretical value as:

$$k_a \cdot \frac{I_m^{rated} \cdot \left(m_a\right)^2}{200 \cdot \pi \cdot \left|V_b\right|^{rated}} \le C \tag{24}$$

V. EXPERIMENTAL SETUP

A motor-dynamometer set was used as test platform to validate the theory proposed in this paper. The schematic for the test platform is shown in Fig. 5.

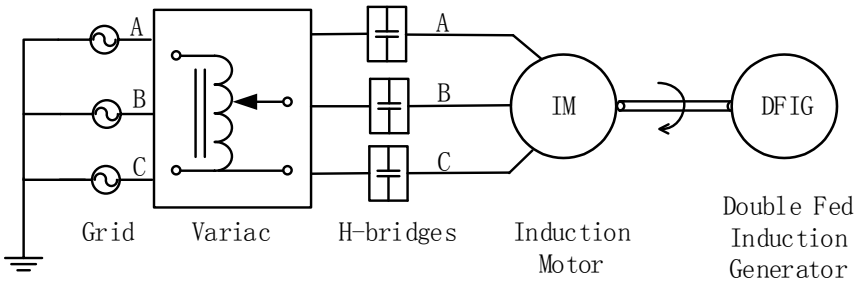
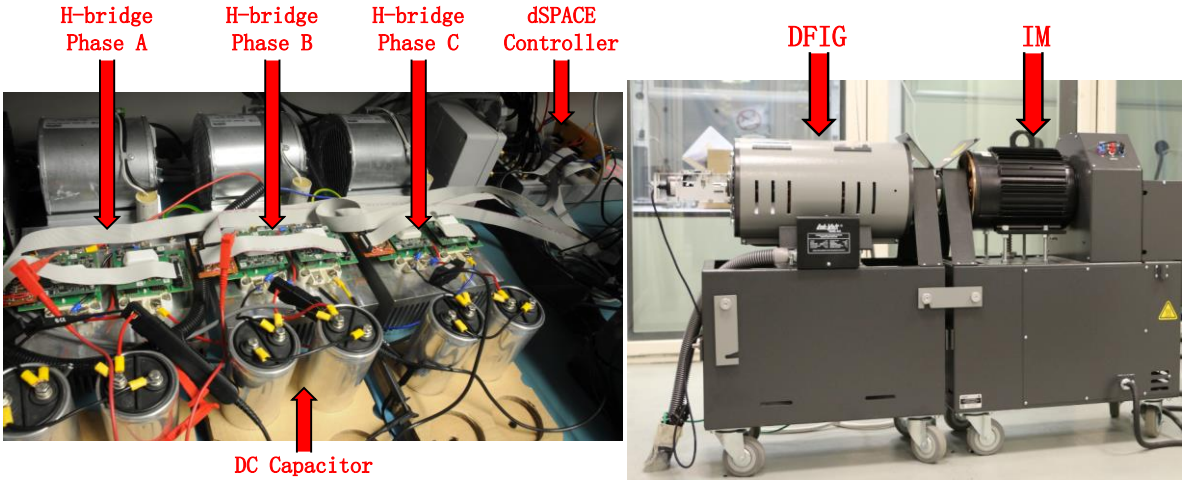


Fig. 5. Test platform for the H-bridge motor drive.

From Fig. 5, it can be seen that a variac is used to step down the 415V 50Hz grid voltage to 330V and feed it to the H-bridges. The reason behind such configuration is to see if under slim DC capacitance condition, the proposed system can still boost the motor voltage to its rated value [21] and the answer is positive. Three single-phase floating capacitor H-bridges are installed between the variac and the induction motor. A Double Fed Induction Generator (DFIG) is mechanically coupled with the induction motor as dynamometer to achieve a torque load. The experimental facility is shown in Fig. 6.



(a) (b)

Fig. 6 Experimental facility (a) floating capacitor H-bridges and controller (b) Induction motor with dynamometer

The control algorithm shown in Fig. 3 is implemented in a dSPACE DS1104 platform, with a sampling frequency of 7.5kHz and a switching frequency of 7.5 kHz. Each H-bridge is made up of two separate inverter legs using Semikron IGBT modules (SEMiX202GB12E4s). In total, six IGBT inverter modules are used (12 switches). The DC capacitors are Metalized Polypropylene Film Capacitors made by EPCOS (B25620-B0407-K881) with a capacitance of 400 uF each and a rated voltage of 880VDC. In order to investigate the performance of the proposed system under different DC capacitance values, five identical 400 uF capacitors are used in each phase. These capacitors can be connected in series, in parallel or in a mixed configuration (Fig. 6 (a) shows two DC capacitors connected in series, C=200uF). In this way, the range of equivalent DC capacitance per phase is between 2000 uF to 200 uF, which is equivalent to 33 p.u. to 3.3 p.u. with V_{base}=380V, S_{base}=2200/0.8=2750 VA. The reason for varying DC capacitance from 2000 uF to 200 uF is to see if the proposed topology can operate well under slim DC capacitance condition. If it does, this means instead of expensive, bulky, and unreliable electrolyte capacitor banks, cheaper, small, and reliable Metalized Polypropylene Film (MPPF) capacitors can be used for the proposed system, which greatly improves its competitiveness over other motor drive topologies.

The motor-dynamometer set shown in Fig. 6 (b) was previously used for wind energy research [40] but modified to accommodate research requirement for this paper. The main change is that the original Mitsubishi VFD is replaced with three H-bridges to drive the induction motor, as is shown in Fig. 5. The induction motor under test is a general purpose 4-pole 3 HP (2.2kW) 60Hz motor made by Marathon Electric. The nameplate states that rated voltage for the induction motor is 460V / 60 Hz with a full load current of 4.2 A. Taking into account the fact that the motor will be operating from a 50Hz grid, the rated motor voltage has been reduced to 380V to accommodate the V/f characteristics. The DFIG is a 4-pole 2 HP (1.5 kW) machine made by Lab-Volt. Loading of the DFIG is controlled by a dSPACE DS1103 controller so that a constant electromagnetic torque can be provided by the DFIG, independent of the shaft speed.

VI. EXPERIMENTAL RESULTS

The performance of the proposed floating capacitor H-bridge motor drive system under the influence of different DC capacitance values will be shown in this section. It should be noted that soft-start results are not provided in this paper mainly because soft-start control algorithm used in this paper is the same as the one used in reference [20]. Since reference [20] had already provided detailed waveforms showing transient state (from no load condition up to full load condition), the commonly-known results regarding soft start are not shown in this paper.

A. H-bridge Output Voltage

Fig.7 shows the motor current, H-bridge output voltage as well as capacitor voltage ripple in phase A under very small DC capacitance and full motor load condition (C = 200 uF, m_a=1.1, I_m=4.2A).

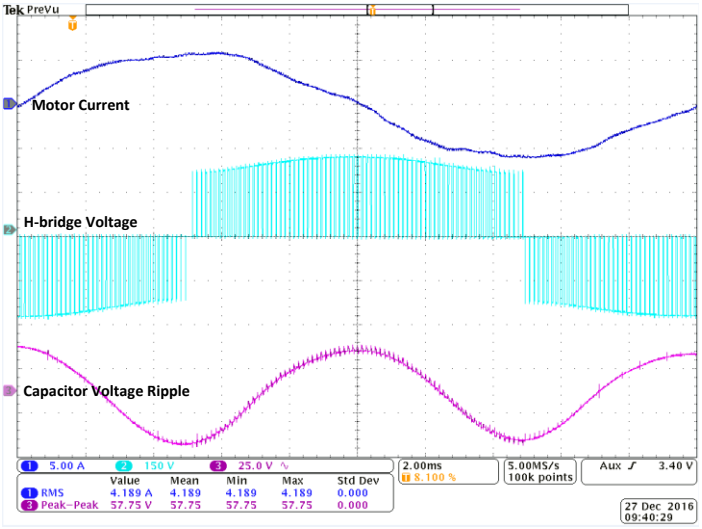


Fig. 7. H-bridge output voltage under very small DC capacitance and full motor load condition.

The first observation from Fig. 7 is that there is a hump for each half cycle of the H-bridge output voltage, which is different from what can be obtained from conventional SVPWM. It should also be noted that in Fig. 7, for the DC capacitor voltage measurement, the DC offset has been filtered out, leaving only AC component. In this way, the ripple can be more easily seen. It can be seen that the DC capacitor voltage ripple is oscillating at 100 Hz, which is twice the grid frequency (50 Hz). It can also be seen that despite large DC ripple (57.75V, peak to peak), the motor current remains sinusoidal. In addition, the voltage

injected by the H-bridge is about 90 degrees lagging the motor current, which means the average energy flowing in/out of the H-bridge per cycle is near zero. This explains why the capacitor voltages for the proposed system only oscillate but they do not collapse or increase to infinity under steady state. Comparing Fig. 4 with Fig. 7, it can be seen that the waveform obtained from experiment agrees very well with theoretical curves.

B. Capacitor Voltage Ripple

Fig. 8 shows three capacitor voltage ripples under very small DC capacitance and full motor load condition (C = 200 uF, m_a=1.1, I_m=4.2A).

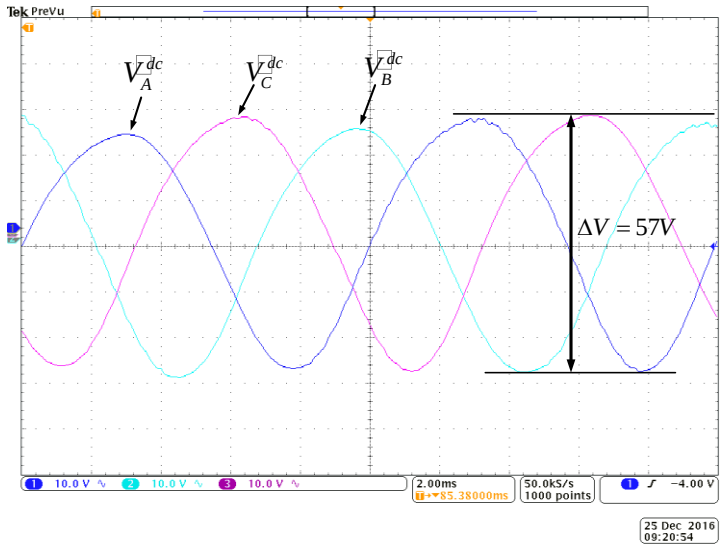


Fig. 8. Capacitor voltage ripples under very small DC capacitance and full motor load condition.

According to equation (7), under the condition shown in Fig. 8 (C=200uF, m_a=1.1, I_m=4.2A), the magnitude of the voltage ripple (peak to peak) should be 56.9V. It can be seen from Fig. 8 that actual voltage ripple amplitude is 57V, which perfectly matches the theory. It is worth noting that despites large ripple in the individual capacitor voltage (57V, peak to peak), such 2nd order ripples are well balanced, as is shown in Fig. 8. This means averaging three DC capacitor voltages can successfully filter out the 2nd order harmonic component, leaving only DC offset value, which is used in the control block diagram shown in Fig. 3. This explains why the proposed system can remain stable despite large oscillations in the DC link. It can also be observed from Fig. 8 that ripple voltages have a negative sequence. To further

prove the correctness of equation (7) which describes the ripple magnitude, Fig. 9 is plotted where the magnitude of DC ripple is recorded under various DC capacitance values. It should be noted that for Fig. 9, the induction motor is always running under full load condition.

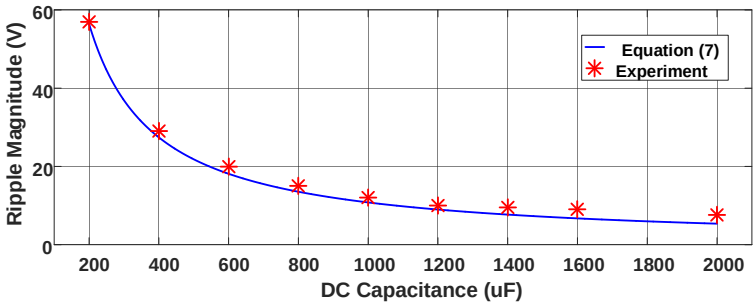


Fig. 9. Ripple magnitude versus DC capacitance under full motor load condition.

From Fig. 9, it can be seen that the experimental results matches the theory very well. Generally, the smaller the DC capacitance, the larger the ripple magnitude.

C. Third Harmonic Injection

In order to analyze the frequency spectrum, Fig. 10 is plotted where Fast Fourier Transform (FFT) is performed for H-bridge output voltage. The actual DC capacitor voltage (purple signal) and H-bridge output voltage (blue signal) are super-imposed in Fig. 10. It clearly explains that the hump for each half cycle of the H-bridge output voltage is indeed caused by the oscillating DC capacitor voltage.

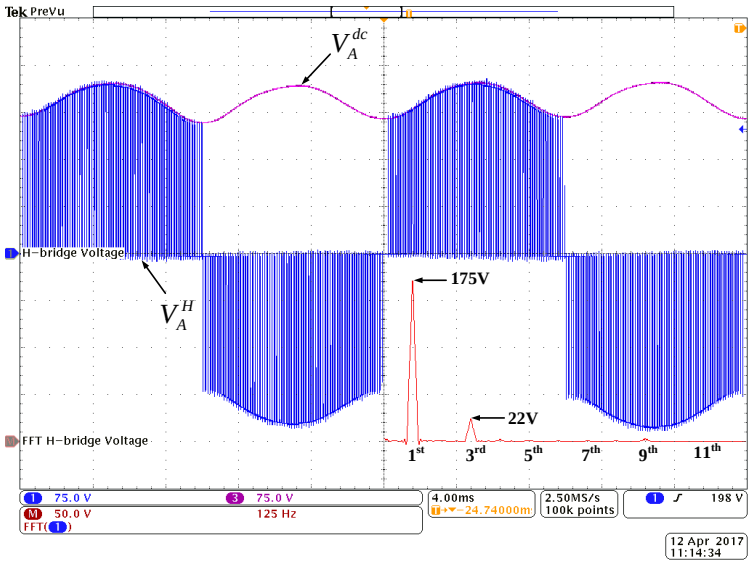


Fig. 10.FFT analysis for H-bridge output voltage under very small DC capacitance and full motor load condition.

Equation (12) shows that besides the fundamental component, only third harmonic component will be introduced to the H-bridge output voltage. This is confirmed in Fig. 10. It shows that besides the fundamental component (175V), only third harmonic component is present (22V). In fact, according to equation (12), under the conditions shown in Fig. 10 (C = 200 uF, m_a =1.1, I_m = 4.2 A), the magnitude of third harmonic should be around 22V, which perfectly matches the experiment result. To further prove the correctness of equation (12) describing the third harmonic injection, Fig. 11 shows the magnitude of the 3rd harmonic component under various DC capacitances. It should be noted that for Fig. 11, the induction motor is always running under full load condition.

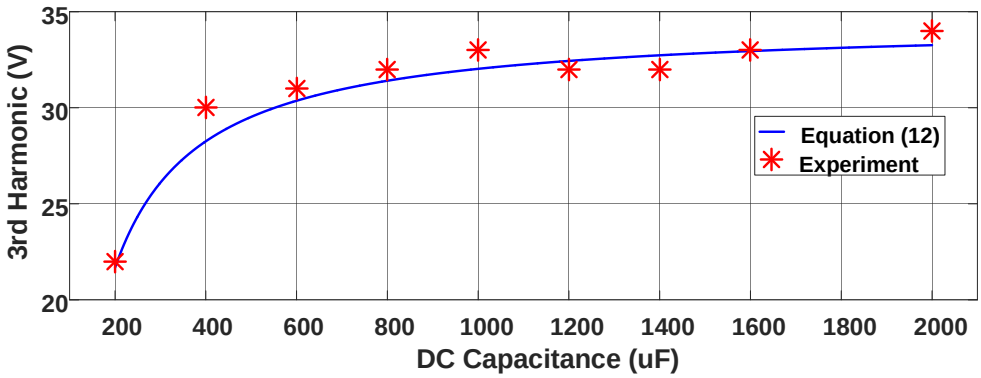


Fig. 11. Third harmonic magnitude versus DC capacitance under full motor load condition.

From Fig. 11 it can be seen that the experimental results matches theory well. Fig. 11 proves that the third harmonic component created by DC ripple voltage will cancel part of the third harmonic component generated by SVPWM, causing overall third harmonic component to dip under small DC capacitance regions.

D. Equivalent Modulation Index

According to equation (15), by measuring three DC capacitor voltages and motor current RMS, it is sufficient to estimate the equivalent modulation index for H-bridge. Fig. 12 is shows equivalent modulation index obtained from this method under very small DC capacitance and full motor load condition (C = 200 uF, m_a=1.1, I_m=4.2A).

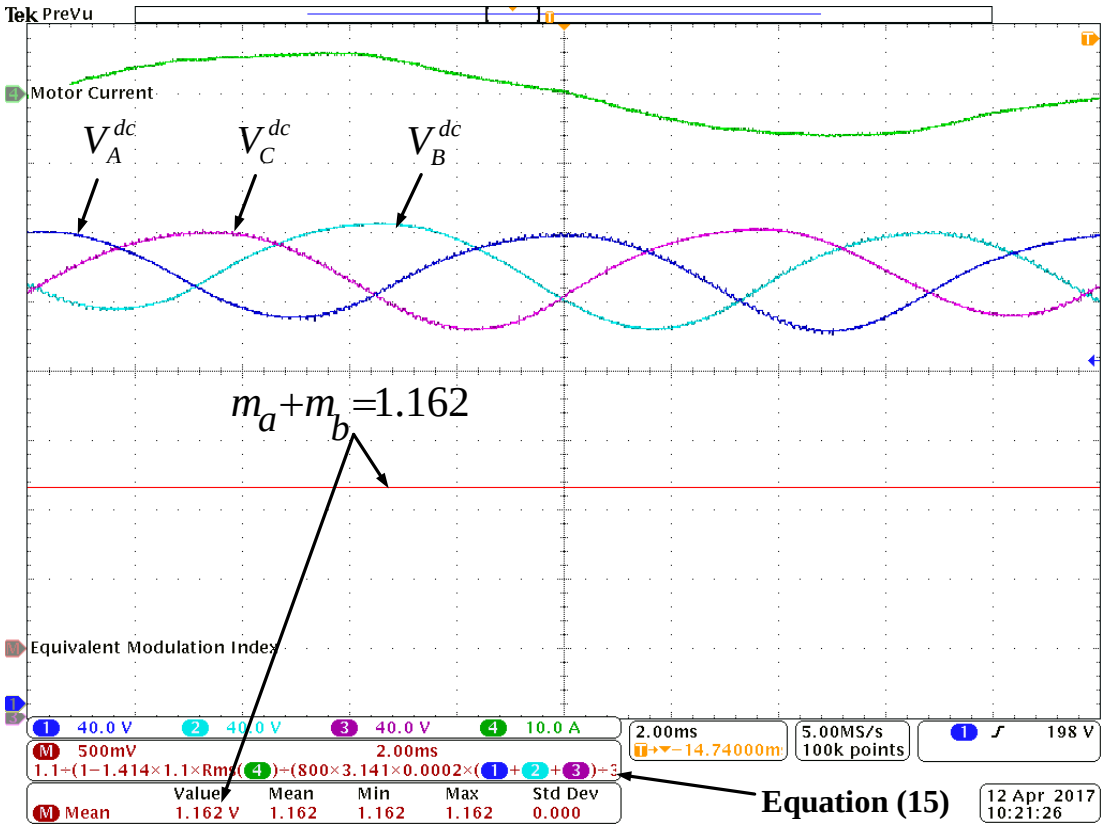


Fig. 12. Equivalent modulation index under very small DC capacitance and full motor load condition.

It is interesting to point out that the equivalent modulation index (m_a+m_b=1.162) has exceeded the upper limit of 1.1547 for the conventional SVPWM, as can be seen from Fig. 12. In the meanwhile, the DC/AC inversion is still in the linear region and the AC voltage injected by the H-bridge only contains the fundamental and third harmonic, as has been shown in Fig. 10. It is also worth noting that conventional SVPWM increases modulation index at the expense of more third harmonic injection. In contrast, modulation index boost caused by DC ripple voltage will cancel part of the third harmonic component generated by SVPWM, causing overall third harmonic injection to dip under small capacitance regions, as has been shown in Fig. 11.

Fig. 13 is plotted to further prove equation (15) describing the modulation index boost of H-bridge under ripple voltage condition. For Fig. 13, the induction motor is always running under full load condition.

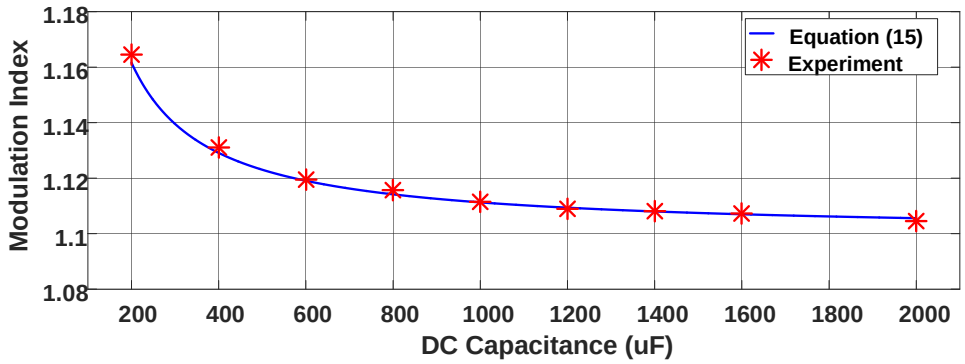


Fig. 13. Equivalent modulation index versus DC capacitance under full motor load condition.

From Fig. 13, it can be seen that the equivalent modulation index for H-bridge is always higher than the conventional modulation index used in SVPWM. For example, m_a is fixed at 1.1 for the SVPWM used in this paper. However, through experiments, it is found that m_a+m_b is always higher than 1.1. The additional boost is caused by 2nd order ripple voltage, as has been described in equation (15).

E. Motor Line Voltage

Fig. 14 shows an FFT analysis for motor line voltage under very small DC capacitance and full motor load condition (C = 200 uF, m_a=1.1, I_m=4.2A).

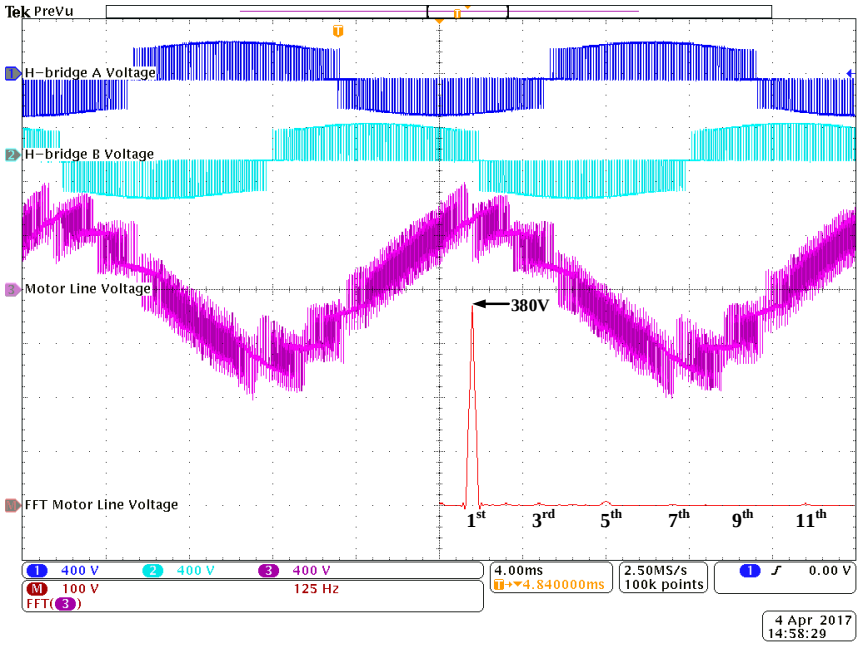
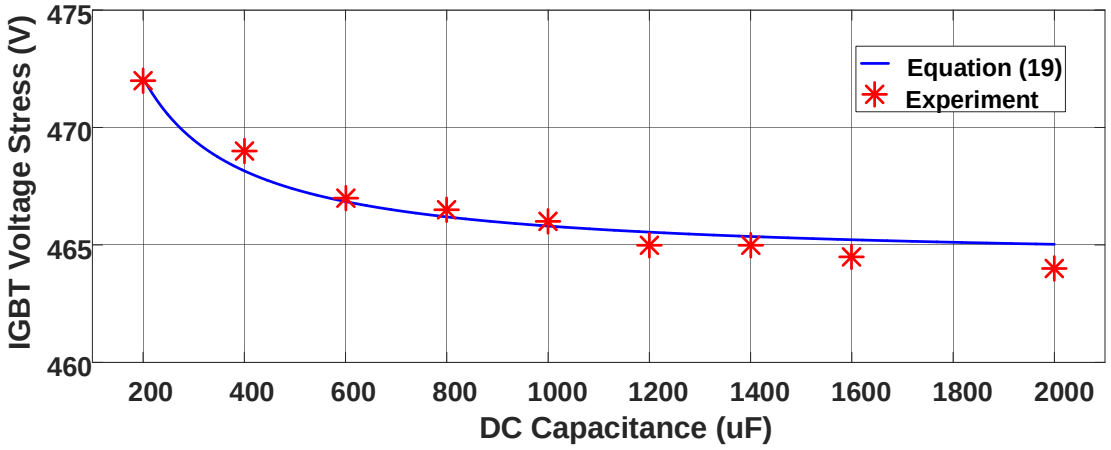


Fig. 14. FFT analysis for motor line voltage under very small DC capacitance and full motor load condition.

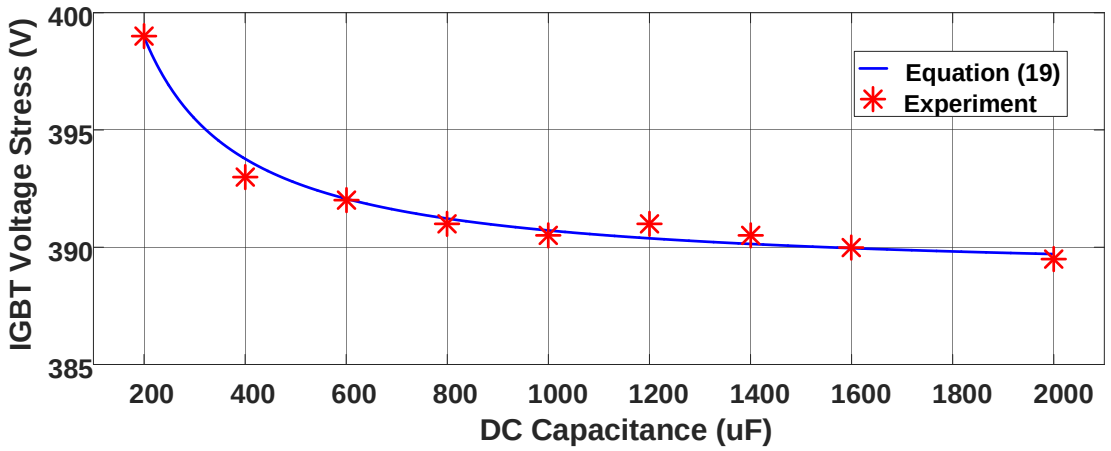
The proposed floating capacitor H-bridge motor drive system works on the principle of series voltage injection. Therefore, the motor line voltage results from grid line voltage (not shown in Fig. 14) and line voltage produced by H-bridges. It can be seen that the third harmonic no longer exist in motor line voltage, leaving only fundamental component, which agrees well with equation (14). From Fig. 14, it can be seen that the proposed system can supply five-level line PWM waveforms to the induction motor. In contrast, a VFD system supplies induction motor with three-level line PWM waveforms and much larger voltage steps. This is one of the disadvantages for VFD because the higher voltage step introduces higher dV/dt stresses on the insulation of the motor windings. Moreover, the 3-level line PWM output voltages from the VFD, using a higher DC link voltage, usually requires bulky 3/5 % reactors inserted between VFD and motor to mitigate reflected wave or standing wave phenomenon. However, such practice affects the ability of the induction motor to produce rated torque due to voltage drops. In contrast, the proposed floating capacitor H-bridge system does not require such reactors (see Fig. 1). Note that replacing iron with silicon is often considered advantageous.

F. IGBT Voltage Stress

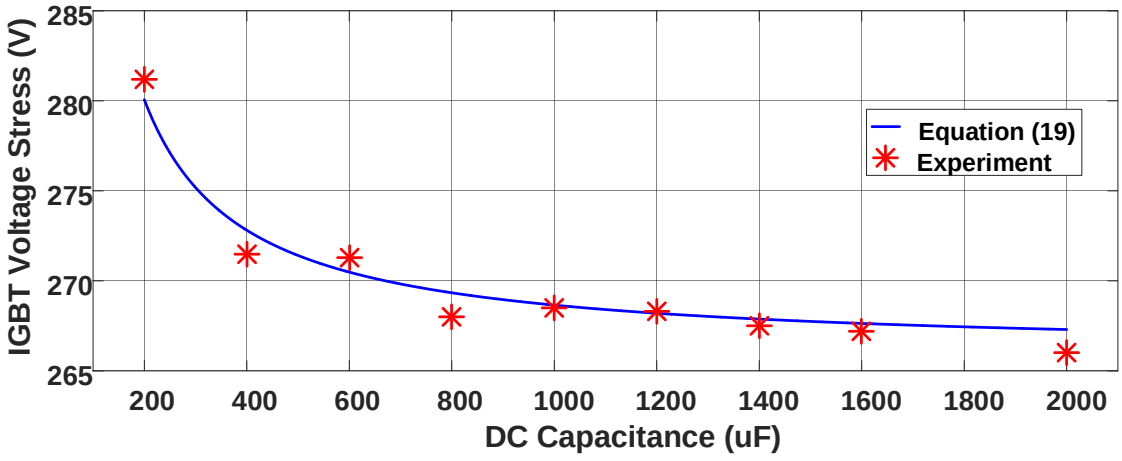
Fig. 15 shows IGBT voltage stress (peak DC capacitor voltage) under various DC capacitance and various motor load condition: a) quarter motor load (m_a=1.1, I_m=2.55A, ϕ_m =63.85^o); b) half motor load (m_a=1.1, I_m=3.23A, ϕ_m = 51.1^o); c) full motor load (m_a=1.1, I_m=4.2A, ϕ_m = 37^o) . From Fig. 15, it can be seen that the experiment results match theoretical predictions well. Generally, the bigger the DC capacitance, the lower IGBT voltage stress. Also, it can be observed from Fig. 15 that generally the higher motor load condition, the lower IGBT voltage stress. This is because the size of V_b is a function of motor power factor angle ϕ_m (see Equitation (18)). Under heavy motor load condition, the stator power factor of induction motor is usually high [39], which yields a low ϕ_m angle, which puts less demand on DC capacitor voltage. In contrast, under light motor load condition, the stator power factor of induction motor is usually low [39], which means a high ϕ_m angle, which puts more demand on DC capacitor voltage.



(a)



(b)



(c)

Fig. 15. IGBT voltage stress versus DC capacitance under different motor load condition: (a) quarter motor load (b) half motor load (c) full motor load

G. Capacitor Current

Fig. 16 shows FFT analysis for capacitor current under very small DC capacitance and full motor load condition (C = 200 uF, m_a=1.1, I_m=4.2A).

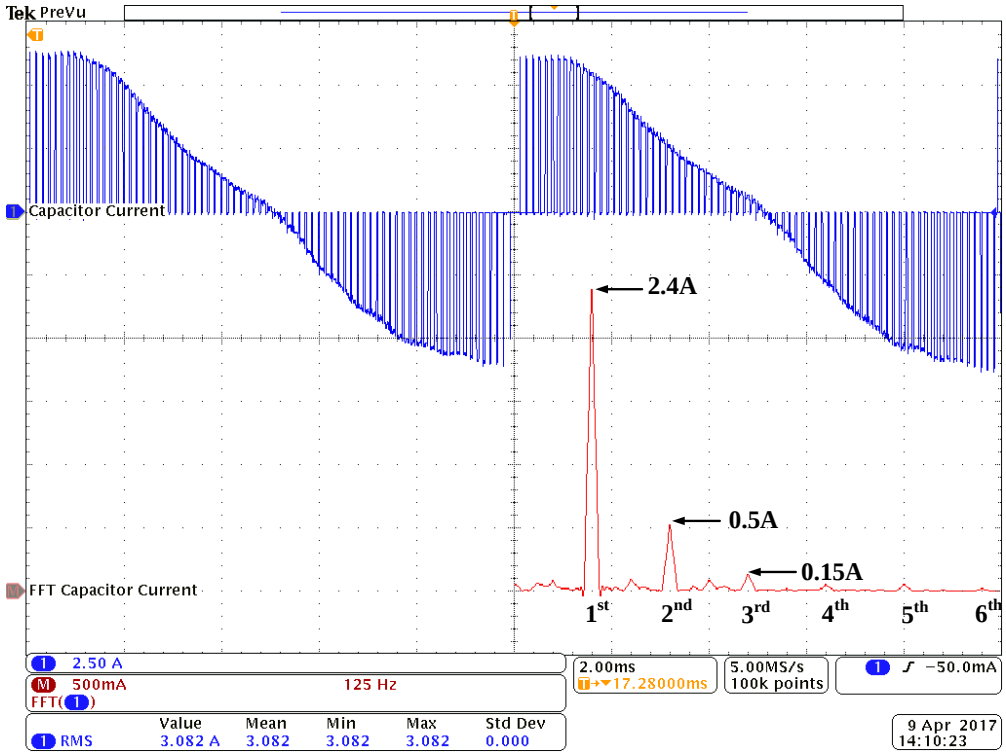


Fig. 16. FFT analysis for capacitor current under full motor load condition.

Fig. 16 shows that the capacitor current is oscillating at 100 Hz, which agrees with equation (22). It can also be seen from Fig. 16 that the magnitude of the fundamental component (100Hz) is 2.4A, while equation (22) predicts this value to be 2.44A, which is a good match. However, the RMS value of the capacitor current is 3.08A, which is 25% higher than what equation (22) had predicted. The explanation for such deviation is that equation (22) is a rough approximation of capacitor current. From Fig. 16 it can be seen that there are other harmonic components (200Hz, 300Hz) that cannot be captured by equation (22), which causes the actual RMS capacitor current to be higher than what equation (22) had predicted.

Fig. 17 is plotted where the RMS capacitor ripple current is recorded under various DC capacitances. It should be noted that for Fig. 17, the induction motor is always running under full load condition.

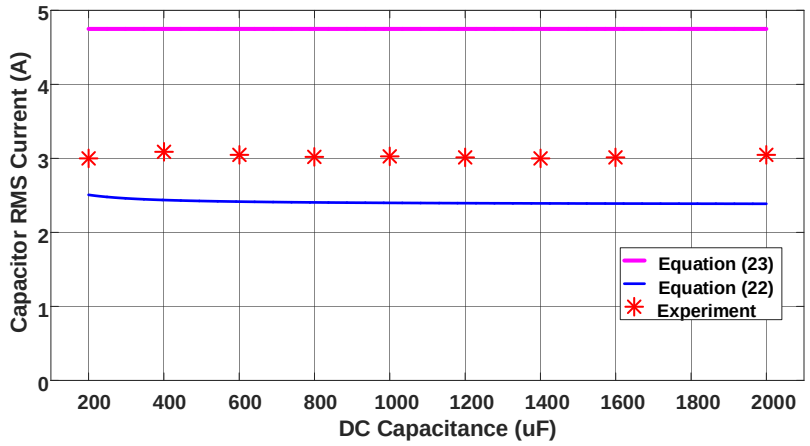


Fig. 17. Capacitor RMS current versus DC capacitance under full motor load condition.

From Fig. 17, it can be seen that the capacitor RMS current value remains almost flat despite large DC capacitance variation. The actual experiment value is always 25% higher than what equation (22) had predicted, but stays below the theoretical maximum value shown by equation (23). It should be noted that over-sizing is commonly practiced in engineering and Fig. 17 proves that equation (23) can be used to select the capacitor current rating during design phase.

H. Ripple Effect Compensation

Due to the 2nd order voltage ripple, instead of constant modulation index, the equivalent modulation index for the H-bridge is boosted. Such phenomenon will be taken into account in the control algorithm so that more accurate motor voltage control can be achieved, as it is shown in Fig. 18. It should be noted that for Fig. 18, the induction motor is always running under full load condition with its reference value fixed at 380V ($\left|V_m^*\right| = 380\,V$, see Fig. 3).

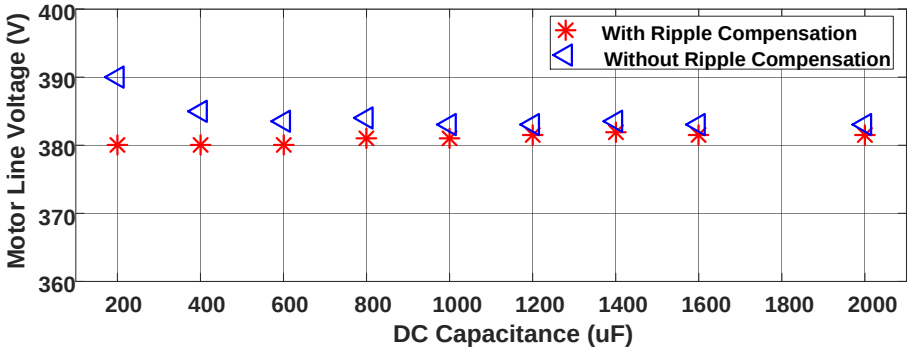


Fig. 18. Motor line voltage versus DC capacitance under full motor load condition.

It can be seen from Fig. 18 that generally, with ripple compensation, a better motor terminal voltage control can be achieved. When the DC capacitance is relatively large, the difference between the two control schemes is small. This is because the modulation index boost can be neglected under relatively large DC capacitance, (see equation (15)). However, as the DC capacitance gets smaller, the previously proposed control scheme [19]-[21] begin to lose accuracy, while the advantage of taking the ripple effect into account in the controller becomes obvious.

I. Minimum DC Capacitance

According to equation (24), the minimum DC capacitance for the proposed H-bridge motor drive is between 120-160 uF. Where k_a=3-4, I_m=4.2A, m_a=1.1,V_g=330V,V_m=380V, $\phi_m = 37^o$, V_b=206.8V. Through experiments, it is found that when connecting three 400 uF capacitors in series (C =133 uF), the proposed system can barely soft start and reach steady state condition. However, when connecting four 400 uF capacitors in series (C =100 uF), the system was never able to soft start and reach steady state, which proves that equation (24) can be used to roughly estimate the minimum DC capacitance during the design phase. For engineering practice, some margins are usually required, which is the reason that C=200 uF was chosen as the minimum DC capacitance value for this paper.

J. Power Loss Difference due to ESR Variation

For Metalized Polypropylene Film capacitor, its ESR is significantly smaller than that of electrolyte capacitor, which is one of its advantages. The DC capacitors used in this paper are MPPF Capacitors made by EPCOS (B25620-B0407-K881) with a capacitance of 400 uF and ESR of 3.8 milliohms and a tolerance of 10%. The worst-case scenario for power loss difference between phases is that under full motor load condition, the ESR of one phase is 20% higher than that of other phases. This will cause maximum power loss difference between phases as is shown in Fig. 19.

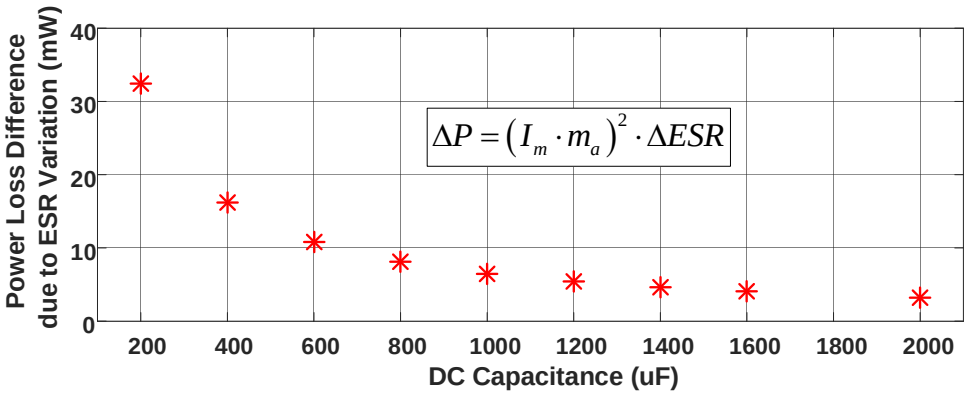


Fig. 19. Power loss difference due to ESR variation under full motor load condition.

From Fig. 19, it can be seen that under the worst-case scenario, the power loss difference between phases is between 3.24 mW to 32.4 mW, which is almost negligible compared with maximum allowable ESR power loss of 7695 mW for this type of film capacitor. Therefore, it can be concluded that the way to handle ESR variation between different capacitors is by three means: a) Use MPPF capacitor instead of electrolyte capacitor; b) Choose MPPF capacitors that have relatively small tolerance in terms of capacitance; c) Tight quality control during manufacturing stage so that individual capacitor ESR variation can be compensated by combination of different capacitors into equal capacitor banks.

VII. CONCLUSION

This work examines the possibility of implementing slim DC capacitance on an induction motor drive under balanced grid voltage condition. Using rigorous mathematical formulations supported by hardware experiments, it is found that the 2nd order DC ripple voltage does not cause problematic low-order harmonics in motor line voltage. In fact, allowing the 2nd order DC ripple voltage to fluctuate can boost equivalent modulation index of H-bridge to be higher than that of conventional SVPWM. As a result, the theoretical boundary condition for modulation index can be extended from 1.1547 to 2.0. Accordingly, motor terminal voltage control algorithm has been improved to take such phenomenon into account. Interestingly, allowing the 2nd order DC ripple voltage to fluctuate will also generate opposing third harmonic voltage to the one injected by SVPWM. In addition, the worst case scenario for capacitor RMS

current and IGBT voltage stress can be accurately predicted and the lower limit for DC capacitance can also be quantified. Based upon the above discoveries, it can be concluded that the proposed floating capacitor H-bridge motor drive can operate well under slim DC capacitance condition. This means expensive, bulky, and unreliable electrolyte capacitor banks can be replaced with cheaper, small, and reliable Metalized Polypropylene Film (MPPF) capacitors, which greatly improves the competiveness of the proposed motor drive topology.

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