Design and implementation of a novel three-phase cascaded half-bridge inverter

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Abstract: In this paper, a new circuit topology of a three phase half-bridge multilevel inverter (MLI) is proposed. The proposed MLI that consists of cascaded half-bridge structure along with modified full-bridge structure requires less number of dc-power supplies and power semiconductor devices, e.g. insulated gate bipolar transistors and diodes when compared with the existing MLI topologies, which significantly reduces the size and cost of the inverter. Two different structures; isolated and non-isolated dc-power supply-based three-phase half-bridge MLIs are investigated. A number of generalized methods are proposed to determine the magnitude of the input dc-power supplies that has a great impact on the number of levels of the output voltage waveform. To verify the feasibility of the proposed MLI topology, a scaled down laboratory prototype three-phase half-bridge MLI is developed and the experimental results are analyzed and compared with the simulation results. Experimental and simulation results reveal the feasibility and excellent features of the proposed inverter system.

1. Introduction

Three phase cascaded multilevel inverter (MLI) has been gaining significant attention in the modern high-power and high-voltage applications due to its advantageous that include modular construction, less common mode voltage problem and lower voltage stress (dv/dt) on the switching devices which increase circuit reliability and minimize the inverter cost [1–5]. In spite of the several advantages that MLI possess over other inverter types, some drawbacks, such as the use of large numbers of semiconductor devices, complexity of switching gate drive circuits, and requirements of multiple balanced dc-power supplies are still challenging to be overcome [6]. The aforementioned drawbacks are also responsible for the high cost of the MLI.

Many efforts have already been done in order to maximize the number of output voltage levels and minimize the number of power semiconductor devices and isolated dc-power supplies of the inverter circuit. Three-phase cascaded half-bridge MLI is a very well established structure, which utilizes minimum number of components. Different symmetric and asymmetric structures of half-bridge cascaded MLI have been presented in [7–13]. A three phase symmetric dc-linked half-bridge cascaded MLI that utilizes three identical

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phase arms for generating three phase voltages is implemented in [7, 8]. In this topology, each phase arm contains several dc-linked half-bridge cells and a full-bridge cell. Another three-phase half-bridge topology has been proposed in [9, 10], where the requirement of extra full-bridge was omitted and hence, the proposed topology utilizes reduced amount of power electronic components. In [11, 12], half-bridge cell-based three phase hybrid topology is proposed with the aim of reducing two dc power supplies in comparison to the topology proposed in [7–10]. A three phase non-isolated symmetric half-bridge MLI structure is proposed in [13]. In this topology, same dc-power supplies were utilized for the three phase arms and the number of input dc-power supplies is significantly reduced in comparison to the topologies proposed in [7–11]. Although the proposed inverter topology in [13] could reduce the number of dc-power supplies, the number of power semiconductor switches remains unchanged and it requires extra twelve switching devices in comparison to the MLI topologies proposed in [9–12]. Moreover, it cannot be configured for asymmetric structure and three single phase transformers have to be used to connect the inverter output to a three-phase load. The physical size, weight, cost and maintenance will be of a great concern if this topology is implemented for high-power and high-voltage applications. The requirement of multiple dc-power supplies from a single dc source can be achieved by utilizing a common high-frequency magnetic-link (HFML) which could be employed for the topologies presented in [9–12] to achieve reliable and cost effective topology [14–18].

For three phase inverter implementation for all aforementioned half-bridge topologies, the number of power semiconductor devices becomes three times than that of a single phase inverter. This will significantly increase the cost, size and complexity of the 3-phase MLI.

In this paper, a new concept of three phase cascaded half bridge MLI is proposed which significantly reduces the number of power electronic switching devices in comparison to the existing conventional half-bridge cascaded inverter topologies. This concept may equally be applicable for isolated and non-isolated dc-power supply-based three-phase half-bridge cascaded inverter. The fundamental frequency staircase modulation scheme is used for generating the switching gate pulses [19–21]. The key advantages of the proposed inverter are its requirement for less power semiconductor devices and input dc-power supplies, low switching losses and no electromagnetic interference problem.

2. Proposed multilevel Inverter

The proposed inverter topology consists of half-bridge structure along with modified full-bridge structure, as shown in Fig. 1. Fig. 1a and Fig. 1b show the non-isolated and isolated dc-power supply-based half-bridge configuration of the proposed topology, respectively. In each configuration, the half-bridge structure comprises n-number of series connected half-bridge modules. Each half-bridge module comprises

two switches, G_{k1} and G_{k2} and a dc-power supply, E_k, where k can be any integer number. Each pair of switches, G_{k1} and G_{k2} in any half-bridge module are always working in complementary mode, i.e. if one switch is turned on, the other switch must be turned off. On the other hand, the modified full-bridge structure consists of three modified Full-bridge modules for the three-phase voltage generation. Each modified Full-bridge module has four switches, S_{x1}–S_{x4} and four power diodes, D_{x1}–D_{x4}, where x represents phase a, b or c. An input dc-power supply, $E_{(n+1)}$ is connected in parallel with all modified Full-bridge modules. All utilized switches in the half-bridge and modified full-bridge structure are unidirectional. While the switches in the half-bridge structure contain internal anti-parallel diodes, switches in modified full-bridge structure do not utilize any diodes.

The modified Full-bridge modules are connected with the half-bridge structure at a junction point 'J'. Only the modified Full-bridge modules are responsible to generate the maximum output voltage level (when S_{x2} is turned on) and zero voltage level (when S_{x4} is turned on) as shown in Fig. 2a and 2b, respectively. The switches S_{x2} and S_{x4} are always operated in complementary mode on each phase arm a, b and c to avoid any short circuit fault. Both of the modified full-bridge and the half-bridge structures take part to generate the intermediate voltage levels between maximum, $E_{(n+1)}$ and zero voltage levels, as shown in Fig. 2c. The switches S_{x1} and S_{x3} are always turned on at a time while operating with the half-bridge structure to generate the intermediate voltage levels for any particular phase arm. Table 1 and Table 2 show the generalized switching mode of the non-isolated and isolated input supply-based half-bridge topologies shown in Fig. 1a and Fig. 2a, respectively. In these tables, the switches G_{k1} and G_{k2} of the half-bridge modules are kept in "don not care" mode, as denoted by "**", while generating maximum or zero voltage levels (Fig. 2a and Fig. 2b) as the two switches will have no impact on the generated voltage in these cases. The half-bridge structure contributes to the output voltage when S_{x1} and S_{x3} are turned on, as shown in Fig. 2c.

The pole voltages, V_{xg} can be expressed by

$$V_{xg} = 0 + V_{Jg} + E_{n+1} \tag{1}$$

where $V_{xg}\ \varepsilon\ (V_{ag}, V_{bg}, V_{cg})$

The maximum amplitude of the pole voltage, $V_{xg,\,max}$ is

$$V_{xg,\,max} = E_{n+1} \tag{2}$$

The maximum number of levels, N_p in the pole voltage can be calculated from

$$N_p = \left(\frac{V_{xg,\,max}}{V_{DC}}\right) + 1 \tag{3}$$

where $x \in (a, b, c)$

The three phase line-line voltage can be obtained from

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = \begin{bmatrix} V_{ag} - V_{bg} \\ V_{bg} - V_{cg} \\ V_{cg} - V_{ag} \end{bmatrix} \tag{4}$$

The number of levels in the line voltages can be calculated from

$$N_{level} = 2N_p - 1 \tag{5}$$

On the other hand the phase voltage, V_{XN} as a function of the pole voltage, V_{xg} is given as

$$\begin{bmatrix} V_{aN} \\ V_{bN} \\ V_{cN} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} \tag{6}$$

The blocking voltage of the switches is an important parameter that identifies the total inverter semiconductor cost. The voltage rating of a semiconductor device is directly related to the value of the blocking voltage. Lower blocking voltage may reduce the switching losses significantly [14]. Therefore, any reduction in the blocking voltage will not only reduce the semiconductors overall cost but it will also improve the inverter efficiency. The voltage blocked by the switching devices of the proposed inverter is given by:

$$\left. \begin{aligned} V_{G_{k1}} = V_{G_{k2}} = E_k \\ V_{S_{x1}} = V_{S_{x2}} = V_{S_{x3}} = V_{S_{x4}} = E_{n+1} \end{aligned} \right\} \tag{7}$$

Table 3 and Table 4 list different input voltage combinations with related generalized parameters for the non-isolated and isolated half-bridge structure, respectively. According to (7), the symmetric method will show minimum blocking voltage on the switches, but the number of output voltage levels is less than that of asymmetric structures. On the other hand, the switching devices in asymmetric structures exhibit higher blocking voltage but it provides more voltage levels in the output voltage than the symmetric structure for any specific number of modules in the half-bridge stage. For example, for two modules (n=2) in the non-isolated dc-supply based half-bridge structure, three dc-power supplies and sixteen semiconductor switches are required for the symmetric ($E_1=E_2=V_{dc}$, $E_3=2V_{dc}$) and asymmetric ($E_1= V_{dc}$; $E_2=2V_{dc}$, $E_3=4V_{dc}$) structures as shown in Table 3. Although the number of required components is the same for both structures, the switches in asymmetric structure exhibit more blocking voltage according to (7). On the other hand, seven levels will be shown in the line voltage when symmetric structure is implemented while the line voltage comprises nine levels for asymmetric configuration as shown in Table 3.

3. Simulation method and experimental setup

In the proposed topology, staircase modulation is employed to achieve proper switching sequence (S_A, S_B, S_C) generations. The pole voltages, V_{xg} are considered as reference for switching signal generation to achieve three phase output voltages. The number of switching states, S depends on the levels in the pole voltages, N_p and can be calculated as:

$$S = 6(N_p - 1) \tag{8}$$

The generalized switching states can also be represented by the space vector diagram as shown in Fig. 3. The diagonal points of the smallest hexagon represents the six switching states [(S_A, S_B, S_C) = (011, 010, 110, 100, 101, 001)] for achieving two levels in the pole voltage, N_p=2. However, the next hexagon represents twelve switching states, [(S_A, S_B, S_C) = (022, 021, 020, 120, 220, 210, 200, 201, 202, 102, 002, 012)] for achieving three levels in the output pole voltage, N_p=3. Similarly the next hexagons can be developed for getting any specific number of pole voltage levels, N_p= 4, 5……etc., according to (8).

For simplicity, the symmetric input algorithm with two modules in the half-bridge structure (non-isolated source) is chosen for implantation as shown in Fig. 4. As shown in Table 1, there are four switching modes for the chosen two modules (n=2) in the half-bridge structure. Hence four switching modes or switching combinations are required in achieving four levels (N_p=4), $[0, E_1, (E_1 + E_2), E_3]$ in the output pole voltages (V_{xg}). Since the symmetric input algorithm is considered, the input voltage sources can be expressed as $E_1 = E_2 = V_{dc}$; $E_3 = 3V_{dc}$.

Fig. 5 shows the switching modes of the topology in Fig. 4 where the turned on switches are marked by red color. The maximum and zero voltage level generation are explained in detail in Fig. 2. Fig. 5b and Fig. 5c show the intermediate level generation for the considered inverter structure in which it could be seen that G_{12} is always turned on while G_{11} always turned off during two intermediate levels, $[E_1, (E_1+E_2)]$ generation. According to Fig. 2, the switches of the half-bridge structure can stay at any valid switching mode during maximum and zero level generation. Hence during maximum and zero voltage generation, (G_{12}, G_{21}) can be kept in 0 or 1 mode which can lead to a reduction in the switching frequency of the two switches.

As the output pole voltage will have four levels, hence 18 switching states (300, 310, 320, 330, 230, 130, 030, 031, 032, 033, 023, 013, 003, 103, 203, 303, 302, 301) are expected according to (8). All the switching states are located on the edges of the black marked hexagon in Fig. 3. The aforementioned 18-

switching states (S_A, S_B, S_C) are listed in Table 5 for a complete cycle of the three phase output line voltages. The time period $T_1=T_2=T_3=...T_s$ of any switching state S_A–S_C can be expressed in generalized form by (9).

$$T_1 = T_2 = T_3 = ...= T_S = \frac{\frac{1}{f_{line}}}{S} = \frac{\frac{1}{50 Hz}}{S} = \frac{0.02}{6(N_p - 1)} \text{ (Second)} \qquad (9)$$

where f_{line} is the switching frequency of the line voltage.

Therefore, according to (9), the time period of each switching state in Table 5 can be written as

$$T_1 = T_2 = T_3 = ...= T_{18} = \frac{0.02}{S} = \frac{0.02}{18} \text{ (Second)}$$

This means that the switching logic combination of all switches will be changed every 1.11 ms to achieve the next switching state. The switching modes are chosen such that the switching frequency of the half-bridge structure is kept minimum. To achieve this goal, the red marked switching modes of G_{11}, G_{12}, G_{21}, and G_{22} are selected for switching signal generation during time period T_1, T_4, T_7, T_{11}, and T_{13}, as shown in Table 5.

MATLAB/Simulink software is used to simulate the proposed MLI topology as shown in Fig. 4. Furthermore, a laboratory prototype is developed to verify the simulation results. Digital signal processor (DSP), TMS320F2812 is used to achieve the real time switching signals. The insulated gate bipolar transistor (IGBT), IRG4BC40W, 600V/20 A and the diode, RHRP1540, 400V/15 A are used to build the prototype model for the modified Full-bridge modules. Four IGBTs, HGTG20N60B3D, 600V/40 A are used to implement the half-bridge structure. On the other hand, each modified Full-bridge module requires four diodes and four IGBTs. Fundamental frequency staircase modulation is applied as a control strategy. The calculated time period of each switching state for the 16-IGBT switches is equal to 1.11 ms. According to the number of pulses per cycle, the operating switching frequencies, f_{swt} of all switches are not equal. Each pair of S_{x2} and S_{x4} in the modified H-bride modules are operated at switching frequency $f_{swt} = f_{line}=50$ Hz while the switching frequency for each pair of S_{x1} and S_{x3} is $f_{swt} = 2f_{line} = 100$ Hz. For switches of the second (G_{21}, G_{22}) and first (G_{11}, G_{12}) half-bridge modules, the switching frequency is $f_{swt} = 3f_{line} = 150$ Hz and $f_{swt} = 0$ Hz, respectively.

Fig. 6 shows the simulated switches gate signals of the cascaded half-bridge module and the modified Full-bridge module for phase-a. The gate signal waveforms of G_{11}, G_{21}, S_{a1}, S_{a3}, and S_{a2} are shown in Fig. 6. As can be seen, each pair of the switches (G_{11}, G_{12}), (G_{21}, G_{22}) and (S_{a2}, S_{a4}) operates in a toggle mode with each other.

Fig. 7 shows the functional block diagram of the developed hardware setup. The logic block is responsible to arrange the switching states sequence and manipulate the switching logics according to the switching states shown in Table 5. The logic block in the PC transfers all the switching signals to the DSP, TMS320F2812 to generate the real time switching signals. As the DSP output signals are non-isolated of low amplitude, they cannot be directly connected to the IGBTs gate terminals. Hence the DSP output signals are passed through different gate drive circuits for isolating the common ground of the gate signals and increasing its amplitude.

The input dc-power supplies are adjusted such as $E_1=E_2=V_{DC}=40$ V and $E_3=3V_{DC}=120$V. Three-phase R-L load is considered in the simulation and experimental results. Two different load values (R=40 Ω and L=15 mH in each phase), (R=120 Ω and L=90 mH in each phase) are investigated to observe the line current for different load condition.

4. Results and discussions

Fig. 8 shows the simulation results obtained using MATLAB/Simulink software. Fig. 8a and 8b show the pole voltages, V_{ag}, V_{bg} and V_{Jg} for phase arms-a and b and the junction point J, respectively. As shown in the Figure, the pole voltages comprises four levels (0, 40 V, 80 V, 120 V) while V_{Jg} has two levels, 40 V and 80 V. The V_{Jg} plot verifies that the half-bridge structure has no contribution on the zero and maximum levels of the pole voltages, V_{xg}. The line voltage, V_{ab} is provided in Fig. 8c which shows seven different voltage levels (0, ±40 V, ±80 V, ±120 V) in the waveform. The phase voltage, V_{aN} for phase arm-a, is shown in Fig. 8d. The line current, I_{a1} and I_{a2} are depicted in Fig. 8e for load values (R=40 Ω and L=15 mH) and (R=120 Ω and L=90 mH), respectively.

The total harmonic distortion (THD) in the generated voltage or current waveforms can be calculated as:

$$THD(\%) = \frac{100\%}{H_1} \times \sqrt{\sum_{k=2}^{\infty} H_k^2} \tag{10}$$

where H_1 is the fundamental component of line current or voltage and k is harmonic order.
Fig. 8(f) and (g) show the THD of the unfiltered line voltage and line current, respectively. To satisfy IEEE 1547-2003 standard, the THD value should be less than 5 % [22]. Although the current THD fulfils the IEEE standard, the voltage THD is slightly above 5% in the implemented 7-level topology. The amount of THD can be reduced by increasing the number of levels in the output voltage which could be achieved through adopting asymmetric input voltage supply or adding more half bridge modules.

Fig. 9 shows the experimental verification of the simulated three-phase MLI. The figure shows the good agreement between simulation and practical results in terms of the phase to ground voltages V_{ag}, V_{bg} and output line voltage V_{ab}. It is worth mentioning that the proposed half-bridge comprising non-isolated or isolated input dc-power supply based half-bridge structure can be extended to provide any desired number of levels in the output voltage waveform.

5. Comparison study

The main goal of the proposed 3-phase hybrid MLI topology in this paper is to maximize the number of levels in the output voltage while minimizing the number of power electronic components and input dc power supplies which will reduce the inverter cost, physical size and complexity of gate drive circuit. In order to highlight the superiority of the proposed topology over existing MLI topologies, a comprehensive comparison including the required number of semiconductor switches, gate driver circuits, diodes, input dc-power supplies and the generated voltage levels per switch of the proposed three-phase topology in this paper and other three-phase symmetric half-bridge and full-bridge topologies in the literatures is given in Table 6. The voltage levels generated per switch (levels to switch ratio) is considered as an important parameter that reflects the contribution of each switch in producing the output voltage. As shown in Table 6, the proposed topology exhibits the highest level to switch ratio. Figs. 8a and 8b show a generalized comparison for the number of power electronic components and input dc power supplies required by the proposed MLI topology in this paper and some conventional half-bridge topologies in the literatures. As shown in Fig. 8, the proposed topology requires the least number of components for any desired number of levels in the output voltage. To generate 95 levels in the line voltages, Fig. 8 shows about 65% reduction in the required number of power electronic components and number of dc-power supplies when the proposed topology is compared with other topologies.

6. Conclusion

This paper presents a novel topology for a three phase half-bridge multilevel inverter that could be a better cost effective option than the existing conventional cascaded modular MLI inverter topologies as it comprises a reduced number of power switches, dc sources which significantly reduces the inverter cost, size and complexity. Results show that the number of power switches and dc-power supplies can be reduced by about 65% when the proposed topology is compared with other conventional half-bridge topologies. The proposed inverter is easy to implement and extend to generate any desired number of levels in the output

voltage waveform. The THD of the output voltage waveform can be reduced by either increasing the number of half-bridge modules or by adopting asymmetric dc voltages among the half-bridge modules. The proposed topology can be facilitated for renewable energy applications by employing a common high-frequency magnetic-link. It is expected that the proposed new inverter topology will have great potential for renewable generation systems and smart grid applications.

7. References

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Table 1 Generalized switching states of the non-isolated dc-power supply-based proposed half-bridge MLI

Switches states										Pole voltage/ switching modes	Contributing inverter structure
G_{11}	G_{12}	G_{21}	G_{22}	$\cdots$	G_{n1}	G_{n2}	S_{x1}, S_{x3}	S_{x2}	S_{x4}	V_{Xg}	
**	**	**	**	**	**	**	0	0	1	0	

G11	G12	G21	G22	...	Gn1	Gn2	S_{x1}, S_{x3}	S_{x2}	S_{x4}	Pole voltage/switching modes V_{Xg}	Contributing inverter structure
**	**	**	**	**	**	**	0	1	1	E_{n+1}	Only modified full-bridges structure
0	1	0	0	...	1	0	1	0	0	$\sum_{j=1}^{n} E_j$	Mutual contribution of half and modified full-bridge structures (V_{Jg})
0	1	0	0	...	0	1	1	0	0	$\sum_{j=1}^{n-1} E_j$	
...	...	...	...	...	...	...	...	...	...	...	
0	1	1	0	...	0	1	1	0	0	$\sum_{j=1}^{2} E_j$	
1	0	0	1	...	0	1	1	0	0	E_2	
0	1	0	1	...	0	1	1	0	0	E_1	

Table 2 Generalized switching states of the isolated dc-power supply-based proposed half-bridge MLI

Switches states										Pole voltage/ switching modes	Contributing inverter structure
G_{11}	G_{12}	G_{21}	G_{22}	...	G_{n1}	G_{n2}	S_{x1}, S_{x3}	S_{x2}	S_{x4}	V_{Xg}	
**	**	**	**	**	**	**	0	0	1	0	Only modified full-bridge structure
**	**	**	**	**	**	**	0	1	1	E_{n+1}	
1	0	1	0	...	1	0	1	0	0	$\sum_{j=1}^{n} E_j$	Mutual contribution of half and modified full-bridge structures (V_{Jg})
...	...	...	...	...	...	...	...	...	...	...	
1	0	1	0	...	0	1	1	0	0	$\sum_{j=1}^{2} E_j$	
0	1	1	0	...	0	1	1	0	0	E_2	
1	0	0	1	...	0	1	1	0	0	E_1	

Table 3 Different dc-power supply choosing methods and related parameters for non-isolated half-bridge based MLI

Proposed algorithm	Magnitude of dc-power supplies	$V_{Xg, max}$	N_p	N_{level}	N_{switch}	N_{source}
Symmetric	$E_k = V_{DC}$ $E_{n+1} = (n+1)V_{DC}$ For k = 1, 2, 3, ….., n	$(n+1)V_{DC}$	$(n + 2)$	$(2n + 3)$		$n+1$

Asymmetric	$\begin{aligned}E_1 &= E_3 = \ldots = V_{DC}\\ E_2 &= E_4 = \ldots = 2V_{DC}\end{aligned}$ $E_{n+1} = \sum_k^n E_k + E_1$ $= \begin{cases}\dfrac{(3n+2)}{2}\,V_{DC}\,;\,n=\text{even no}\\[2mm] \dfrac{(3n+1)}{2}\,V_{DC}\,;\,n=\text{odd no}\end{cases}$	$\begin{cases}\dfrac{(3n+2)}{2}V_{DC}\,;\,n=\text{even no}\\[2mm] \dfrac{(3n+1)}{2}V_{DC}\,;\,n=\text{odd no}\end{cases}$	$\begin{cases}\dfrac{(3n+4)}{2}\,;\,\text{even}\\[2mm] \dfrac{(3n+3)}{2}\,;\,\text{odd}\end{cases}$	$\begin{cases}(3n+3);\,\text{even}\\ (3n+2);\,\text{odd}\end{cases}$	$2n+12$	

Table 4 Different dc-power supply choosing methods and related parameters for isolated Half-bridge based MLI

Proposed algorithm	Magnitude of dc-power supplies	$V_{Xg,\,max}$	N_p	N_{level}	N_{switch}	N_{source}
Symmetric	$E_k = V_{DC}$ $E_{n+1} = (n+1)V_{DC}$ For $k = 1, 2, 3, \ldots, n$	$(n+1)\,V_{DC}$	$(n+2)$	$2n+3$	$2n+12$	$n+1$
Asymmetric-1	$E_1 = V_{DC}$ $E_k = 2V_{DC}$ $E_{n+1} = \sum_k^n E_k + 2E_1$ For $k = 2, 3, \ldots, n$	$(2n)\,V_{DC}$	$(2n+1)$	$(4n+1)$		
Asymmetric-2	$E_k = kV_{DC}$ $E_{n+1} = \sum_k^n E_k + E_1$ $= [\dfrac{n(n+1)}{2}+1]V_{DC}$ For $k = 1, 2, 3, \ldots, n$	$[\dfrac{n(n+1)}{2}+1]\,V_{DC}$	$\dfrac{n(n+1)}{2}+2$	$n(n+1)+3$		
Asymmetric-3	$E_k = 2^{k-1}V_{DC}$ $E_{n+1} = \sum_k^n E_k + E_1$ For $k = 1, 2, 3, \ldots, n$	$(2^n)V_{DC}$	2^n+1	$2^{n+1}+1$		

**Table 5** Switching states sequence for a complete one cycle of three phase line voltage generation

S_A	S_B	S_C	Period T[s]	G_{11}	G_{12}	G_{21}	G_{22}	S_{a1},S_{a3}	S_{a2}	S_{a4}	S_{b1},S_{b3}	S_{b2}	S_{b4}	S_{c1},S_{c3}	S_{c2}	S_{c4}	V_{AB}	V_{BC}	V_{CA}
3	0	0	T_1	**0**	**1**	**0**	**1**	0	1	0	0	0	1	0	0	1	3	0	-3
				1	0	0	1												
				0	1	1	0												
3	1	0	T_2	0	1	0	1	0	1	0	1	0	0	0	0	1	2	1	-3
3	2	0	T_3	0	1	1	0	0	1	0	1	0	0	0	0	1	1	2	-3
3	3	0	T_4	0	1	0	1	0	1	0	0	1	0	0	0	1	0	3	-3
				1	0	0	1												
				0	**1**	**1**	**0**												
2	3	0	T_5	0	1	1	0	1	0	0	0	1	0	0	0	1	-1	3	-2
1	3	0	T_6	0	1	0	1	1	0	0	0	1	0	0	0	1	-2	3	-1
0	3	0	T_7	**0**	**1**	**0**	**1**	0	0	1	0	1	0	0	0	1	-3	3	0
				1	0	0	1												
				0	1	1	0												
0	3	1	T_8	0	1	0	1	0	0	1	0	1	0	1	0	0	-3	2	1
0	3	2	T_9	0	1	1	0	0	0	1	0	1	0	1	0	0	-3	1	2
0	3	3	T_{10}	0	1	0	1	0	0	1	0	1	0	0	1	0	-3	0	3
				1	0	0	1												
				0	**1**	**1**	**0**												
0	2	3	T_{11}	0	1	1	0	0	0	1	1	0	0	1	0	0	-2	-1	3
0	1	3	T_{12}	0	1	0	1	0	0	1	1	0	0	1	0	0	-1	-2	3
0	0	3	T_{13}	**0**	**1**	**0**	**1**	0	0	1	0	0	1	0	1	0	0	-3	3
				1	0	0	1												
				0	1	1	0												
1	0	3	T_{14}	0	1	0	1	1	0	0	0	1	0	1	0	0	1	-3	2
2	0	3	T_{15}	0	1	1	0	1	0	0	0	1	0	1	0	0	2	-3	1
3	0	3	T_{16}	0	1	0	1	0	1	0	0	1	0	1	0	0	3	-3	0
				1	0	0	1												
				0	**1**	**1**	**0**												
3	0	2	T_{17}	0	1	1	0	0	1	0	0	0	1	1	0	0	3	-2	-1
3	0	1	T_{18}	0	1	0	1	0	1	0	0	0	1	1	0	0	3	-1	-2

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Table 6 Comparison of the implemented 7-level topology over other inverter topologies

	Proposed 3-phase topology	DC linked three phase Half-bridge inverter [7]	Symmetric al Hybrid MLI [8]	3-Phase Cascaded MLI Using Power Cells [10]	3-phase reversing voltage (RV) topology [13]	H-bridge cascade inverter [23, 24]
No of levels in line voltage (N_{level})	7	13	9	9	7	7
No of switching devices for 3-phase	16	48	24	24	30	36
No of Diodes	16	48	24	24	30	36
Line voltage levels/ switch ratio	0.44	0.27	0.375	0.375	0.233	0.20
No of dc-power supplies or capacitor	3	18	6	12	3	9
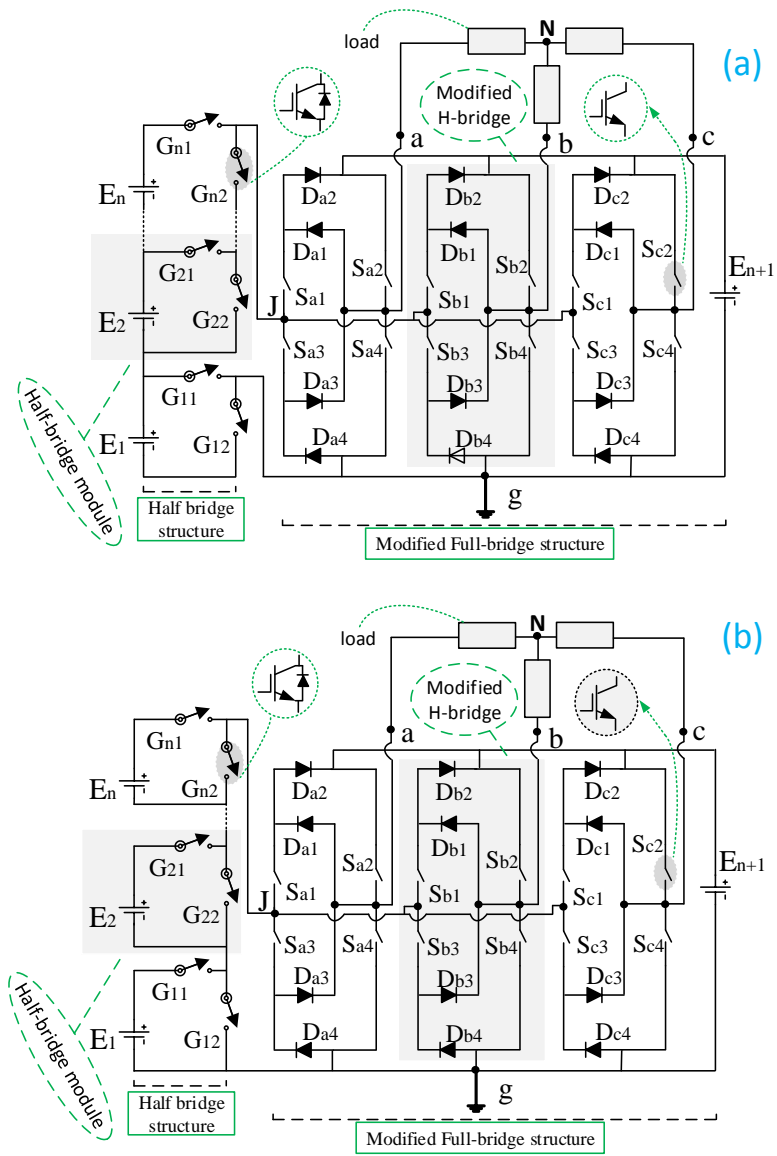
Fig. 1. *Proposed generalized three phase half-bridge topology*
(a) Non-isolated input dc-power supply-based half-bridge topology
 (b)Isolated input dc-power supply-based half-bridge topology
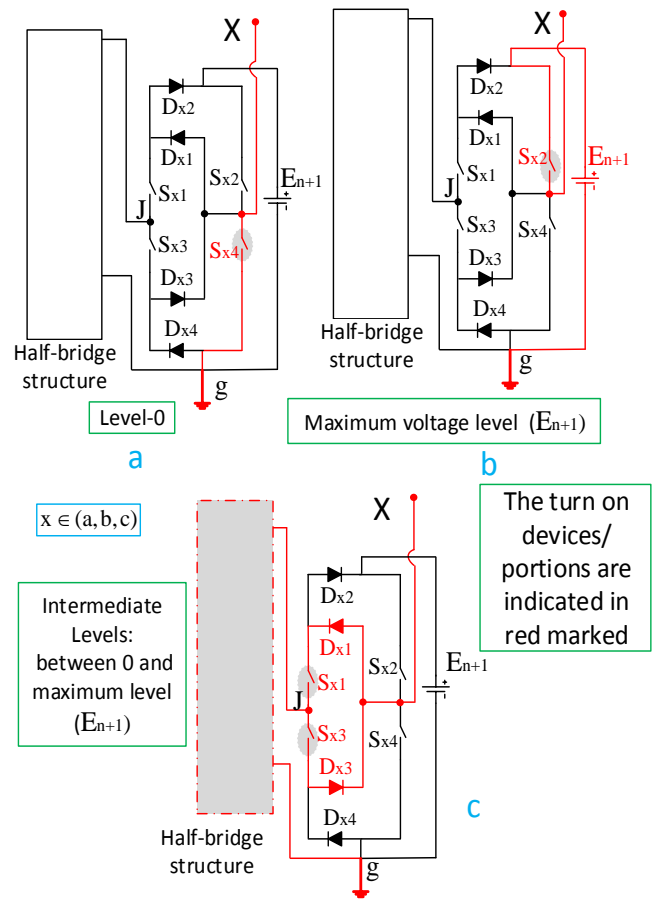
Fig. 2. *Generalized overview of the output voltage level generation for*

(a) Zero level

(b) Maximum level

 (c) Intermediate levels between zero and maximum level.
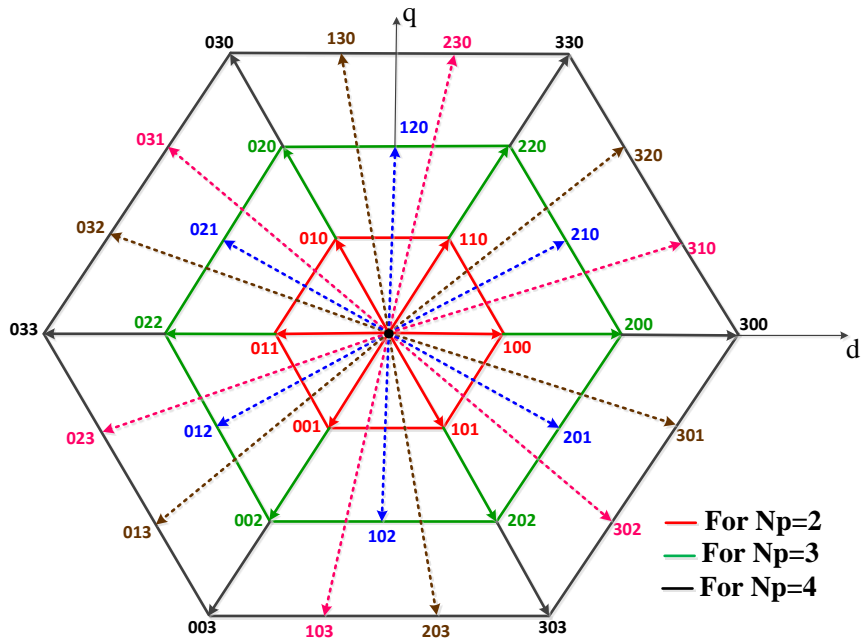
Fig. 3. Generalized switching states presentation by hexagon in d-q complex plane
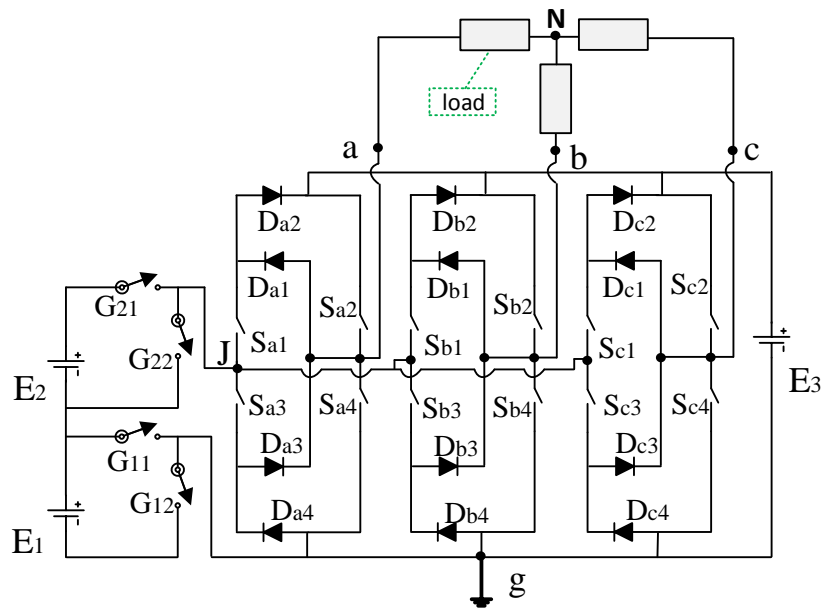
Fig. 4. Schematic of the implemented topology
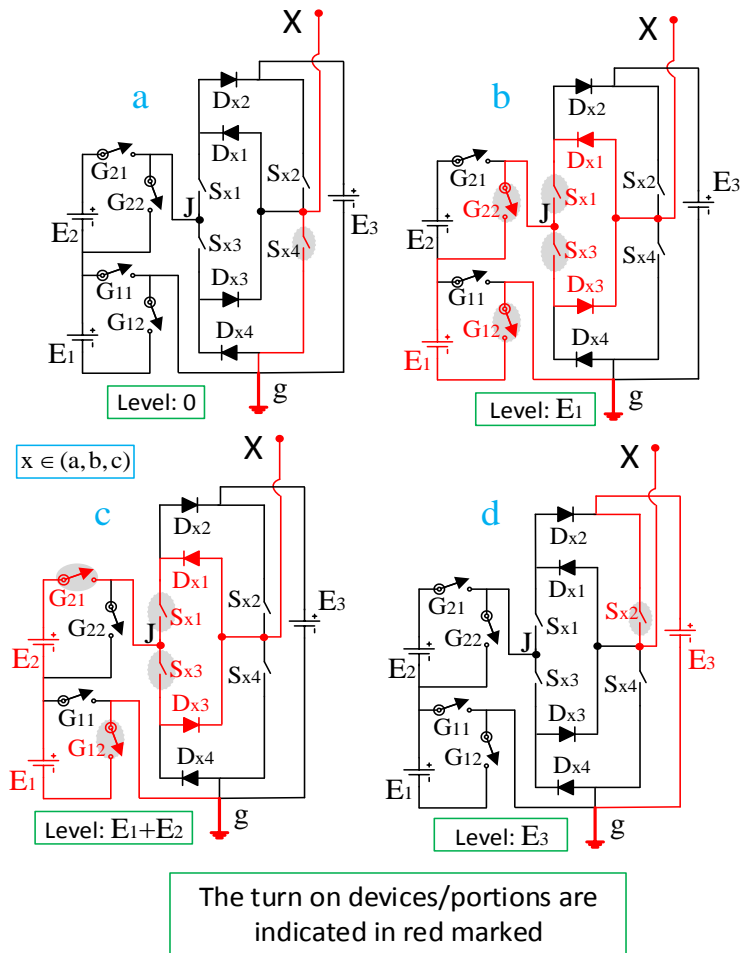
Fig. 5. Different switching mode to generate all the possible levels in the pole voltage

(a) Level: zero

(b) Level: E_1

(c) Level: $(E_1 + E_2)$

(d) Level: E_3
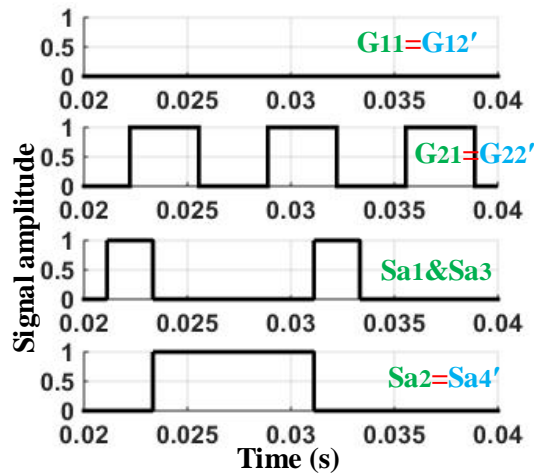
Fig. 6. The switching signals for a complete cycle of the switches $(G_{11}, G_{22}, S_{a1}, S_{a2}, S_{a3})$
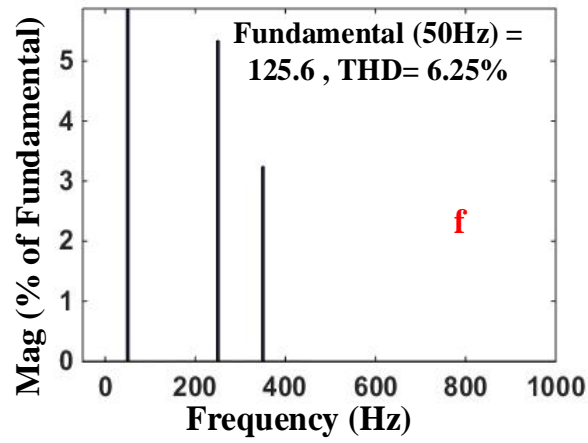
18
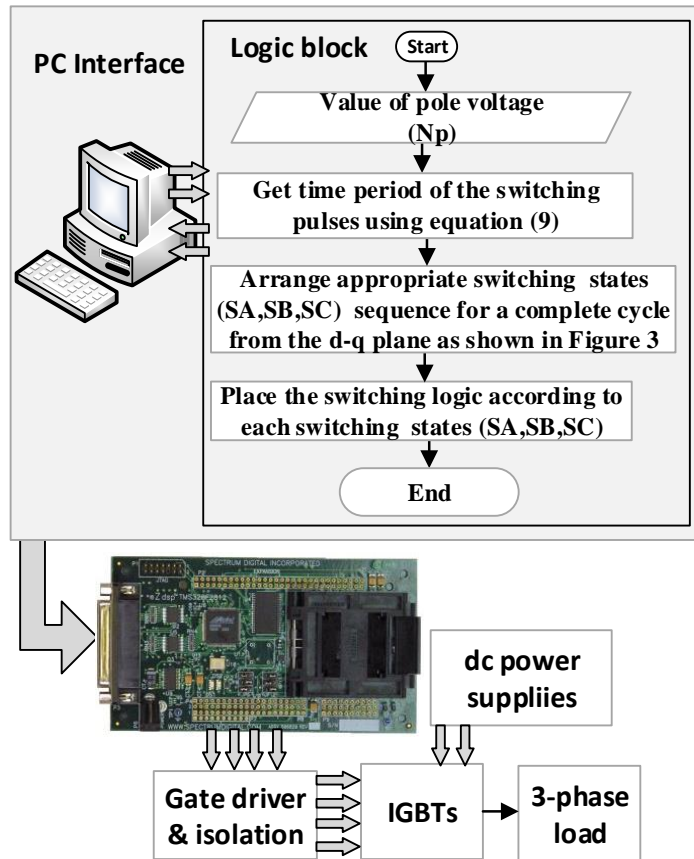
Fig. 7. *The functional block diagram of the experimental setup*

Fundamental (50Hz) = 125.6 , THD= 6.25%

f

Fundamental (50Hz) = 0.5764, THD= 2.51%

g
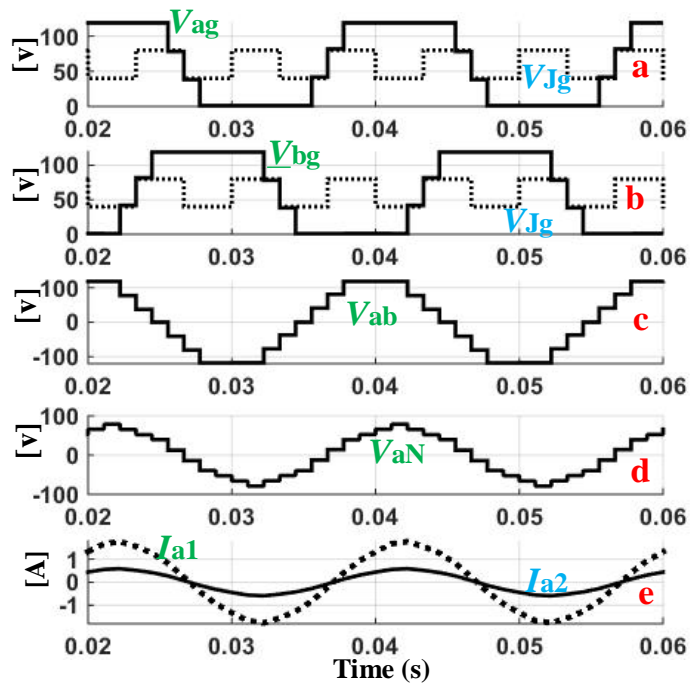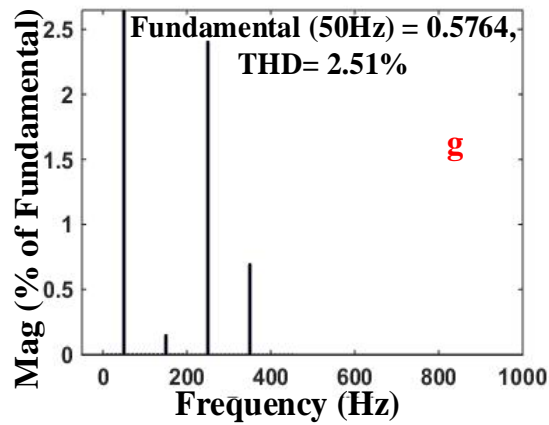
Fig. 8. Simulation results

(a) Intermediate voltage, V_{Jg} and pole voltage, V_{ag} ,

(b) Intermediate voltage, V_{Jg} and pole voltage, V_{Bg},

 (c) Line voltage, V_{AB}, which is generated by utilizing, V_{ag} and V_{bg},

(d) Phase voltage, V_{aN}

(e) The line current, I_{a1} and I_{a2} for (R=40 Ω and L=15 mH in each phase) and (R=120 Ω and L=90 mH in each phase),

respectively.

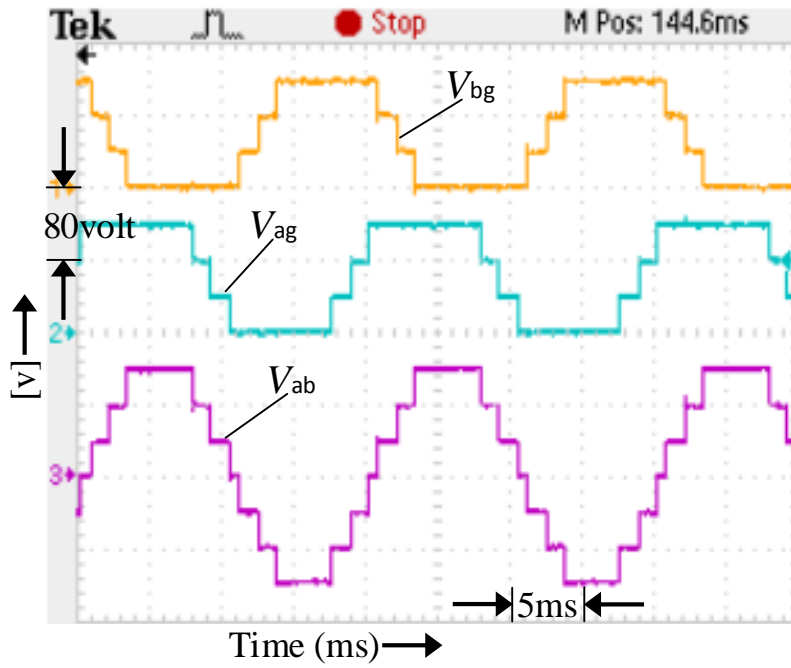(f) THD of the line voltage

(g) THD of the line current

Fig. 9. *Experimental results of pole voltage, V_{ag} and V_{bg} [80 V/div, 5 ms/div], and line voltage, V_{ab} [80 V/div, 5 ms/div]*
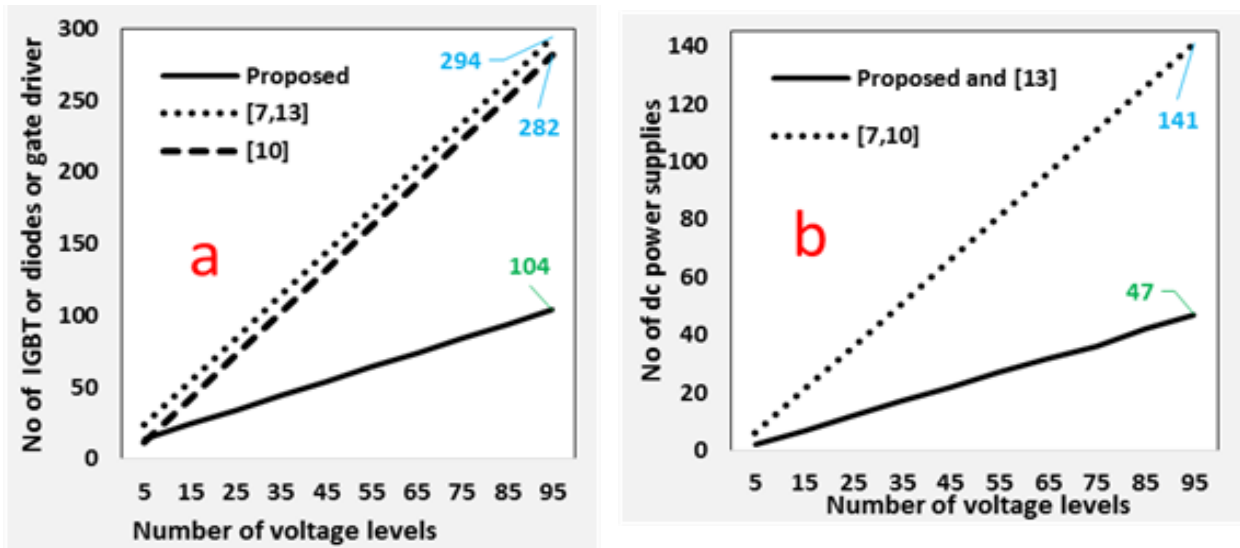

Fig. 8. *Comparison study for the symmetric method in the half-bridge stage*

(a) Number of semiconductor devices (IGBT or diode or gate drive circuit) versus number of levels in the line voltage (V_{level})

(b) Number of dc-power supplies versus number of levels in the line voltage (V_{level})