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Efficient three variables reversible logic synthesis using mixed-polarity Toffoli gate

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Abstract

In this paper, we present an efficient reversible logic synthesis algorithm that uses Toffoli and mixed-polarity based Toffoli gate. In this paper, we propose an algorithm to synthesizereversible function in their positive-polarity Reed Muller (PPRM) expansion and usethe Hamming Distance (HD) approach to select suitable transformation path. Once a transformation path is defined, suitable gates for substitution are selected through the gate matching factor and reduction is performed. The algorithm does not generate any extra lines and thus keeping the synthesized function in its simplest form. The algorithm target on efficient way to synthesize three variables based reversible function into a cascade of Toffoli and mixed-polarity based Toffoli gate in term of quantum cost and gate count. Experimental results showthat the proposed algorithm is efficient in terms of the realization of all three variable based reversible functions.

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1. Introduction

Research on reversible logic has been motivated by it theoretical research on low-power computing and had recently attracted interest as components of quantum computing, optical computing, nanotechnology, bioinformatics and cryptography[1, 2]. However due to difference in properties between reversible logic and traditional irreversible logic, algorithm used for synthesis irreversible logic cannot be carried on to synthesis reversible logic. Therefore a new set of algorithm is developed specifically for the synthesis of reversible logic.

Over the last decade, reversible logic synthesis has been intensively studied and plenty of algorithms have been developed [1]. Research attention has been focused on the synthesis of circuits build using the NCT library which consists of NOT, CNOT and Toffoli gates [1]. NCT gate library has been explored and extended such as increasing its variable size of theToffoli gate [3] and recently researcher has started to include polarity control into its operation [4]. Toffoli gate with polarity control isknown as the mixed-polarity Toffoli gate. Usage of this gate into synthesis algorithm has been proposed in [4-8]. Although various researchworks have been presented by using this gatebut to our best knowledge, recently,synthesis algorithms only proposed to generates suboptimal circuits.

2. Basic Definition

Definition 1: A n-input n-output Boolean $f(x_1)$ function $f(x_1, x_2, x_3, ..., x_n)$ is reversible if the number of inputs n is equal to the number of outputs n with a unique one to one mapping relationship.

Definition 2: Quality of a reversible circuit is determined by overall gate count and quantum cost. Gate count denotes the total number of reversible gate needed to realize a reversible function and quantum cost denotes the overall cost required to realize the given reversible function. All reversible gate is assigned to a specific quantum cost number which is determined by the number of elementary quantum gate disclose within it to perform the gate operation [9]. The quantum cost used in this paper is referred from [10-12].

Definition 3: Reversible gate implements reversible function. If a reversible gate has n inputs (and n outputs), we can call it as a $n \times n$ gate. The three commonly used gates, composing the NCT gate library, are the NOT, CNOT and Toffoli gates[1] respectively.By introducing the mixed-polarity Toffoli gate to the NCT gate library, it can form the m-NCTgate library. The details of the gates are as follow:

NOT gate:A NOT gate is a one bit reversible gate. It has a quantum cost of 1 [11]. Fig. 1 shows the accepted symbol of the gate with its function.

$$x_1 \ \text{———} \bigoplus \text{———} \ \overline{x_1}$$

$$x_1 \text{———} \bullet \text{———} x_1$$
$$x_2 \text{———} \bigoplus \text{———} x_1 \oplus x_2$$

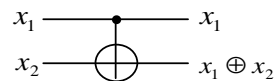Fig. 1. NOT gate   Fig. 2. CNOT gate

CNOT gate:A CNOT gate is a two bit reversible gate. It has a quantum cost of 1 [11].Fig. 2showsthe symbol of the CNOTgate with its function.

Toffoli gate: A Toffoli gate [13] is a three bit reversible gate. It has a quantum cost of 5. Fig.3shows the symbol with its function and the quantum realization disclosed, where $V = \dfrac{1+i}{2}\begin{bmatrix} 1 & -i \\ -i & 1 \end{bmatrix}$ and $V^+ = \dfrac{1-i}{2}\begin{bmatrix} 1 & i \\ i & 1 \end{bmatrix}$, and such that $V^2 = \text{NOT}$ and V^+ represents the adjoint of V [9, 14, 15].
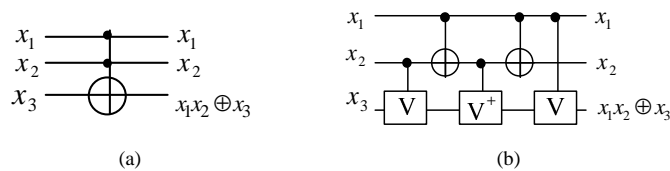
Fig.3. (a) Toffoli gate symbol [16] (b) Quantum realization [16]

Mixed-Polarity Toffoli gate: A mixed-polarity Toffoli gate is a three bit reversible gate. Depending on the number of negative control bit, there are two combinations which are mixed-polarity Toffoli gate with single negative control bit and two negative control bits. Mixed-polarity Toffoli gate with single negative bit has a quantum cost of 5 whereas mixed-polarity Toffoli gate with two negative bit has a quantum cost of 6 [12]. Fig.4 and Fig.5 show the symbol of these gates with their corresponding function and the quantum realization disclosed [12].
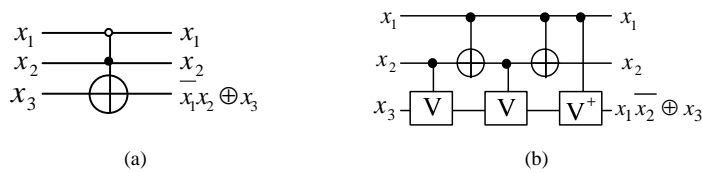

Fig.4. (a) Mixed-Polarity Toffoli gate symbol with single negative control bit [12] (b) Quantum realization [12]
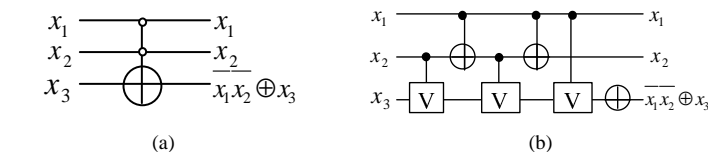

Fig.5. (a) Mixed-Polarity Toffoli gate symbol with two negative control bits [12] (b) Quantum realization [12]

3. Positive-Polarity Reed Muller Expansion

Unlike other Boolean expansion, a reversible function can be expressed into different Boolean expansion and this may affect the outcome of the synthesized result. Hence, in the proposed algorithm, reversible function is synthesized using the Positive Polarity Reed-Muller (PPRM) expansion of the reversible function. The PPRM expansion directly reflects the logic gates' operation; this enables the algorithm to perform gate selection and substitution easily. Besides that the PPRM expansion is unique and intrinsic expression where a reversible function can only be expressed into one PPRM expansion. The PPRM expansion of a reversible function can be derived from the prime implicant of the reversible function.

To express any Boolean function into the PPRM expansion, the Boolean function is first expressed in their exclusive sum-of-product (SOP) expansion. Then the un-complement rule $\overline{x_n} = 1 \oplus x_n$ is applied to all complemented term, where $\overline{x_n}$ refers to the complemented term. Thus the PPRM expansion is obtained.

4. Hamming Distance

Hamming Distance (HD) is the amount of bits that differ between two binary specifications [17]. In the proposed algorithm, the HD is used for calculating the bits different between the input terms and the output terms in every transformation path. The path that contains the lowest non-zero HD value will be selected as the next transformation path. According to our findings, path that contains the lowest non-zero HD value will often yield to a solution faster.

When a HD of a path reaches zero, there will be no bit difference between the input terms and output terms. Further reduction is not required because a solution has been found.

5. Gate Matching Factor and Substitution

For each selected transformation path, a variety of reversible gates are selected. For each selected reversible gate, a new transformation path is created and the gate's function is substituted into the original PPRM expansion for Boolean reduction. The reversible gates are selected through matching the current PPRM expansion with the gate matching factors. The gate matching factor and their substitution is defined as the followings:

NOT gate: Matching factors will be the PPRM expansion term containing a variable '1' and a single value variable term. A substitution of $x_{out} = x \oplus 1$ will be performed on single value variable term. Where x refers to the single value variable and x_{out} refers to the unique output line labeled by x.

CNOT gate: Matching factors will be the PPRM expansion term containing two or more single value variables term. A substitution of $x_{out} = x \oplus single\ value\ term$ will be performed.

Toffoli gate: Matching factors will be the PPRM expansion term containing one single value variables term and multiplied value variables. A substitution of $x_{out} = x \oplus two\ othermultiplied\ single\ variable\ terms$ will be performed.

Mixed-Polarity Toffoli gate with single negative bit: Matching factors will be the PPRM expansion term containing at least two single valued variables term and multiplied value variables. A substitution of $x_{out} = x \oplus two$ *other multiplied single variable terms with one inverted* will be performed.

Mixed-Polarity Toffoli gate with both negative bits: Matching factors will be the PPRM expansion term containing at least two single valued variables term, a constant 1 and multiplied value variables. A substitution of $x_{out} = x \oplus two\ other\ multiplied\ single\ variable\ terms\ with\ both\ inverted$ will be performed.

6. Methodology

The main steps of the synthesis algorithm are described in the following steps illustrated in Fig.6. In the first step of the algorithm, the input Boolean function to be synthesized is expressed in its PPRM expansion. The algorithm explores the PPRM expansion and finds all possible matching reversible gates. For each selected reversible gate, a new transformation path is assigned and the gate's function is substituted into the original PPRM expansion for Boolean reduction. The HD for each transformation path is also calculated.

Then, the algorithm explores the next lowest non-zero HD transformation path for further reduction. The search process continues until a solution is found such that the HD of the transformation path reaches 0. During the process, all the details of the path such as gate connection from the beginning to the end, gate count and quantum cost are captured.

Next, the algorithm continues to find a better solution by continue exploring the next lowest non-zero HD transformation path. The algorithm iterates itself until all possible solution are found or reached the timeout set by the user. In the process, if the algorithm finds a better solution, the current existing ones, the old solution is overwritten. A transformation path is terminated halfway, if it does not generate a better solution. For example, while optimizing the gate count, if the path where its current gate count exceeds the best solution's gate count, the process will be terminated.
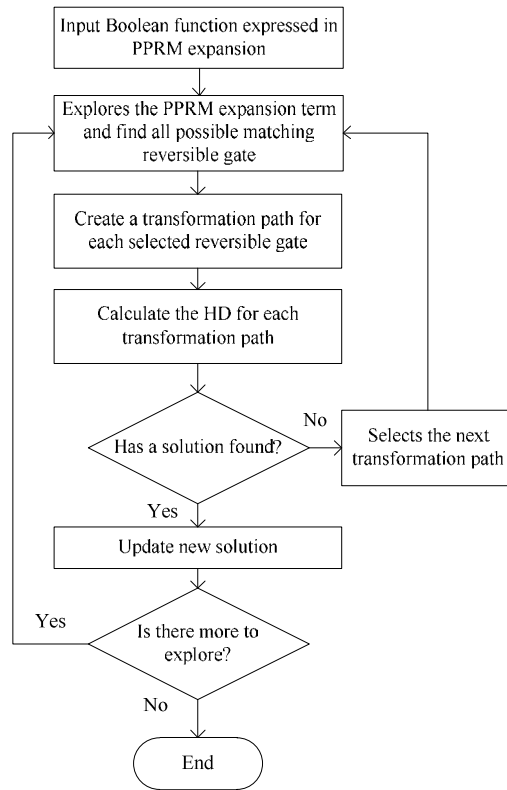
Fig.6. Flow chart of the synthesis algorithm

7. Synthesis Result

Table 1 shows the results of applying various algorithms to all three variables reversible functions (a total number of 40,320 reversible functions). For fare comparing the performance of the proposed algorithm with the existing algorithms, we use the same gate library for obtaining the gate count results. As can be seen from the Table 1 that the proposed algorithm produces a lowaverage gate count and does not produce any circuits larger than 9. Comparing the results for NCT and m-NCTwith the use of m-NCT gate library, the proposed synthesis algorithm no longer generate circuits larger than 8 and as for circuit of size 1, the m-NCT based gate library is able to generate 21 circuits which cannot be achieved using only NCT based gate library.

Furthermore, we evaluate the performance of the proposed synthesis algorithm in term of quantum cost. It is observed that the existing synthesis algorithms [18-20]are unable to synthesis in terms of quantum cost. Hence, we can only compare the performance of the proposed synthesis algorithm in term of quantum cost. Table 2shows the quantum cost table which is generated from all three variables reversible functions. It can be noticed from the Table 2 that there are significant improvements in term of quantum cost compared to the one set to synthesize in term of gate count.

Table 1. Gate count for all three variables reversible functions

Number of Gates	Proposed Work NCT	Proposed Work m-NCT	[18] NCT	[19] NCT	[20] NCT
0	1	1	1	1	1
1	12	21	12	12	12
2	102	225	102	102	90
3	625	1527	625	567	476

4	2702	6058	2642	2125	1833
5	7932	14139	7479	5448	4996
6	14384	14995	13596	9086	9126
7	12201	3273	12476	9965	10630
8	2339	81	3351	7274	7820
9	22	0	36	3837	3788
10	0	0	0	1444	1265
11	0	0	0	391	258
12	0	0	0	62	25
13	0	0	0	6	0

Table 2.Quantum Cost for all three variables reversible functions

Quantum Cost Size	Result NCT (set for qc*)	Result m-NCT (set for qc*)	Result NCT (set for gc#)	Result m-NCT (set for gc#)
0	1	1	1	1
1	9	9	9	9
2	51	51	51	51
3	187	187	187	187
4	387	387	387	387
5	426	432	426	432
6	305	353	305	353
7	350	560	350	560
8	1305	1812	1305	1803
9	2952	3458	2946	3392
10	3418	2938	3388	2817
11	1416	1001	1377	879
12	946	1964	937	1973
13	3543	5728	3543	5622
14	7278	7851	7246	7291
15	6095	2798	5945	2573
16	1017	856	949	1057
17	950	2601	980	2668
18	3319	5048	3358	4816
19	4884	2221	4893	2266
20	1461	64	1463	381
21	20	0	62	336
22	0	0	138	283
23	0	0	74	102
24	0	0	0	54
25	0	0	0	6
26	0	0	0	9
27	0	0	0	12

*qc: algorithm set to synthesize in term of quantum cost
#gc: algorithm set to synthesize in term of gate count

8. Conclusion

In this paper, we presented a synthesis algorithm that uses the NCT library with the mixed-polarity Toffoli gate. The proposed algorithm cansynthesis any reversible function using its PPRM expansions. In the proposed synthesis algorithm, lowest HD value path is selected for transformation. Gate substitution is done through finding the matching terms from the PPRM expansion. The algorithm does not generate extra lines and thus able to keep the synthesized function in its simplest form. We applied our algorithm to synthesis all three variables reversible functions and numerical results show that the proposed synthesis algorithm outperforms the existing synthesis algorithm in term of gate count and quantum cost. It is noticed from the numerical examples that inpresence of mixed-polarity Toffoli gate, the proposed synthesis algorithm dramatically improves the overall gate count and quantum cost.

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