An Analysis of a Voltage Clamped Zero-Voltage Switching Two-Inductor Boost Converter with a Wide Load Range

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ABSTRACT

The Zero-Voltage Switching (ZVS) two-inductor boost converter has been previously developed for the dc-dc conversion stage in a photovoltaic (PV) Module Integrated Converter (MIC) and is able to operate with variable load condition under variable frequency control. However, the converter only offers a narrow output voltage range and this is limited by the MOSFET voltage stress. In this paper, a voltage clamped ZVS two-inductor boost converter is proposed. The converter is able to operate under a wide output voltage range with a lower MOSFET voltage stress while maintaining the resonant transitions. The state analyses of three different operation modes are provided. The design process is also demonstrated in detail and explicit control functions for a 200-W converter are established. Finally, a brief comparison of the advantages and the disadvantages of the two ZVS converters is provided.

1. INTRODUCTION

The two-inductor boost converter has been proved to be one of the favourable candidates for the voltage boosting stage in many applications such as grid interactive PV converters and uninterrupted power supplies [1]-[8]. The resonant two-inductor boost converter is shown in Figure 1, which is able to achieve ZVS at MOSFET turn-on [9].

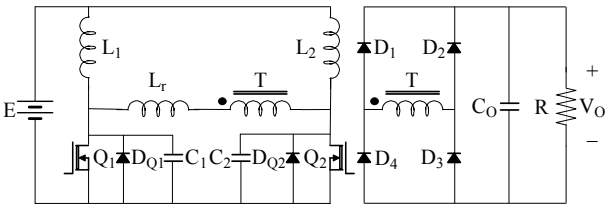

Figure 1: ZVS Two-Inductor Boost Converter

In grid interactive PV applications, Maximum Power Point Tracking (MPPT) requires the resonant dc-dc converter to operate with variable input output voltage ratios. It has been established that the variable load operation of the ZVS two-inductor boost converter can be achieved by variable frequency control, where the three circuit parameters including the load factor, the timing factor and the delay angle are adjusted to maintain the resonant switching transitions [10].

However, the ratio of the maximum to the minimum output voltages of the ZVS two-inductor boost converter is limited to 2.3 if the MOSFET voltage rating of 200 V is applied to a converter with an input voltage of 20 V and a rated power of 200 W [10]. In order to operate the converter with a wider output voltage range and without the penalty of the high MOSFET voltage stress, mechanisms which are able to control the MOSFET voltage below a certain level are required. This paper studies the variable frequency operation of the ZVS two-inductor boost converter with a simple voltage clamping circuit as shown in Figure 2.

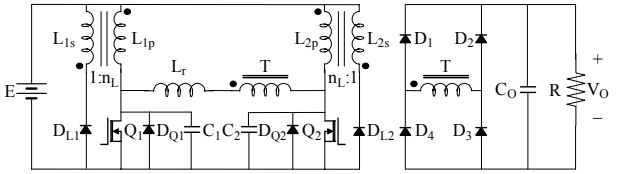

Figure 2: ZVS Two-Inductor Boost Converter with the Voltage Clamp

In Figure 2, the voltage clamping circuit is made of two coupled inductors L_{1p}, L_{1s} and L_{2p}, L_{2s} and two additional diodes D_{L1} and D_{L2}. L_{1p} and L_{2p} are the inductances of the inductor main windings. L_{1s} and L_{2s} are the inductances of the inductor clamp windings. The turns ratio of the coupled inductor main winding to the clamp winding is n_L:1. When the voltage across the main winding of each coupled inductor reaches $n_L E$, dot negative, the diode D_{L1} or D_{L2} will conduct and this clamps the voltage across the MOSFET to V_c, which is defined as:

$$V_c = (1 + n_L)E \tag{1}$$

This paper provides the state analyses of three operation modes of the two-inductor boost converter with the voltage clamp. A detailed converter design process is also presented for a 200-W converter with 20-V input voltage and 340-V output voltage. This confirms that the ZVS converter with the voltage clamp offers an output voltage range of 5.3 while the peak MOSFET voltage is 90 V. The theoretical and simulation waveforms are provided for three selected operating points. A brief comparison of the two ZVS converters is also given at the end of the paper.

2. THREE CIRCUIT PARAMETERS

There are three key circuit parameters in analysing the operation of the ZVS two-inductor boost converter with the voltage clamp shown in Figure 2. They are labeled in bold characters in the resonant waveforms of one operation mode shown in Figure 3, which can be identified as those in Mode 1 operation in due course. The three circuit parameters are respectively:

- The timing factor Δ_1, which determines the initial resonant inductor current $i_{Lr}(0) = -\Delta_1 I_0$ when the MOSFET Q_1 turns off. I_0 is the average current in the inductor main windings L_{1p} and L_{2p} over the duration when the voltage clamping circuit is not active. The initial inductor current is zero in the operation mode shown in Figure 3.

- The load factor k, defined by $I_0 Z_0 = kV_d$, where $Z_0 = \sqrt{L_r/C_1} = \sqrt{L_r/C_2}$ is the characteristic impedance of the resonant tank made up by the resonant inductor and capacitors and V_d is the output capacitor voltage referred to the transformer primary winding. L_r is the effective resonant inductor and C_1 and C_2 are the effective resonant capacitors.

- The delay angle α_d, defined as the angle between the instant when the resonant inductor current reaches zero and the instant when the corresponding MOSFET turns off, which respectively corresponds to $\omega_0 t'$ and $\omega_0 t''$ in Figure 3. It can be found that $\alpha_d = \omega_0 t'' - \omega_0 t'$, where $\omega_0 = 1/\sqrt{L_r C_1} = 1/\sqrt{L_r C_2}$ is the characteristic angular frequency of the resonant tank.

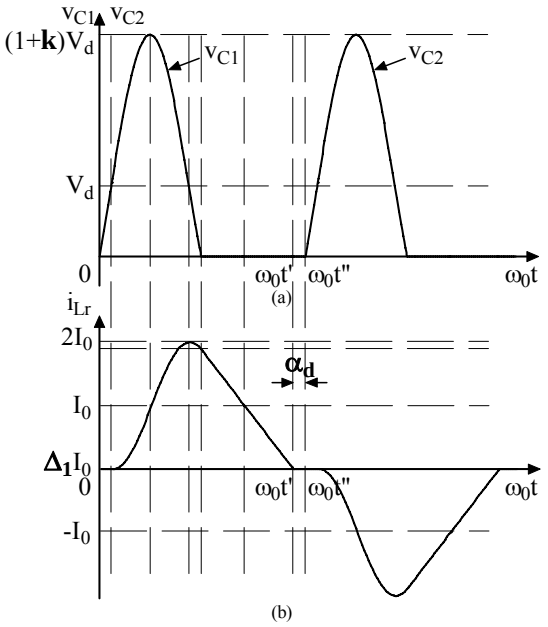

Figure 3: Resonant Waveforms of One Operation Mode (a) Capacitor Voltage (b) Inductor Current

3. THREE OPERATION MODES

It can be identified that the two-inductor boost converter with the voltage clamp shown in Figure 2 can operate in three different modes depending on the combinations of the two circuit parameters including the load and the timing factors as the delay angle does not affect whether or when the voltage clamping circuit becomes active in the converter operation. The state analyses of one mode where the voltage clamping circuit remains inactive in the converter operation and two modes where the voltage clamping circuit becomes active in the converter operation will be provided in this section.

In the individual modes, the values of Δ_1 and k will only be qualitatively discussed as the quantitative analysis requires the exact numerical value of the turns ratio of the coupled inductor n_L. Before Q_1 turns off, both of Q_1 and Q_2 are on. The possible states after Q_1 turns off and before Q_2 turns off will be shown for each mode as follows.

3.1. MODE 1

In this mode, the timing factor Δ_1 and the load factor k are both small (Δ_1 can be zero) or both medium and the switch voltage does not reach the clamping voltage V_c in the converter operation at all. Therefore, the voltage clamping circuit remains inactive and the converter topology shown in Figure 2 can be simplified to that shown in Figure 1. The converter will move through up to four states as shown in Figure 4 [11]. The equations for the capacitor voltage v_{C1} and the inductor current i_{Lr} in each state are listed in Table 1.

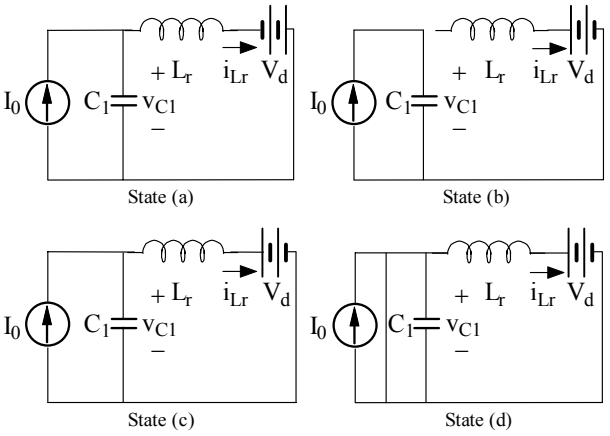

Figure 4: Four Possible States in Mode 1

State	Equations	
State (a) $0 \le t \le t_1$	$v_{C1}(t) = (1+\Delta_1) I_0 Z_0 \sin\omega_0 t + V_d \cos\omega_0 t - V_d$	(2)
	$i_{Lr}(t) = (V_d/Z_0)\sin\omega_0 t - (1+\Delta_1) I_0 \cos\omega_0 t + I_0$	(3)
State (b) $t_1 \le t \le t_2$	$v_{C1}(t) = (I_0/C_1)(t-t_1) + v_{C1}(t_1)$	(4)
	$i_{Lr}(t) = 0$	(5)
State (c) $t_2 \le t \le t_3$	$v_{C1}(t) = I_0 Z_0 \sin\omega_0 (t-t_2) + V_d + [v_{C1}(t_2) - V_d]\cos\omega_0 (t-t_2)$	(6)
	$i_{Lr}(t) = \{[v_{C1}(t_2) - V_d]/Z_0\}\sin\omega_0 (t-t_2) - I_0 \cos\omega_0 (t-t_2) + I_0$	(7)
State (d) $t_3 \le t \le t_4$	$v_{C1}(t) = 0$	(8)
	$i_{Lr}(t) = i_{Lr}(t_3) - (V_d/L_r)(t-t_3)$	(9)

Table 1: Equations in Each State in Mode 1

3.2. MODE 2

In this mode, the timing factor Δ_1 is greater than zero and the load factor k is large enough and the voltage clamping circuit becomes active in State (a) in Figure 4. The converter will move through five states as shown in Figure 5. The equations for the capacitor voltage v_{C1} and the inductor current i_{Lr} in each state are listed in Table 2.

In States (b) and (c), the diode D_{L1} conducts and the resonant capacitor voltage v_{C1} is clamped to V_c. The coupled inductor can be modelled by an equivalent circuit made up of a single-winding inductor L_e, a diode D_c and a voltage source V_c. The inductor L_e has the same number of turns as L_{1p} therefore the inductor L_e current must be I_0 in order to maintain the flux linkage or the Ampere-turns balance. In these states, the resonant inductor current i_{Lr} is also the coupled inductor main winding current and the diode D_c current i_{Dc} is the coupled inductor clamp winding current reflected to the main winding. It can be observed from Equation (13) that one condition for ZVS operation is $V_c \geq 2V_d$.

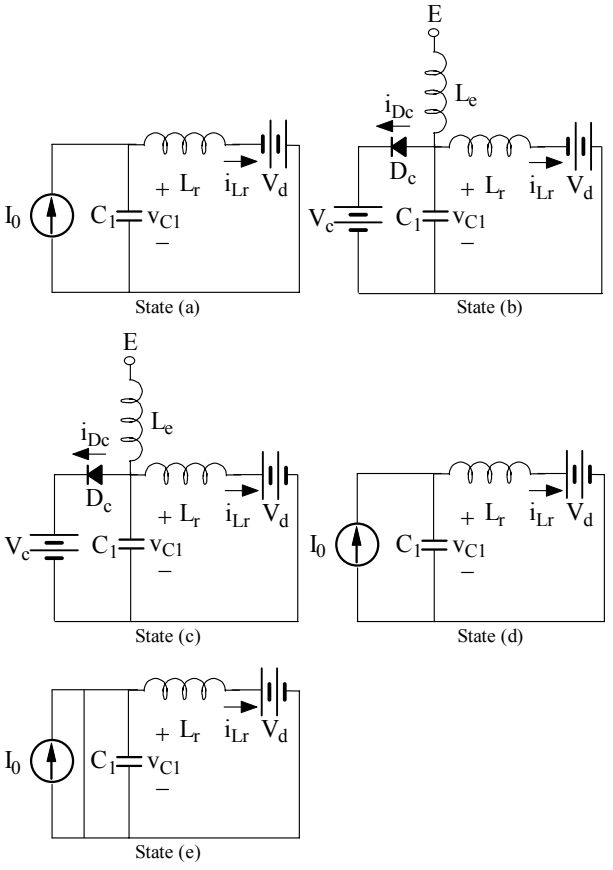

Figure 5: Five Possible States in Mode 2

State	Equations	
State (a) $0 \leq t \leq t_1$	$v_{C1}(t) = (1+\Delta_1)I_0 Z_0 \sin\omega_0 t + V_d \cos\omega_0 t - V_d$	(2)
	$i_{Lr}(t) = (V_d/Z_0)\sin\omega_0 t - (1+\Delta_1)I_0 \cos\omega_0 t + I_0$	(3)
State (b) $t_1 \leq t \leq t_2$	$v_{C1}(t) = V_c$	(10)
	$i_{Lr}(t) = i_{Lr}(t_1) + [(V_c + V_d)/L_r](t - t_1)$	(11)
State (c) $t_2 \leq t \leq t_3$	$v_{C1}(t) = V_c$	(10)
	$i_{Lr}(t) = i_{Lr}(t_2) + [(V_c - V_d)/L_r](t - t_2)$	(12)
State (d) $t_3 \leq t \leq t_4$	$v_{C1}(t) = (V_c - V_d)\cos\omega_0(t - t_3) + V_d$	(13)
	$i_{Lr}(t) = [(V_c - V_d)/Z_0]\sin\omega_0(t - t_3) + I_0$	(14)
State (e) $t_4 \leq t \leq t_5$	$v_{C1}(t) = 0$	(8)
	$i_{Lr}(t) = i_{Lr}(t_4) - (V_d/L_r)(t - t_4)$	(15)

Table 2: Equations in Each State in Mode 2

3.3. MODE 3

In this mode, the timing factor Δ_1 is small and the load factor k is medium or Δ_1 is zero and k is large and the voltage clamping circuit becomes active in State (c) shown in Figure 4. The converter will move through up to six states as shown in Figure 6. The equations for the capacitor voltage v_{C1} and the inductor current i_{Lr} in each state are listed in Table 3.

In Mode 3, State (d) is the only voltage clamping state and can be analysed as discussed in Section 3.2.

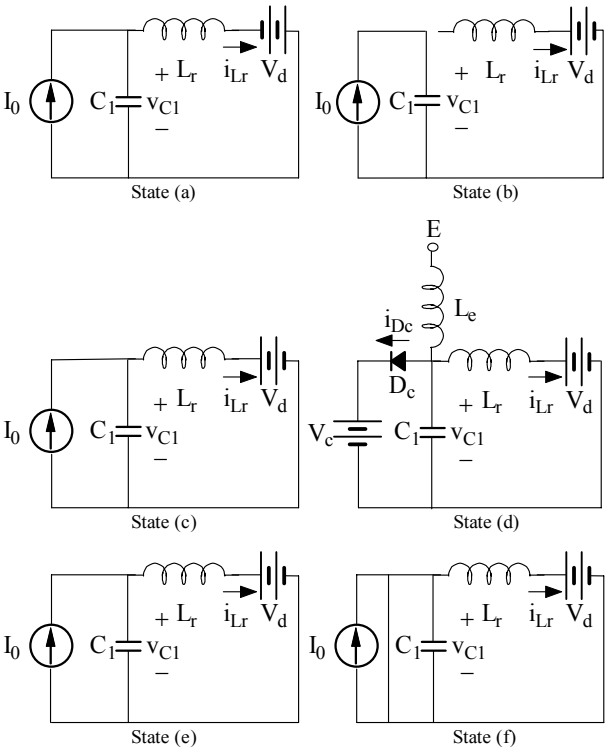

Figure 6: Six Possible States in Mode 3

State	Equations	
State (a) $0 \leq t \leq t_1$	$v_{C1}(t) = (1+\Delta_1)I_0 Z_0 \sin\omega_0 t + V_d \cos\omega_0 t - V_d$	(2)
	$i_{Lr}(t) = (V_d/Z_0)\sin\omega_0 t - (1+\Delta_1)I_0 \cos\omega_0 t + I_0$	(3)
State (b) $t_1 \leq t \leq t_2$	$v_{C1}(t) = (I_0/C_1)(t - t_1) + v_{C1}(t_1)$	(4)
	$i_{Lr}(t) = 0$	(5)
State (c) $t_2 \leq t \leq t_3$	$v_{C1}(t) = I_0 Z_0 \sin\omega_0(t - t_2) + V_d + [v_{C1}(t_2) - V_d]\cos\omega_0(t - t_2)$	(6)
	$i_{Lr}(t) = \{[v_{C1}(t_2) - V_d]/Z_0\}\sin\omega_0(t - t_2) - I_0 \cos\omega_0(t - t_2) + I_0$	(7)
State (d) $t_3 \leq t \leq t_4$	$v_{C1}(t) = V_c$	(10)
	$i_{Lr}(t) = i_{Lr}(t_3) + [(V_c - V_d)/L_r](t - t_3)$	(16)
State (e) $t_4 \leq t \leq t_5$	$v_{C1}(t) = (V_c - V_d)\cos\omega_0(t - t_4) + V_d$	(17)
	$i_{Lr}(t) = [(V_c - V_d)/Z_0]\sin\omega_0(t - t_4) + I_0$	(18)
State (f) $t_5 \leq t \leq t_6$	$v_{C1}(t) = 0$	(8)
	$i_{Lr}(t) = i_{Lr}(t_5) - (V_d/L_r)(t - t_5)$	(19)

Table 3: Equations in Each State in Mode 3

4. CONVERTER DESIGN

The ZVS two-inductor boost converter with the voltage clamp is able to operate in two regions: Region 1 where $\Delta_1 = 0$ and $\alpha_d \geq 0$ and Region 2 where $\Delta_1 > 0$ and $\alpha_d = 0$. It is also required that $k \geq 1$ to maintain ZVS conditions in both regions. As a higher output voltage appears in Region 1, the maximum output voltage, 340 V, must be designed in Region 1. Therefore the converter design process in Region 1 is given first. That in Region 2 is similar and will be given briefly in due course. An input voltage of 20 V and a load resistance of 576 Ω are also used in the converter design.

In order to design the converter parameters such as L_r, C_1 or C_2 and the transformer turns ratio n, α_d and k must be given initially. When the voltage clamping circuit is active, part of the energy stored in the resonant tank will be fed back to the voltage source E through the inductor clamp windings. Therefore, the average input power of the converter P_{IN} is not $E \cdot 2I_0$ as in the converter shown in Figure 1 and must be established first.

If $\hat{T}$ is defined as the half switching period, t_c is defined as the duration when the resonant capacitor voltage is clamped within $\hat{T}$, t_{nc} is defined as the duration when the voltage clamping circuit is not active within $\hat{T}$, $\hat{g}_{\alpha,c}(\alpha_d, k)$ is defined as the ratio of the average resonant inductor current against a specific set of α_d and k values to I_0 over the duration when the resonant capacitor C_1 voltage is clamped, Equations (20) and (21) can be derived as follows:

$$\hat{T} = t_c + t_{nc} \tag{20}$$

$$P_{IN} = E \cdot 2I_0 - EI_0 (n_L + 1)[1 - \hat{g}_{\alpha,c}(\alpha_d, k)]t_c / \hat{T} \tag{21}$$

By defining $\hat{r}_\alpha(\alpha_d, k)$ to be

$$\hat{r}_\alpha(\alpha_d, k) = (n_L + 1)[1 - \hat{g}_{\alpha,c}(\alpha_d, k)]t_c / \hat{T} \tag{22}$$

Equation (21) can be simplified as:

$$P_{IN} = E \cdot 2I_0 - EI_0 \hat{r}_\alpha(\alpha_d, k) \tag{23}$$

Therefore four design equations can be established:

$$E \cdot 2I_0 - EI_0 \hat{r}_\alpha(\alpha_d, k) = V_O^2 / R \tag{24}$$

$$V_d \hat{g}_\alpha(\alpha_d, k) I_0 = V_O^2 / R \tag{25}$$

$$I_0 Z_0 = kV_d \tag{26}$$

$$V_O = nV_d \tag{27}$$

where E is the input source voltage, V_O is the output load voltage and R is the load resistance. Function $\hat{g}_\alpha(\alpha_d, k)$ is the ratio of the average of the absolute current in the resonant inductor or the transformer primary to I_0 and is determined by two independent variables, α_d and k. From Equations (24) to (27), if E, V_O and R are also known, I_0, V_d, Z_0 and n can be solved. Then the converter parameters including L_r and C_1 or C_2 can be easily obtained once the converter switching frequency f_c is selected.

As an example in the converter design, an initial set of the circuit parameters are selected to be $\alpha_d = 4$ and $k = 25$ and the calculation results obtained from Equations (24) to (27) are listed in Table 4.

I_0 (A)	$\hat{g}_\alpha(\alpha_d, k)$	V_d (V)	$\hat{r}_\alpha(\alpha_d, k)$	n	Z_0 (Ω)
9.39	0.494	43.1	0.934	7.9	114.75

Table 4: Initial Calculation Results in Region 1

After the values of L_r, C_1 or C_2 and n are calculated through the design equations, the load factor k is no longer an independent variable deciding V_d or V_O. Then the dependent variable k needs to be removed from Equations (24) and (25), which can be respectively rewritten by replacing $\hat{r}_\alpha(\alpha_d, k)$ with $r_\alpha(\alpha_d)$ and $\hat{g}_\alpha(\alpha_d, k)$ with $g_\alpha(\alpha_d)$ to Equations (28) and (29):

$$E \cdot 2I_0 - EI_0 r_\alpha(\alpha_d) = V_O^2 / R \tag{28}$$

$$V_d \cdot g_\alpha(\alpha_d) \cdot I_0 = V_O^2 / R \tag{29}$$

Manipulations of Equations (28) and (29) yield:

$$V_d = [2 - r_\alpha(\alpha_d)]E / g_\alpha(\alpha_d) \tag{30}$$

Equation (30) is clearly in the format of the control function for the ZVS two-inductor boost converter with the voltage clamp, relating the transformer primary voltage V_d to the circuit delay angle α_d. However, function $g_\alpha(\alpha_d)$ cannot be solved directly. An indirect method is to maintain the load factor k as a variable initially in Equation (30) as:

$$V_d = [2 - \hat{r}_\alpha(\alpha_d, k)]E / \hat{g}_\alpha(\alpha_d, k) \tag{31}$$

and then to eliminate it by applying the inherent circuit constraint obtained through Equations (25) to (27):

$$k = n^2 Z_0 / [R\hat{g}_\alpha(\alpha_d, k)] \tag{32}$$

As the analytical solution of function $\hat{g}_\alpha(\alpha_d, k)$ in Equation (31) consists of the inverse trigonometric functions and presents a significant level of complexity, function $\hat{g}_\alpha(\alpha_d, k)$ is solved numerically by MATLAB against a range of α_d and k values through the state analysis of the converter. Figure 7 shows the surface V_d where $0 \leq \alpha_d \leq 4$ and $10 \leq k \leq 25$. Then the two functions in Equation (32) $h_{1,\alpha}(\alpha_d, k) = k$ and $h_{2,\alpha}(\alpha_d, k) = n^2 Z_0 / [R\hat{g}_\alpha(\alpha_d, k)]$ are drawn in Figure 8. The intersection curve u_α represents the numerical relationship between α_d and k, which is back substituted to Equation (31) to remove the dependent variable k and derive the control function in its numerical form. Then the control function can be obtained by polynomial fitting as in Equation (33) and plotted in Figure 9.

$$V_d = M_\alpha(\alpha_d) = 0.0024\alpha_d^3 - 0.0413\alpha_d^2 + 0.9032\alpha_d + 40.0161 \tag{33}$$

In Region 2, the design equations share the same format of their counterparts in Region 1 except that the variable α_d needs to be replaced by Δ_1 and the subscript α by Δ.

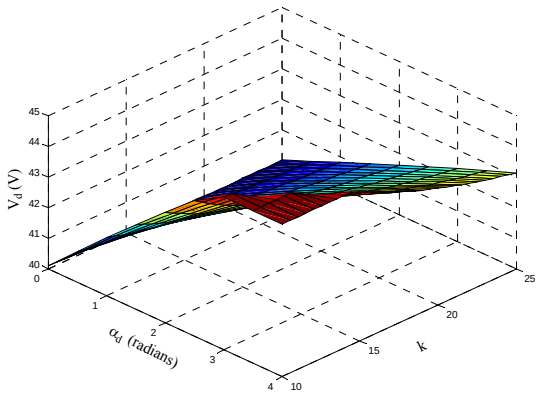

Figure 7: Surface V_d in Region 1

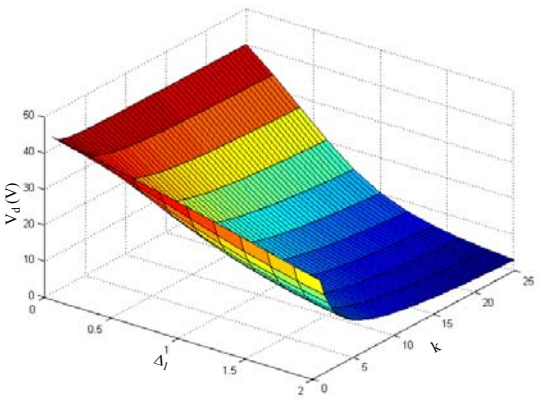

Figure 10: Surface V_d in Region 2

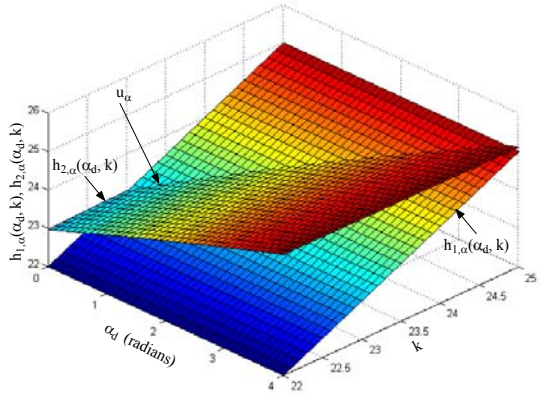

Figure 8: Surfaces $h_{1,\alpha}(\alpha_d, k)$ and $h_{2,\alpha}(\alpha_d, k)$

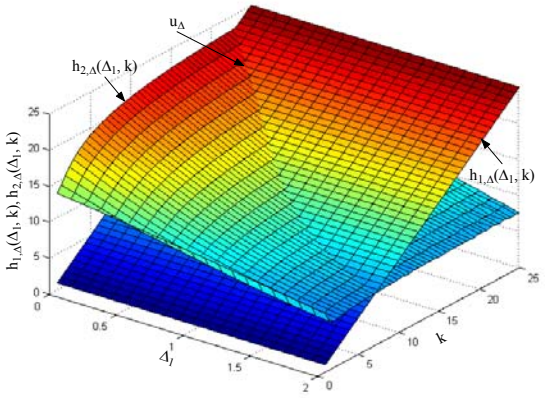

Figure 11: Surfaces $h_{1,\Delta}(\Delta_1, k)$ and $h_{2,\Delta}(\Delta_1, k)$

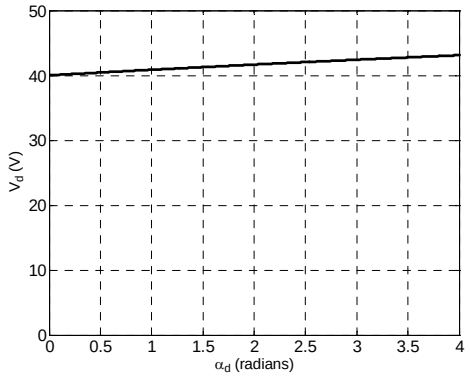

Figure 9: Control Function $M_\alpha(\alpha_d)$

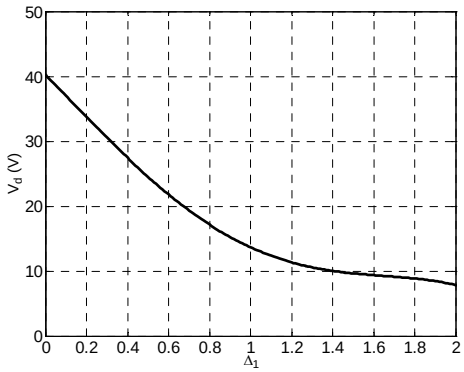

Figure 12: Control Function $M_\Delta(\Delta_1)$

In this region, k continues to decrease. Figure 10 shows the surface V_d where $0 \le \Delta_1 \le 2$ and $1 \le k \le 25$. The surfaces $h_{1,\Delta}(\Delta_1, k)$ and $h_{2,\Delta}(\Delta_1, k)$ are drawn in Figure 11. The intersection curve u_Δ determines the numerical relationship between Δ_1 and k, which is substituted to the counterpart of Equation (31). Through polynomial fitting, the control function can be found as in Equation (34) and plotted in Figure 12.

$$V_d = M_\Delta(\Delta_1) = -4.4120\Delta_1^4 + 15.8906\Delta_1^3 - 6.4097\Delta_1^2 - 31.6496\Delta_1 + 40.2458 \quad (34)$$

It is worth noting that the voltage V_d will further decrease when $\Delta_1 > 2$. However, the change of V_d is very likely to be small according to the tendency shown in Figure 12. As k is relatively large in the design, the voltage clamping circuit always becomes active in the converter operation in the entire operating range and the converter only operates in Modes 2 and 3 in this case.

If 1 MHz is selected as the maximum converter switching frequency f_c, corresponding to 500-kHz device switching frequency, the two border operating points can be summarised as in Table 5.

Δ_1	α_d (radians)	k	V_O (V)	f_c (kHz)	ω_0 (Mrad/s)	L_r (μH)	C_1, C_2 (nF)
2.0	0	7.19	64	1000	6.676	17.19	1.31
0	4.0	25.00	340	121			

Table 5: Two Border Operating Points

It can be observed from Table 5 that the ratio of the maximum to the minimum output voltages is 5.3, which is much higher than that achieved by the resonant converter without the voltage clamp. A higher ratio of the maximum to the minimum voltages can be obtained by a higher value of k in the initial converter design.

5. THEORETICAL AND SIMULATION WAVEFORMS

Three operating points in the operating range are listed in Table 6 and their corresponding theoretical and simulation waveforms are shown in Figures 13 to 18. From top to bottom, the waveforms are respectively the MOSFET gate voltage, the resonant capacitor voltage and the resonant inductor current. The theoretical and the simulation waveforms agree reasonably well.

Δ_1	α_d (radians)	k	Theoretical Waveforms	Simulation Waveforms
0	4.0	25.00	Figure 13	Figure 16
0	0	23.04	Figure 14	Figure 17
2.0	0	7.19	Figure 15	Figure 18

Table 6: Three Selected Operating Points

6. COMPARISON OF THE TWO CONVERTERS

Table 7 provides a comparison of several parameters in the two ZVS converters. Compared with the ZVS two-inductor boost converter shown in Figure 1, the proposed converter is able to achieve a much wider output voltage range with a much lower switch voltage stress. However the trade off is a potential lower efficiency due to a larger resonant inductor, a larger *dv/dt* over MOSFET switching transitions and a higher energy circulation.

7. CONCLUSIONS

This paper studies the ZVS two-inductor boost converter with the voltage clamp, which is able to achieve a maximum to minimum output voltage ratio of 5.3 with 90-V switch voltage stress. Both the state analyses of the three operation modes and the design process of the 200-W converter are elaborated. The theoretical and the simulation waveforms are provided for three selected operating points at the end of the paper. However, if no further measures are taken, the efficiency of the converter with the voltage clamp is likely to be lower than that without the voltage clamp and this remains a challenge in the hardware implementations of the ZVS two-inductor boost converter with the voltage clamp.

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Parameter	ZVS Two-Inductor Boost Converter without the Voltage Clamp	ZVS Two-Inductor Boost Converter with the Voltage Clamp
Output Voltage Range	147 V to 340 V	64 V to 340 V
Switch Voltage Stress	200 V	90 V
Converter Switching Frequency Range	328 kHz to 1 MHz	121 kHz to 1 MHz
Resonant Inductance and Capacitance	6.85 μH and 8.82 nF	17.19 μH and 1.31 nF
MOSFET turn-on and turn-off *dv/dt*	Small	Large
Circulated Energy	Low	High

Table 7: Comparison of Two ZVS Converters

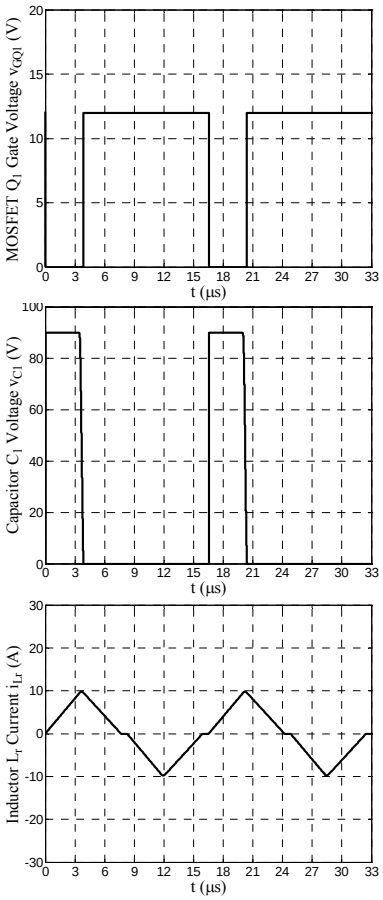

Figure 13: Theoretical Waveforms

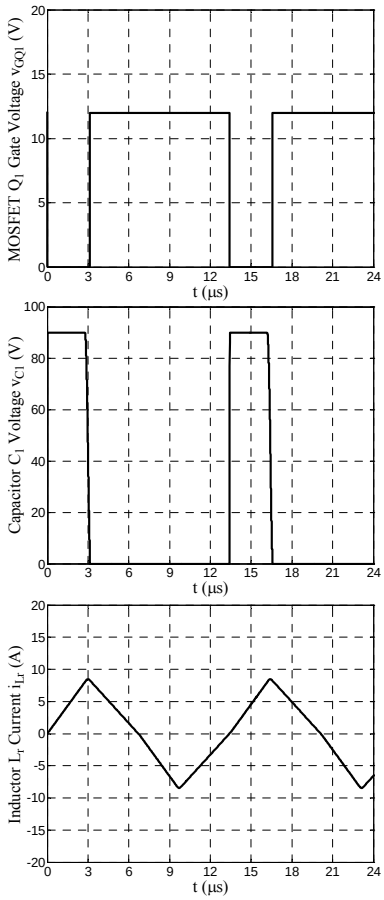

Figure 14: Theoretical Waveforms

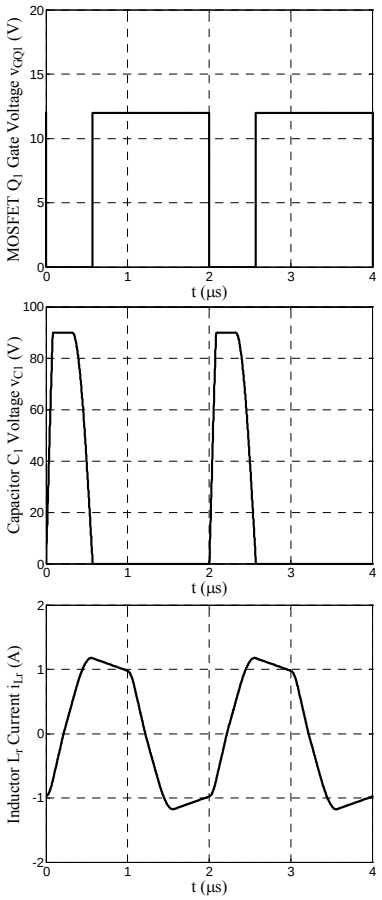

Figure 15: Theoretical Waveforms

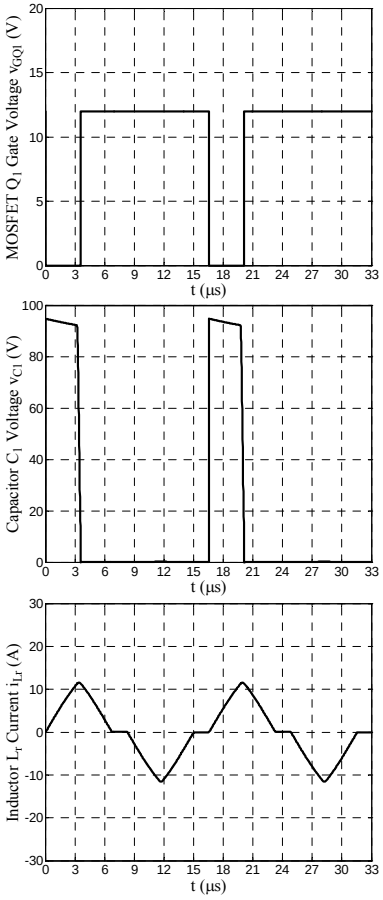

Figure 16: Simulation Waveforms

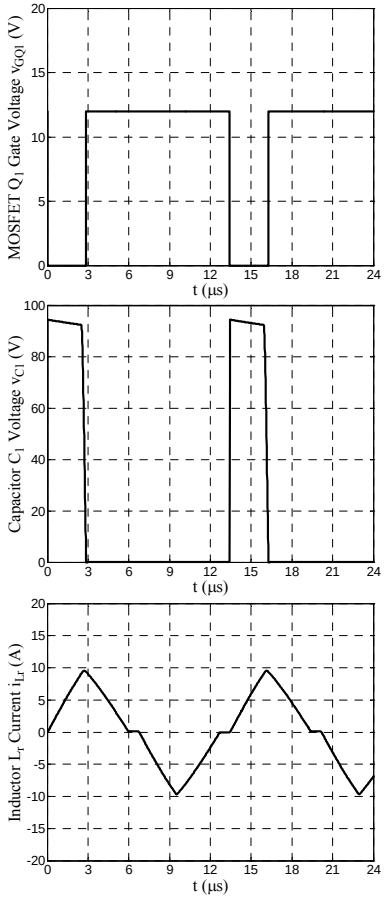

Figure 17: Simulation Waveforms

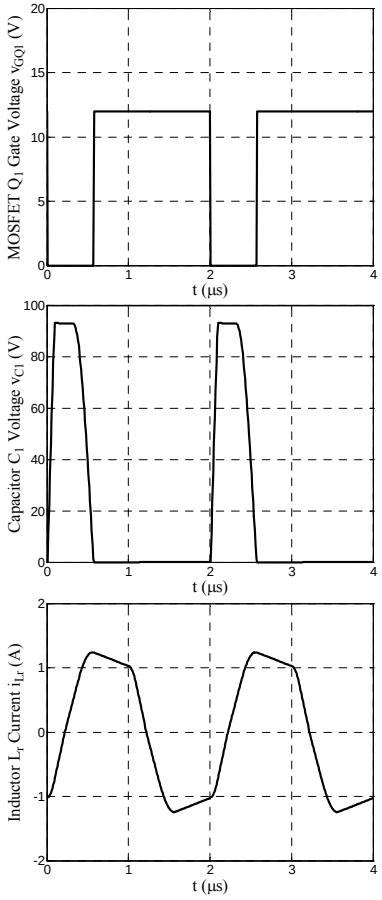

Figure 18: Simulation Waveforms