Steady-State Analysis and Designing Impedance Network of Z-Source Inverters

Sumedha Rajakaruna, *Senior Member, IEEE*, and Laksumana Jayawickrama

***Abstract*—All possible steady states of a Z-source inverter are identified and analyzed with the objective of deriving design guidelines for the symmetrical impedance network. This paper shows that, in addition to the desired three dynamic states, an operating cycle can contain another three static states that do not contribute to the power conversion process. These three static states can be avoided by selecting suitably large capacitors and inductors. By using the equations derived in the steady-state analysis, this paper presents guidelines to design the impedance network accurately for the case where the inverter is operated only in active and shoot-through states. The proposed design method can also be used to predict the critical values of capacitance and inductance below which static states appear during the operating cycle. Computer simulations and laboratory experiments are used to verify the design method and to demonstrate the appearance of static states when the capacitors and inductors are sized lower than their critical values.**

***Index Terms*—Impedance network, operating states, ripple factor, Z-source.**

I. Introduction

DUE TO THE recent advancements in the fields of energy conversion and energy storage, a need has arisen to design inverters which can operate successfully with variable-voltage sources such as fuel cells and ultracapacitors. The conventional voltage source inverter (VSI), which is the most commonly used type of inverter, suffers from the drawback that it cannot boost the voltage of the input source. Thus, a separate voltage-boosting dc/dc converter is needed to interface the variable-voltage source with the conventional VSI. This cascaded arrangement of two power converters increases not only the complexity of circuitry and control but also the cost and the space requirement. In order to satisfy the pressing needs for a single converter that is capable of both voltage boosting and inversion, many new inverter topologies have been proposed in the recent past. [1], [2]. Among these new topologies, Z-source inverter (ZSI) has attracted wide attention over the others mainly because it continues to employ a conventional VSI as the power converter yet with a modified dc-link stage [2]–[18].

Manuscript received October 19, 2005; revised July 18, 2006; accepted August 18, 2006. Date of publication April 15, 2010; date of current version June 11, 2010.

S. Rajakaruna was with Nanyang Technological University, Singapore. He is now with Curtin University of Technology, Perth, W.A. 6845, Australia (e-mail: s.rajakaruna@curtin.edu.au).

L. Jayawickrama was with Nanyang Technological University, Singapore. He is now with Parsons Brinckerhoff, Melbourne, Vic. 3006, Australia (e-mail:ljayawickrama@pb.com.au).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIE.2010.2047990

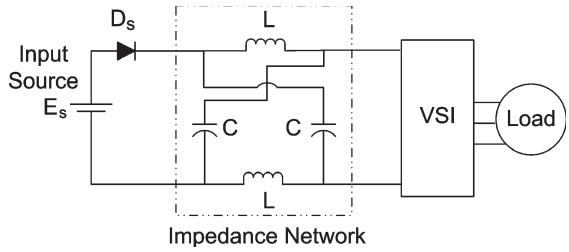


Fig. 1. ZSI with a symmetrical impedance network.

As shown in Fig. 1, a diode (D_s) and an impedance network connected between the variable dc voltage source and the conventional VSI are the main differences in the power circuit. As can be seen in the figure, a symmetrical impedance network consists of two identical inductors and two identical capacitors connected in a specific manner to achieve the desired properties. The impedance network changes the circuit configuration from that of a voltage source to an impedance source (i.e., Z-source). It allows the VSI to be operated in a new state called the shoot-through state in which the two switching devices in the same inverter leg are simultaneously switched-on to effect a short circuit to the dc link. As the capacitors may be charged to higher voltages than the input source voltage, the diode D_s is necessary to prevent discharging of them through the input source.

Due to the obvious advantages of ZSI, it has been adopted for various applications, as evident from recent literature [3]–[9]. They include ac motor drives [3], fuel cell vehicles [4], uninterruptible power supplies [5], residential photovoltaic systems [6], electronic loads [7], wind power conversion [8], and distributed generation [9]. Furthermore, new converter topologies based on the ZSI concept have also been proposed to improve the performance of the original converter in specific applications [9]–[13]. Some of the currently available literature on ZSI [14]–[16] mainly focuses on how to control the switching devices of the VSI with the additional degree of freedom brought in by the shoot-through state. Maximizing the voltage-boost ratio while minimizing the device stresses is the aim of most of the work published so far in this area. However, only a few publications can be found on the topic of designing the impedance network of the ZSI and the possible modes of operation in steady state. Shen and Peng [17] have identified five possible states of operation when the inductance becomes low. However, the capacitance is still assumed to be large, and there is no method proposed to calculate the critical values of inductance and capacitance below which unwanted operating modes would appear. Both the capacitor and inductor are assumed to vary

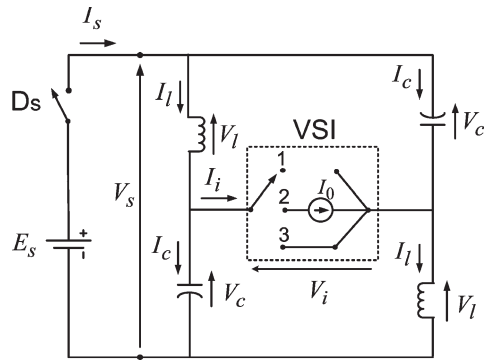


Fig. 2. Switching equivalent of ZSI.

over a large range, and the waveforms are considered to be nonlinear in [18]. Consequently, it systematically shows that there are six possible operating states. However, a guideline to size the inductor and capacitor so that ZSI does not operate in the unnecessary operating states has not been presented so far. Therefore, the objective of this paper is to present such a design guideline, after presenting a clear analysis of the steady-state operation of the impedance network. It also demonstrates how the critical values of inductance and capacitance can be calculated.

The next section of this paper is devoted to a detailed steady-state analysis of ZSI. The set of nonlinear equations derived in Section II is then used in Section III to propose a method to size the impedance network for the case where the inverter operates only in active and shoot-through states. Computer simulations and experimental results are presented in Section IV to verify the accuracy of the design method. Finally, derived conclusions are presented in Section V.

II. Steady-State Analysis of ZSI

The operating state of the impedance network at the dc link is decided by the switching states of the semiconductor devices on its input and output terminals. As shown in Fig. 2, the diode D_s on its input side has two switching states as "On" and "Off," and the VSI on its output side has three switching states as 1, 2, and 3. In state 1, which is known as "Open" state [2], VSI applies one of the two zero-switching vectors to the load while open circuiting its input terminals. Similarly, in state 2, known as "Active" state [2], VSI applies one of the six nonzero-switching vectors to the load while drawing a load-dependent current from its input source. The current drawn from the impedance network during this state can be represented by a constant current source I_0 by neglecting its ripple content [2]. A conventional VSI can only be operated in one of these two input states. However, with the impedance network on the dc link, the VSI of the ZSI can be operated in a third input state, which is known as the "Shoot-Through" state [2]. During this state, input terminals of the VSI are effectively short-circuited by switching on the devices at the top and bottom of one or more of its three legs. Thus, in general, the impedance network of the ZSI at a given time can operate in any one of the six possible states given in Table I.

TABLE I
Possible Operating States of the Impedance Network

VSI	Open		Active		Shoot-Through	
Diode (D_s)	On	Off	On	Off	Off	On
Impedance Network	Open-1	Open-2	Active-1	Active-2	Sh.Th.-1	Sh.Th.-2

During a switching cycle of the VSI, the impedance network may operate in up to a maximum of six states. However, as will be seen later in the following sections, the Open-1, Active-1, and Shoot-Through-1 states are the desired states in practical applications. The other three states, namely, Open-2, Active-2, and Shoot-Through-2 states, are undesirable and are to be avoided by proper sizing of the inductors and capacitors of the impedance network.

Prior to analyzing the voltage–current variations in each of the six possible states, the common equations that describe the impedance network in general can be written as

$$V_l = L(dI_l/dt) \qquad I_c = C(dV_c/dt) \tag{1}$$

$$V_s = V_c + V_l \qquad I_s = I_c + I_l \tag{2}$$

$$V_i = V_c - V_l \qquad I_i = I_l - I_c \tag{3}$$

where V_l and I_l are the voltage across and current through any of the two inductors, V_c and I_c are the voltage and current of any of the capacitors, V_s and I_s are the voltage and current at the input terminals of the impedance network connected to the source through the diode, and V_i and I_i are the voltage and current at the input terminals of the VSI. The characteristics of each operating state can be described separately, as given in the following sections by neglecting the presence of parasitic resistances of the source, inductors, and the capacitors.

A. Open-1 State

The equations that define the Open-1 state are given by

$$V_s = E_s \qquad I_i = 0. \tag{4}$$

By substituting (4) in (1)–(3), the voltage across the capacitor and its current can be expressed as

$$\frac{d^2V_c}{dt^2} + \frac{V_c}{LC} = \frac{E_s}{LC}$$

$$V_c = E_s + X_O \sin(\omega t + \Phi_O) \tag{5}$$

$$I_c = I_l = I_s/2 = X_O \omega C \cdot \cos(\omega t + \Phi_O) \tag{6}$$

where

$$\omega = 1/\sqrt{LC} \tag{7}$$

$$X_O = \sqrt{(V_{ciO} - E_s)^2 + [I_{liO}/(C\omega)]^2} \tag{8}$$

$$\Phi_O = \tan^{-1}\left((V_{ciO} - E_s)\omega C/I_{liO}\right) \tag{9}$$

with the initial values of capacitor voltage and inductor current in Open-1 state denoted by V_{ciO} and I_{liO}, respectively. With positive values of V_{ciO} and I_{liO}, the range of the initial angle

is $\Phi_0 < \pi/2$. As a result, the capacitor voltage will increase in a sinusoidal manner with time. Furthermore, the inductor and output voltages in this state are given by

$$V_l = E_s - V_c \qquad V_i = 2V_c - E_s. \tag{10}$$

At $\omega t + \Phi_O = \pi/2$, the capacitor voltage achieves its peak value, and the inductor and source currents drop to zero. If the VSI is operated in Open state beyond the limiting time of $t_{O\max} = (\pi/2 - \Phi_O)/\omega$, the diode D_s would turn off as the source current tries to flow in the reverse direction. This signifies the end of Open-1 state and the beginning of Open-2 state.

B. Open-2 State

In the Open-2 state, the diode remains in the OFF state and the VSI in the Open state. Therefore, the state-defining equations are given as

$$I_s = 0 \qquad I_i = 0. \tag{11}$$

Since the impedance network remains isolated from the source and the load, all the system variables remain constant during this state. In order to avoid this state, the necessary condition can be seen as

$$I_{lfO} > 0 \tag{12}$$

where I_{lfO} is the final value of inductor current in the Open-1 state.

C. Active-1 State

As can be seen in the equivalent circuit given in Fig. 2, the only difference between Open-1 and Active-1 states is the presence of the constant current source I_0 across the input terminals of the VSI.

The state-defining equations for Active-1 state are

$$V_s = E_s \qquad I_i = I_0. \tag{13}$$

Substituting (13) in (1)–(3), the capacitor voltage and system currents can be derived as

$$V_c = E_s + X_A \sin(\omega t + \Phi_A) \tag{14}$$

$$I_c = I_l - I_0 = (I_s - I_0)/2 = X_A \omega C \cdot \cos(\omega t + \Phi_A) \tag{15}$$

where

$$X_A = \sqrt{(V_{ciA} - E_s)^2 + [(I_{liA} - I_0)/(C\omega)]^2} \tag{16}$$

$$\Phi_A = \tan^{-1}\left((V_{ciA} - E_s)\omega C/(I_{liA} - I_0)\right) \tag{17}$$

with the initial values of the capacitor voltage and inductor current in Active-1 state given by V_{ciA} and I_{liA}, respectively. As for the inductor voltage and output current, their relationships with capacitor voltage, as given by (10), hold true even for the Active-1 state. Comparing (14) and (15) with those for the Open-1 state given in (5) and (6), it can be seen that Open-1 state is a special case of Active-1 state, where $I_0 = 0$. As the load current I_0 increases from zero, the peak value of the sinusoidal components of both capacitor voltage and inductor current will decrease and reach a minimum when $I_0 = I_{lA}$. Furthermore, the initial angle Φ_A will increase with increasing I_0 and reach a value of $\pi/2$ at $I_0 = I_{liA}$.

From (15), it can be seen that the current through the diode I_s will be zero and the diode will turn off when $I_l = -I_c = I_0/2$. It is interesting to note here that the capacitor voltage charges to the peak value and then discharges before approaching the above operating point which marks the end of Active-1 state and the beginning of Active-2 state. If the duration of the Active-1 period is t_A, the final values of the two state variables can be written as

$$V_{cfA} = E_s + X_A \sin(\omega t_A + \Phi_A) \tag{18}$$

$$I_{lfA} = I_0 + X_A \omega C \cdot \cos(\omega t_A + \Phi_A). \tag{19}$$

D. Active-2 State

The state-defining equations for Active-2 state are

$$I_i = I_0 \qquad I_s = 0. \tag{20}$$

Substituting (20) in (2) and (3), it can be seen that the currents remain constant at $I_l = -I_c = I_0/2$ and the capacitor discharges linearly with time at the rate of $I_0/(2C)$.

In order to avoid Active-2 state from appearing during operation, the necessary condition is

$$I_{lfA} > I_0/2. \tag{21}$$

E. Shoot-Through-1 State

The state-defining equations for shoot-through-1 state are

$$I_s = 0 \qquad V_i = 0. \tag{22}$$

Substituting (22) in (1)–(3), the capacitor voltage and its current can be found as

$$V_c = V_l = V_s/2 = X_S \sin(\omega t + \Phi_S) \tag{23}$$

$$I_c = -I_l = X_S \omega C \cdot \cos(\omega t + \Phi_S) \tag{24}$$

where

$$X_S = \sqrt{(V_{ciS})^2 + (-I_{liS}/C\omega)^2} \tag{25}$$

$$\Phi_S = \tan^{-1}(-V_{ciS}\omega C/I_{liS}) \tag{26}$$

with the initial values of capacitor voltage and inductor current in Shoot-Through-1 state given by V_{ciS} and I_{liS}, respectively. Since $\pi/2 < \Phi_S < \pi$ with positive capacitor voltages and inductor currents found in practical converters, the capacitor voltage given by (23) drops from its initial value in a sinusoidal manner with increasing time in this state. Simultaneously, the inductor current given by (24) increases toward its peak value in a sinusoidal manner with increasing time. This indicates that

the energy stored in the capacitors during Open and Active states is transferred to inductors during the Shoot-Through state, thereby allowing the boosting of the voltage applied to the VSI. The Shoot-Through-1 state ends and the Shoot-Through-2 state begins when the diode D_s gets forward biased and comes in to conduction. This occurs when V_s drops to the level of E_s. Thus, from (23), it can be seen that $V_c = E_s/2$ at the end of Shoot-Through-1 state. If the duration of the Shoot-Through-1 state is t_S, the final values of the two state variables can be written as

$$V_{cfS} = X_S \sin(\omega t_S + \Phi_S) \tag{27}$$

$$I_{lfS} = -X_S \omega C \cdot \cos(\omega t_S + \Phi_S). \tag{28}$$

F. Shoot-Through-2 State

The defining equations of Shoot-Through-2 state can be written as

$$V_s = E_s \qquad V_i = 0. \tag{29}$$

Substituting (29) in (1)–(3), it can be seen that $V_c = V_l = E_s/2$ and $I_c = 0$ in this state. Moreover, the inductor current ramps up linearly at a rate of $E_s/(2L)$ with time. Thus, it is unsafe to let the converter operate for long periods in this state, as the increasing currents could soon damage the diode D_s and the switching devices of the VSI. In order to prevent appearing of Shoot-Through-2 state during operation, the necessary condition is

$$V_{cfS} > E_s/2. \tag{30}$$

G. Overview of Operating States

From the preceding discussion, it is clear that the Open-2, Active-2, and Shoot-Through-2 states do not contribute to the power conversion process and should be avoided. Thus, they are named as "static states" in this paper. Practical converters are operated only in two or three of the Open-1, Active-1 and Shoot-Through-1 states. They are hereby named as "dynamic states." Since the three static states appear only when the capacitor voltage and inductor current fluctuate in a wide range, leading to the violation of conditions given in (12), (21), and (30), it is necessary to limit the ripples of the related voltage and current by increasing the sizes of the inductors and capacitors appropriately. Thus, after designing the circuit, a check can be made with these three conditions to ensure the limitation of operation only to the three dynamic states.

III. Designing of Impedance Network

A. Design Based on Sinusoidal Waveforms

As discussed in Section II, Open-1 and Active-1 states behave in a similar manner. Therefore, Open-1 period can be considered as part of the Active-1 period without much error in the design. The three static states are also neglected as they

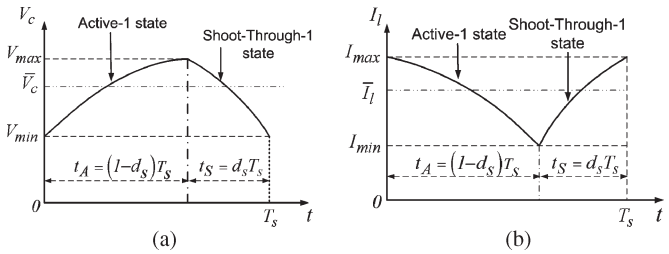


Fig. 3. Steady-state waveforms of (a) capacitor voltage and (b) inductor current.

are not useful to the power conversion process and should be avoided by appropriately sizing the inductors and capacitors. Therefore, ZSI is assumed to be operating only in the Active-1 and Shoot-Through-1 states, as proposed in [2].

Since the final value of a variable in one state is the initial value of the same variable in the other state, the boundary conditions can be defined as

$$V_{ciA} = V_{cfS} = V_{\min} \qquad V_{ciS} = V_{cfA} = V_{\max} \tag{31}$$

$$I_{liA} = I_{lfS} = I_{\max} \qquad I_{liS} = I_{lfA} = I_{\min} \tag{32}$$

where $V_{\min}$ and $V_{\max}$ are the minimum and maximum values of the capacitor voltage and $I_{\min}$ and $I_{\max}$ are the minimum and maximum values of inductor current, respectively. Furthermore, since one switching cycle of VSI consists of only Shoot-Through-1 and Active-1 states, the two periods can be written as $t_S = d_s T_s$ and $t_A = (1 - d_s)T_s$, respectively, where T_s is the period of switching cycle at the dc link and d_s is the duty ratio of the Shoot-Through-1 state. It should be noted here that T_s in these equations is one-half of the switching period of VSI, as the two half cycles of a VSI switching cycle produce identical switching patterns on the dc link. The variables introduced before are used to describe the waveforms of capacitor voltage and inductor current, as shown in Fig. 3(a) and (b), respectively.

By substituting (31) and (32) in (16)–(19) and (25)–(28), they can be rewritten as follows:

$$X_A = \sqrt{(V_{\min} - E_s)^2 + \left[(I_{\max} - I_0)/(\omega C)\right]^2} \tag{33}$$

$$\Phi_A = \tan^{-1}\left[(V_{\min} - E_s)/\left((I_{\max} - I_0)/\omega C\right)\right] \tag{34}$$

$$X_S = \sqrt{(V_{\max})^2 + (-I_{\min}/\omega C)^2} \tag{35}$$

$$\Phi_S = \tan^{-1}\left[V_{\max}/(-\mathrm{I}_{\min}/\omega C)\right] \tag{36}$$

$$F(1) = -V_{\max} + E_s + X_A \sin\left(\omega(1 - d_s)T_s + \Phi_A\right) = 0 \tag{37}$$

$$F(2) = -I_{\min} + I_0 + X_A \omega C \cdot \cos\left(\omega(1 - d_s)T_s + \Phi_A\right) = 0 \tag{38}$$

$$F(3) = -V_{\min} + X_S \sin(\omega d_s T_s + \Phi_S) = 0 \tag{39}$$

$$F(4) = I_{\max} + X_S \omega C \cdot \cos(\omega d_s T_s + \Phi_S) = 0. \tag{40}$$

Since the equivalent dc-link voltage applied to the VSI is given by the average value of V_i during the Active-1 state $(\overline{V}_{iA})$, it can be expressed using (10), (14), and (15) as

$$\overline{V}_{iA} = \frac{1}{t_A}\int_0^{t_A} V_i \cdot dt = E_s + 2[I_{liA} - I_{lfA}] / \left[\omega^2 C(1-d_s)T_s\right]. \tag{41}$$

For a three-phase VSI operated with sinusoidal PWM, the peak value of fundamental line to neutral output voltage (V_m) is given by [19], $M\overline{V}_{iA}/2$, where M is the modulation index. Therefore, by substituting for $\overline{V}_{iA}$ in (41), it can be expressed as

$$F(5) = -2V_m/M + E_s + 2[I_{\max} - I_{\min}] / \left[\omega^2 C(1-d_s)T_s\right] = 0. \tag{42}$$

By neglecting the power losses in the inverter and the effects of harmonics on the ac side, the average power transferred from the dc link can be equated to the power delivered to the ac load over one ac cycle as [19]

$$\overline{V}_{iA} I_0 (1 - d_s) = (3/2) V_m I_m \cos\phi \tag{43}$$

where I_m is the peak phase current on the ac side and ϕ is the power factor angle of the load on the ac side of the inverter. By substituting $\overline{V}_{iA} = 2V_m/M$ in (43), it can be rewritten as

$$F(6) = -I_0 + (3/4) M I_m (\cos\phi)/(1 - d_s) = 0. \tag{44}$$

Finally, the relationship between M and d_s is a result of the control strategy that is adopted to switch the VSI. For example, in simple-boost control [2] and constant-boost control [15], d_s is kept constant at $(1 - M)$ and $(1 - \sqrt{3}M/2)$, respectively. Therefore, in general, M can be written as a function of d_s as

$$M = f(d_s). \tag{45}$$

In order to determine the inductor and capacitor sizes for a given operating condition, six nonlinear equations (37)–(40), (42), and (44) should be solved together with the six algebraic equations (7), (33)–(36), and (45).

B. Solution Process

In view of solving the derived equations, it is necessary to categorize the 19 variables used in the equations, as given in the following:

1) input data (known circuit parameters): E_s, T_s, V_m, I_m, and ϕ;
2) output data (unknown variables): L, C, d_s, I_0, $V_{\max}$, and $I_{\max}$;
3) design variables (specified by the user): $V_{\min}$ and $I_{\min}$
4) internal variables (only used to maintain the clarity of the equations): X_A, Φ_A, X_S, Φ_S, ω, and M.

In order to obtain the values for the six unknown variables, six nonlinear equations [$F(1)$ to $F(6)$], given in (37)–(40), (42), and (44), should be solved simultaneously using a numerical iterative routine such as "Fsolve" of Matlab. The six internal variables are directly expressed in terms of the other variables and parameters by the six algebraic equations (7), (33)–(36), and (45). If necessary, these internal variables can be eliminated by substituting them in the six nonlinear simultaneous equations to be solved by the numerical method. However, they can also be retained in the iteration routine to maintain clarity of the equations.

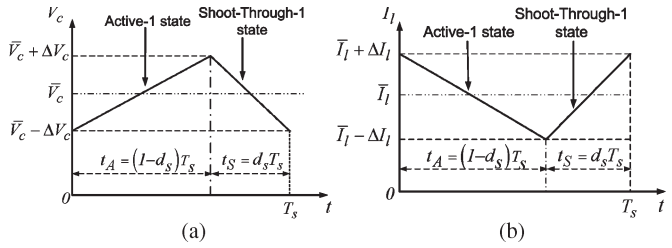


Fig. 4. Waveforms of (a) capacitor voltage and (b) inductor current, for small ripples.

In order to start the iteration process, a set of initial values for the unknown variables must also be provided to the numerical routine. The approximate method of design described in the following section using linear waveforms is therefore proposed to obtain the initial values of the six unknown variables.

C. Initial Values

The design method described here assumes that the capacitor voltage and inductor current vary linearly with time. This assumption is accurate when the ripples of these variables are small compared to their average values. Since larger ripple contents increase the current and voltage ratings of all the devices in ZSI and also increase the harmonic content in the output ac waveform, practical ZSI is normally designed with large capacitors and inductors. Therefore, the method given hereinafter can be used to approximately size the components in most cases.

Fig. 4 shows the linear waveforms of the capacitor voltage and inductor current for one switching cycle of the dc link. By taking the peak ripples and average values of capacitor voltage and inductor current as ΔV_c, $\overline{V}_c$, ΔI_l, and $\overline{I}_l$, respectively, the maximum and minimum values of the two variables can be written as

$$V_{\min} = \overline{V}_c - \Delta V_c = (1 - k_v)\overline{V}_c$$
$$I_{\min} = \overline{I}_l - \Delta I_l = (1 - k_i)\overline{I}_l \tag{46}$$
$$V_{\max} = \overline{V}_c + \Delta V_c = (1 + k_v)\overline{V}_c$$
$$I_{\max} = \overline{I}_l + \Delta I_l = (1 + k_i)\overline{I}_l \tag{47}$$

where $k_\nu = \Delta V_c/\overline{V}_c$ and $k_i = \Delta I_l/\overline{I}_l$ are the ripple factors of the two waveforms and indeed are the two "design variables" for a design based on linear waveforms.

With linear variations of waveforms, from (1), ΔV_c and ΔI_l can be expressed as

$$\Delta V_c = (\overline{I}_c \Delta t)/C \qquad \Delta I_l = (\overline{V}_l \Delta t)/L. \tag{48}$$

Considering the Shoot-Through-1 period

$$C = (\overline{I}_l d_S T_s)/(2\Delta V_c) \qquad L = (\overline{V}_c d_S T_s)/(2\Delta I_l). \tag{49}$$

Since the average inductor voltage and average capacitor current over a complete switching cycle in steady state are zero [2]

$$\overline{V}_c/E_s = \overline{I}_l/I_0 = \lambda \tag{50}$$

where $\lambda = (1 - d_S)/(1 - 2d_S)$.

By combining (49) and (50)

$$C = I_0 d_S T_s/(2k_v E_s) \qquad L = E_s d_S T_s/(2k_i I_0). \tag{51}$$

By substituting for I_0 in (51) from (44)

$$C = \frac{3d_S T_s M I_m \cos\phi}{8k_v E_s(1 - d_s)} \qquad L = \frac{2E_s d_S T_s(1 - d_s)}{3k_i M I_m \cos\phi}. \tag{52}$$

Thus, if E_s, I_m, ϕ, d_s, T_s, and M are known, C and L, for any control strategy, can be calculated from (48) to result in the desired levels of ripples.

Furthermore, by using (10) and (50)

$$\overline{V}_{iA} = (2\lambda - 1)E_s \Rightarrow \overline{V}_{iA} = E_s/(1 - 2d_s). \tag{53}$$

1) Simple-Boost Control: For simple-boost control, the relationship between M and d_s is [2]

$$M = 1 - d_s. \tag{54}$$

Substituting this in (44)

$$I_0 = (3/4)I_m \cos\phi. \tag{55}$$

By equating $\overline{V}_{iA} = 2V_m/M$ in (53) and substituting for M from (54)

$$\lambda = 2V_m/E_s \Rightarrow d_S = (2V_m - E_s)/(4V_m - E_s). \tag{56}$$

With the substitution of λ and d_S from (56) in (50) and (52), respectively, it can be found that

$$\overline{V}_c = 2V_m \quad \overline{I}_l = 2V_m I_0/E_s \tag{57}$$

$$C = \frac{3T_s I_m \cos\phi(2V_m - E_s)}{8k_v E_s(4V_m - E_s)}$$

$$L = \frac{2E_s T_s(2V_m - E_s)}{3k_i I_m \cos\phi(4V_m - E_s)}. \tag{58}$$

Hence, the sizing of capacitance and inductance can be easily done with (58) for simple-boost control.

2) Constant-Boost Control: For constant-boost control, the relationship between M and d_s is [15]

$$M = 2(1 - d_s)/\sqrt{3}. \tag{59}$$

With this as the only change, the corresponding equations of (55)–(58) can be written as follows, respectively:

$$I_0 = \left(\sqrt{3}/2\right) I_m \cos\phi \tag{60}$$

$$\lambda = \sqrt{3}V_m/E_s \Rightarrow d_S = \left(\sqrt{3}V_m - E_s\right)/(2\sqrt{3}V_m - E_s) \tag{61}$$

$$\overline{V}_c = \sqrt{3}V_m \quad \overline{I}_l = \sqrt{3}V_m I_0/E_s \tag{62}$$

$$C = \frac{\sqrt{3}T_s I_m \cos\phi(\sqrt{3}V_m - E_s)}{4k_\nu E_s(2\sqrt{3}V_m - E_s)}$$

$$L = \frac{E_s T_s(\sqrt{3}V_m - E_s)}{\sqrt{3}k_i I_m \cos\phi(2\sqrt{3}V_m - E_s)}. \tag{63}$$

D. Determining the Critical Values of Capacitance and Inductance

As given by (30), the Shoot-Through-2 state appears when the minimum capacitor voltage $V_{\min}$ drops below one-half of the dc source voltage. The capacitance C that produces the critical condition

$$V_{\min} = E_s/2 \tag{64}$$

is defined as the "critical capacitance." It can be determined by the design method described in Section III-A by using (64) to set the value of the design variable $V_{\min}$.

In the same manner, the Active-2 state appears when the minimum inductor current $I_{\min}$ drops below one-half of the load current I_0, as predicted by (21). The inductance L that produces the critical condition

$$I_{\min} = I_0/2 \tag{65}$$

is therefore defined as the "critical inductance." The value of critical inductance can be obtained by using (65) as the related design variable in the design method given in Section III-A. When both (64) and (65) are used together, both variables are corresponding to their critical values. Further reduction in CC or L will introduce static states during the operation.

IV. Design Examples

In the selected example, a three-phase 50-Hz 55-V (line) 5-A Y-connected load with a lagging power factor of 0.8 is supplied by a dc source of 20 V through a ZSI operating at 5 kHz and controlled by simple-boost control. For this case, the known input data of the system can be listed as $E_s = 20$ V, $T_s = 10^{-4}$ s, $V_m = 44.9$ V, $I_m = 7.071$ A, and $\phi = 36.87°$.

A. Design for 5% Ripple in Both Capacitor Voltage and Inductor Current

In order to demonstrate a design with low ripple in both capacitor voltage and inductor current, a ripple factor of 5% (i.e., $k_\nu = k_i = 0.05$) is selected. For the simple-boost control, the initial values of the unknown variables and the values of

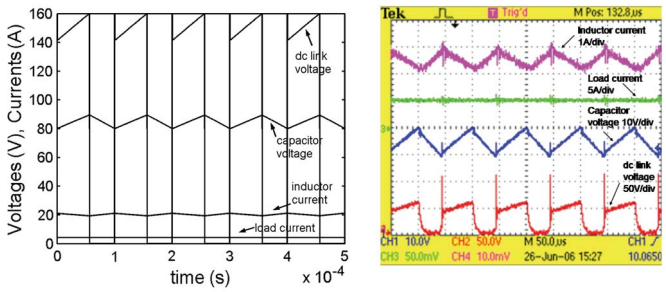


Fig. 5. Results of the converter designed for 5% ripple. (a) Simulation. (b) Experimental.

two design variables can be obtained by using (46) and (47), and (55)–(58) as

$$\overline{V}_c = 89.8 \text{ V} \quad V_{\max} = 94.29 \text{ V} \quad V_{\min} = 85.31 \text{ V}$$
$$\overline{I}_l = 19.05 \text{ A} \quad I_{\max} = 20 \text{ A} \quad I_{\min} = 18.1 \text{ A}$$
$$I_0 = 4.24 \text{ A} \quad d_s = 0.437 \quad C = 92.77\ \mu\text{F}$$
$$L = 2.06 \text{ mH}.$$

With all the circuit parameters, design variables, and initial values of the unknown variables known, the set of nonlinear equations (37)–(40), (42), and (44) are solved simultaneously by using "fsolve" routine of Matlab. The resulting values of the unknown variables are

$$V_{\max} = 94.15 \text{ V} \quad I_{\max} = 19.97 \text{ A} \quad d_s = 0.437$$
$$I_0 = 4.24 \text{ A} \quad C = 94.25\ \mu\text{F} \quad L = 2.1 \text{ mH}.$$

It is evident from the results of the design that the final values are very close to the supplied initial values. Therefore, when low ripple factors are selected, initial values given by Section III-C can be treated as the final values without much error. Furthermore, in the case of simple-boost control and maximum constant-boost control methods, the current I_0 is constant, as given by (55) and (60), respectively. Therefore, the number of unknown variables and, hence, the number of simultaneous nonlinear equations to be solved can be reduced to five in such cases.

Since the focus of this paper is designing the impedance network and not the operation of the VSI, the simplified circuit shown in Fig. 2 is employed during simulations and experiments. Hence, a highly inductive RL load that draws the desired load current I_0 is connected to the dc link during the active period. During the shoot-through period, a semiconductor switch across the dc link is turned on to effect a short circuit to the dc link.

1) Simulation Results: The computer simulation results obtained using Matlab/Simulink software for the data resulted from the design process, i.e., $C = 94.25\ \mu$F, $L = 2.1$ mH, and $d_s = 0.437$ are shown in Fig. 5(a). All the parasitic resistances were ignored, and an RC snubber was included across the switch. The capacitor voltage and inductor current followed the predicted values very closely, as given in Table II. As can be seen from these results, the ripple factors are very close to the predicted value of 0.05, and the average inductor current is also very close to the predicted value of 19.03 A. The 5% drop in the average voltage can be attributed to the effect of the snubber circuit and the voltage drops across the diode and the semiconductor switch.

TABLE II
RESULTS FOR THE DESIGN WITH 5% RIPPLE

	ΔV (V)	$\overline{V}_c$ (V)	k_V	ΔI (A)	$\overline{I}_l$ (A)	k_i
(a) Calcu.	4..5	89.8	0.05	0.93	19.03	0.05
(b) Simu.	4.4	85.0	0.05	0.9	19.4	0.05
(c) Exp.	5.5	34.5	0.16	0.5	19.0	0.03

2) Experimental Results: In the converter implemented in the laboratory for the aforementioned design, measured circuit parameters were as given next

$$C = 79.7 \text{ and } 78.6\ \mu\text{F} \qquad L = 2.037 \text{ and } 2.114 \text{ mH}.$$

Note here that the available capacitance was about 20% lower than the designed value of 94.25 μF. Experimental results for this design are shown in Fig. 5(b), and the numerical values extracted from the figure are given in Table II. According to the waveforms and data given in Table II, it is clear that the converter operates as expected with linear waveforms. The average value and peak ripple of inductor current and the peak ripple of capacitor voltage match very well with the values predicted by the design process. However, there is a very significant drop in average capacitor voltage. This can be attributed to parasitic resistances in the circuit components. The ripple factor of capacitor voltage is high compared to the expected value of 5% mainly due to the drop of average capacitor voltage. Second, the capacitors used in the converter were smaller than the designed value.

B. Design for Critical Values of Capacitance and Inductance

In order to design ZSI so that it operates under the critical condition with regard to the capacitor voltage and inductor current, the values of the two design variables should be set as $V_{\min} = 10$ V and $I_{\min} = 2.12$ A, according to (64) and (65). Noting here that the initial values of $\overline{V}_c$, $\overline{I}_l$, d_s, and I_0 remain the same for any ripple factor, the two ripple factors can be calculated using (45) as $k_\nu = (89.8 - 10)/89.8 = 0.89$ and $k_i = (19.05 - 2.12)/19.05 = 0.89$. Then, the maximum values of capacitor voltage and inductor current are calculated using (46) as $V_{\max} = 169.7$ V and $I_{\max} = 36.0$ A. The initial values of capacitance and inductance are finally calculated using (58) as $C = 4.93\ \mu$F and $L = 109.5\ \mu$H.

With the known input data, design variables, and the initial values, the design process yields the following final values of unknown variables:

$$V_{\max} = 134.8 \text{ V} \quad I_{\max} = 28.6 \text{ A} \quad d_s = 0.449$$
$$I_0 = 4.24 \text{ A} \quad C = 6.7\ \mu\text{F} \quad L = 148.8\ \mu\text{H}.$$

From these values, it is clear that they are significantly different from their initial values. Therefore, when the ripple

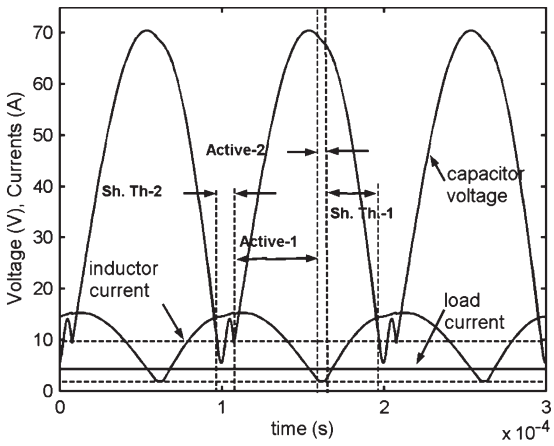
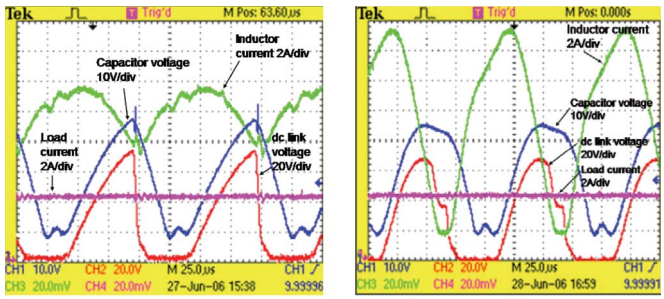


Fig. 6. Simulation results showing the appearance of static states.



(a) (b)

Fig. 7. Experimental results around the critical values of capacitance and inductance. (a) $C = 6\ \mu$F; $L = 148\ \mu$H. (b) $C = 6\ \mu$F; $L = 44\ \mu$H.

factors can be allowed to be high, higher accuracy can be obtained by using the equations derived in Section III-A.

1) Simulation Results: In order to demonstrate that the static states appear when the C and L are sized slightly lower than the designed values, computer simulations were performed for $C = 5\ \mu$F and $L = 140\ \mu$H. The other parameters were set at their designed values. As shown in Fig. 6, one switching cycle contains all four possible states. During the Shoot-Through-2 state, the capacitor voltage oscillates around $E_s/2 = 10$ V, and the inductor current increases linearly. Similarly, the inductor current remains at $I_0/2 = 2.1$ A, and the capacitor voltage drops linearly during the Active-2 state, as predicted in Section II.

2) Experimental Results: Fig. 7 shows two sets of results obtained for the same capacitance and two different values of inductance. In both figures, the zero level for all waveforms is set at the bottom line of the figures. As shown in Fig. 7(a) for $C = 6\ \mu$F and $L = 148\ \mu$H, the Shoot-Through-2 state occurs for a small period where the capacitor voltage oscillates around $E_s/2 = 10$ V and the inductor current increases linearly. This can be expected because the capacitance used is slightly below the design value of 6.7 μF. However, the Active-2 period does not occur because the minimum inductor current is above the critical value of $I_0/2 = 2.1$ A. When the impedance network is built with a lower inductance $L = 44\ \mu$H and the same capacitance as before, both Active-2 and Shoot-Through-2 states appear, as can be seen in Fig. 7(b).

Therefore, when the capacitance and inductance are sized below the designed values, unwanted static states appear in the waveforms. From Fig. 7(b), it is clearly seen that the waveforms predicted in Section II for the various steady states appear in the same manner in the practical setup. The capacitor voltage oscillates around $E_s/2 = 10$ V, and the inductor current increases linearly in the Shoot-through-2 state. Similarly, the inductor current remains at $I_0/2 = 2.1$ A, and the capacitor voltage drops linearly during the Active-2 state. Furthermore, it is also clear that the dc-link voltage waveform is far from being constant during the Active-1 state. As a result, the output voltage of ZSI will contain large amounts of harmonics if operated with larger ripples in capacitor voltage.

V. Conclusion

All possible operating states of a ZSI were analyzed and the equations were derived to predict the behavior of ZSI in steady state. Through the analysis, it was shown that, as the ripples of the capacitor voltage and inductor current become large, three additional static states appear in addition to the commonly used three dynamic states. Based on the equations derived, a method has been proposed to design the impedance network accurately for any operating condition by considering the nonlinearity of waveforms. This nonlinear design method can be used to lower the sizes of inductors and capacitors by allowing the ripples to be large. Furthermore, it can also be used to obtain the critical values of capacitance and inductance. However, larger ripple content in capacitor voltage results in a larger harmonic content in the output ac waveform and increases voltage ratings of all the components. On the other hand, larger ripple in inductor current results in higher current ratings for the dc supply and all the other components. Therefore, a compromise should be made in deciding the allowable ripple factor of the capacitor voltage and inductor current. When the ripple factors are set to small values, the initial values derived by assuming linear waveforms can be used to simplify the numerical calculations without much error in accuracy. The accuracy of the design methods was verified by computer simulations and laboratory experiments. In the experimental setup, the parasitic resistances of the converter were seen to cause a significant drop in the voltage gain of the converter, particularly when operated with relatively large currents.

References

[1] C. Cecati, A. Dell'Aquila, and M. Liserre, "A novel three-phase single-stage distributed power inverter," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1226–1233, Sep. 2004.

[2] F. Z. Peng, "Z source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, Mar./Apr. 2003.

[3] F. Z. Peng, A. Joseph, J. Wang, M. Shen, L. Chen, Z. Pan, E. Ortiz-Rivera, and Y. Huang, "Z-source inverter for motor drives," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 857–863, Jul. 2005.

[4] M. Shen, A. Joseph, J. Wang, F. Z. Peng, and D. J. Adams, "Comparison of traditional inverters and Z-source inverter for fuel cell vehicles," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1453–1463, Jul. 2007.

[5] Z. J. Zhou, X. Zhang, P. Xu, and W. X. Shen, "Single-phase uninterruptible power supply based on Z-source inverter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2997–3004, Aug. 2008.

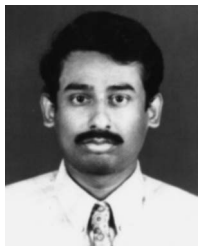
[6] Y. Huang, M. Shen, F. Z. Peng, and J. Wang, "Z-source inverter for residential photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1776–1782, Nov. 2006.

[7] J. C. Rosas-Caro, F. Z. Peng, H. Cha, and C. Rogers, "Z-source-converter-based energy-recycling zero-voltage electronic loads," *IEEE Trans. Ind. Electron.*, vol. 56, no. 12, pp. 4894–4902, Dec. 2009.
[8] U. Supatti and F. Z. Peng, "Z-source inverter based wind power generation system," in *Proc. IEEE ICSET*, 2008, pp. 634–638.
[9] D. Vinnikov and I. Roasto, "Quasi-Z-source-based isolated DC/DC converters for distributed power generation," *IEEE Trans. Ind. Electron.*, DOI: 10.1109/TIE.2009.2039460, to be published.
[10] P. C. Loh, F. Gao, and F. Blaabjerg, "Embedded EZ-source inverters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 1, pp. 256–267, Jan./Feb. 2010.
[11] H. Xu, F. Z. Peng, L. Chen, and X. Wen, "Analysis and design of bi-directional Z-source inverter for electrical vehicles," in *Proc. IEEE APEC*, 2008, pp. 1252–1257.
[12] S. Rajakaruna and B. Zhang, "Design and control of a bidirectional Z-source inverter," in *Proc. AUPEC*, 2009, pp. 1–6.
[13] X. Ding, Z. Qian, S. Yang, B. Cui, and F. Z. Peng, "A high-performance Z-source inverter operating with small inductor at wide-range load," in *Proc. IEEE APEC*, 2007, pp. 615–620.
[14] F. Z. Peng, M. Shen, and Z. Qian, "Maximum boost control of the Z-source inverter," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 833–838, Jul. 2005.
[15] M. Shen, J. Wang, A. Joseph, F. Z. Peng, L. M. Tolbert, and D. J. Adams, "Constant boost control of the Z-source inverter to minimize current ripple and voltage stress," *IEEE Trans. Ind. Appl.*, vol. 42, no. 3, pp. 770–778, May/Jun. 2006.
[16] S. Yang, X. Ding, F. Zhang, F. Z. Peng, and Z. Qian, "Unified control technique for Z-source inverter," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 3236–3242.
[17] M. Shen and F. Z. Peng, "Operation modes and characteristics of the Z-source inverter with small inductance or low power factor," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 89–96, Jan. 2008.
[18] S. Rajakaruna and Y. R. L. Jayawickrama, "Designing impedance network of Z-source inverters," in *Proc. IPEC*, Singapore, 2005, pp. 962–967.
[19] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*., 3rd ed. Hoboken, NJ: Wiley, 2003.

Sumedha Rajakaruna (M'93–SM'07) received the B.Sc.Eng. degree in electrical engineering from the University of Moratuwa, Moratuwa, Sri Lanka, in 1986, the M.Sc. degree in electrical engineering from the University of Calgary, Calgary, AB, Canada, in 1989, and the Ph.D. degree in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 1993.

From 1986 to 2000, he was with the Department of Electrical Engineering, University of Moratuwa, at the levels of a Lecturer and a Senior Lecturer. In 2000, he joined Nanyang Technological University, Singapore, Singapore, as an Assistant Professor. Since 2007, he has been a Senior Lecturer with the Department of Electrical and Computer Engineering, Curtin University of Technology, Perth, W.A., Australia. His current research interests include the control of power converters and the conversion of renewable energy.

Dr. Rajakaruna is a member of the Institution of Engineering and Technology and a Chartered Engineer registered in U.K. He was a recipient of the Canadian Commonwealth Scholarship for graduate studies in Canada from 1987 to 1993.



Laksumana Jayawickrama was born in Sri Lanka in 1971. He received the B.Sc.(Eng.) degree in electrical engineering from the University of Moratuwa, Moratuwa, Sri Lanka, in 1997 and the Ph.D. degree in electrical engineering from Nanyang Technological University, Singapore, Singapore, in 2007.

After graduation, he joined Ceylon Electricity Board as an Electrical Engineer in 1998. He is currently with the Power Networks Division, Parsons Brinckerhoff, Melbourne, Vic., Australia, as a Senior Protection Engineer.