A Unity Power Factor Boost Rectifier with a Predictive Capacitor Model for High Bandwidth DC Bus Voltage Control

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ABSTRACT

Single phase rectifiers with power factor correction circuits based on the boost converter find broad application in consumer equipment. A fundamental design difficultly is caused by the need to trade off the input line current wave shape and the dynamic response of the output energy storage capacitor voltage regulation loop. The energy balance requirement inherent in single phase systems forces a significant 100Hz voltage ripple on the output capacitor. A high bandwidth voltage regulation loop will feed back enough of the 100Hz component to distort the current reference signals for the inner current control loop distorting the line wave shape. A reference model can be used to construct a ripple free estimate of the capacitor voltage. This paper shows that improved output capacitor voltage regulation can be achieve simultaneously with a high quality input current spectrum.

1. INTRODUCTION

Boost rectifier power factor correction circuits are intensively applied and have been extensively studied, [1, 2]. The focus of the majority of publications has been upon the control of an inner current loop and much less attention has been given to the dynamic response of the converter output voltage. All single phase AC-DC converters must provide energy storage at twice the line frequency if a constant output power is to be delivered. The boost power factor correction circuit commonly uses a DC bus capacitor to provide that energy storage. Due to the double frequency power fluctuation inherent in a single phase design, the capacitor voltage must exhibit a significant voltage ripple.

The storage capacitor voltage is regulated by adjusting the magnitude of the line current that is drawn by the boost stage. Resistive emulation, controlling the converter to draw a line current proportional to voltage, is common. Two approaches, the voltage follower approach or the multiplier approach are popular, [3]. The voltage follower approach relies on an inductor peak or average current being proportional to the volt second product applied by the line voltage during a switching period. This method can be current sensor free. The multiplier approach normally uses an explicit current control loop and is used at higher powers. An output capacitor voltage controller responds to the voltage error and drives a multiplier to produce a current demand signal that tracks the supply wave shape. This is in turn is applied to the inner current control loop. Fuzzy mode controllers have also been proposed as the voltage regulation element, [4]. The control loop design must balance two conflicting needs:

- The need to respond rapidly to changes in capacitor voltage on the application of load and especially on the removal of load to avoid unnecessary voltage stress on the storage capacitor;
- The need to provide a power demand signal that is free from ripple frequency components, as that signal is used to generate a current reference signal for an inner control loop and fed back ripple increases harmonic distortion in the converter input current.

This paper proposes the use of a capacitor current balance model to provide a ripple free estimate of the storage capacitor voltage which can be used as an input to a high bandwidth voltage regulation loop. This allows very high speed responses to load changes and tighter control of the capacitor voltage while maintaining high quality line current inputs. Responses are effectively complete within one half cycle of the mains supply and this is a significant improvement on past designs where response times of five to ten cycles occur.

The paper presents a continuous mode, three-way interleaved boost converter with an improved predictive current control method. Dual interleaved converters operating at the discontinuous-mode continuous-mode boundary have been proposed primarily as a method for reducing diode reverse recovery, [5]. In principle interleaving can be extended to any number of converters. High converter numbers present a manufacturing advantage if the ratings of devices can be reduced to the point where predominantly surface mount components can be used.

The target application area is single phase power converters of up to a few kilowatts rating as may be applied for UPS battery charging or single phase input variable speed drive systems for heat pumps and air conditioners. In these applications a digital signal processor such as the TMS320F2808 or other high end microcontrollers can be readily justified as a cost effective control device.

2. PREDICTIVE CURRENT CONTROL

Many current control methods can be applied based on current mode control, average current control, [6], sliding controls [7], one cycle control [8] or variations on these, [9].

Each of the three boost cells uses an inner most loop with a digital predictive current controller, [10], which has been applied in PWM bridge rectifier applications. The basic principles are:

- The boost inductor current, the DC bus voltage and input diode rectifier voltage are sampled at the beginning of each control period, in this case the control period is 12.5μS;
- At the beginning of the control period the actual inductor current is subtracted from a current reference which indicates the desired current to be achieved at the end of the control period - this gives a current error signal;
- The current error signal is multiplied by the inductor value to give the necessary volt-second product that must be applied to the inductor during the control period to force the current error to zero;
- The volt-second product is used with a knowledge of the diode rectifier voltage and the DC bus voltage to determine the duty cycle during the control period;
- The duty cycle requirement is converted into switching signals for the devices.

3. INTERLEAVED BOOST CONVERTER

Figure 1 shows a three way interleaved boost rectifier. The individual cells switch at 80kHz and the converters are phase displaced to achieve current ripple cancellation. Each stage has a dedicated predictive current controller as an inner loop. The predictive current controllers have their sampling instants displaced by one third and two thirds of the 12.5μS control period respectively.

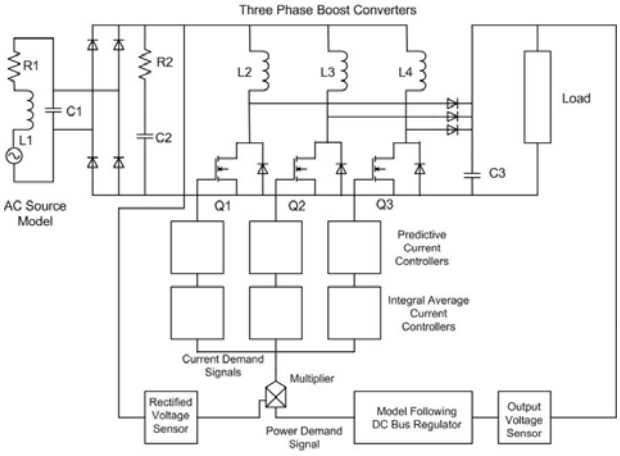

Figure 1. Boost Rectifier.

An average mode controller is overlaid as a second current control mechanism. As with peak current mode controls the predictive method will produce a small amount of harmonic distortion as the end point current rather than the average current is controlled, [6].

Resistive load emulation is applied by a common DC bus voltage regulator. This generates a power demand signal which is multiplied by the absolute value of the mains voltage to provide a shared current demand signals for each of the boost cells. Precise current sharing is forced by the individual current loops.

4. SINUSOIDAL OPERATION OF THE BOOST CONVERTER STAGE

Initially, to illustrate the ripple cancellation effects of interleaving, the operation of the inner current loops is examined using simulation of a 3 500W, 240Vrms, 50Hz input 400Vdc output rectifier. A reference signal equivalent to the full rating of the converter is applied. This is derived from the rectified mains voltage in the converter power circuit.

The boost converter currents are seen in Figure 2. The boost inductors, L2 to L4, are each 200μH and the 80kHz ripple currents in each group, shown as the top three traces, are relatively high with a maximum value of 6.25App. Significant cancellation occurs in the group currents shown in the lower trace. Current ripple zeroes occur at one third and two thirds duty ratio. It is note worthy that the boost converters do operate in a discontinuous mode for a significant part of the mains cycle. This will cause a prediction error with the current control method but this is compensated for by the integral control of average inductor current.

In order to absorb the ripple frequency components RFI filters will be required. In combination with the mains impedance these pose a stability risk for the rectifier controls. The simulation model includes a series inductor resistor representation of the mains source impedance with 1Ω and 3.18mH, or 1 Ω inductive used in this case. This results in a 6% voltage drop at full load and would be at the upper end of what would be expected in terms of voltage regulation. Capacitor C1 is 4μF and represents the lumped sum of class X capacitors in any RFI suppression networks. Components R2 and C2, 50 Ω and 1 μF respectively, provide some small signal damping at the natural frequency of the mains impedance and the RFI capacitors. Additionally they provide an alternative ripple current path that avoids the rectifier diodes. This ensures that high frequency voltages can not occur across the diodes which would be expected to have poor reverse recovery characteristics. It also excludes the possibility of ripple voltages existing at the rectified voltage sensing point.

The selected control gains in the integral control loop give a current control bandwidth of 100krad/s or approximately 15kHz. The inner loop removes the inductor from the small signal models and the loop dynamics are dominated by the controller integral response.

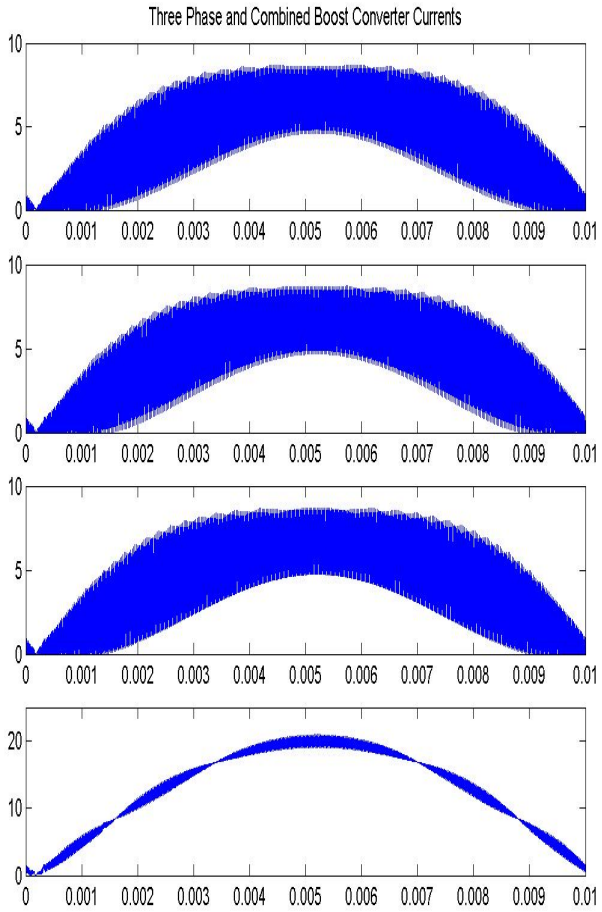

Figure 2. Boost Converter and Total Converter Group Current

This results in a first order system with good phase margins. No adverse stability issues are observed. Figure 3 shows the resulting line current wave shape and spectrum under integral current mode control. In this case a current demand equivalent to full load or 20Ap is applied. The third harmonic is 53dB down or 0.23%. This converter will mimic a resistive load and will draw harmonic current if the supply voltage waveform is distorted. In practice the line voltage distortions will be much higher and as a consequence the current will be as distorted as the voltage waveform.

It is possible to use a PLL to provide a pure sine wave reference and to force a pure line current. It is not advised. The existing scheme which mimics a resistive behaviour provides positive damping for harmonics and will tend to reduce the supply voltage distortion. This is a better operational outcome. The major simulation parameters for the SIMULINK model include:

- Switch characteristics, initial forward drop, 0.0V, slope resistance 66mΩ, snubber 100Ω in series with 2000pF;
- Inverse diode, initial forward drop 0.8V, slope resistance 40mΩ, snubber 100Ω in series with 2000pF;

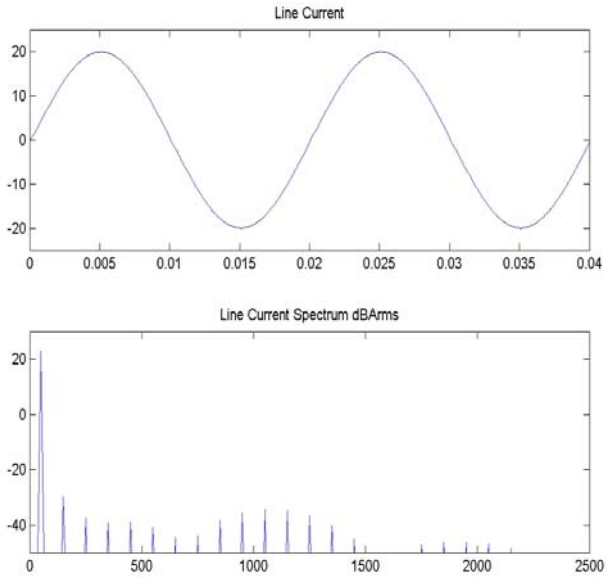

Figure 3. Line Currents under Sinusoidal Demand Signal Operation

- Device switching frequency 80kHz;
- Filter inductor, 200μH.

This simulation does not include the effects of a DC bus voltage regulator which will significantly contribute to the overall line current distortion. As the voltage loop responds on a much slower time scale it is simulated separately using a continuous signal rather than a switching model for the internal current loops.

5. A MODEL REFERENCE APPROACH TO DC BUS REGULATION

In most designs DC bus ripple has an adverse effect on the line current wave shape. In a low power voltage follower approach, [8], a compensation method was proposed, but not tested, where the ripple voltage adjusted the resistance emulated by the duty cycle modulator.

This approach does not apply in higher power systems using the multiplier approach where the bus voltage is controlled by adjusting the peak value of the sinusoidal demand current applied to the line current regulator and hence adjusting the rectifier input power. If the bandwidth of the voltage loop is increased the ripple voltage distorts the current reference giving rise to a harmonic distortion of the input wave shape. A slow voltage loop results in a good current wave shape but has a poor dynamic response to load changes. Specifically the step reduction of load will cause DC bus overshoots that can be damaging, especially when the DC bus uses electrolytic capacitors that often have limited over-voltage margins. Often secondary protective measures are required to shut down the boost converters in the face of DC bus over voltages.

Figure 4 shows a DC bus voltage regulator based on a capacitor voltage reference model. A similar approach has been proposed for PWM single phase boost rectifiers in railway applications, [10]. A current integration model generates an estimate of the capacitor voltage which has a greatly reduced ripple component. The capacitor is modeled by an integrator that has the following inputs:

- A current term reflecting the average input power from the rectifier;
- The DC bus load current which may be measured directly or inferred from DC bus power.

The average current injected by the rectifiers into the capacitor is simply the average power divided by the DC bus voltage. The average rectifier power is estimated by multiplying the RMS value of the input voltage by expected value of the RMS input current. The RMS input current is directly proportional the power demand signal driving the current controlled rectifiers. In applications where the supply voltage varies considerably, an on line estimator may be required to track the RMS value of the input voltage.

The model voltage and the actual capacitor voltage are held in alignment using a PI control that responds to the voltage tracking error. The bandwidth of this loop is limited to avoid a response to the capacitor 100Hz ripple voltage.

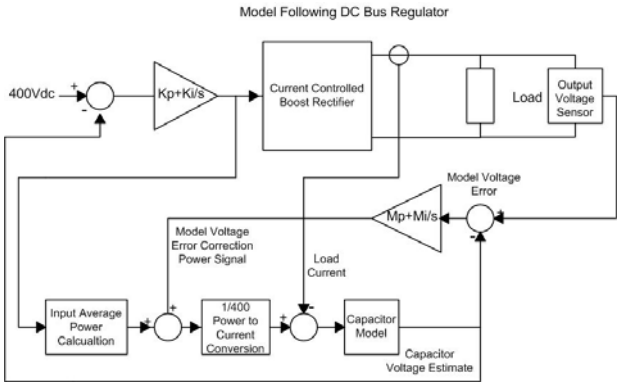

Figure 4. A Reduced Ripple Capacitor Voltage Model

The simulation parameters for the SIMULINK model are:

- Bus capacitor 2 000μF;
- Nominal voltage – 400Vdc;
- Load step 3 500W constant power load;
- K_p=2; K_i=50; 1V at the amplifier output corresponds to $1A_{peak}$ of line current, for a 240Vac nominal system this is an average power of 170W;
- The *Input Average Power Calculation* block has a gain of 170W/V;
- M_p=30; M_i=1000.

The current controlled boost rectifiers are simulated using a continuous model as shown in Figure 5. As the inner current loops have been shown to have a very high bandwidth the boost converter stages can be modeled by a controllable current source. At any point in the 50Hz cycle, this source delivers charge to the capacitor equivalent to the charge injected by the boost converters over each of their switching periods. The demand signal is converted into an instantaneous line current and resulting instantaneous power, and this is divided by the capacitor voltage to give the instantaneous current that would be injected into the capacitor for power balance in the boost converters. Once load current is subtracted, the residual current is readily integrated to give the capacitor voltage. This approach faithfully replicates the 100Hz voltage ripple and the other lower frequency capacitor voltage transients.

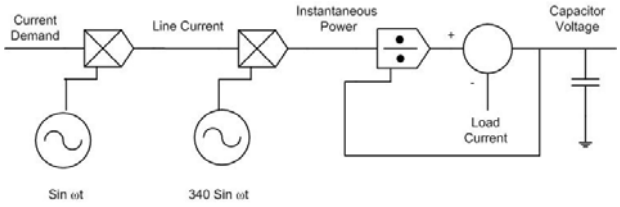

Figure 5. Continuous Model for the Boost Rectifier

Figure 6 shows the simulated step response of a system with a DC bus voltage regulator based on a capacitor voltage model. From a zero load condition full load is applied at 0.1s and then removed at 0.3s. The traces are:

- The actual capacitor voltage;
- The “reduced ripple” capacitor model voltage;
- Line current.

The DC bus voltage reduces on the application of the load current which occurs at a 0.1s which is a line current zero. This is an unfavorable timing for the load application as it is not possible to extract real power from the incoming supply at this point in the cycle so a bus voltage fall is unavoidable. However the correct level of line current is nearly fully achieved by the next mains peak 5mS later and the voltage drop of 10V is comparable to the normal ripple.

On the removal of load at 0.3s the line current is extinguished in less than a fraction of a half cycle and the DC bus overshoots by less much less than 10V. In this case the timing of the load removal is more favorable. Higher overshoots would occur if the load step occurred at the mains peak. A Fourier analysis of the full load line current shows a THD of 1.7% which is largely third harmonic.

The true quality of this response is easily demonstrated by considering two equivalent step responses for the conventional regulator structure. The two step responses are for a:

- High gain voltage regulator which consequently has poor line current wave shape;

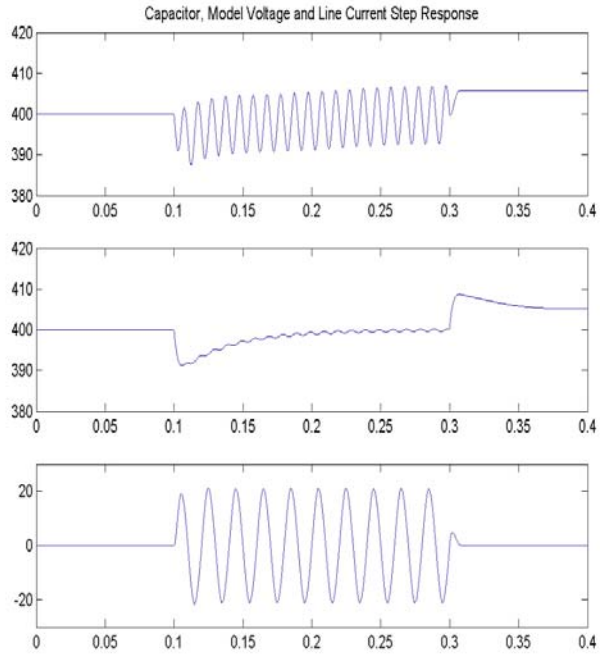

Figure 6. Response for a 100% Step Load Changes

- A low gain regulator that retains reasonable line current quality but has a much increased DC bus overshoot.

Figure 7 shows the same load step response in the absence of a capacitor voltage reference model. In this case the Dc bus regulator gains are maintained at K_p=2 and K_i=50. The storage capacitor voltage ripple will now adversely affect the line current regulators. The speed of response has been approximately maintained but the voltage undershoot and overshoot have increased somewhat. The line current is visibly and unacceptably distorted with a THD of 25% and it is not possible to maintain the control loop gains due to this effect.

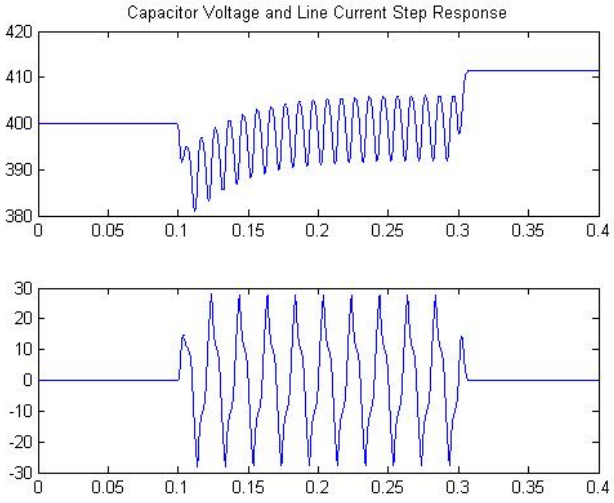

Figure 7. Load Step Response in the Absence of a Capacitor Voltage Model – Equal Gains

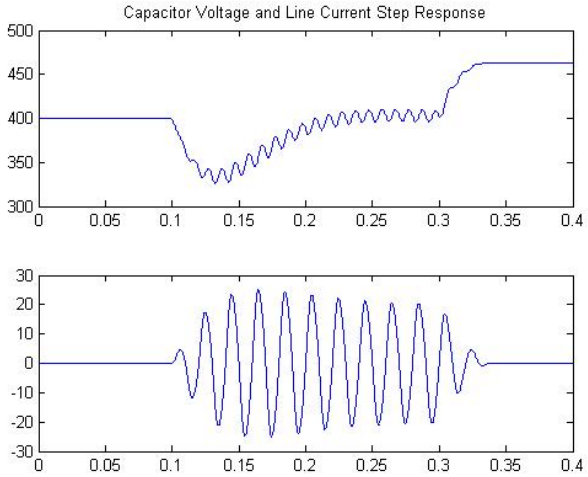

Figure 8. Load Step Response in the Absence of a Capacitor Voltage Model – Reduced Gain

In order to recover the line current wave shape the voltage regulator loop gains must reduce. Figure 8 shows the resulting response for an order of magnitude drop in the control gains with K_p =0.2 and K_i=5.

At this point the line current shape is much improved but the DC bus voltage overshoot increases to 60V, approximately a factor of ten times larger than the capacitor voltage model approach. The overshoot is clearly related to the line current response time and this case is still relatively fast with the response time being approximately 5 cycles for a 100% load step. By comparison, an earlier work using a standard PI regulation approach, [8], on a 120Vac 60Hz input rectifier reported a response time of more than 10 cycles for a load step from 50% to 100% which resulted in a 60V drop on a nominal 240Vdc bus.

6. A NOTE ON THE DYNAMIC MODEL AND EXPERIMENTAL RESULTS

The voltage regulator system includes four states, the physical capacitor voltage, the model voltage and two integrator states within PI regulators. It is a fourth order system and a systematic design approach has not yet been developed. In the railway rectifier application a full bridge was used as boost converter, [10]. A classical control approach was used and a dominant pole pair could be identified and the pole locations controlled by selecting the PI control gains. In both cases the rectifier dynamics are similar and this approach was used to guide the existing design.

One weakness of the classical model developed for railway rectifiers, [10], was the use of a resistive load model. The largest use of the boost rectifier is in consumer appliances as a unity power factor pre-regulator which is then followed by an isolated DC-DC converter. In this paper constant power loads were used to examine the load step responses. Constant power loads have a negative incremental input resistance. These loads will not provide any damping as the classical model suggests and will potentially be a

destabilizing influence. It is well understood, for example, that the negative input resistance of DC-DC DC-DC converters can excite oscillations with their own input filters.

A future goal for this work is to extend the classical approach to include this effect or to consider a state variable design which includes the negative resistance load characteristics and attempts a pole placement design approach. A 3500W converter with a TMS320F2808 based control has been constructed to confirm the results and the experimental work is progressing.

7. CONCLUSIONS

A considerable improvement can be obtained in the regulatory responses of the boost power factor correction circuit by using a capacitor model to estimate the "ripple free" capacitor voltage. As the ripple voltages do not circulate in the DC bus voltage regulation loop higher bandwidths can be applied without 100Hz components distorting the current reference signals that the inner current loops follow. Consequently the overshoot voltages of the energy storage capacitor can be reduced without any degradation of the line current wave shape.

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