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A Current Fed Two-Inductor Boost Converter With an Integrated Magnetic Structure and Passive Lossless Snubbers for Photovoltaic Module Integrated Converter Applications

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***Abstract*—In this paper, a photovoltaic (PV) module integrated converter is implemented with a current fed two-inductor boost converter cascaded with a line frequency unfolder. The current source is a sinusoidally modulated two-phase buck converter with an interphase transformer. The boost cell operates at a fixed duty ratio and has an integrated magnetic structure. The two inductors and the transformer are integrated into one magnetic core. Passive lossless snubbers are employed to recover the energy trapped in the transformer leakage inductance and to minimize the switching losses. The two-inductor boost converter output interfaces with the mains via an unfolding stage, where the MOSFETs are driven by the PV gate drivers. Experimental results are provided for a 100-W converter developing a single phase 240-V 50-Hz output.**

***Index Terms*—Integrated magnetics, lossless snubber, two-inductor boost converter.**

I. Introduction

TO DATE, three different systems are widely used in grid interactive photovoltaic (PV) applications—the centralized inverter system, the string inverter system, and the ac module or module integrated converter (MIC) system [1]–[3]. Among these approaches, MICs provide an attractive means to interface PV systems with ac distribution networks and have become increasingly popular in recent years [4]. As the MIC is most often fed from a single PV module, its typical power rating is less than 500 W [1], [4]. Modules with power ratings between 100 and 200 W are also quite common [5]–[10]. The module can also be equipped with a maximum power point tracker (MPPT) [11]–[13]. Key system requirements are compactness, high reliability and low cost [6].

The two-inductor boost converter, derived by applying the duality principle to the conventional voltage fed half bridge converter [14], has been previously developed as a dc–dc conversion stage to supply a dc–ac inverter in MIC applications [15]. The converter is shown in Fig. 1. In this arrangement, the voltage fed two-inductor boost converter generates a constant dc link and pulsewidth modulation (PWM) must be used in the dc–ac inversion stage to produce ac waveforms that meet the prevailing harmonic standards. However, PWM control introduces additional switching losses and requires additional control circuitry. Gate drivers for example are more complex.

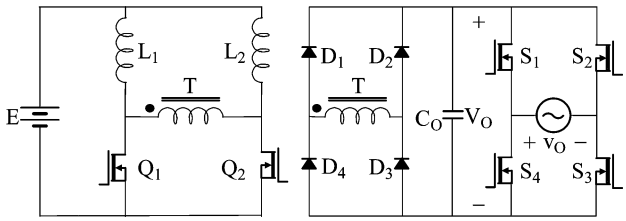

Fig. 1. Voltage fed two-inductor boost converter with an inverter.

In order to avoid the penalties associated with a pulse-width modulated inversion stage, this paper proposes a two-inductor boost converter, which has a current source supply from a two-phase buck converter and generates rectified sinusoidal waveforms on the dc link. This makes it possible to reduce the output stage inverter to an unfolder using a more straightforward square-wave control. The proposed topology is shown in Fig. 2, where the front-end two-phase buck converter functions as the current source and feeds the two-inductor boost cell through an auto transformer. The rectification stage of the boost cell employs a voltage doubler. The unfolder operates at the line frequency and the switching losses are completely removed.

The paper studies thoroughly the operation of the individual stages of the converter including the buck, the boost and the inversion stages. The key features in the individual stages are also discussed in detail. The theoretical waveforms are demonstrated to explain the converter operations including the switching waveforms for the buck and the boost stages, the flux waveforms in the individual limbs of the integrated magnetic core and the voltage and current waveforms in the passive non-dissipative snubbers in the boost cell. Experimental results of a 100-W converter with 20-V input and 240-V output are also provided at the end of the paper to confirm the theoretical analysis.

II. Two-Phase Buck Converter

In a hard-switched voltage fed two-inductor boost converter shown in Fig. 1, a variable output voltage can be achieved by

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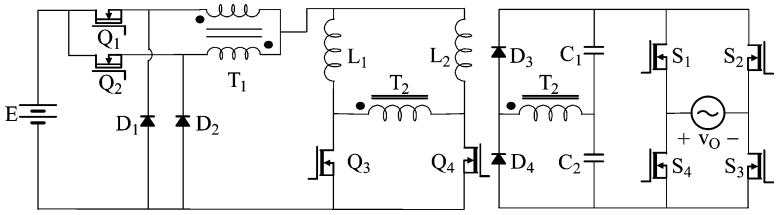

Fig. 2. Current fed two-inductor boost converter with an unfolder.

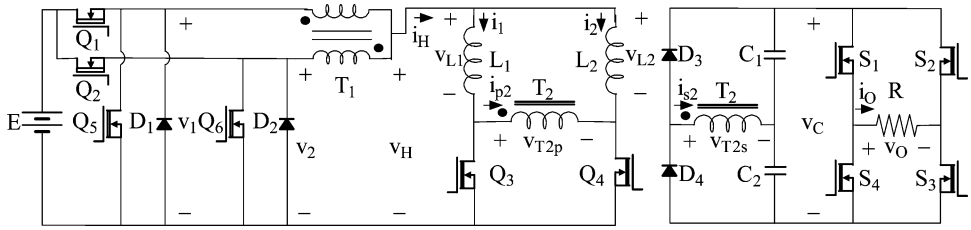

Fig. 3. Two-inductor boost converter fed from a two-phase synchronous buck converter.

varying the switching duty ratios according to the converter transfer function given in [14]:

$$\frac{V_O}{E} = \frac{n}{1 - D_s} \tag{1}$$

where V_O and E are, respectively, the output and the input voltage of the two-inductor boost converter, n is the transformer T turns ratio and D_s is the duty ratio of the MOSFETs Q_1 and Q_2.

Because the inductors act as current sources, continuity of current requires a minimum switch duty ratio of 50%. This results in a minimum output voltage of twice the input voltage and obviously zero output voltage cannot be reached. In order to achieve a zero output voltage, a step-down stage must be placed before the boost-derived converter. In Fig. 2, a two-phase buck converter is used to obtain the advantages of higher equivalent switching frequencies without higher switching losses in the buck converter MOSFETs.

Multiphase converter arrangements have recently been widely adopted as an efficient approach to parallel multiple converters to provide high current output [16], [17]. Under multi-phase operation, the currents with an equal phase shift are added together and the equivalent input and output ripple current frequency will be multiplied by the number of the phases. The converter also has less input and output current ripples as those in each phase cancel [18]. These benefits ease the requirement on bulky filter components such as inductors and capacitors.

The topology shown in Fig. 2 can be further improved by using synchronous rectifiers as shown in Fig. 3. In Fig. 2, the conduction loss is higher as it is partly determined by the diode forward voltage drop. In the synchronous rectifier, the diode is replaced by the MOSFET. This design is able to largely reduce the conduction loss, as the forward resistance of the synchronous MOSFET can be very low [19]. Dead time must be applied to prevent "shoot-through". A Schottky diode is placed in reverse parallel with the synchronous MOSFET in a standard design to prohibit the load current from flowing through the body diode during the dead time [20].

The output of the two-phase synchronous buck rectifier is fed to the two-inductor boost converter through an interphase transformer (IPT), with 1:1 turns ratio [21], [33], [22], [23]. The IPT enables the equivalent switching frequency of the buck stage to be doubled but not at the cost of a higher switching loss in the hard-switched buck converter. The use of an IPT does require current mode control for each phase to ensure good current sharing and flux balance. The buck converter output voltage v_H has an average value of V_H over one high frequency cycle of

$$V_H = D_{\text{buck}} E \tag{2}$$

where D_{buck} is the duty ratio of the buck stage MOSFETs Q_1 and Q_2 and E is the input voltage of the converter. D_{buck} is modulated in a sinusoidal manner as

$$D_{\text{buck}} = |\sin(2\pi f_m t)| \tag{3}$$

where f_m is the mains or the grid frequency.

Although the two-phase synchronous buck converter is highly efficient, additional semiconductor components and control circuitry are needed in this design. The design complexity can be greatly reduced if an integrated switching control chip is employed. As the additional MOSFETs and diodes in the buck converter appear on the low voltage side of the system, they can be easily implemented with compact low-voltage components. The cost increase will be minimal with the modern semiconductor technology and this can be further justified by the near-zero switching power loss and the ease in the gate driver design in the line frequency unfolder. As mentioned before, the current mode control is a must in the selection of the switching controller to prevent the IPT from saturation.

III. Two-Inductor Boost Cell

As the duty ratio of the two-phase synchronous buck converter is modulated in a sinusoidal manner, the two-inductor boost cell is able to produce the rectified sinusoidal waveform

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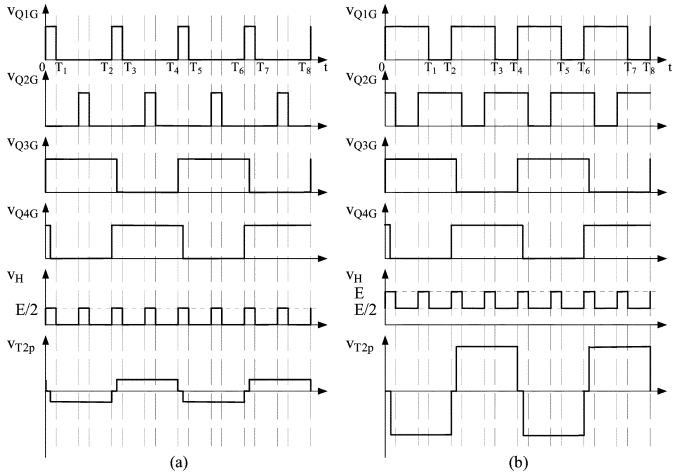

Fig. 4. Theoretical buck and boost stage switching waveforms. (a) $D_{\rm buck}$ <50%. (b) $D_{\rm buck}$ >50%. ($T_1 = D_{\rm buck}T_{\rm buck}, T_2 = T_{\rm buck}, T_3 = T_{\rm buck} + D_{\rm buck}T_{\rm buck}, T_4 = T_{\rm buck}, T_5 = T_{\rm buck} + D_{\rm buck}T_{\rm buck}, T_6 = 3T_{\rm buck}, T_7 = 3T_{\rm buck} + D_{\rm buck}T_{\rm buck}, T_8 = 4T_{\rm buck}$).

on the dc link with a fixed duty ratio. The transfer function of the two-inductor boost converter is

$$v_C = \frac{2n_{T2}}{1 - D_{\rm boost}} V_H \tag{4}$$

where $D_{\rm boost}$ is the duty ratio of the boost stage MOSFETs Q_3 and Q_4 and $n_{\rm T2}$ is the turns ratio of the transformer T_2. In this case, $D_{\rm boost}$ is fixed at a value slightly greater than 50%, which is the best case for device voltage stress.

The switching frequency of the buck stage MOSFETs $f_{\rm buck}$ and that of the boost stage MOSFETs $f_{\rm boost}$ are respectively selected to be $f_{\rm buck} = 150$ kHz and $f_{\rm boost} = 75$ kHz in the converter design. The theoretical switching waveforms in the buck and boost stages with above parameters over high frequency cycles are shown in Fig. 4, where $T_{\rm buck}$ and $T_{\rm boost}$ are, respectively, the switching periods of the buck and the boost stages and $T_{\rm boost} = 2T_{\rm buck}$. Fig. 4(a) and (b), respectively, shows the converter waveforms when $D_{\rm buck}$ <50% and $D_{\rm buck}$ >50%. The voltage after the IPT swings between zero and the half input voltage when $D_{\rm buck}$ <50%, while it swings between the half and the full input voltage when $D_{\rm buck}$ >50%. The three voltage levels and the frequency doubling effect can be seen in v_H waveform in both cases. In each case, the transformer T_2 primary voltage waveform is shown. The peak MOSFET voltage in the boost cell is slightly greater than twice the average voltage supplied by the buck converter. This voltage doubling is an inherent feature of the boost cell.

The boost cell employs the integrated magnetics, the passive non-dissipative snubbers and the silicon carbide rectifiers to achieve a converter design with the minimized size and loss. The detailed discussion of these important features is provided below.

A. Magnetic Core Size Reduction

Magnetic integration, which merges more than one discrete magnetic components into a single core configuration, assists in reducing the size of the switched mode power converters [24],

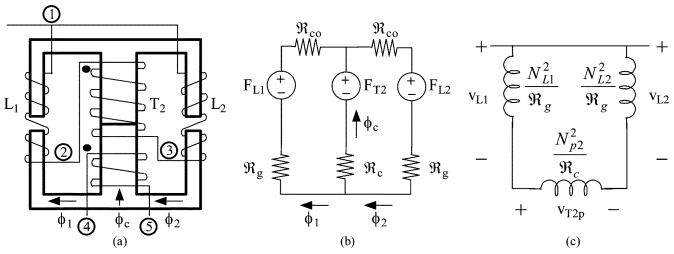

Fig. 5. Integrated transformer and inductors. (a) Top-view. (b) Magnetic circuit. (c) Electrical circuit.

[25]. Application of the KVL in the primary side of the two-inductor boost cell in Fig. 3 yields

$$v_{T2p} = v_{L2} - v_{L1} \tag{5}$$

where $v_{\rm T2p}, v_{\rm L2}$, and $v_{\rm L1}$ are, respectively, the voltages across the transformer T_2 primary, the inductors L_2 and L_1. Applying Faraday's Law, respectively, to the windings of the two inductors and the transformer primary gives

$$N_{p2} \cdot \dot{\phi}_{T2} = N_{L2} \cdot \dot{\phi}_{L2} - N_{L1} \cdot \dot{\phi}_{L1} \tag{6}$$

where $n_{\rm p2}$ and $\dot{\phi}_{\rm T2}$ are, respectively, the number of turns and the derivative of the flux in the transformer T_2 primary winding, $n_{\rm L2}$ and $\dot{\phi}_{L2}$ are, respectively, the number of turns and the derivative of the flux in the inductor L_2 winding and $n_{\rm L1}$ and $\dot{\phi}_{L1}$ are, respectively, the number of turns and the derivative of the flux in the inductor L_1 winding. If $N_{p2} = N_{L1} = N_{L2}$, (6) can be simplified to (7), which allows the magnetic integration to be carried out

$$\dot{\phi}_{T2} = \dot{\phi}_{L2} - \dot{\phi}_{L1}. \tag{7}$$

Three cores for the two inductors and the transformer can be integrated if a three-limb core structure is selected and the individual windings are configured in a way such that the relationship between the individual fluxes given in (7) is fulfilled. An ETD core with equal air gaps in both of the two outer limbs is used. A top-view diagram of the winding construction, the equivalent magnetic circuit and the equivalent electrical circuit are shown in Fig. 5.

In Fig. 5, $\Re_g, \Re_c$, and $\Re_{\rm co}$ are respectively the reluctances of the air gap in the outer core limb, the centre core limb and the lumped sum reluctance of the sections of the outer core limb other than the air gap. Fluxes ϕ_1, ϕ_2 and ϕ_c are respectively the instantaneous fluxes in three core limbs and correspond to $\phi_{\rm L1}, \phi_{\rm L2}$, and $\phi_{\rm T2}$ in (7). $F_{\rm L1}, F_{\rm L2}$, and $F_{\rm T2}$ are, respectively, the magnetomotive forces of the two inductor windings and the transformer winding. In Fig. 5(a), the windings between terminals 1 and 2 form the inductor L_1, those between terminals 1 and 3 form the inductor L_2, those between terminals 2 and 3 form the transformer T_2 primary and those between terminals 4 and 5 form the transformer T_2 secondary. The transformer primary and the two inductor windings have the same number of turns. As $\Re_g \gg \Re_{\rm co}$, the equivalent electrical circuit in Fig. 5(c) is obtained by applying the duality principle to the magnetic circuit shown in Fig. 5(b) and rescaling the circuit parameters [26]. It can be clearly seen that the two input inductances are inversely proportional to the reluctance of the air gap in the outer core

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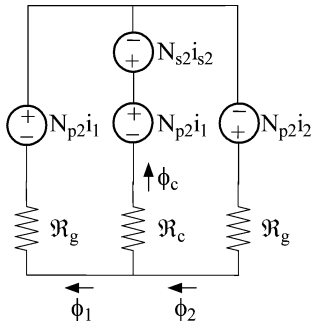

Fig. 6. Magnetic circuit when Q_4 is on and Q_3 is off.

limb and the magnetising inductance is inversely proportional to that of the centre core limb. The air gaps in the outer core limbs are used to store energy as required by the discrete inductor design.

In the magnetic design, the peak and ac flux densities are also two important parameters in the core saturation and loss analysis. According to (2) and (3), the input voltage of the two-inductor boost cell follows the rectified sinusoidal waveform therefore the flux magnitudes will vary over half cycle of the mains or the grid. An analysis of the dc and the ac fluxes in the individual core limbs can be made at a specific operating point.

Due to the magnetic integration, the flux distribution in the magnetic core can be more complicated. Therefore, the dc fluxes in the individual core limbs are discussed first. When Q_4 is on and Q_3 is off, the current in the inductor L_1 flows through the transformer T_2 primary. In this interval, the magnetic circuit shown in Fig. 5(b) can be redrawn as Fig. 6, where i_1 and i_2 are respectively the current in the inductors L_1 and $L_2, i_{\rm s2}$, and $n_{\rm s2}$ are, respectively, the current and the number of turns of the transformer T_2 secondary and $\Re_{\rm co}$ is neglected. Three independent relationships for the instantaneous fluxes in three core limbs ϕ_1, ϕ_2, and ϕ_c are

$$\Re_g\phi_1 + \Re_g\phi_2 = N_{p2}(i_1 + i_2) = N_{p2}i_H \tag{8}$$

$$\Re_g\phi_1 - \Re_c\phi_c = N_{s2}i_{s2} \tag{9}$$

$$\phi_c = \phi_2 - \phi_1 \tag{10}$$

where i_H is the instantaneous input current of the two-inductor boost cell.

As the converter operation is half cycle symmetrical, the average transformer T_2 secondary current $I_{\rm s2}$ in the interval shown in Fig. 6 can be represented by the average cell input current I_H over one high frequency cycle as

$$I_{s2} = \frac{N_{p2}}{N_{s2}} \cdot \frac{I_H}{2}. \tag{11}$$

Assuming that Φ_1, Φ_2, and Φ_c are, respectively, the dc components of ϕ_1, ϕ_2, and ϕ_c in the above interval, (8) to (10) can be rewritten as

$$\Re_g\Phi_1 + \Re_g\Phi_2 = N_{p2}I_H \tag{12}$$

$$\Re_g\Phi_1 - \Re_c\Phi_c = \frac{N_{p2}I_H}{2} \tag{13}$$

$$\Phi_c = \Phi_2 - \Phi_1. \tag{14}$$

As Φ_1, Φ_2, Φ_c, and I_H are also the dc components of ϕ_1, ϕ_2, ϕ_c and I_H over the entire high frequency switching cycle, (12) to (14) are valid over the entire switching cycle and the dc fluxes in the individual core limbs over one high frequency cycle can be solved as

$$\Phi_1 = \Phi_2 = \frac{N_{p2}I_H}{2\Re_g} \tag{15}$$

$$\Phi_c = 0. \tag{16}$$

In order to analyze the ac fluxes in the individual core limbs, the voltage waveforms in the boost cell at a fixed operating point are shown in Fig. 7. Applying Faraday's law to the two inductor windings on the outer core limbs and the transformer secondary windings on the centre core limb over the specified time durations as defined in Fig. 7 yields

$$N_{p2}\frac{d\phi_1}{dt} = V_H, \quad T_9 \le t \le T_{12} \tag{17}$$

$$N_{p2}\frac{d\phi_2}{dt} = V_H, \quad T_{11} \le t \le T_{14} \tag{18}$$

$$N_{s2}\frac{d\phi_c}{dt} = \frac{N_{s2}}{N_{p2}} \cdot \frac{V_H}{1 - D_{\rm boost}}, \quad 0 \le t \le T_9. \tag{19}$$

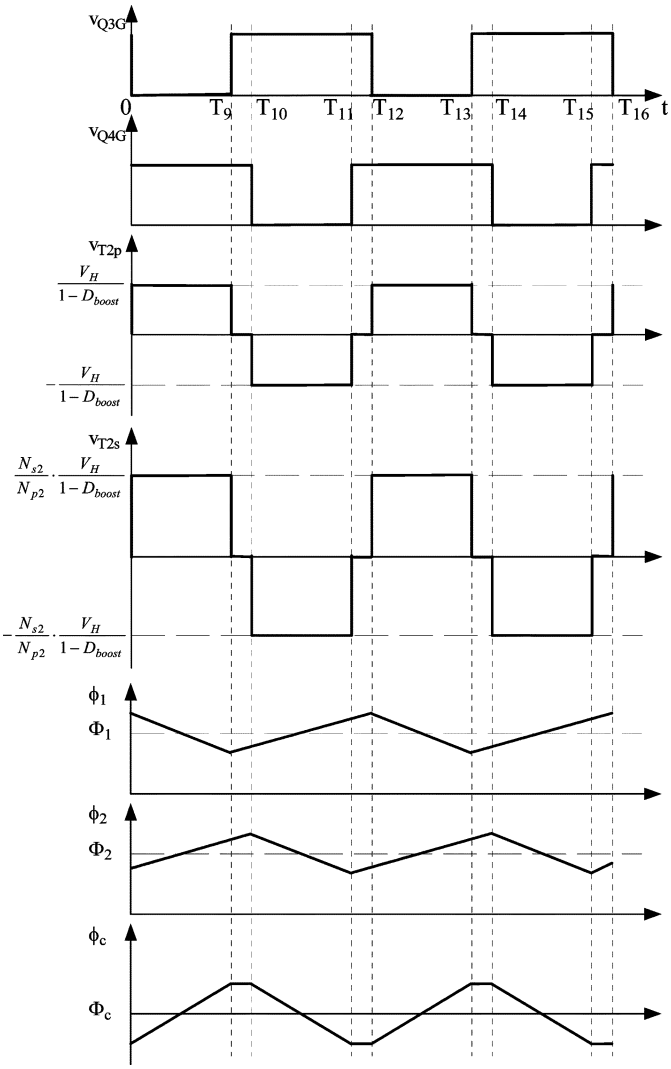

Fig. 7. Theoretical voltage and flux waveforms in the boost cell. ($T_9 = (1 - D_{\rm boost})T_{\rm boost}, T_{10} = T_{\rm boost}/2, T_{11} = (3/2 - D_{\rm boost})T_{\rm boost}, T_{12} = T_{\rm boost}, T_{13} = (2 - D_{\rm boost})T_{\rm boost}, T_{14} = 3T_{\rm boost}/2, T_{15} = (5/2 - D_{\rm boost})T_{\rm boost}, T_{16} = T_{\rm boost}$).

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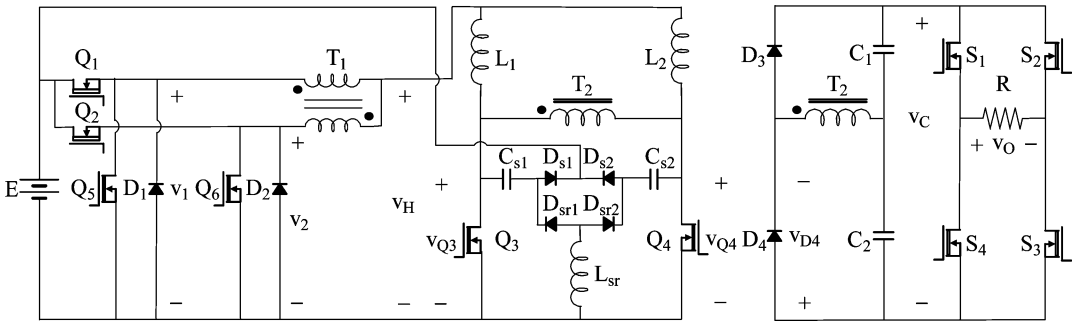

Fig. 8. Two-inductor boost converter with passive nondissipative snubbers.

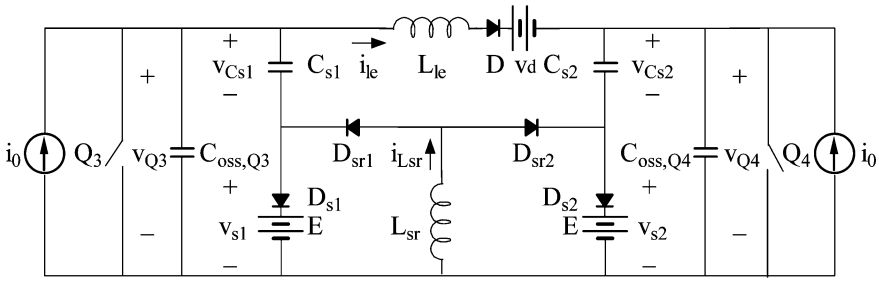

Fig. 9. Equivalent snubber circuit.

From (17)–(19), the ac fluxes in the two outer core limbs over one high frequency cycle $|\Delta\phi_1|$ and $|\Delta\phi_2|$ and that in the centre core limb $|\Delta\phi_c|$ can be, respectively, calculated as

$$|\Delta\phi_1| = |\Delta\phi_2| = \frac{V_H D_{\text{boost}} T_{\text{boost}}}{N_{p2}} \tag{20}$$

$$|\Delta\phi_c| = \frac{V_H T_{\text{boost}}}{N_{p2}}. \tag{21}$$

The cross section area of the outer core limb is normally made to be half that of the centre core limb in ETD core types. If A_o and A_c are, respectively, the cross section areas of the outer and centre core limbs, (22) can be obtained

$$A_o = \frac{A_c}{2}. \tag{22}$$

From (15), (16), and (20) –(22), the peak flux density in each core limb over one high frequency cycle can be calculated as

$$B_{1,\max} = B_{2,\max} = \frac{\Phi_1}{A_o} + \frac{|\Delta\phi_1|}{2A_o} = \frac{N_{p2} I_H}{\Re_g A_c} + \frac{V_H D_{\text{boost}} T_{\text{boost}}}{N_{p2} A_c} \tag{23}$$

$$B_{c,\max} == \frac{\Phi_c}{A_c} + \frac{|\Delta\phi_c|}{2A_c} = \frac{V_H T_{\text{boost}}}{2N_{p2} A_c}. \tag{24}$$

The flux waveforms are also shown in Fig. 7. It can be seen that the dc fluxes in the two outer core limbs are cancelled while the ac fluxes are added together in the centre core limb.

To check for the possibility of core saturation, the above analysis can be performed at mains peak voltage which will correspond to the peak of the input voltage V_H. From a thermal performance and loss viewpoint it is appropriate to perform the above analysis at an "averaged" value of the input voltage V_H. Many ferrites will have a loss that will vary as the square of the peak to peak flux excursion. In this case the root mean square average of the input voltage V_H would give a representative loss estimate.

B. Passive Non-Dissipative Snubbers

In the operation of the hard-switched two-inductor boost converter, the transformer leakage inductance is an adverse factor and causes switch over voltage at the MOSFET turn-off. In order to utilize MOSFETs with low voltage ratings or recover the associated loss terms, voltage clamping or snubber circuits must be used. A nondissipative snubber, which does not require additional control circuit, has been previously introduced with the two-inductor boost converter [14]. The snubber circuit in [14] uses two snubber inductors, two snubber capacitors and four diodes. Fig. 8 shows the converter with a variation of the passive nondissipative snubber, where one less snubber inductor is required. Space-saving is possible as the inductors are generally bigger than the capacitors and the diodes.

As the input voltage and current to the boost cell follow the rectified sinusoidal waveforms, the peak switch voltage varies. The snubber circuit is therefore only active when the buck stage duty ratio is relatively high. This avoids the energy circulation in the snubber circuit under lower buck stage duty ratios, which could potentially cause additional power losses due to the parasitic effects.

The snubber circuit can be analyzed using the equivalent circuit in Fig. 9. The current source I_0 models the inductor L_1 or L_2. The MOSFET Q_3 or Q_4 output capacitance is $C_{\text{oss},Q3} = C_{\text{oss},Q4} = C_{\text{oss}}$. The snubber capacitance is $C_{s1} = C_{s2} = C_s$. The transformer T_2 leakage inductance is L_{le}. The voltage source v_d is the capacitor C_1 or C_2 voltage reflected to the transformer T_2 primary and the diode D corresponds to the diode D_3 or D_4 in the voltage-doubler rectifier. The arrangement for v_d

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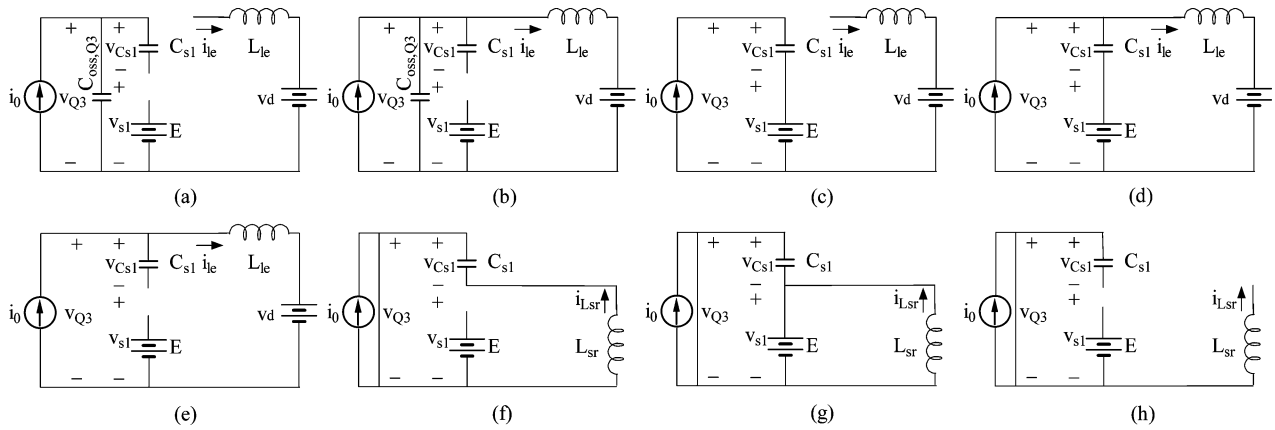

Fig. 10. Eight possible states in the snubber circuit.

TABLE I
SNUBBER CIRCUIT STATES FOR THREE SNUBBER OPERATION MODES

Mode	State (a)	State (b)	State (c)	State (d)	State (e)	State (f)	State (g)	State (h)
1			✓	✓	✓	✓	✓	✓
2	✓		✓	✓	✓	✓		✓
3	✓	✓		✓	✓	✓		✓

and D in Fig. 9 assumes a positive current $i_{\rm le}$ as illustrated and their polarities reverse when $I_{\rm le}$ becomes negative.

If $V_{\rm Cs0}$ is defined as the initial voltage across the snubber capacitor $C_{\rm s1}$ before Q_3 turns off or that across the snubber capacitor $C_{\rm s2}$ before Q_4 turns off, it can be established that $-E \leq V_{\rm Cs0} \leq 0$. The snubber circuit can operate in three active modes when $-E \leq V_{\rm Cs0} < 0$ and one inactive mode when $V_{\rm Cs0} = 0$. As the buck stage duty ratio varies to follow the low frequency mains sinusoidal cycle the relationship between the input voltage applied to the boost cell V_H and the source voltage E changes. The magnitude of V_H determines the snubber capacitor voltage at the end of the snubber operation cycle, which is also the corresponding initial snubber capacitor voltage $V_{\rm Cs0}$ in the following snubber operation cycle. When the buck stage duty ratio is large enough to cause $V_{\rm Cs0}$ to reach $-E$ at the end of the snubber operation cycle, the snubber circuit is involved in the converter operation instantaneously after the MOSFET Q_3 or Q_4 turns off. In this case, the snubber circuit operates in Mode 1. When the buck stage duty ratio becomes smaller, the magnitude of $V_{\rm Cs0}$ decreases at the end of the snubber operation cycle and $V_{\rm Cs0} > -E$. In this case, the snubber circuit is involved in the converter operation some time after the MOSFET Q_3 or Q_4 turns off but before the MOSFET output capacitance resonates with the transformer leakage inductance and the snubber circuit operates in Mode 2. When the buck stage duty ratio drops further, $V_{\rm Cs0} > -E$ and magnitude of $V_{\rm Cs0}$ is lower than that in Mode 2. In this case, the snubber circuit is only involved in the converter operation some time after the MOSFET output capacitance resonates with the transformer leakage inductance and the snubber circuit operates in Mode 3. When the buck stage duty ratio is small enough, the snubber circuit is inactive all the time and $V_{\rm Cs0} = 0$. The border conditions in terms of the buck stage duty ratio for each operation mode will be established after the state analysis of the snubber circuit is performed.

Due to the circuit symmetry, only the snubber circuit for Q_3 will be analyzed here. The snubber circuit has totally eight possible states as shown in Fig. 10. The states of the snubber circuit within one boost switching period for each operation mode are summarized in Table I. First, Mode 1 operation will be discussed in detail and the analysis of the states which do not appear in Mode 1 will be given for Modes 2 and 3 operations in due course.

In Mode 1, Q_3 turns off at $t = 0$ and the snubber circuit for Q_3 moves through totally six states as shown in Table I.

1) State (c) $(0 \leq t \leq t_1)$*:* The diode $D_{\rm s1}$ is forward biased and the current source I_0 linearly charges $C_{\rm s1}$. In this state, $C_{\rm oss,Q3}$ can be neglected as the snubber capacitance is normally selected to be much bigger than the MOSFET output capacitance. The diodes D and $D_{\rm sr1}$ are both reverse biased. The initial conditions are $v_{Cs1}(0) = -E$ and $i_{le}(0) = 0$. The voltage and current in the circuit are given by

$$v_{Cs1}(t) = -E + (i_0/C_s)t \tag{25}$$

$$i_{le}(t) = 0 \tag{26}$$

$$v_{Q3}(t) = (i_0/C_s)t \tag{27}$$

$$v_{s1}(t) = E. \tag{28}$$

2) State (d) $(t_1 \leq t \leq t_2)$*:* This state starts when $v_{\rm Q3}$ reaches v_d at $t_1 = v_d C_s/i_0$. Both of the diodes $D_{\rm s1}$ and D are forward biased and $C_{\rm s1}$ resonates with $L_{\rm le}$. The diode $D_{\rm sr1}$ remains reverse biased. The initial conditions are $v_{Cs1}(t_1) = v_d - E$ and

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$i_{le}(t_1) = 0$. The voltage and current in the circuit are given by

$$v_{Cs1}(t) = v_d - E + i_0 Z_1 \sin\omega_1(t - t_1) \quad (29)$$
$$i_{le}(t) = i_0 - i_0 \cos\omega_1(t - t_1) \quad (30)$$
$$v_{Q3}(t) = v_d + i_0 Z_1 \sin\omega_1(t - t_1) \quad (31)$$

where $Z_1 = \sqrt{L_{le}/C_s}$ is the characteristic impedance and $\omega_1 = 1/\sqrt{L_{le}C_s}$ is the angular resonant frequency of the resonant tank.

3) State (e) $(t_2 \le t \le t_3)$*:* This state starts when I_{le} reaches I_0 at $t_2 = t_1 + \pi/(2\omega_1)$. The diode D_{s1} becomes reverse biased. If the damped oscillations due to the transformer leakage inductance, the MOSFET output capacitance and the parasitic resistance in the resonant path is negelected, the diode D remains forward biased and the current source I_0 flows through L_{le} and v_d. The diode D_{sr1} is still reverse biased. The voltage and current in the circuit are given by

$$v_{Cs1}(t) = v_d - E + i_0 Z_1 \quad (32)$$
$$i_{le}(t) = i_0 \quad (33)$$
$$v_{Q3}(t) = v_d \quad (34)$$
$$v_{s1}(t) = E - i_0 Z_1. \quad (35)$$

4) State (f) $(t_3 \le t \le t_4)$*:* This state starts when Q_3 turns on at $t_3 = (1 - D_{boost})T_{boost}$. The diode D_{s1} remains reverse biased. The diode D_{sr1} becomes forward biased and L_{sr} resonates with C_{s1}. The initial conditions are $v_{Cs1}(t_3) = v_d - E + i_0 Z_1$ and $i_{Lsr}(t_3) = 0$. The voltage and current in the circuit are given by

$$v_{Cs1}(t) = (v_d - E + i_0 Z_1)\cos\omega_2(t - t_3) \quad (36)$$
$$i_{Lsr}(t) = [(v_d - E + i_0 Z_1)/Z_2]\sin\omega_2(t - t_3) \quad (37)$$
$$v_{Q3}(t) = 0 \quad (38)$$
$$v_{s1}(t) = (E - v_d - i_0 Z_1)\cos\omega_2(t - t_3) \quad (39)$$

where $Z_2 = \sqrt{L_{sr}/C_s}$ is the characteristic impedance and $\omega_2 = 1/\sqrt{L_{sr}C_s}$ is the angular resonant frequency of the resonant tank.

5) State (g) $(t_4 \le t \le t_5)$*:* This state is the energy recovery state and starts when v_{Cs1} reaches $-E$ at T_4. The diode D_{s1} becomes forward biased and the diode D_{sr1} remains forward biased. The voltage source E linearly discharges L_{sr} and the energy in L_{sr} is returned to E. The initial conditions are $v_{Cs1}(t_4) = -E$ and $i_{Lsr}(t_4) = [(v_d - E + i_0 Z_1)/Z_2]\sin\omega_2(t_4 - t_3)$. The voltage and current in the circuit are given by (28), (38), and

$$v_{Cs1}(t) = -E \quad (40)$$
$$i_{Lsr}(t) = i_{Lsr}(t_4) - (E/L_{sr})(t - t_4). \quad (41)$$

6) State (h) $(t_5 \le t \le t_6)$*:* This state starts when I_{Lsr} reaches 0 at $t_5 = t_4 + i_{Lsr}(t_4)L_{sr}/E$. The snubber circuit will become active when Q_3 turns off again at $t_6 = T_{boost}$ except that L_{sr} will be earlier involved in the operation of the snubber circuit for Q_4 when Q_4 turns on.

Modes 2 and 3 snubber operations can be analyzed in the same way. Unlike Mode 1, these two modes do not have the energy recovery state, State (g) in Fig. 10. The analyses of States (a) and (b) are briefly provided below.

In state (a) when $0 \le t \le t_1$, the diode D_{s1} is reverse biased as $V_{Cs0} > -E$ and the current source I_0 linearly charges $C_{oss,Q3}$ when Q_3 turns off at $t = 0$. The diodes D and D_{sr1} are both reverse biased. The voltage and current in the circuit are given by (26) and

$$v_{Cs1}(t) = V_{Cs0} \quad (42)$$
$$v_{Q3}(t) = (i_0/C_{oss})t \quad (43)$$
$$v_{s1}(t) = -V_{Cs0} + (i_0/C_{oss})t. \quad (44)$$

In state (b) when $t_1 \le t \le t_2$, v_{Q3} reaches v_d and the diode D becomes forward biased at $t = t_1$. The diode D_{s1} is still reverse biased as $v_{s1} < E$. The diode D_{sr1} remains reverse biased and $C_{oss,Q3}$ resonates with L_{le}. The voltage and current in the circuit are given by (42) and

$$i_{le}(t) = i_0 - i_0 \cos\omega_3(t - t_1) \quad (45)$$
$$v_{Q3}(t) = v_d + i_0 Z_3 \sin\omega_3(t - t_1) \quad (46)$$
$$v_{s1}(t) = v_d - V_{Cs0} + i_0 Z_3 \sin\omega_3(t - t_1). \quad (47)$$

where $Z_3 = \sqrt{L_{le}/C_{oss}}$ is the characteristic impedance and $\omega_3 = 1/\sqrt{L_{le}C_{oss}}$ is the angular resonant frequency of the resonant tank.

As mentioned earlier in the paper, the operation mode of the snubber circuit is intrinsically determined by the buck stage duty ratio. In order to establish the range of the buck stage duty ratios for each operation mode, the current source i_0 and the voltage source v_d in Fig. 10 must first be written in terms of D_{buck}

$$v_d = D_{buck}E/(1 - D_{boost}) \quad (48)$$
$$i_0 = D_{buck}P_{avg}/E \quad (49)$$

where P_{avg} is the converter average output power over a low frequency sinusoidal cycle.

In Mode 1, v_{Cs1} must reach $-E$ before I_{Lsr} reaches 0 in State (f) in Fig. 10. According to (36) and (37), the border condition is

$$2E - v_d - i_0 Z_1 = 0. \quad (50)$$

Substituting (48) and (49) to (50) and replacing D_{buck} with $D_{buck,1}$ yields

$$D_{buck,1} = 2 \Big/ \left(\frac{1}{1 - D_{boost}} + \frac{P_{avg}}{E^2} Z_1 \right). \quad (51)$$

Therefore, the range of the buck stage duty ratio for the snubber circuit to operate in Mode 1 is $D_{buck} \geqslant D_{buck,1}$. If $D_{buck} < D_{buck,1}$, the snubber circuit starts to operate in Mode 2. It is also required that v_{s1} reaches E before v_{Q3} reaches v_d in State (a) in Fig. 10. According to (36), (43), and (44), the lower border condition is

$$2E - 2v_d - i_0 Z_1 = 0. \quad (52)$$

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TABLE II
THREE ACTIVE SNUBBER CIRCUIT OPERATION MODES

Mode		Mode 1	Mode 2	Mode 3
Time when snubber circuit becomes active		When Q_3 or Q_4 turns off	After Q_3 or Q_4 turns off and before v_{Q3} or v_{Q4} reaches v_d	After v_{Q3} or v_{Q4} reaches v_d
V_{Cs0}		V_{Cs0}=-E	-E<V_{Cs0}<0	-E<V_{Cs0}<0
D_{buck}	Upper Border	D_{buck}=1	$D_{buck}=\dfrac{2}{\dfrac{1}{1-D_{boost}}+\dfrac{P_{avg}}{E^2}Z_1}$	$D_{buck}=\dfrac{1}{\dfrac{1}{1-D_{boost}}+\dfrac{P_{avg}}{2E^2}Z_1}$
	Lower Border	$D_{buck}=\dfrac{2}{\dfrac{1}{1-D_{boost}}+\dfrac{P_{avg}}{E^2}Z_1}$	$D_{buck}=\dfrac{1}{\dfrac{1}{1-D_{boost}}+\dfrac{P_{avg}}{2E^2}Z_1}$	$D_{buck}=\dfrac{1}{\dfrac{1}{1-D_{boost}}+\dfrac{P_{avg}}{E^2}Z_3}$
Energy Recovery		Yes	No	No

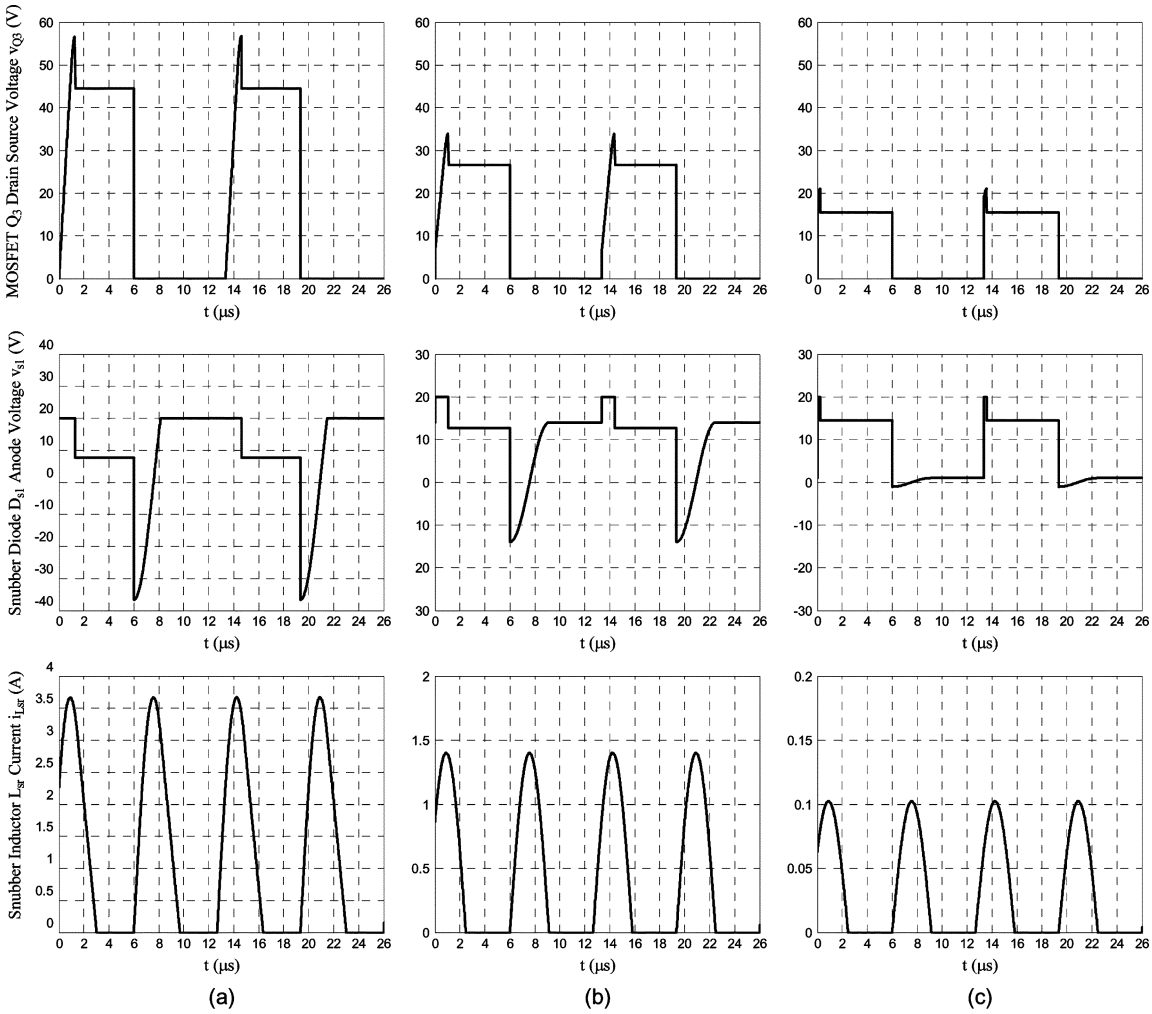

Fig. 11. Voltage and current waveforms in the snubber circuit. (a) Mode1. (b) Mode 2. (c) Mode 3.

Substituting (48) and (49) to (52) and replacing $D_{\rm buck}$ with $D_{\rm buck,2}$ yields

$$D_{\rm buck,2}=1\Big/\left(\frac{1}{1-D_{\rm boost}}+\frac{P_{\rm avg}}{2E^2}Z_1\right). \tag{53}$$

Therefore the range of $D_{\rm buck}$ for the snubber circuit to operate in Mode 2 is $D_{\rm buck,2}\le D_{\rm buck}<D_{\rm buck,1}$. If $D_{\rm buck}<D_{\rm buck,2}$, the snubber circuit starts to operate in Mode 3. It is also required that $v_{\rm s1}$ reaches E in State (b) in Fig. 10. It is obvious that $V_{\rm Cs0}=0$ when the snubber circuit operates at the lower border of Mode 3. According to (47), the lower border condition is

$$v_d+i_0Z_3=E. \tag{54}$$

Substituting (40) and (41) –(46) and replacing $D_{\rm buck}$ with $D_{\rm buck,3}$ yields

$$D_{\rm buck,3}=1\Big/\left(\frac{1}{1-D_{\rm boost}}+\frac{P_{\rm avg}}{E^2}Z_3\right). \tag{55}$$

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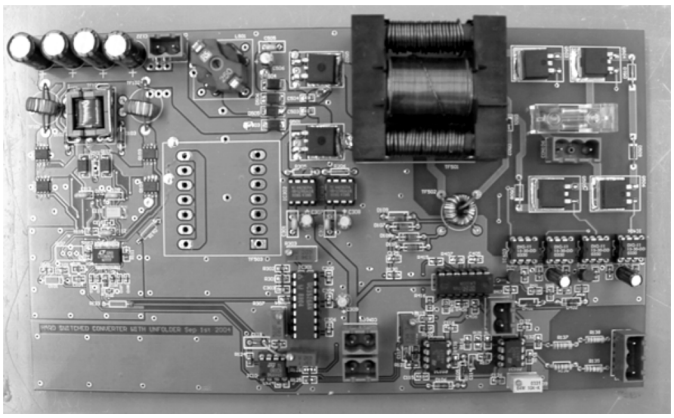

Fig. 12. Prototype 100-W converter.

Therefore, the range of $D_{\rm buck}$ for the snubber circuit to operate in Mode 3 is $D_{\rm buck,3} \leq D_{\rm buck} < D_{\rm buck,2}$. If $D_{\rm buck} < D_{\rm buck,3}$, the snubber circuit starts to operate in the inactive mode, where the snubber diodes remain reverse biased all the time.

The three active snubber circuit operation modes can be summarised in Table II.

The snubber capacitor and inductor are respectively designed to be 0.1 μF and 10 μH. The theoretical waveforms of $v_{\rm Q3}, v_{\rm s1}$, and $I_{\rm Lsr}$ in three operation modes are shown in Fig. 11. The transformer leakage inductance of 0.60 μH and the MOSFET output capacitance of 990 pF are also used in (25)–(47) to obtain the plots. Mode 1 is characterized by the $v_{\rm Q3}$ waveform with a small voltage slope at the turn-off due to the linear charging of the relatively large snubber capacitance. Mode 2 is characterized by the $v_{\rm Q3}$ waveform with an initial large voltage slope followed by a small voltage slope at the turn-off due to the linear charging of the much smaller MOSFET output capacitance first and then the larger snubber capacitance. Mode 3 is characterized by the $v_{\rm Q3}$ waveform with large voltage slopes at the turn-off almost until $v_{\rm Q3}$ reaches its peak due to the linear charging of the MOSFET output capacitance first and the resonance between the MOSFET output capacitance and the transformer leakage inductance. Then the resonance between the snubber capacitance and the transformer leakage inductance only happens in a very short time before the transformer primary current reaches i_0.

C. Silicon Carbide Rectifier

The rectification stage of the two-inductor boost cell is configured as a voltage-doubler rectifier. Silicon junction diodes at 600-V repetitive peak reverse voltage have relatively long reverse recovery times. The resulting switching losses can potentially cause thermal runaways which may lead to the converter failure. The diodes face operating conditions that are similar to those found in other boost converter applications. If the transformer leakage inductance is reduced to avoid over voltages for the primary switches, high di/dt values result for the output diodes. Silicon Carbide Schottky diodes have high reverse breakdown voltage ratings and near zero reverse recovery time [27]. If SiC Schottky diodes are used as the rectifiers, the power losses related to the reverse recovery can be removed and the converter reliability can be improved.

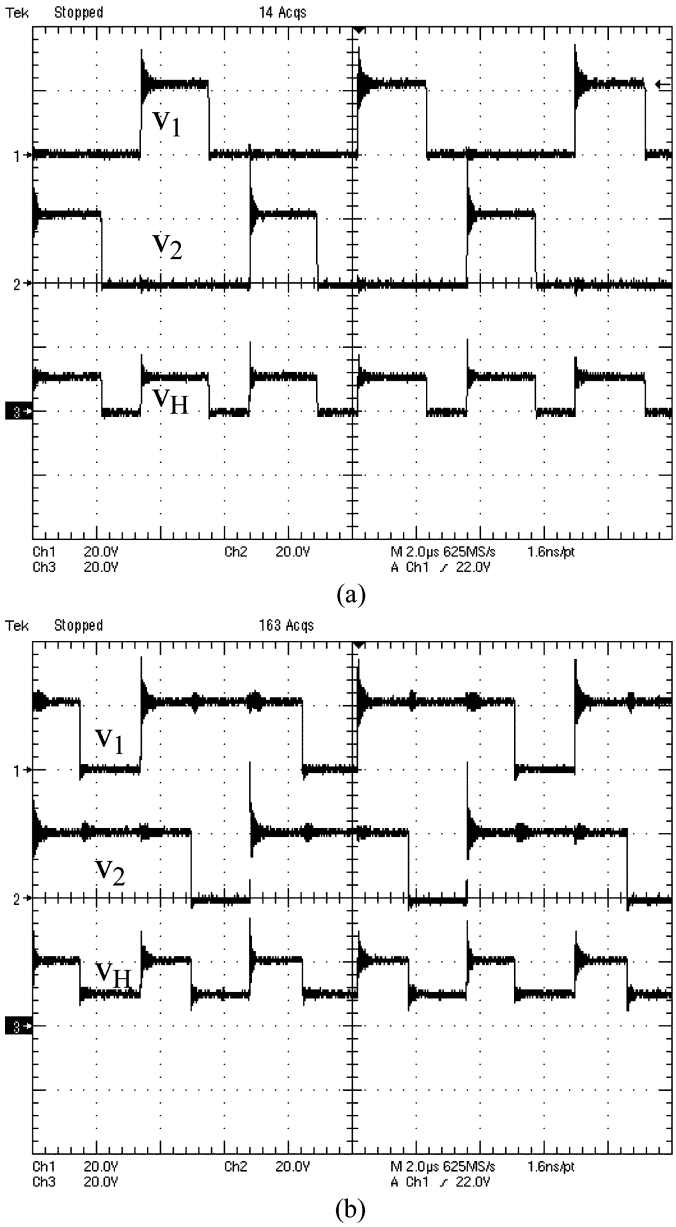

Fig. 13. Voltage waveforms in the two-phase synchronous buck converter. (a) $D_{\rm buck}$ <50%. (b) $D_{\rm buck}$ >50%.

IV. Unfolder

As the input of the dc–ac inverter is the rectified sinusoidal waveform, the square-wave control can be applied and the dc–ac inverter is reduced to an unfolder. In the unfolding stage, the switches turn on and off under the line frequency and this avoids high switching losses caused by PWM control. The transfer function of the unfolder is

$$v_O = \begin{cases} v_C, & S_1 \text{ and } S_3 \text{ on} \\ -v_C, & S_2 \text{ and } S_4 \text{ on} \end{cases}. \tag{56}$$

The output voltage of the converter can be obtained by multiplying (2), (4), and (56) as

$$v_O = \begin{cases} \frac{2n_{T2}D_{\rm buck}}{1-D_{\rm boost}}E, & S_1 \text{ and } S_3 \text{ on} \\ -\frac{2n_{T2}D_{\rm buck}}{1-D_{\rm boost}}E, & S_2 \text{ and } S_4 \text{ on} \end{cases}. \tag{57}$$

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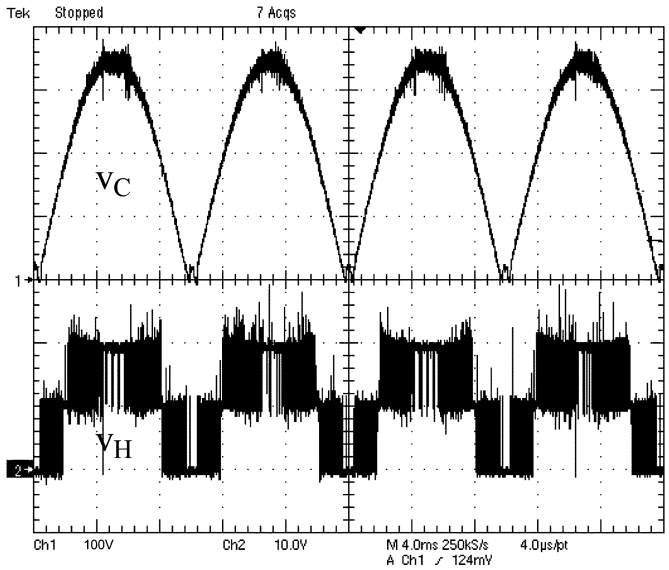

Fig. 14. Output and input voltage waveforms in the two-inductor boost cell.

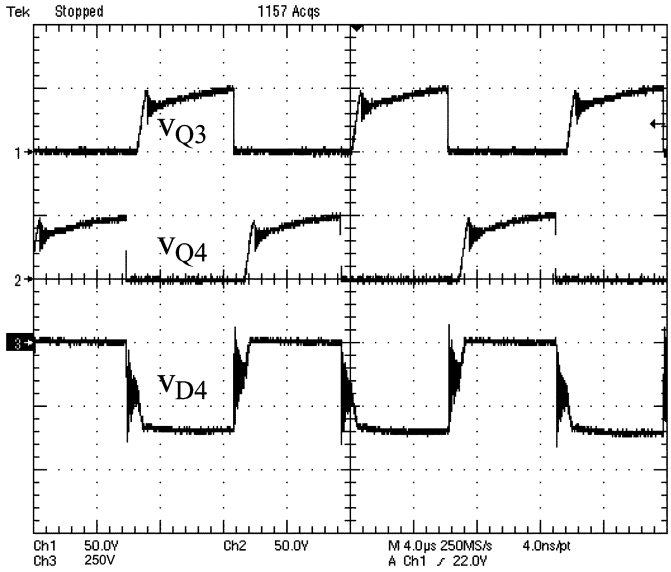

Fig. 15. MOSFET drain source and diode voltage waveforms in the two-inductor boost cell.

To avoid the high side drivers and the additional control circuitry for the MOSFETs, electrically isolated optical MOSFET drivers are used to provide the gate signals. The MOSFET gate charging current is developed from a PV source [28]. The optical MOSFET drivers must also have an embedded active discharge circuit to discharge the MOSFET gate capacitance to obtain fast turn-off behaviours [29].

V. Experimental Results

To confirm the theoretical analysis, a prototype 100-W converter was built in the laboratory as shown in Fig. 12. The experimental waveforms will be shown separately for the three power conversion stages as below.

A. Buck Stage

The buck conversion stage is based upon a commercial two-phase synchronous step-down switching regulator—Linear Technology LTC1929 [30]. Minor modifications are required to the normal control loop to obtain a widely variable output voltage range. The switching elements are implemented with surface mount MOSFETs and diodes with compact packages. The IPT is implemented with an EFD15 core, whose effective volume is 510 mm^3 (0.03 cubic inches) [31]. The total Print Circuit Board (PCB) area allocated to the buck converter is 40 mm $\times$ 70 mm (1.6 in $\times$ 2.8 in) and this can be reduced if further optimisation is performed in the component selection and the PCB design. The switching of the buck converter is synchronized through the switching controller in the two-inductor boost cell.

Fig. 13 shows the buck converter waveforms under static dc–dc conversion tests. From top to bottom, Fig. 13(a) and (b), respectively, shows the waveforms of v_1, v_2 and v_H with duty ratio D_{buck} lower and greater than 50%. The voltage after the IPT swings between zero and the half input voltage or the half and the full input voltage depending on the value of D_{buck}. In both cases, the frequency of the voltage v_H after the IPT is twice that of voltage v_1 or v_2.

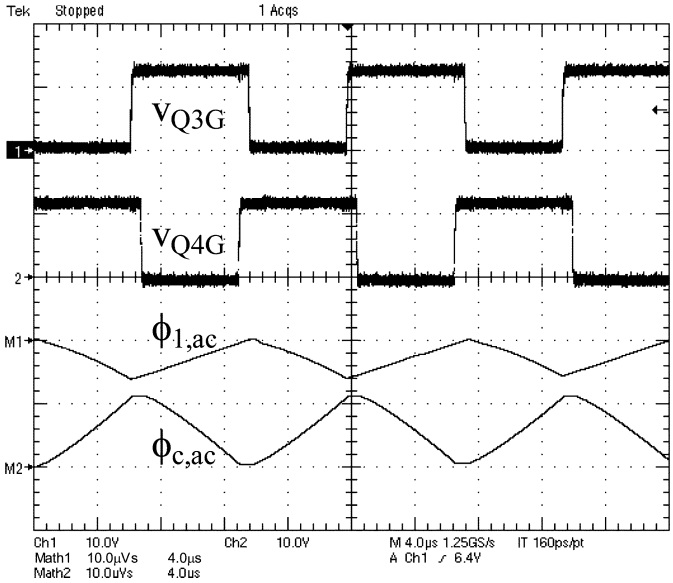

Fig. 16. MOSFET gate voltage and core limb flux waveforms in the two-inductor boost cell.

B. Boost Stage

Fig. 14 shows the two-inductor boost converter output voltage v_c and the input voltage v_H from top to bottom during sinusoidal modulation. A three-level modulation can be clearly seen from the v_H waveform although the captured waveform is heavily aliased. Small voltage spikes appear between the half sinusoidal waveforms because all four switches in the unfolder turn off around the zero crossing of the sinusoidal waveforms.

Fig. 15 shows the MOSFETs Q_3 and Q_4 drain source voltages and the voltage across the SiC Schottky diode when the converter output voltage is close to its peak. The snubber circuit controls the maximum peak switch voltage in a low frequency cycle to around 50 V. This allows the MOSFETs with drain-source breakdown voltage ratings of 55 V to be used in the two-inductor boost cell. MOSFET forward resistances are

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TABLE III
DC AND AC FLUXES AND FLUX DENSITIES IN THE INDIVIDUAL CORE LIMBS

Core Limb	DC Flux (μWb)	AC Flux (μWb-pp)	AC Flux Density (mT-pp)	Peak Flux (μWb)	Peak Flux Density (mT)
Outer	17.77	6.38	104	20.96	341
Centre	0	11.59	94	5.80	47

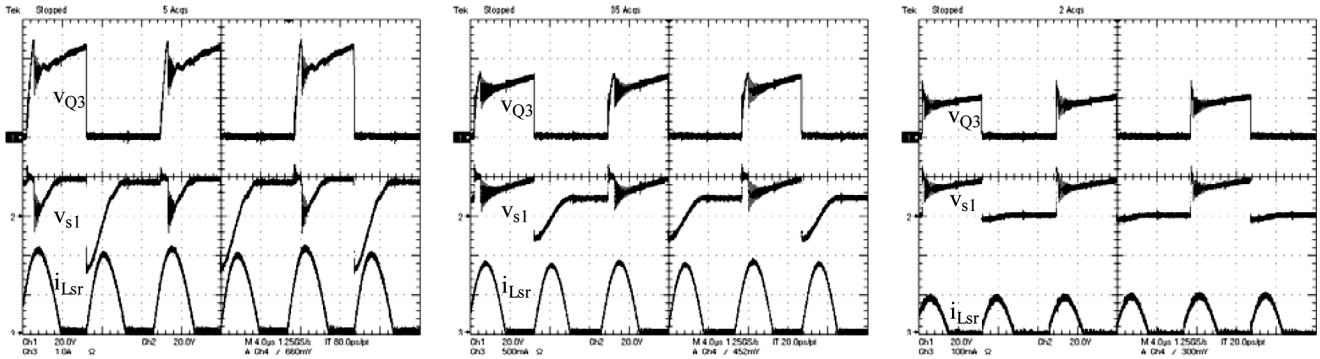

Fig. 17. Voltage and current waveforms in the snubber circuit. (a) Mode 1. (b) Mode 2. (c) Mode 3.

low under low voltage ratings and this minimizes the conduction losses. The SiC diode voltage waveform is relatively clean although some high frequency oscillations exist due to the resonance between the transformer leakage inductance and the diode junction capacitance.

In this converter, a Ferroxube ETD39 core with a 0.5-mm air gap in each of the outer core limbs is used. The cross section area of the ETD39 centre core limb is 123 mm^2 [32]. The number of turns are, respectively, $n_{\rm L1} = n_{\rm L2} = n_{\rm p2} = 23$ and $n_{\rm s2} = 98$. The dc and ac fluxes and flux densities in the individual core limbs when $D_{\rm buck} = 1$ are given in Table III.

Fig. 16 shows the MOSFETs Q_3 and Q_4 gate voltage and the ac components of the fluxes in the outer and centre core limbs ϕ_1 and ϕ_c over high frequency cycles when the converter output voltage is close to its peak. The flux waveforms are obtained through integrating the voltage across one search turn wound around the corresponding core limbs. The waveforms shown in Fig. 16 agree well with those shown in Fig. 7.

Fig. 17 shows the MOSFET Q_3 drain source voltage, the snubber diode $D_{\rm s1}$ anode voltage and the snubber inductor $L_{\rm sr}$ current under three snubber circuit operation modes. The characteristics of the individual operation modes given by Fig. 11 can be clearly observed here although the corresponding operating point in each mode in the practical converter is not exactly the same as that in the theoretical plots. Some differences between the theoretical and the experimental waveforms lie on the damped oscillations after the MOSFET Q_3 drain source voltage reaches its peak due to the resonance between the MOSFET output capacitance and the transformer leakage inductance and as well on the voltage source in the snubber equivalent circuit shown in Fig. 11 being not a constant due to the charging of the capacitors in the rectification stage of the boost cell.

C. Unfolding Stage

Fig. 18 shows the gate waveforms of the low frequency unfolder switches, the output voltage v_O and the output current I_O from top to bottom. In this case a resistive load is supplied and this is adjusted to give the rated power, 100 W at 240 V ac, which is equivalent to the nominal mains voltage.

A conversion efficiency of 92% was obtained for the three-stage converter with the rated power. Input and output powers were measured using the mathematical functions of a Tektronix TDS5034 four-channel oscilloscope equipped with converter input and output voltage and current probes. The current probes are Tektronix TCP202. The power loss includes the losses in all three conversion stages—the buck, the boost and the unfolding stages. Fig. 19 shows the converter efficiencies under a range of load conditions.

The power ratings, the efficiencies and the sizes of several published MICs are compared in Table IV. The existing board has dimensions of 125 mm by 200 mm (5 in by 8 in) however no explicit attempt has been made to reduce the PCB size at this prototype stage. If an unused area of 5100 mm^2 (7.9 square inches) on the prototyping PCB as shown in Fig. 12 is considered, the size of the converter proposed in this paper reduces to 125 mm by 160 mm (5 in × 6.4 in) and this is certainly comparable to the sizes of the other converters listed in Table IV.

VI. CONCLUSION

In this paper, a current fed two-inductor boost converter with an unfolder is proposed for the MIC applications for grid interactive PV systems. The two-phase synchronous buck converter is sinusoidally modulated and supplies rectified sinusoidal current to the two-inductor boost cell. Therefore, the boost stage is able to generate the rectified sinusoidal voltage on the dc link and this eases the design of the dc–ac inversion stage to an unfolding stage operating at the line frequency.

Some important technologies such as the multiphase converter, the synchronous rectifier, the magnetic integration, the non-dissipative snubber, the Silicon Carbide Schottky diodes and the electrically isolated optical MOSFET drivers are employed in the converter to achieve a compact design with an overall high efficiency.

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TABLE IV
COMPARISONS OF MIC PARAMETERS

Converter	Power Rating (W)	Efficiency	PCB Size (mm × mm)
OK4-100 in [5]	100	94%	93 × 120
Converter Proposed in [6]	110	87%	95 × 130
Converter Proposed in [7]	105	-	130 × 150
Converter Proposed in [8]	160	86.7%	-
Converter Proposed in [10]	100	84%	-
Converter Proposed in This Paper	100	92%	125 × 200

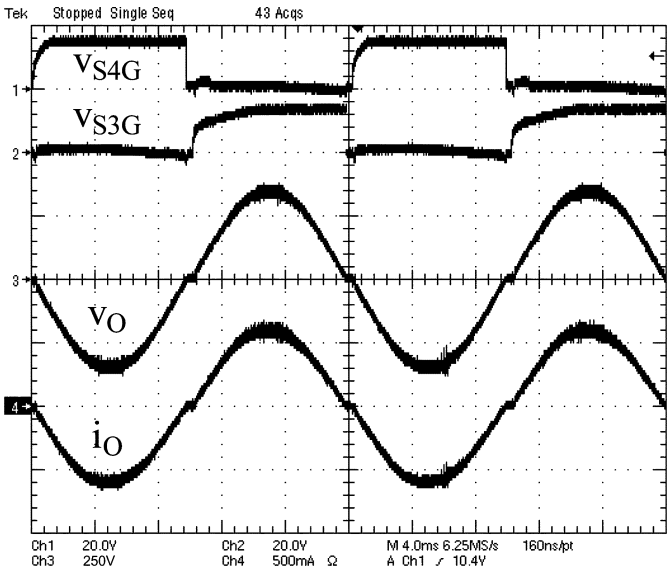

Fig. 18. MOSFET gate voltage, output voltage and current waveforms in the unfolder.

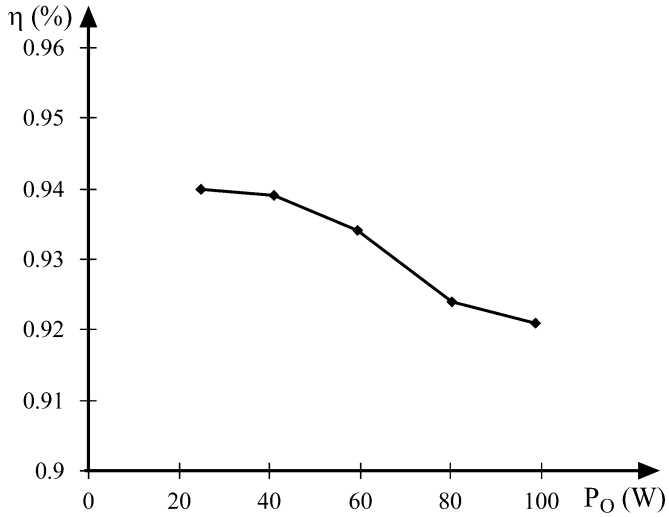

Fig. 19. Converter efficiencies over the load range.

Finally, some experimental waveforms are provided for a 100-W 240-V converter to validate the theoretical analysis. The measurement through the oscilloscope shows that an efficiency of 92% has been achieved for the PV module integrated converter.

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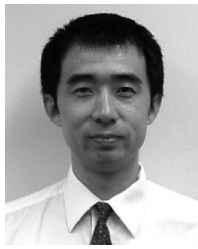

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