A THIN FILM TRIODE TYPE CARBON NANOTUBE FIELD ELECTRON EMISSION CATHODE

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A THIN FILM TRIODE TYPE CARBON NANOTUBE FIELD ELECTRON EMISSION CATHODE

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To my late father

CDR Richard C. Sanborn, M.D., USN

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LIST OF SYMBOLS OR ABBREVIATIONS

A	Emission area
a	Bond length
a_1/a_2	CNT lattice unit vectors
ADCS	Attitude determination and control systems
AFIT	Air Force Institute of Technology
BOE	Buffered oxide etch
CEX	Charge exchange ions
CFEA	Carbon nanotube field emission array
C_h	Chiral Vector
$\|C_h\|$	The magnitude of the chiral vector
CNT	Carbon nanotube
CVD	Chemical vapor deposition
d	Separation distance, diameter
$D(E)$	Transmission probability of electrons
E	Energy
e	The elementary charge
EDS	Energy-dispersive X-ray spectroscopy
E_g	Band gap energy
E_{th}	Threshold Field
E_{to}	Turn-on Field
eV	Electron volts
E_x	Kinetic energy of electrons
F	Electric field

$f(E)$	Probability of an electron having energy E
FE	Field electron emission
F-N	Fowler-Nordheim
h	Plank's constant, height
HET	Hall effect thruster
HMDS	Hexamethyldisilazane
HPEPL	High Power Electric Propulsion Laboratory
I	Current
IAD	Ion assisted deposition
iMESA	Integrated miniaturized electrostatic analyzer
IR	Infrared
J	Current density
k	Boltzmann's constant
LN_2	Liquid nitrogen
LPCVD	Low pressure chemical vapor deposition
m	Mass or slope
MRL	Manufacturing readiness level
MWNT	Multi walled carbon nanotube
n	Integer number
OM	Optical microscopy
p	Momentum
PECVD	Plasma enhanced chemical vapour deposition
p-Si	Polycrystalline silicon
Q	Heat
r	Radius

R	Resistance
RF	Radio frequency
RIE	Reactive ion etch
sccm	Standard cubic centimeters per minute
SEM	Scanning electron microscopy
SWNT	Single walled carbon nanotube
T	Temperature
TEM	Transmission electron microscopy
TRL	Technology readiness level
V	Potential, Voltage
$V(x)$	Potential field distribution
VACNT	Vertically aligned carbon nanotube
VI	Virtual instruments
V_{im}	The image potential
VLS	Vapor-liquid-solid
VTF-2	Vacuum test facility 2
WKB	Wentzel-Kramers-Brillouis
β	Field enhancement factor
Δp	Uncertainty in momentum
Δx	Uncertainty in position
θ	Angle, angle between C_h and the unit vector a_1
λ	Wavelength
μ	Fermi level
v	Frequency
v_F	Fermi velocity

π	Valence band
π^*	Conduction band
φ	work function

SUMMARY

Carbon nanotubes (CNTs) show favorable properties for field electron emission (FE) and performance as electron sources. This dissertation details the developments of a low power, thin film electron source that takes advantage of the unique material properties of CNTs. The seminal work in this type of design is attributed to the Spindt cathode, which contain internally gated arrays of metal emission tips by separating a conductive substrate and a gate electrode with a dielectric layer. Recently, high aspect ratio nanomaterials, such as CNTs, have been of interest for electron sources in thin film triode designs. A uniquely designed Spindt type CNT field emission array (CFEA) is developed in this work, from initial concept to working prototype, to specifically prevent electrical shorting of the gate. The CFEA is patent pending in the United States.

Due to the nature of the integrated gate design, several changes to the fabrication process were made to maintain the electrical isolation of the gate. These changes include optimizing deposition of the oxide and gate layers, removing gate material where the wafer is diced, precisely controlling where the metal CNT catalyst is deposited, and optimizing the pit geometry by etching into the Si substrate and using isotropic etching to prevent CNTs from contacting the gate.

A chemical vapor deposition (CVD) CNT synthesis process was also developed. Initially, it was found that the preferred plasma enhanced CVD technique caused shorting by arcing between the floating gate and substrate layers. Several attempts to temporarily ground the gate were unsuccessful in preventing shorting. A process was subsequently developed for low pressure CVD without plasma. Catalyst and process tuning resulted in precisely controlled CNT height with uniform and consistent CNT growth.

All of the above changes enabled fabrication of a CFEA that wasn't electrically shorted. Furthermore, a novel oxygen plasma etch process was developed to reverse shorting after CNT synthesis and increase yield. This process briefly exposes shorted CFEAs to an oxygen plasma, which has minimal effect on the CNTs but reverses shorting and increased open circuit CFEA yield by an average of 71%. Overall, the process improvements resulted in an open circuit chip yield of up to 82% on final generation wafers.

FE testing results are presented for both individually tested and large scale testing of many CFEAs together. For the large scale testing, a full electronic system was developed with collaborators. CFEAs were wire bonded to electronic packages and integrated into arrays in custom circuit boards and a mounting apparatus in the vacuum test chamber. Custom switchboards, electronics, and LabVIEW programs were integrated with the array so that the apparatus could simultaneously test up to eighty CFEAs at once while individually measuring cathode current.

CFEA testing demonstrates FE with a current density of up to 293 $\mu A/cm^2$ at the anode and 1.68 mA/cm^2 at the gate, where current density is calculated from total area of the device. For comparison to planar CNT sources, current density calculated using the CNT area gives a maximum anode current density of 241 mA/cm^2. In addition, several microamps of anode current are achieved at as little as 40 V. Cumulative lifetimes are achieved in excess of 100 hours with a constant emission of slightly less than 50 $\mu A/cm^2$.

The performance and lifetime between samples was found to be very inconsistent. In high volume work, eighty different CFEAs were tested with various failure and emission results. During this FE testing, a "burnout" technique was developed to reverse

shorting from FE testing, which showed a 69% success rate of reversing electrical shorting. While under vacuum, a voltage limited current was applied, which normally caused a current spike and subsequent drop with a return to an open circuit.

A detailed analysis of the eighty tested CFEAs revealed three distinct types of damage from FE testing: gate melting, melting within the etch pit, and material ejecta. Of the eighty CFEAs, 43% show at least one type of damage. Surprisingly, about half of the damaged chips are not electrically shorted and all of the heavily damaged pits are not shorted. These observations reveal that the CFEA design is very robust and able to withstand significant damage without shorting.

Potential applications of this technology include cathodes for Hall effect thrusters (HETs), spacecraft neutralization, and tethers for spacecraft deorbiting. The use with HETs was explored in a collaboration with the HPEPL at Georgia Tech. These thrusters are a type of electric propulsion for spacecraft that normally use inefficient hot cathodes to ionize a gas propellant. To study the effect of the HET plasma environment on the CFEAs, the cathode array holding 41 chips was mounted around a HET and exposed for a total of forty minutes. The HET exposure caused significant sputtering of the Au plating on the electronic packages. However, no significant effect or damage was found on the chips or CNTs, showing that the CFEA is able to withstand exposure to the HET environment and could be a viable cathode for HETs.

A second effort on applications in spacecraft propulsion is a collaboration with the Air Force Institute of Technology (AFIT). CFEAs have been provided to AFIT to test their emission in the space environment and compare their performance to that on earth. AFIT has internally developed a CubeSat, called ALICE, to run the experiments with the

CFEAs as the payload. ALICE has passed all flight tests and is currently awaiting launch scheduled for December 2013.

For this dissertation, a number of unique and original contributions have been made to the field, including:

1. The development of a novel Spindt type CNT field emission array (CFEA).

2. The development of an oxygen plasma resurrection technique to reverse electrical shorting of CFEAs after CNT synthesis to greatly improve yield.

3. The development of an electrical "burnout" resurrection technique to reverse CFEA shorting from FE testing.

4. The analysis of 80 FE tested CFEAs identifies three distinct damage modes and demonstrates a robust design.

5. The first exposure of a CNT field emitter to an operating Hall effect thruster.

6. The first planned launch and operation of a CNT field emitter in space.

CHAPTER 1

MOTIVATION

The current technological age is embodied by a constant push for increased performance and efficiency of electronic devices. This push is particularly observable for technologies that comprise free electron sources, which are used in various technologies including electronic displays, x-ray sources, telecommunication equipment, and spacecraft propulsion [1]. Performance of these systems can be increased by reducing weight and power consumption, but is often limited by a bulky electron source with a high energy demand. Considering the advancement of electronics in recent times, free electron sources have not changed significantly. This work explores the development of a low power, thin film, and light weight electron source in a design that takes advantage of the unique material properties of carbon nanotubes (CNT).

Most electron sources utilize thermionic emission, which involves heating a metal filament to several thousand degrees Celsius in order to produce electrons [1]. Thermionic emission sources possess inherent inefficiencies because they are relatively bulky and must be heated to high temperatures, thus consuming more energy [2]. An alternative to thermionic emission is field electron emission (FE), which involves the application of electric fields at room temperatures to induce electron emission via tunnelling. Normally, large electric fields (100's of V/μm) are needed for FE [3], but this field is highly dependent on the electron source geometry, where sharp tips can reduce

the macroscopic electric field needed. Since no heating is necessary, these sources can be much more efficient and reliable if emission can be achieved at a sufficiently low potential, providing marked improvement over current technologies [1, 2, 4].

Recently, the unique properties of conductive, high aspect ratio nanomaterials have been utilized to improve FE performance. One nanomaterial of interest is the CNT which has ideal properties for FE, including very high electrical conductivity, high temperature stability, chemical inertness, and a nanoscale geometry [5-7]. The first demonstration of the remarkable FE properties of CNTs was reported in 1994 [8], and thousands of papers have been published ever since [9]. Single CNT emitters are able to field emit over a very large current range and have a large maximum current of 0.2 mA for a single CNT [10-12].

Some work has explored an internally gated CNT field emitter using a Spindt cathode-based design by separating a conductive substrate and gate electrode with a dielectric layer [6, 13-15]. Even though this design has a lower emitter density, it is offset by higher field enhancement and less screening of the electrostatically isolated emission sites. Even though CNT FE in this design is well studied, electrical shorting of the gate and non-scalable techniques have prevented the production of a commercializable internally gated CNT electron source.

Realization of a Spindt-type CNT electron source could enable application in any technology which would benefit from low-power, light weight electron sources. These specifications are due to the compact design and relatively low total emission current abilities for CNT electron sources. Ideal applications include spacecraft electric propulsion, flat panel displays, and electrodynamic space tethers.

CHAPTER 2

BACKGROUND

2.1 Field Emission

This section will give an introduction to the background and theory of field emission. The mechanisms and types of electron emission will be introduced, followed by field emission history and the basic mechanism of field emission. From this, the idea of manipulating the potential barrier of a material during field emission is described. Finally, the work of Fowler and Nordheim are presented and their equation is analyzed.

2.1.1 Introduction to Electron Emission

Electron emission can be defined as the liberation of free electrons from the surface of a condensed phase into another phase, normally vacuum [3]. Electron sources, which elicit electron emission in a variety of ways, have a diverse set of applications ranging from high intensity electron guns for microscopy and thin film evaporation, X-ray sources, cathode ray tubes for television displays, vacuum electronics, spacecraft propulsion, and atomic excitation in lighting. Electron emission for lighting can act as a primary lighting mechanism such as in discharge lamps or fluorescent lamps, or even as a consequence of the lighting as in incandescent lamps. Electron emission is a widely used phenomenon that is utilized in a large variety of fields.

A material's properties affect the ability and type of electron emission that can occur, and include melting temperature, reactivity, geometry, electronic structure and

work function, φ, which is the minimum amount of energy needed to remove an electron from an atom or molecule. In a solid-state analog, φ can be defined as the energy difference between the highest filled energy state, or Fermi level (μ), and a field free vacuum near the surface, which generally ranges from 2-6 eV for metals [3]. The lower the work function of a material, the easier it will be for it to emit electrons. The type of energy applied to a material to overcome φ can determine the type of electron emission that will occur, given the appropriate material properties. The applied energy can come in the form of electromagnetic radiation, heating, or electrostatic fields, and cause photoemission, thermionic emission, or field emission, respectively [1-3, 16].

Photoemission occurs as a consequence of the photoelectric effect. When a material is irradiated with electromagnetic radiation with a frequency, v, the energy of that radiation is hv, where h is Planck's constant. If that associated energy is greater than the work function ($hv > \varphi$) and if an electron absorbs a photon of the radiation, then the electron is emitted from the material at a characteristic energy ($hv - \varphi$). Thus, the energy of emitted electrons does not depend on the radiation intensity, but only on v. The minimum v needed for emission is called the threshold frequency, and normally lies in the visible or ultraviolet wavelengths. This phenomenon is not within the scope of this work, although the effect has useful applications for spectroscopy and photomultipliers.

During thermionic emission, the potential barrier is overcome by supplying sufficient thermal energy for electrons to surmount the potential barrier φ. Very high temperatures (>2,000 °C) are typically needed to supply the necessary energy for emission, thus materials that will not melt, degrade, or react with the environment at these temperatures are needed. Normally, filaments made of refractory metals, such as

tungsten or molybdenum, are used as thermionic sources. In a crude analogy, electrons are essentially “boiled off” from the surface of the material during thermionic emission. Thermionic sources are by far the most common electron source used, mainly because their emission is robust and relatively easy to achieve [1, 17, 18].

In contrast to thermionic emission, field electron emission (FE), which is also known as Fowler-Nordheim or cold cathode emission, does not require thermal activation of the electrons. FE is achieved at room temperatures by thinning and lowering the potential barrier at the surface of a material with an electric field until there is a significant probability of electrons tunneling through the barrier. FE normally requires electric fields on the order of $10–10^2$ V/μm, which normally translates to very large macroscopic potentials. However, since FE is dependent on electric fields, the geometry of the emission device and material used is very influential [1-3].

Electron Emission Metrics

All of the electron source applications have different specifications based on the needs of a device. These specifications include current output, current density, emission stability, and lifetime. The current output is the amount of current in the form of electrons released by the source. Many devices often have a minimum output needed for operation. For example, a 200-W Hall effect thruster for satellite propulsion requires 1 A of emission current.

Current density is defined as the current output per unit area of emitter device. The area should normally be the total area footprint of the emission components, but is sometimes given as an estimation of the area of the emission sites when emission points

are being studied and compared. Consequently, the current density based on emission site area will be an inflated value.

Emission stability measures how emission changes over time due to degradation or changes in the emitter structure, and is determined by measuring the fluctuation of output current from a constant input. Finally, lifetime measures the length of time a material can sustain a certain emission current and is often measured by maintaining a constant emission current over time until degradation or failure. These metrics help show how different types of emitters are better suited for certain applications.

An indicator of efficiency for FE is given by two metrics which specify the electric field required for specific current densities. The turn-on field (E_{to}) and threshold field (E_{th}) are standards for a given current density and give a way to compare the performance of different electron sources. These standards arose from the electronic display industry, where the current density for E_{to} corresponds to the density needed to turn on one pixel and E_{th} corresponds to the density needed to saturate one pixel. Although they are not universally accepted, they are normally defined, and will be defined for this work, as 10 μA/cm^2 for E_{to} and 10 mA/cm^2 for E_{th}.

2.1.2 Introduction to Field Emission

In 1897 FE was first observed by Wood through the "fireworks" in his discharge tube [19]. Although he confirmed the emission of electrons, it was not fully realized until Schottky's experimentation in the 1920s that showed that the emission occurred under large electric fields and was not related to thermionic emission [5, 20]. Following Schottky's theory, in 1928 Fowler and Nordheim used wave mechanics and

approximations for the description of the potential field on the surface of a flat metal to model the emission current due to FE [1, 21]. This model is still used for a large variety of materials today, and has played a central role in the characterization of electron emission over the history of FE science, even for new materials being developed today such as emitter arrays, carbon thin films, and carbon nanotubes [1].

FE was widely used as a powerful technique in surface physics with the development of FE microscopy in the 1940s. This application developed into traditional electron microscopy for high-end electron microscopes that take advantage of the low energy dispersion and high brightness of FE sources to achieve high resolution [5]. The next relevant development was the invention of the Spindt FE cathode in 1968 [15], which incorporated arrays of emission tips with an internal gate electrode using silicon microfabrication techniques. This development opened the door for applications in "vacuum microelectronics" such as flat panel displays and microwave amplifiers [5, 22].

FE is fundamentally based on the tunneling of electrons through a potential barrier, a quantum mechanical phenomenon. Fortunately, FE can be well understood using mostly classical theories without losing understanding of the science. The following discussion of band theory and other specific concepts give a detailed description of the processes involved in FE [3].

For materials undergoing FE, Fermi-Dirac statistics are used to describe the energy states of the electrons, which are assumed to be indistinguishable particles. The electrons follow the Pauli Exclusion Principle, requiring that only two electrons (spin +½ and -½) can occupy each translational state. The distribution dictates that at zero Kelvin all electrons will have an energy below the Fermi level, μ:

$$f(E) = \frac{1}{e^{\frac{(E-\mu)}{kT}} + 1} \tag{1}$$

where *f(E)* is the probability of an electron having energy *E*, *k* is Boltzmann's constant, *T* is temperature, and *kT* represents the thermal energy [16].

Band theory uses Fermi-Dirac statistics to describe the electrical properties of materials. When atoms are closely packed together in a crystal, the discrete energies of valence electrons in the atoms interact with each other but must have slightly different energies, following the Pauli Exclusion Principle. As the number of atoms increases towards Avogadro's number, the distinct energy levels become virtually indistinguishable and can be estimated as energy bands. A conductor has energy levels available to its electrons, either in the form of a partially filled valence band or an overlap of the conduction and valence bands [16]. For this discussion of FE, one only needs to consider one partially filled conduction band and treat it as it corresponds to electrons contained in a rectangular potential well [3].

Fermi-Dirac statistics can be used to describe the mechanism of thermionic emission. At room temperatures, the thermal energy available, *kT*, is only about 0.026 eV, which is much smaller than the Fermi level for the electrons (typically several eV). This small amount of thermal energy has little effect on the electron distribution, resulting in almost no electrons with energy greater than μ. In order for thermionic emission to occur, there must be enough thermal energy present to have a significant number of electrons with energy greater than the Fermi level plus the work function of the material. Thus, thermionic emission needs very high temperatures to achieve electron

emission. High melting temperature metals have a work function of 4-5 eV, which requires temperatures in excess of 1,300 °C in order to have a nonzero distribution of electrons with energy greater than the work function [3]. For FE, the small effect of temperature on the energy distribution explains why the phenomenon is virtually temperature independent and it is often assumed that all electrons have energies less than or equal to the Fermi level.

The fundamental difference between thermionic and FE is how the electrons escape the potential barrier at the surface of the material. Thermionic emission provides enough thermal energy so that there is a significant population of electrons with energy greater than the work function, so that they pass *over* the barrier. In contrast, FE thins the potential barrier at the surface of the material so drastically that the electrons which are around the Fermi level are able to escape *through* the potential barrier. Figure 1 graphically shows this process for the two types of emission. Following the Fermi-Dirac distribution, electron energies are shown on the y-axis and the distribution function from Equation 1 is on the left side of the x-axis (shaded). The horizontal line to the right of the shaded region represents the surface of a material and the region to the right represents distance (x-axis) and potential field, V(x). Figure 1(a) describes electron emission via thermionic emission where there are elevated temperatures, and Schottky emission where there are elevated temperatures and electric fields. The potential barrier for thermionic emission is square because there is no electric field present, and there is a distribution of electrons shown with energy slightly greater than the work function due to heating. Figure 1(b) describes FE where the potential barrier is now triangular due to an applied field, and electrons around the Fermi level are able to tunnel through the potential barrier.

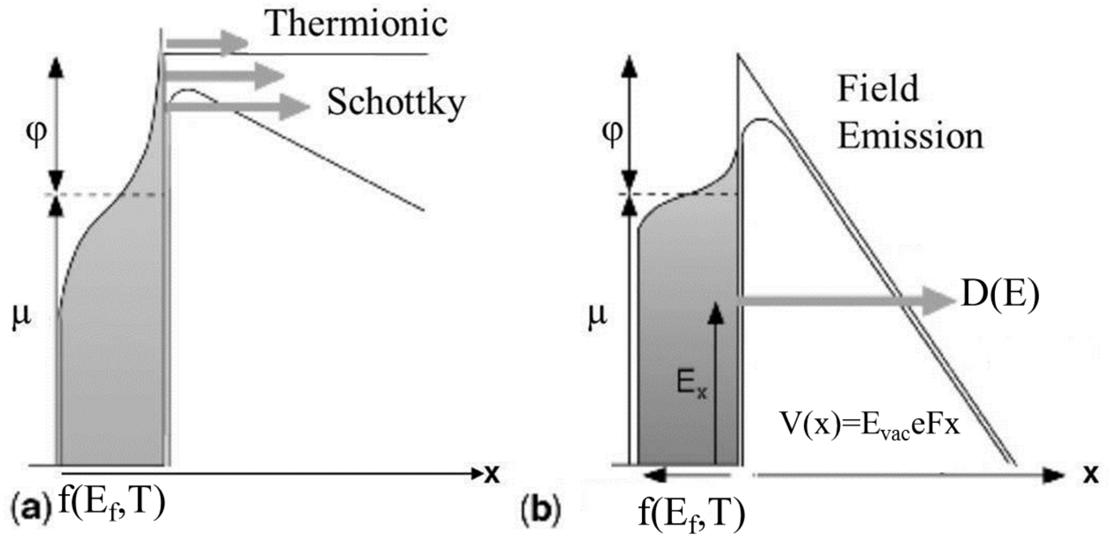


Figure 1: Processes which control emission of electrons. (a) Thermionic emission at high temperature and low field, (b) field emission at low temperature and high field [5].

The process of electrons transmitting through the potential barrier during FE is called tunneling, which is a purely quantum mechanical process with no classical analog. A cognitive way to approach this phenomenon is to consider the wave-particle duality of electrons. In this manner, an electron can simultaneously be considered to be 1) a wave with wavelength λ, which corresponds to its quantum mechanical wavefunction and 2) a particle with position x. The wavefunction corresponds to the probability of finding the electron at any point in space. Momentum p can be determined from the wavelength using the equation $p=h/\lambda$ where h is Planck's constant. The Heisenberg Uncertainty Principle states that there is an absolute minimum value for the product of the uncertainties of any two related quantities, such as a measured position (Δx) and momentum (Δp):

$$\Delta x \Delta p > \frac{\hbar}{2} \tag{2}$$

where $\hbar = h/2\pi$. This value is inherent in the nature of a particle and completely independent of measurements. Thus, if the momentum of a wave particle is precisely known, then the position of the particle is completely uncertain and could be anywhere along the wave function of the particle.

The concept of the Heisenberg Uncertainty Principle can be related to FE in order to understand how tunneling can occur. From the diagram in Figure 1(b), the barrier height is equal to $\varphi + \mu - E_x$, where E_x is the kinetic energy of electrons. If one considers electrons near the Fermi level, then the barrier height is approximately φ. From the relationship between kinetic energy ($\frac{1}{2}mv^2$) and momentum (mv), the pertinent Δp can be expressed as $(2m\varphi)^{1/2}$. After substituting this Δp into Equation 2, the corresponding uncertainty of the position is

$$\Delta x \approx \frac{\hbar}{2\sqrt{2m\varphi}} \tag{3}$$

Since an electric field is applied during FE, the potential barrier will not be rectangular but rather triangular, and will have an approximate width of φ/Fe, where F is the electric field and e is the elementary charge. If the potential barrier width is on the order of the uncertainty in position in Equation 3 due to the applied field, then it is possible to have an electron on either side of the barrier. This possibility of an electron just existing on the

other side of the potential barrier is called *tunneling*. When substituting the approximate potential width into Equation 3, this requirement can be expressed as

$$\frac{\varphi}{Fe} \approx \frac{\hbar}{2\sqrt{2m\varphi}} \tag{4}$$

or

$$\frac{2\varphi^{\frac{3}{2}}}{Fe}\sqrt{\frac{2m}{\hbar^2}} \approx 1 \tag{5}$$

A non-zero value of the wave function past the potential barrier represents the finite probability of an electron tunneling and escaping the material [3]. Although this is just a rough estimate for tunneling, Equation 4 quantitatively shows how tunneling can occur and can be shown to be an approximate requirement for the minimum electric field needed for FE [3].

Another necessary concept for an understanding of FE involves using the method of image charges, which is used to solve for the interaction of an electric field on the surface of a material. Assuming there is an image charge greatly simplifies this calculation and the solution shows there is a reduction of the potential barrier near the surface of a material. This reduction in the potential effectively decreases the work function of the material and causes electron emission to be greater than if a triangular

potential is assumed. For a surface under the influence of an electric field, the surface potential is a triangular barrier as seen in Figure 1(b) [3]:

$$V = \mu + \varphi - Fex \tag{6}$$

An image term, V_{im} can be added to the potential equation to account for the image charge where

$$V_{im} = \frac{-e^2}{4x} \approx \frac{3.6}{x} \tag{7}$$

where e is the elementary charge and the approximation of V_{im} is in volts and angstroms [3]. The curved potential barrier showing the image charge correction is shown below the triangular barrier in Figure 1(b). The image charge correction has significant effects on models that determine the emission current from a surface and is widely used today.

2.1.3 The Fowler-Nordheim Equation

In 1928 Fowler and Nordheim developed a model to describe the electron emission current obtained when a large electric field is applied to metals. They used quantum mechanics and various assumptions to determine a tunneling probability of electrons. These assumptions are:

1. The emitter is an atomically smooth and clean metal surface.

2. The metal is a free electron gas and can be described by band theory with electrons obeying Fermi-Dirac statistics.

3. Emission occurs at 0 K and the work function is uniform and independent of applied field. This assumption requires that all electrons have energies at or below the Fermi level and the barrier is constant.

4. The electron tunneling probability can be described by the Wentzel-Kramers-Brillouis (WKB) approximation, detailed below [2, 21].

These assumptions allowed Fowler and Nordheim to provide a consistent and informative description of FE, although it was not highly accurate due to its assumptions. However, the assumption of 0 K requiring energies at or below the Fermi level does not have a large effect on accuracy since electron distribution doesn't significantly depend on temperature. At temperatures above 0 K some electrons will have energies above the Fermi level, hence an increase in emission is expected, but calculations on the increased emission show that at room temperatures only a 2% increase in emission occurs and the effect remains insignificant for temperatures less than 1,000 K [4, 23].

In order to derive the FE current from a surface, an expression is needed for the probability that electrons will tunnel through the potential barrier. This transmission probability, D(E) uses the electron distribution from Fermi-Dirac statistics and is derived by solving the Schrödinger equation under these conditions. There is an analytical solution for the transmission probability using a triangular potential. As mentioned in

Section 2.1.2, the triangular potential does not accurately describe the surface potential due to the image charge, thus a more complex approach is needed. The WKB approximation gives an expression for the transmission probability of electrons through a potential barrier of arbitrary shape.

Fowler and Nordheim were the first to use the WKB approximation to take account of the image charge [3]. With a more accurate transmission probability for tunneling using this approximation, the emission current can be calculated by multiplying the transmission probability by the arrival rate of electrons and integrating over energies from zero to the Fermi level. A simplified version of the emitted current density, known as the Fowler-Nordheim (F-N) equation, is

$$J = \frac{aF^2}{t^2(y)\varphi} \exp\left(\frac{-b\varphi^{3/2}v(y)}{F}\right) \tag{8}$$

where current density, J is in V/cm^2, F is the electric field at the site of emission, φ is the work function, a and b are constants equal to 1.54 x 10^{-6} AV^{-2}eV and 6.83 x 10^7 eV$^{-3/2}$Vcm^{-1}, respectively. It is important to note here that F is the *localized* electric field at the emission site, which may not be the same as the macroscopic electric field.

The functions $v(y)$ and $t(y)$ arise from using the image charge correction in the WKB approximation. They are related to elliptical functions where y corresponds to a decrease in the work function due to the image charge. Tabulations of the functions are available [24] and can be approximated in most cases by 1.1 and 0.96 for $t^2(y)$ and $v(y)$, respectively. Ordinarily the F-N equation is approximated by setting these functions

equal to unity, even though this approximation on *v(y)* can cause large deviations in *J*. The large deviations arise from the fact that although *v(y)* ≈ 1, its multiplier in the exponential of the F-N equation is very large so that even small deviations of *v(y)* will cause large errors in *J*, especially at large fields and temperatures [25]. Regardless of these limitations, the F-N equation is widely used for validating electron emission data as being truly FE as opposed to some other phenomenon.

Since the physical quantity that is measured in FE experiments is current, the F-N equation is often expressed in terms of emission current, *I*, simply by multiplying by an approximation of the emission area, *A* (*J=I/A*). Another common modification of the equation gives a more physical meaning to the electric field at the emission site, *F*, since a direct measurement of the electrical field at a surface is often impossible, especially if the surface is non-planar. Assuming a parallel plate configuration, so that there is no curvature at the emission site, the field at the emission site is

$$F = \frac{V}{d} \tag{9}$$

where *V* is the applied voltage, *d* is the separation distance between the plates, and the localized field, *F*, is the same as the macroscopic field. The F-N equation predicts a turn-on field of ~1,000 V/μm for a parallel plate configuration of a clean tungsten surface [4]. This field is quite enormous: for a separation distance of 500 μm, an applied voltage of 500 kV would be needed. This requirement would be highly impractical for many FE devices if this was the macroscopic voltage needed, but it can be significantly reduced by

changing the emitter geometry. Having curvature on the surface of an emission point effectively enhances the macroscopic field because the gradient of the potential field lines increase with a decrease in the radius of curvature. That is, the local electric field on a sharply curved surface is much greater than the applied macroscopic electric field. This effect is what enables FE to be a viable electron emission technique, especially for the low power and lightweight devices contemplated in this work.

The increase in the local electric field due to curvature of the surface can be expressed in Equation 9 by introducing a geometric field enhancement factor, β:

$$F = \frac{\beta V}{d} \tag{10}$$

Thus, the localized electric field, F, which cannot effectively be measured, can be represented by two easily measured parameters: voltage, V, and electrode spacing, d, along with an enhancement factor, β which depends solely on the geometry of the surface.

From Equation 10, it is evident that there are two ways to increase the localized electric field while maintaining the same voltage input. First, reducing the electrode spacing will increase the electric field, but this quickly reaches a practical limit in the 100's of μm for externally separated electrodes. This distance can be markedly reduced by integrating the two electrodes into the same substrate using thin film deposition. This method can achieve separation distances of less than 10 μm while ensuring no electrical shorting between the two contacts, enhancing the field 1-2 orders of magnitude over the

external electrode configuration. The geometric field enhancement factor β is the most important parameter for increasing the localized field and is able to increase it to values that make FE devices viable for commercial development. As the radius of curvature increases, say for sharp tipped nanomaterials, the localized field is further increased, up to several thousand times [9]. These large enhancements in F can cause a monumental decrease in the voltage needed for FE, and are further discussed in Section 2.3.2.

By including the approximations for $t^2(y)$ and $v(y)$, and the physical meaning of the localized electric field shown in Equation 10, the F-N equation can express the measured emission current in terms of other measurable and experimentally significant variables:

$$I = \frac{aA(\beta V)^2}{d^2 \varphi} \exp\left(\frac{-bd\varphi^{3/2}}{\beta V} \right) \tag{11}$$

This form of the F-N equation is often used with FE experiments where d, A, φ, and V are known and I is measured. Another useful form of this equation is achieved by dividing by V^2 and taking the natural log:

$$\ln\left(\frac{I}{V^2} \right) = \ln\left(\frac{aA\beta^2}{d^2 \varphi} \right) - \frac{bd\varphi^{3/2}}{\beta V} \tag{12}$$

Here, a plot of $ln(I/V^2)$ versus $1/V$ will give a linear plot, known as the Fowler-Nordheim plot. Comparison of the linearity of FE data in the F-N plot is often used as a way to

confirm FE is actually occurring. A significant deviation from linearity may suggest that another emission mechanism is occurring. Furthermore, since the slope, m, of this plot is

$$m = \frac{bd\varphi^{3/2}}{\beta} \tag{13}$$

β can easily be calculated from the slope of a linear fit of the plot. The electrode spacing and voltage are known, and normally the work function is at least approximately known so that the field enhancement can be estimated.

A Note on the Use of the F-N Equation

It is imperative to note that the basic F-N equations presented here have shortcomings and flaws. The simplifications and assumptions in the derivation of the model, along with its unintended use, are the foundation of these shortcomings. It is adequate to use the F-N equation, in addition to updated versions, to analyze experimental data, but most importantly, this equation *should not* be used to theoretically show potential FE performance, such as current density. The main reason for this restriction is that the F-N equation can grossly overestimate parameters: current density can be over-predicted on the order of 10^3 and even up to 10^9 if an area efficiency factor or the macroscopic device area is not used [26]. It should be noted, in this work the macroscopic device area, *not* the emission pit or CNT area, is used for all current density calculations.

The basic F-N equation is over referenced and over depended on in the literature for use as a theoretical model. Forbes has recently attempted to correct this misuse of the F-N equation [26]. Although the experienced scientist would understand the limitations of this equation, the danger of its overuse in the literature lies in the potential to mislead non-experts in the scientific community. For any theoretical FE work, it is highly suggested to use modern revisions of the F-N equation [23, 26, 27]. These revisions add a barrier form correction factor to correct for the poor modeling of an image barrier for small tip radii. A local pre-exponential correction factor accounts for several simplifications of the F-N equation, such as effects of temperature, from taking the summation over electron states, and from atomic wavefunctions [26]. These methods are important to the science, but are outside the scope of this work.

This section introduced electron emission, gave a summary of field emission theory and presented the work of Fowler and Nordheim. Considering all of the assumptions and simplifications used for the Fowler-Nordheim equation, it is not an entirely accurate model. Nonetheless, it remains a powerful experimental tool.

2.2 Carbon Nanotubes

Carbon nanotubes (CNT) are presented by first giving a brief history of new carbon allotropes, including carbon nanotubes. A summary of CNT structure and bonding and how this influences their electronic, mechanical, and thermal properties are presented. Next, the chemical vapor deposition synthesis method is described along with the theorized growth mechanism. This leads to a summary of the FE properties of CNTs. The vertical alignment and geometry of CNTs provide an opportunity for great FE

performance. The common FE designs for CNT are given, including the Spindt cathode. Finally, possible failure mechanisms during CNT FE are presented.

2.2.1 History

Carbon has seen much scientific attention in the past 25 years with the identification of two new stable allotropes and a realization of their properties. The well-known allotropes of carbon (diamond, graphite, and amorphous carbon) were joined by fullerenes in 1985 and CNTs in 1991 (Figure 2). More recently, individual sheets of graphite, known as graphene, have seen an explosion of scientific interest in the past decade due to its successful synthesis, unique geometry, and fascinating electronic properties.

Fullerenes were discovered in 1985 by Smalley, et al. on accident by arc discharge while studying carbon production in stars [28]. Whereas graphite consists of one atom thick sheets of carbon atoms arranged in hexagons with trigonal bonds, fullerenes consists of a rolled up ball of graphene with pentagons of carbon atoms introduced. The pentagonal rings induce positive curvature in the sheet and enable closure of the fullerene. The first fullerene discovered was C_{60} and consisted of 60 carbon atoms, but other larger fullerenes were soon discovered which have an elongated form of C_{60} due to the introduction of rings of 10 carbon atoms to the center of the structure (see C_{70} Figure 2(e)).

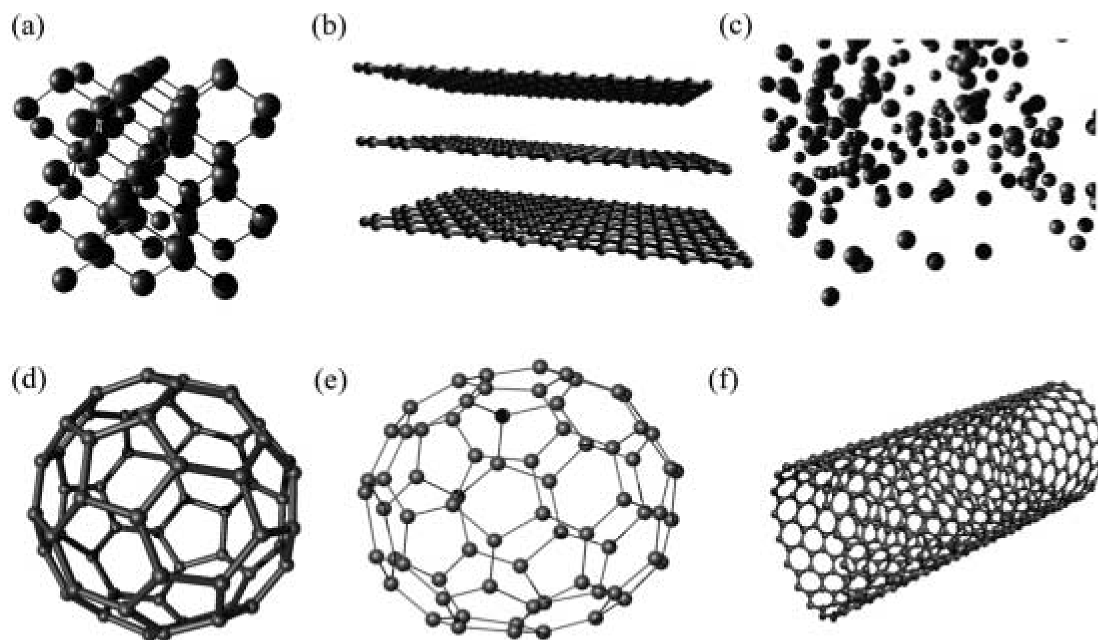


Figure 2: Allotropes of carbon: a) diamond, b) graphite or sheets of graphene, c) amorphous carbon, d) C_{60} fullerene e) C_{70} fullerene and f) a carbon nanotube [9]

The structure of CNTs can be visualized as sheets of graphene rolled into tubes, with capped ends of half fullerene molecules. CNTs can be single walled (SWNT) when they contain just one tube of carbon, or multi-walled (MWNT) where concentric tubes of carbon are contained within one another. CNTs have a much longer and more interesting history than fullerenes. The first documented account of “carbon filaments” was in 1889 during the time of Thomas Edison when there was a search for small carbon filaments in incandescent light bulbs [29]. The actual nanoscale or crystalline structure of these carbon filaments is a mystery because the tools of the time were limited to optical microscopy. The observed filaments must have been at least a few microns in diameter in order to be observed in the microscope. However, the synthesis method involved the thermal decomposition of methane, and based on the details and methods described in the corresponding patent, it was possible that CNTs could have been synthesized [9, 29, 30].

The first documented case of transmission electron microscopy (TEM) evidence of the nanoscale and tubular structure of the "filamentous growth of carbon" was first published in 1952 by a Russian journal [31]. This work clearly documented images of hollow tubes of carbon with diameters of about 50 nm, meaning they were probably MWNTs (Figure 3(a)). Unfortunately, this publication did not disseminate through the scientific community, largely because of the nature of the Cold War and because the journal was in Russian [9, 32]. There were several other documented observations of the nanoscale carbon tubes over the next 40 years with little international scientific recognition. In all cases the carbon tubes were greater than 5 nm in diameter, indicating they were most likely MWNTs (Figure 3(b)) [33-35].

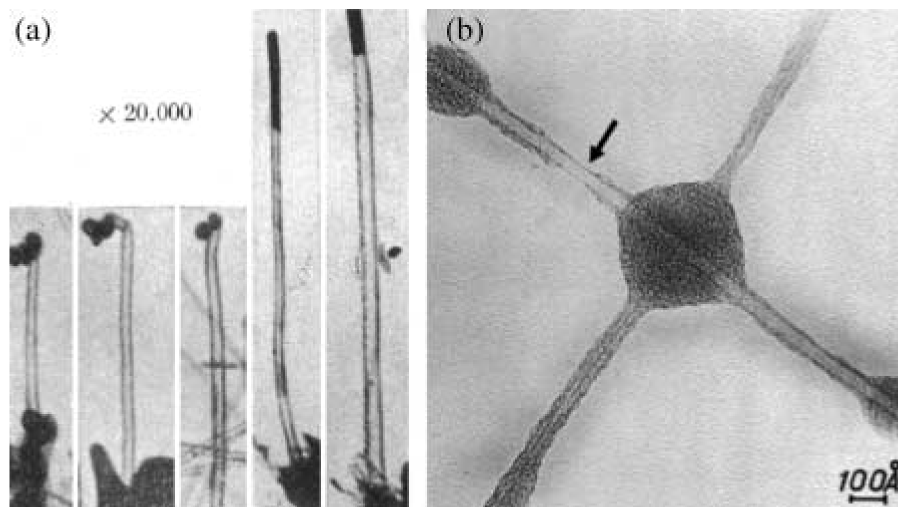


Figure 3: (a) First TEM evidence of possible MWNTs published in 1952 [31] and (b) later in 1976 [35].

The discovery of fullerenes in 1985 spurred a growing scientific interest in nanomaterials. Later, Iijima was studying the synthesis of fullerenes by the arc discharge

method when he noticed tubular graphitic structures in the product. Finally, in 1991 Iijima published TEM images which detailed the graphitic and hollow layered structure of MWNTs, which caused a global realization of the properties and possible applications for CNTs [36]. As a result, Iijima is attributed with the pioneering discovery of CNTs. Indeed, an explosion of theoretical and experimental work followed his publication. Single walled CNTs were discovered shortly after in 1993 using a similar method as Iijima with the addition of transition metal catalysts [37, 38]. CNTs quickly overtook fullerenes as the hottest research topic soon after 1991 as thousands of articles are published every year on CNTs in every field of science and engineering. More recently, publications of graphene have overtaken CNTs as a popular research topic.

2.2.2 Structure and Bonding

Elemental carbon is one of the most chemically versatile elements and can form a variety of organic compounds. Carbon has six electrons, two in the core 1s orbital and four valence electrons in the 2s and 2p orbitals. When bonding, the 2s electron(s) in carbon can easily be promoted to a 2p energy level causing hybridization of the orbitals. This hybridization can create four equivalent sp^3 hybrid orbitals for bonding, as in the case of diamond, to create tetrahedral bonds. Carbon atoms in diamond form four sigma (σ) bonds that are equally spaced from one another by 109.5°. For graphene, three equivalent sp^2 hybridized σ bonds are formed which make a hexagonal structure in a honeycomb shape. The fourth valence electron forms a weak out of plane π bond. The C-C sp^2 σ bond has a bond length of 0.14 nm and is considered the shortest and strongest single bond in nature [39]. The π bond in graphene forms the interlayer bonding in

graphite with a bond length of 0.34 nm. Graphite layers stack in an ABABA… fashion such that every other layer is in the same position, forming a 3-dimensional hexagonal structure [5].

The CNT structure can be thought of a seamlessly rolled up sheet of graphene that is capped by half fullerene molecules. CNTs can also be described as a derivation of a C_{60} fullerene molecule. Larger fullerenes can be formed where rings of 10 carbon atoms are added to the center of the C_{60} molecule, thus forming C_{70}. If *n* such rings of the 10 carbon atoms were added to C_{60}, then an elongated tube is formed consisting of a C_{60+10n} molecule producing a CNT (Figure 4). CNTs form similar bonds as graphene with sp^2 orbitals and one π out of plane orbital. Due to the curvature of the CNT, the sp^2 hybridized bonds mix with some sp^3 character to decrease the strain energy. This bonding in such a high aspect ratio geometry can cause the CNT to have unique properties, such as quantum confinement [10]. The C-C bond length increases as the radius of curvature decreases, and ranges from 0.141 nm for planar graphene to 0.144 nm for C_{60} and the smallest SWNTs [40].

CNTs can be categorized based on the number of walls they have. A SWNT consists of just one tube of carbon atoms with a diameter of 0.4-3 nm. The lower limit of 0.4 nm marks the theoretical and experimental limit achieved [41]. The upper limit occurs because of the tendency of large diameter SWNTs to collapse into a nano-ribbon [40]. SWNTs are the most difficult to synthesize but are extensively used in modeling and theoretical work due to their simplicity, size, and ability to act as 1-dimensional quantum wires. A MWNT consists of multiple layers of axially concentric SWNTs with an average wall spacing of 0.34 nm, the same as graphite [42, 43]. The wall spacing

slightly increases with a decrease in diameter due to increased wall curvature. They often exhibit a high degree of crystallinity due to a regular 0.34 nm spacing of the tube walls. The type and properties of individual walls are often independent [39].

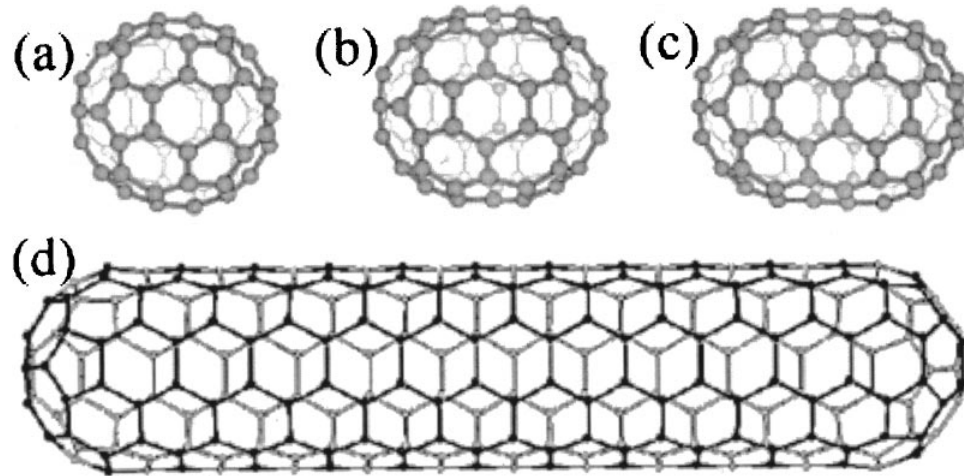


Figure 4: (a) C_{60}, (b) C_{70}, (c) C_{80}, and (d) C_{60+10n} fullerene structures [42]

Up until now, perfectly crystalline and defect free CNT structures have been assumed. However, during the synthesis process, especially when using chemical vapor deposition, a variety of defects can occur. The defects can be minimal, such as pentagons and heptagons in the graphitic walls of the CNT which induce negative and positive curvature in the CNT wall, respectively. In addition, pairs of pentagon-heptagon rings can occur that causes no change in curvature [44]. Extensive bonding defects can cause the formation of what are called carbon nanofibers, which have a broken graphitic structure and are not continuously tubular. Finally, due to the synthesis process, the incorporation of amorphous carbon and/or metallic catalyst particles can be incorporated into the CNT structure.

2.2.3 Properties

Due to the close relationship between CNT and graphite, it is no surprise that they generally show similar properties. Graphite exhibits anisotropic properties, where behavior along the carbon lattice is much different than between each sheet. Similarly, properties in the axial direction of a CNT are often much different than in the radial direction. This anisotropy mainly has to do with the different types of bonding along the graphite sheet versus between each sheet. The overlap of the carbon π orbitals above and below the hexagonal lattice often enhances properties. The high aspect ratio of CNTs also enhances the anisotropy of their properties. A CNT diameter is in the tens of nanometers, while the length can be millimeters or even centimeters in length [45, 46]. These dimensions give an aspect ratio up to $\sim 10^7$, meaning that quite literally CNTs can be both macroscopic and nanoscopic at the same time. This extraordinarily high aspect ratio allows the CNT to exhibit some one-dimensional properties over a macroscopic scale.

Carbon Nanotube Chirality

Before the properties of CNTs are discussed, it would be helpful to have a method to describe every type of CNT. Aside from multi- and single walled, a second way to classify CNTs is based on the orientation the tube is wrapped relative to a graphene sheet. This method of categorizing, called helicity or chirality, was first proposed by Hamada, et al. in 1992 and is very useful because it uniquely identifies each type of CNT and can be related to their properties [47]. The chirality describes the helical arrangement of carbon atoms wrapping around a CNT by referencing the lattice points of graphene.

The 2-D hexagonal lattice of graphene has a basis of two, meaning that each hexagonal lattice point represents two carbon atoms. Thus, the lattice unit vectors, a_1 and a_2, connect every other carbon atom and a lattice consisting of the unit vectors would form the 2-D hexagonal Bravais lattice (Figure 5(a)). If a CNT was split along the axial direction and laid flat so that it resembled a graphene sheet, a chiral vector, C_h, is defined by connecting two equivalent atoms which now lie on the edges of the sheet (Figure 5). Thus, the chiral vector's length is the circumference of the CNT and, in reference to Figure 5, can be defined as

$$\overrightarrow{OA} = \overrightarrow{C_h} = n\overrightarrow{a_1} + m\overrightarrow{a_2} \tag{14}$$

where n and m are integers. Since $|C_h|$ represents the circumference of the CNT, the diameter is

$$d = \frac{\overrightarrow{|C_h|}}{\pi} = \frac{a\sqrt{n^2 + m^2 + nm}}{\pi} \tag{15}$$

where a is ~0.14 nm, the C-C bond length.

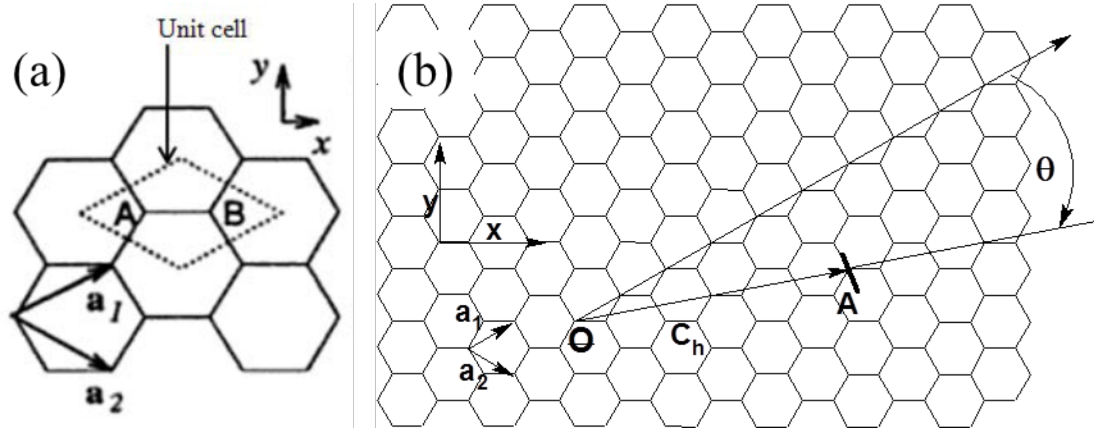


Figure 5: (a) The Bravais lattice vectors, a_1 and a_2, and the unit cell of graphene [48]. (b) Unit vectors, chiral vector, C_h and chiral angle θ of a (4,2) CNT relative to graphene [49].

The chirality of a CNT can be defined by determining the number of iterations of the unit vectors needed to traverse C_h, and is denoted *(n, m)* from Equation 14. A chiral angle, θ is defined as the angle between C_h and the unit vector a_1. Due to the high degree of symmetry in the hexagonal lattice, all of the unique chiralities can be represented for chiral angles ranging from 0-30°, or a 1/12th wedge of the lattice (Figure 6) [50]. A translation vector can be defined on the graphene sheet as normal to C_h and running from the origin to the next lattice point (in the axial direction of the would-be CNT). A combination of the translation and chiral vectors gives the unit cell of the CNT. The chirality notation is a useful way to reference any specific type of CNT [49]. C_h, the translation vector, θ, and the diameter can all be determined from the chiral notation *(n, m)* [40].

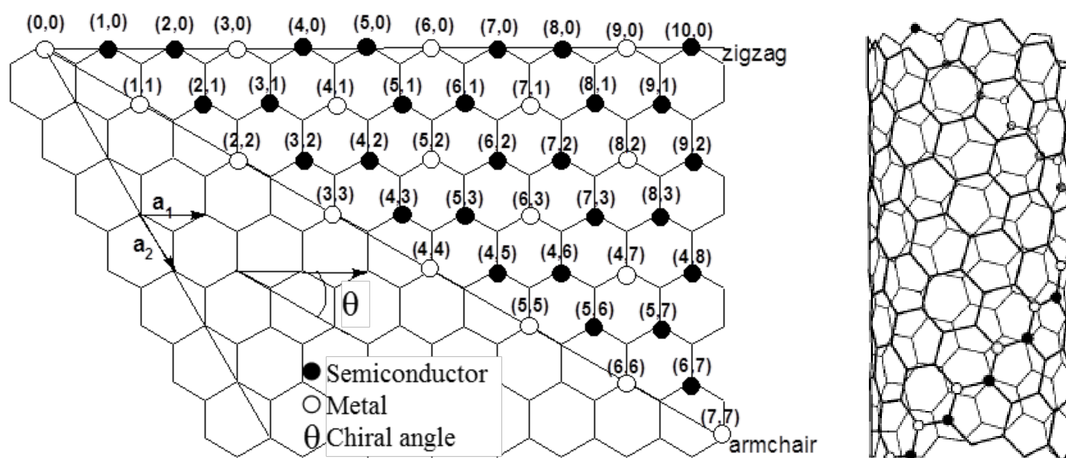


Figure 6: (Left) The unique chiral indices of CNTs showing the metallic and semiconducting indices with zigzag and armchair types noted [49]. (right) Schematic of chiral CNT showing screw axis [32].

The various types of chirality can be split into several categories. Achiral CNTs (i.e. those that are not chiral) are superimposable on their mirror images, meaning that they have a plane of symmetry [51]. One type of this high-symmetry achiral CNT is called “armchair” and occurs when C_h is along the graphene plane that is normal to the five-fold rotation axis (Figure 6). Armchair CNTs have a chiral angle of 30° and occur when n=m [49, 51]. They are called armchair due to the armchair shape of the carbon atoms along C_h. The second type of achiral CNT is called “zigzag” and occurs when C_h is along the graphene plane that is normal to the three-fold rotation axis (Figure 6). They have a chiral angle of 0°, occur for notation *(n, 0)* and always behave metallically [49]. They are called zigzag because of the shape of carbon atoms along C_h. Chiral CNTs are those that have a non-superimposable mirror image or do not have a plane of symmetry. There are a large number of chiral CNTs and they have a chiral angle ranging from 0-30°.

They all contain a screw axis along the CNT axial direction, which forms a helical spiral of hexagons along the tube wall, an example of which is shown in Figure 6 [51].

Electronic Properties

One of the most incredible characteristics of CNTs is that they can be metallic or semiconducting, depending on their chiral structure. This electronic property is another way to categorize CNTs. The conductivity of a CNT can be understood by modifying the band gap structure of graphene. Electronically, graphene is highly anisotropic, giving very high mobility along the hexagonal planes due to overlap of the carbon π orbitals. The resistivity of a perfect graphene sheet at room temperature is ~0.4 $\mu\Omega$m, whereas the mobility between hexagonal planes is relatively low [44]. In the band gap structure of graphene, the first Brillouin zone is a hexagon where the points of the hexagon are called the K-points (white hexagon in Figure 7). The electronic states of the conduction and valence band can be modeled, where the bands meet at the Fermi level, creating a Fermi point. Modeling of graphene shows that the allowed electronic states of the valence (π) and conduction (π^*) bands of graphene meet at the K-points of the hexagon, meaning that the band gap is zero and graphene is metallic (Figure 7) [44].

A modified electronic structure for CNTs can be adapted from that of graphene. The differentiating factor of CNTs from graphene that enhances their anisotropy is their enormous aspect ratio. The macroscopic axial length versus the atomic scale circumference causes very few available electronic states along the circumference, but a large number of available states in the axial direction. Models of graphene can be adapted to predict the band structure of CNTs by modifying the number of available states in the

radial direction [44]. The allowed electronic states are compressed into parallel lines within the graphene Brillouin zone (bottom of Figure 7) [44]. The first electronic structure calculations on CNTs were carried out by Mintmire, et al. and were quickly followed by others [49, 52].

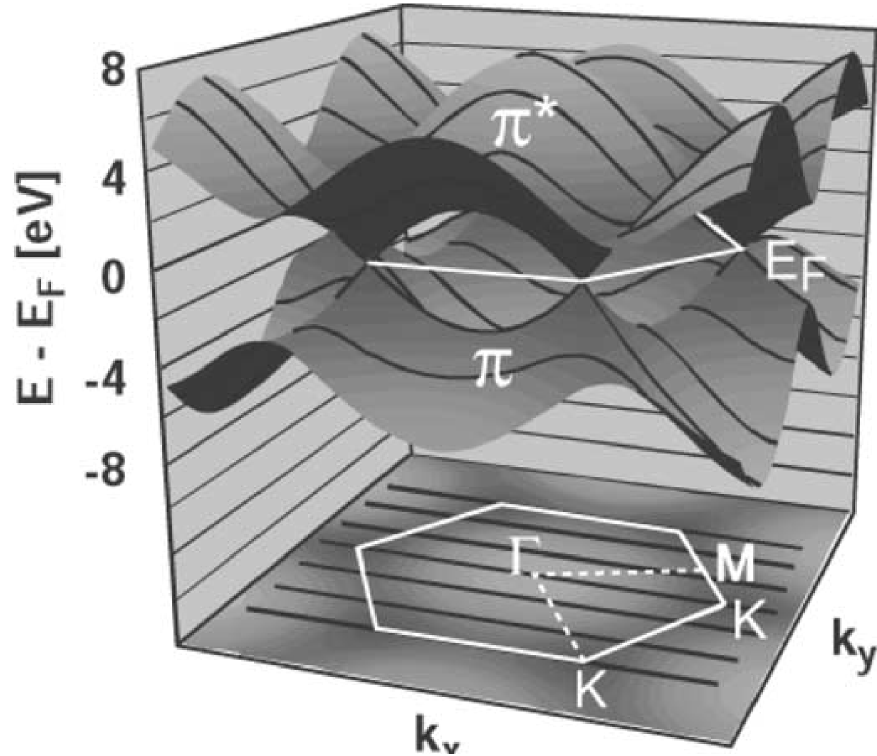


Figure 7: Top: Valence (π) and conduction (π^*) band structure of graphene showing the bands meeting at the K-points lying at the Fermi energy (E_F). Bottom: The first Brillouin zone of graphene in white and the allowed states of a (3, 3) armchair CNT in black. Since the states pass through the K-points, the CNT is metallic [53].

Armchair CNTs have a symmetry such that the orientation of the Brillouin zone will always have an allowed electronic state intersecting a K-point, very similar to graphene. Thus, theory predicts that all armchair CNTs exhibit metallic conduction properties (Figure 7, Figure 8(a)) [44]. Zigzag CNTs still have the symmetry to

specifically orient the Brillouin zone with the allowed electronic states, but modeling predicts a variety of allowed electronic states, depending on the specific structure. As seen in Figure 8(a) and (b), some structures have states that still intersect the K-points, thus predicting metallic behavior, but others do not intersect the K-points. Zigzag CNTs are metallic when n is divisible by 3, and semiconducting otherwise [44]. The electronic structure of chiral CNTs varies on the specific chirality of the tube and are metallic only when

$$n - m = 3q \tag{16}$$

where q is an integer (Figure 8 (d)) [49]. Overall, since one in three zigzag and chiral CNTs are metallic, about one third of all CNTs are metallic and the rest are semiconducting [44].

The previous modifications for the band structures of CNTs considered the limited number of available electronic states in the radial direction due to the high aspect ratio of CNTs. However, this prediction does not always match experimental observations [54]. This disparity can be attributed to the fact that the modeling does not account for curvature of CNTs. In fact, the same band structures would have been produced for flat, high aspect ratio strips of graphene [55]. The curvature adds a hybridization of sp^3 character in the CNT orbitals, thus affecting the band structure. Curvature has no effect on armchair CNTs, but can have significant effects on metallic zigzag or chiral CNTs. The orbital hybridization causes a slight shift in the Fermi points away from the allowed electronic states such that they no longer intersect. Since the

allowed electronic states do not meet at the K-points, the CNT will be a semiconductor with a very small, but finite band gap. The band gap in these semiconducting CNTs is only around a few meV and depends on the curvature and thus the diameter of the CNT. The band gap is proportional to $1/d^2$ such that for CNTs with a diameter greater than 20 nm, the band gap is insignificant. Therefore, this semiconducting band gap due to curvature mostly affects SWNTs, and even then only at lower temperatures [44].

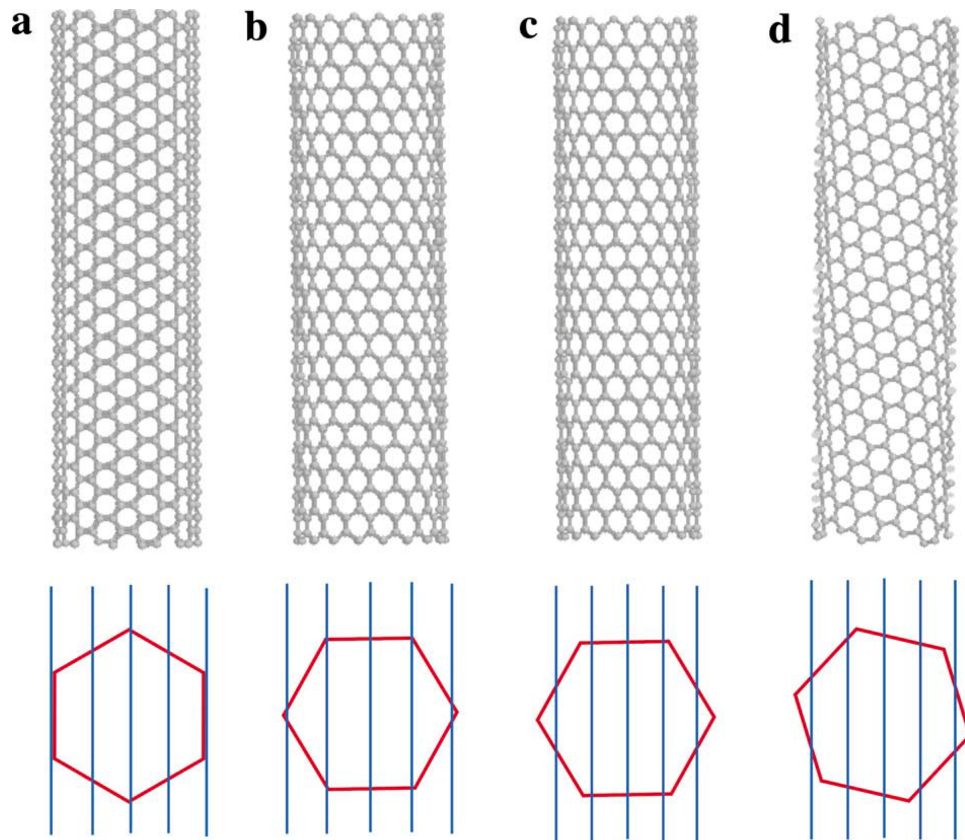


Figure 8: Schematic structures of CNTs with the bottom showing the Brillouin zone of graphene (red) and the allowed electronic states of the CNT. a) A (10, 10) metallic armchair CNT, b) a (12, 0) metallic zigzag CNT, a (14, 0) semiconducting zigzag CNT, and d) a (7, 16) semiconducting chiral CNT [43].

Semiconducting CNTs with a larger band gap (i.e. those predicted as semiconducting without considering curvature) have a band gap that is determined by the smallest separation of a K-point from an allowed electronic state. This band gap, E_g, is still inversely proportional to diameter, d, and it can still be insignificant for larger diameter CNTs [49]. The band gap can be defined by

$$E_g = \frac{4hv_F}{\pi d} \tag{17}$$

where v_F is the Fermi velocity, which is the velocity of electrons associated with the Fermi energy. The band gap can range from 10 meV for near metallic to 1.5 eV for small diameter semiconducting CNTs [56].

Electron transport mechanisms in semiconducting CNTs are considered diffusive, but are not well understood, especially compared to metallic CNTs [44]. Although the band gap of a CNT is dependent on diameter, it is also very sensitive to the environment. Semiconducting CNTs have been shown to be natively p-doped due to adsorption of oxygen atoms and to be highly sensitive to other gases, impurities, or trapped charges [43]. Very small environmental changes can alter the conductivity of CNTs several orders of magnitude as the CNT changes from n-type, intrinsic, or p-type [43, 53]. Due to this high sensitivity, CNTs have promise in gas sensor applications where they can have much higher sensitivity than currently available.

Due to the anisotropic nature of CNTs, metallic tubes should act as one-dimensional quantum wires. Assuming ideal structure with no scattering, there will be no

increase in resistance with increase in length, instead of a constant increase with length seen in conventional conductors. An important aspect of this quantum conduction is that transport in ideal CNTs is ballistic in nature, meaning there is no scattering or resistance to electron flow through the CNT, and thus no energy is dissipated in the CNT [44].

Theoretically, CNTs can conduct very large currents without significant heating. Work by de Heer, et al. showed that a single CNT could conduct at relatively high voltages (6V) which, if the CNT was a classical conductor, would correspond to unrealistically high temperatures of up to 20,000 K from power dissipation. Thus, this work gives evidence of ballistic transport in CNTs, meaning that electrons can flow through CNTs with zero resistance due to scattering [57]. Due to the ballistic transport, CNTs can carry current densities up to 10^9 A/cm^2, compared to 10^6 A/cm^2 for copper [58]. In addition, CNTs do not suffer from any of the electromigration degradation issues that plague the lifetime of metal conductors. Due to these properties, CNTs are considered to be ideal for many different electronic applications. The ability for CNTs to be metallic or semiconducting with a range of band gaps *without* doping is a property that is unique to CNTs and is another cause of interest in electronic applications.

Up until now, most of the experimental and theoretical work mentioned has involved SWNTs, mainly due to the simplicity in modeling their properties. However, it is important to consider MWNTs because they are the most common and easiest to synthesize. It is much more difficult to determine the chirality and transport properties of MWNTs because of the proximity of each layer and the interactions between them. The circumference and chirality of each layer of a MWNT are related because the circumference of each layer increases by approximately $2\pi*0.34$ nm [42]. However, as

depicted in the curve for each circumference in Figure 9, the constraint on the circumference of the CNT doesn't necessarily determine the exact chirality. This relationship is especially true for the larger circumference in Figure 9, where the arc passes close to several (n, m) positions.

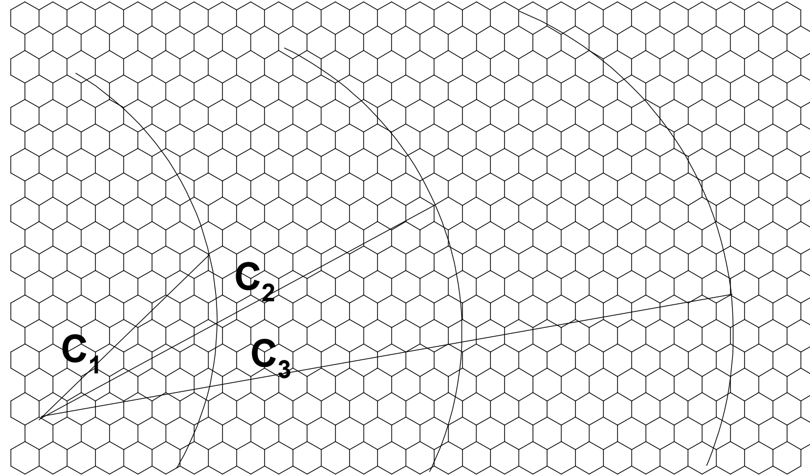


Figure 9: Successive CNT layers in a MWNT with 0.34 nm spacing showing the possibility of multiple chiral angles and (n, m) indexes along the arcs [42].

In theory, there could be as many chiral angles in a MWNT as there are walls. However, TEM diffraction experiments of MWNTs have shown that the number of chiral angles in the MWNT is much less than the number of walls, suggesting that there are groupings of walls with the same chiral angle. It is proposed that as the tube grows, slight deviations of the 0.34 nm interlayer separation occurs to keep the chiral angle constant until accumulated strain forces a change in chiral angle, thus producing groupings of walls with the same chirality [42].

Several different transport properties in MWNTs have been reported in the literature and hence there is some controversy over what actually occurs. Transport has

been shown to be ballistic-like in metallic SWNTs and diffusive-like in semiconducting SWNTs [59-63]. There is also some controversy on the effect of inner tubes on transport as well. Statistically, an outer metallic wall has only a 33% chance of being adjacent to another metallic tube. Since this is a relatively low probability, the inter-wall coupling is often considered weak and most MWNTs can be considered as decoupled layers of SWNTs. Since about one third of the walls are metallic, they are expected to dominate the electrical properties. In addition, the previously mentioned work by de Heer, et al. suggested ballistic conduction in MWNTs [57]. Thus, most MWNTs are considered to behave as conductors [44]. Experiments show that at low bias, most of the electron transport occurs in the outermost wall with some interaction of the inner tubes. This suggests that conduction could be dominated by the outer most wall [60]. Studies on the limit of electron transport in MWNTs show electrical breakdown in a series of sharp current steps instead of a continuous degradation as seen in metals [64]. These series of steps are attributed to the sequential failure of each wall of the tube, thus showing some robustness in their conduction. These unique electronic properties of MWNTs suggest they are favorable for electronic applications, and they will be utilized in this work.

Mechanical Properties

The unique mechanical properties of CNTs have attracted as much interest in CNT applications as their electronic properties. Their mechanical properties have been widely studied, both theoretically and experimentally, although obtaining experimental measurements can be increasingly difficult due to the nanoscale size of the CNT. The literature has established that CNTs are the stiffest and strongest fibers ever made,

achieving a Young's modulus and tensile strength several times that of steel. In addition, they have a low density of ~1.8 g/cm^3 for MWNTs compared to 7.7 g/cm^3 for steel, and exhibit a large fatigue strength. This unique combination of properties show that CNTs have great potential in lightweight structural applications [44]. It should be noted that the cited *per unit area* strength and stiffness of CNTs are extraordinary, especially when compared to steel, however this is not an entirely fair comparison because of the scale differences of these two materials. CNTs have outstanding properties at the nano scale, but steel cannot be made at the same scales. Similarly, CNTs cannot be synthesized on the macroscopic scale of steel beams, and the cited CNT mechanical properties are not sustained across the interface of adjacent CNTs in the axial and radial directions. Thus, a macroscopic CNT beam with comparable properties to steel cannot currently be made. Therefore, CNTs are most commonly incorporated into composites where their nanoscale properties can affect the macroscopic material, such as in [65].

Basic theoretical calculations on the stiffness of a SWNT can describe the nature of mechanical properties in CNTs. For example, assuming a SWNT with an inner diameter of 1 nm and a wall thickness of 0.34 nm, the outer diameter and cross-sectional area can be calculated to be 1.68 nm and 1.43 x 10^{-18} m^2. Applying a tensile load of 100 nN, and assuming a Young's modulus of graphene, 1,060 GPa, results in a stress of ~7 x 10^{10} N/m^2 and a strain of 6.6% [44]. These large values are partially due to the nanoscale geometry of the CNT and the extremely strong C-C bonding in the graphitic walls, as discussed in Section 2.2.2. If the same calculation is made for a larger CNT, say with a 10 nm inner diameter, then a stress of ~9 x 10^9 N/m^2 and a strain of 0.85% results. This large change in strain with a relatively small change in CNT diameter clearly

demonstrates that stiffness always tends to increases with diameter of the CNT. This relationship agrees with experimental measurements (mentioned below) and experimental observations, where TEM images of small diameter SWNTs tend to be very curly, while MWNTs tend to be relatively straight on the nano scale [44].

The above calculation used the Young's modulus of graphene, 1,060 GPa, which is only a basic approximation for CNTs. Many groups have studied the Young's modulus of CNTs using both theoretical and experimental methods. A review of theoretical calculations of CNTs show that a large range of Young's moduli have been calculated, ranging from 500-5,500 GPa [66]. This wide range of values is partially explained by authors using different values for the wall thickness of a SWNT. Generally, it is assumed that the wall thickness is that of the interlayer distance of graphene, 0.34 nm. However, for the studies that found a Young's modulus greater than 5,000 GPa, smaller wall thickness values are used which subsequently skewed other calculations [44]. The first qualitative TEM measurements on CNTs calculated the Young's Modulus by measuring thermal vibrations of free standing MWNTs over a range of temperatures. This method produced an average Young's modulus of 1,800 GPa with a fairly large error of ±900 GPa [67]. Later, AFM experiments measured the bending force as a function of displacement on CNTs with one end fixed [68]. This method produced a value of ~1,300 GPa. A variety of experimental methods and CNT types have produced a wide variety of values for Young's modulus. A generally accepted conservative value for SWNTs is 1,000 GPa, which is about five times that of steel [44].

The behavior of CNTs under tensile strain has also been extensively studied, theoretically and experimentally, although the same difficulties arise for experimental

work. Theoretical calculations show that the maximum tensile strain (i.e. elongation) of SWNTs *without damage* is almost 20% [69]. AFM measurements by applying stress to fixed SWNTs measured a tensile strength of 45 ± 7 GPa and a strain of 5.8%, which are much less than theory [70]. The tensile strength of MWNTs have been theoretically calculated to be up to 300 GPa and experimentally measured up to 150 GPa [40]. Measurements on the tensile strength of a MWNT mounted between two opposing AFM tips observed a failure mode known as "sword-in-sheath", where outer layers fracture while leaving inner walls intact. This method measured a tensile strength of the outer layers from 11-63 GPa [71]. A tensile strength of 63 GPa is extraordinary considering it is about 50 times that of steel [44]. These maximum reported values make CNTs the strongest and stiffest materials known to man [40].

Another extraordinary property of CNTs is their robustness and resistance to fracture. Broken CNTs are normally not observed, even after mechanical grinding or ultrasonication for TEM preparation [44]. Furthermore, CNTs can plastically deform to very large strains and will repeatedly return to an unstrained state, giving them great fatigue strength. Bent CNTs are often observed and strains up to 40% have been shown [72, 73]. When stressed over large angles, it is not uncommon to see regularly spaced buckles or a single buckle in CNTs (Figure 10) [74, 75]. When measuring the bending force versus displacement of a CNT with an AFM, Lieber, et al. noticed an abrupt change in the slope of the curve after about 10° [68]. This sudden change is attributed to buckling in the CNT. Incredibly, these buckles do not cause any broken layers in the CNT walls and is attributed to the flexibility of the graphene sheets. This ability is a differentiating

factor from other fibers, which are often susceptible to fracture when stressed beyond a limit.

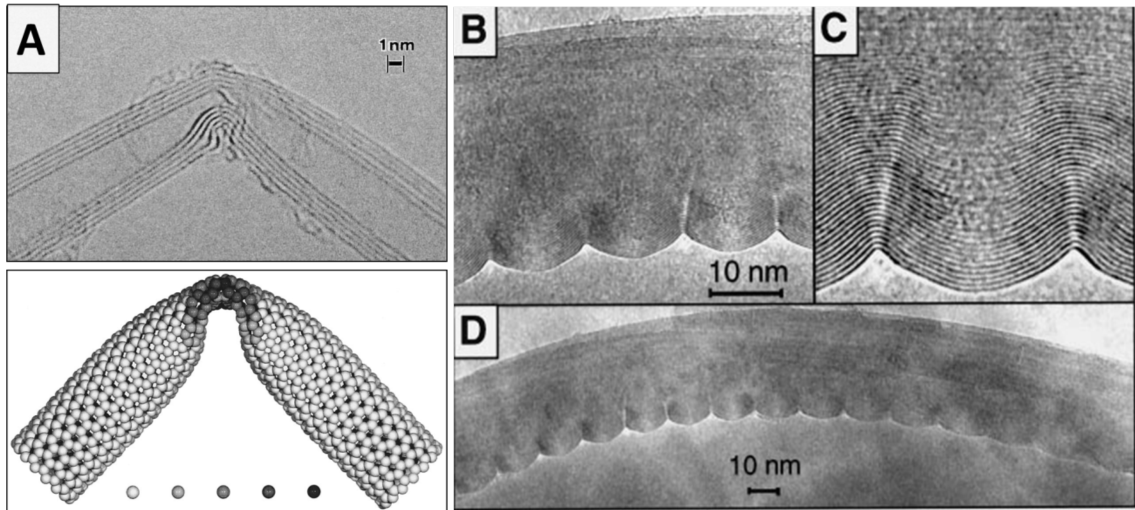


Figure 10: (a) Left: TEM image of a MWNT with a kink, right: atomic structure of a kinked SWNT [74]. (d) TEM image of a bent MWNT [75] with radius of curvature of ~400 nm and magnified views in (b) and (c).

It should be noted that all of the aforementioned studies were carried out on CNTs produced by arc-evaporation. CNTs produced by catalytic methods are generally considered to have many more defects than arc grown CNTs and thus are considered to generally have inferior mechanical properties [44]. Experimental measurements confirm this reduction in properties for catalytically grown CNTs, even after annealing up to 2,400 °C to repair defects [73, 76].

Thermal Properties

Materials of crystalline carbons exhibit the highest thermal conductivities known to man. At room temperature, pure diamond has a thermal conductivity of 2,000-2,500

W/mK, while graphite has an in-plane conductivity of up to 2,000 W/mK [44]. CNTs have the greatest predicted thermal conductivity, calculated to be about 6,600 W/mK for a (10, 10) CNT at room temperature [77].

Unsurprisingly, experimental measurements on the thermal conductivity of CNTs have produced various results. A microfabricated device made to measure the thermal conductivity in individual arc produced MWNTs measured values in excess of 3,000 W/mK [78]. The thermal conductivity of individual SWNTs has been measured to be 3,500 W/mK [79]. Similar to the above properties, the thermal conductivity of catalytically produced CNTs are expected to be lower than arc produced CNTs [44]. Until recently, CNTs had the highest reported thermal conductivities of any material, but in 2008 measurements on single layer graphene by Balandin, et al. produced thermal conductivities of up to 5,300 W/mK [80]. CNTs also exhibit extreme thermal stability. By using a high temperature platform in a real time TEM, atomic scale stability was observed for temperatures approaching 3,000 °C [81]. This result suggests that CNTs have higher thermal stability than diamond or graphite.

Overall, the properties of CNTs are extraordinary. Their ability to have ballistic transport and to behave as conductors or semiconductors without doping is incomparable to any other currently known material. In addition, their large stiffness, strength, fatigue strength and thermal stability combined with low density give them a unique combination of mechanical and thermal properties that complement their electrical properties. The robust nature and high temperature stability of CNTs are favorable for field emission because emission environments often involve high temperatures and ion bombardment.

CNTs are indeed a very unique material that have potential applications as gas sensors, composites, transistors, and electron sources.

2.2.4 CNT Synthesis via Chemical Vapor Deposition

The synthesis of CNTs has been widely researched ever since their pioneering discovery in 1991 [36]. There are many ways of synthesizing CNTs, each of which produces varying purity, alignment, chirality, and yield [82]. Many related methods have developed by an attempt to improve properties, but most can be categorized into three general methods based on the physics of the process: carbon arc-discharge, laser ablation, and chemical vapor deposition (CVD) [5, 10]. This work uses the CVD synthesis method to produce CNTs and will be the focus of this section.

In general, chemical vapor deposition (CVD) applies energy to gaseous precursors in a controlled environment in order to facilitate controlled deposition of material on a substrate. This method is used to deposit a variety of high quality materials including oxides, poly crystalline silicon, and CNTs. The CVD synthesis of CNTs gives a wide variety of process control and the ability to pattern the CNTs using a catalyst material. CVD is scalable, versatile, and a convenient method to produce CNTs directly on a patterned substrate. Thus, CVD has been heavily researched as a method for CNT synthesis.

CVD is a broad category for CNT synthesis, and many techniques have developed which vary with how the energy is applied to the gas precursors, and specific process parameters such as temperature and pressure. Most CVD methods involve two gaseous precursors: a carbon source and a reducing gas. The carbon source is normally acetylene,

methane, or ethane; however a wide variety of hydrocarbon gases can be used. The reducing gas, which is most commonly hydrogen or ammonia, prevents oxidation of the catalyst material and the CNTs during the high temperature synthesis. A metal catalyst, introduced as a gas or thin film, facilitates the growth of CNTs such that CNTs will grow only where catalyst is present. This ability to have high process control *and* controlled patterning makes CVD extremely useful. CNTs synthesized by CVD normally produces MWNTs with a high density of defects that can be up to centimeters long [45]. This method has a yield of up to 99%, so there is often no purification necessary and adds to its usefulness [83]. When the metal catalyst needs to be removed post growth, oxidation or acid treatments are used. Annealing at temperatures in excess of 2,500 °C can be used to remove defects and impurities. Although there are many variations of the CVD method, it can generally be further split into two types: thermal and plasma enhanced CVD [10].

Thermal CVD is the most fundamental method which applies the necessary energy to the gaseous precursors purely through heating. This method involves the pyrolytic decomposition of hydrocarbon gases in a reducing atmosphere at a temperature range of ~550-1,100 °C. As shown in Figure 11, a tube furnace setup with mass flow controllers is most commonly used. SWNTs can be synthesized in specific processes at temperatures of 850-1,100 °C. Normally anneal steps are incorporated in the synthesis process which exposes the catalyst material to only the reducing gas at elevated temperatures. This step reduces oxidized material and helps form the nanoscale catalyst islands necessary for the CNT growth. The catalyst materials have limited carbon solid solubility at the elevated temperatures and thus dissociated carbon atoms diffuse into the

metal, and proceed to nucleate and grow from the catalyst once supersaturation is reached.

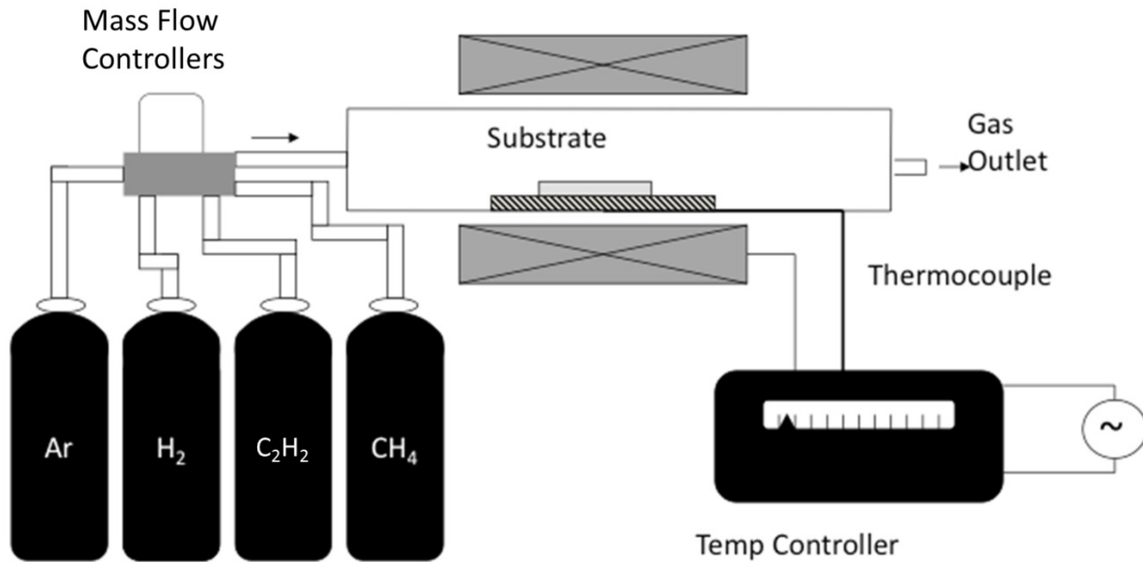


Figure 11: Schematic of a basic thermal CVD furnace for CNT synthesis [32].

The temperature range of the CVD synthesis method allows the use of many substrates, including silicon, carbon fibers, and metals. These substrates enable the controlled synthesis of CNTs to be integrated into applications where substrate compatibility is necessary, such as for microelectronics [5, 10]. A high degree of process control is achieved by precisely controlling temperature, time, pressure, gas flow rates, and gas ratios. Pressure can range from less than a few Torr to greater than 1 atmosphere. CNT growth is highly dependent on the ratio of reducing gas to carbon gas. The carbon gas needs to be at least 6% of the atmosphere, but is generally 10-40% [84]. A variety of specific CVD methods, such as low pressure CVD, are achieved by controlling these parameters.

Another common type of CVD technique is plasma enhanced CVD (PECVD), which utilizes an electric field during growth to generate a plasma within the chamber. This method supplies some of the energy needed for the decomposition of the precursor gases and preparation of the catalyst through the plasma. Thus, one advantage of this method is that lower substrate temperatures can be used. CNT synthesis at temperatures as low as 200 °C have been demonstrated, which enables synthesis on new substrates such as glass or plastics [85]. This ability enables synthesis on low cost substrates for a myriad of applications. The electric field can be achieved using direct current, radio frequency (RF), or microwave power supplies and is usually applied normal to the substrate. Since the electric field can create a higher density of reactive gas species (ions, radicals), CNT synthesis can be achieved at lower pressures than possible in thermal CVD, which can improve synthesis on high surface area substrates. This method is highly advantageous for FE applications because it preferentially grows aligned CNTs in the direction of the electric field. In addition to a thermal anneal, this method can also perform plasma anneals or etching with the reducing or other gases to prepare the catalyst for CNT growth. This method adds to the list of highly controllable parameters and includes plasma power, potential, and current, which gives the ability for a high degree of process tuning and control [39, 86-89].

One of the great advantages of CVD synthesis is the ability to pattern and control growth using the catalyst. The only materials that catalyze CNT growth are compounds containing iron, nickel, cobalt, or alloys of these elements [90]. The catalyst can be incorporated onto the substrate using a variety of methods, many of which are easy to pattern. A gas phase catalyst source, such a ferrocene for Fe, contains the metal catalyst

and will disassociate in the chamber, which will synthesize CNTs everywhere in the chamber and reduces the need for substrate preparation or a substrate at all. The catalyst can also be deposited by spin coating metallic salt solutions or by thin film deposition techniques, such as thermal evaporation, electron beam evaporation, sputtering, and atomic layer deposition. The thin films are easy to pattern using a variety of lithography techniques, which will only grow CNTs in desired locations. The film can be deposited, covered with a patterned mask, then etched away to pattern the catalyst on the substrate. It can also be patterned with a liftoff process, where the catalyst is deposited on the substrate with a patterned mask so that removal of the mask leaves a catalyst pattern. The thickness of the catalyst can vary greatly but generally ranges from 1-20 nm and determines the size of catalyst nano-islands that are formed during the CVD process. Overall, CNT synthesis is highly dependent on the type and preparation of the catalyst material as well as synthesis technique and process parameters [1, 5, 10].

2.2.5 CNT Growth Mechanism

The growth mechanisms of CNTs have been heavily studied ever since the discovery of their structure in 1991. The role of metal catalyst particles in the CNT growth mechanism is inaccessible to direct observation and remains a controversial subject with many different theories [91]. However, all CNT catalytic synthesis methods are believed to be through a nucleation and growth mechanism [5, 10]. Many CNT nucleation and growth models are based off of the vapor-liquid-solid (VLS) model proposed in the 1960s to explain the growth of carbon filaments [92]. This model involves growth by precipitation of a supersaturated catalytic liquid droplet that absorbs

carbon from the vapor phase. As carbon incorporates into the catalyst, carbon filaments continuously precipitate from the supersaturated solution.

CNT nucleation can also be explained by the catalysts' phase diagrams with carbon. Ni, Fe, and Co are the only known pure CNT catalysts and all have similarities in their carbon binary phase diagrams [5]. The catalyst solute behavior is demonstrated through the C-Ni phase diagram in Figure 12 [5, 93]. There is a finite solubility of carbon in the catalyst particle at elevated temperatures which drastically decreases as the temperature of the particle is reduced, thus producing supersaturation and solute segregation. The VLS model and phase diagram can explain why catalyst materials must be able to dissolve carbon at higher temperatures [5, 10].

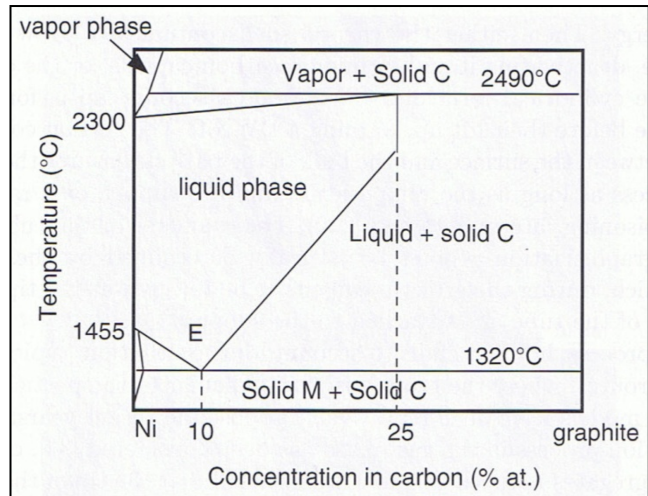


Figure 12: The phase diagram of the C-Ni system [5].

The growth of carbon precipitates from catalyst particles during the CVD process is proposed to occur via a "root" or "tip" growth mechanism [88]. These are the two most popular and accepted CVD growth theories for CNTs (Figure 13). The type of growth

that occurs and their relative amounts is dependent on the growth equipment, growth parameters, and surface energy of the catalyst particle. Tip growth occurs when adhesion between the catalyst and substrate is weak, and involves the growth of CNTs from the bottom of the catalyst particle so that the particle is lifted up on the tip of the CNT [88]. Base growth occurs with strong adhesion between the catalyst and substrate, and involves the formation of CNTs from the top of the catalyst so that the particle remains on the substrate. Experimental work shows compelling evidence for both tip and root growth [33, 39, 82, 86, 94, 95].

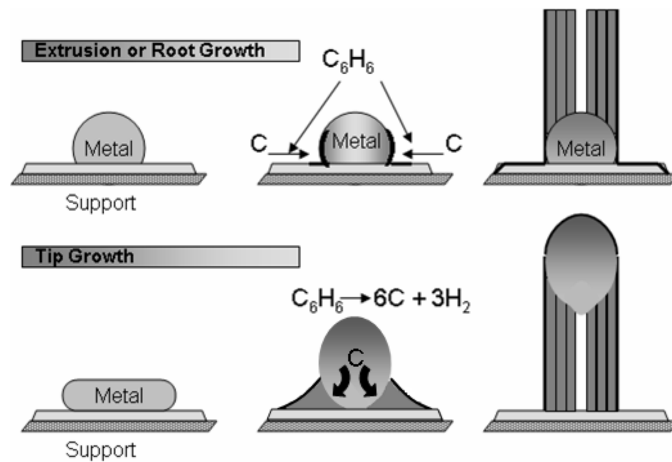


Figure 13: Schematic of the root and tip growth theories for CNT growth [88].

For CVD synthesis, the same three general steps occur for the growth of CNTs regardless if root or tip growth occurs. The first step involves ramping and holding temperature so that the catalyst layer forms nanoscale particles on the substrate. It should be noted that the catalyst doesn't necessarily melt into droplets, but rather can form through strain relief [58]. If the catalyst was melted and the temperature was high enough that the mobility of the metal atoms were high, then the average catalyst particle size

would increase via Ostwald ripening [96]. Thus, although thermal annealing in CVD can be used to create the catalyst particles, the anneal time doesn't necessarily correlate to particle diameter. Next, the hydrocarbon gas is introduced and dissociates in the chamber environment, allowing carbon to dissolve into the catalyst particles. The particles saturate with carbon and start to form CNT precipitates. Finally, the growth process stops, either due to termination of the hydrocarbon feedstock, lack of diffusion of carbon to the catalyst particle (root growth), poisoning of the catalyst with impurities, or carbide/amorphous carbon formation over the catalyst [39].

The size of the catalyst particle formed and the interaction of the catalyst with the substrate has a great effect on CNT growth. Theoretical calculations show that energetically, tubular formations of carbon are favored over small graphene sheets for nanoscale carbon structures of less than 1,000 atoms [88]. This relation is due to the high energy of the dangling edge bonds of graphene which constitutes a relatively large ratio of atoms for a small sheet. By wrapping the sheet into a tube, some of the dangling bonds are eliminated and the overall energy is reduced. In addition, the stability increases with the length and number of shells in the tube [51]. As the number of carbon atoms grows to 1,000-6,000 atoms, the ratio of dangling bonds decreases and the strain energy due to curvature of the tube becomes more significant, causing graphene to become more stable [88]. Thus, if the catalyst particles are too large, such as from Ostwald ripening, CNT growth will not occur. It has also been shown that the thickness of the catalyst is directly correlated to the diameter and growth rate of CNTs, giving evidence that catalyst thickness determines particle size. Figure 14 demonstrates this effect for a Ni catalyst [97].

Other parameters that can effect catalyst particle size are anneal times, plasma etching, and temperature. However, these parameters have multiple influences on the growth process, causing their effect to be less direct. A study on various PECVD parameters explores these effects [98]. For example, increasing temperature was shown to increase growth rate, possibly due to faster gas dissociation and faster carbon diffusion, but after a point the growth rate decreases.

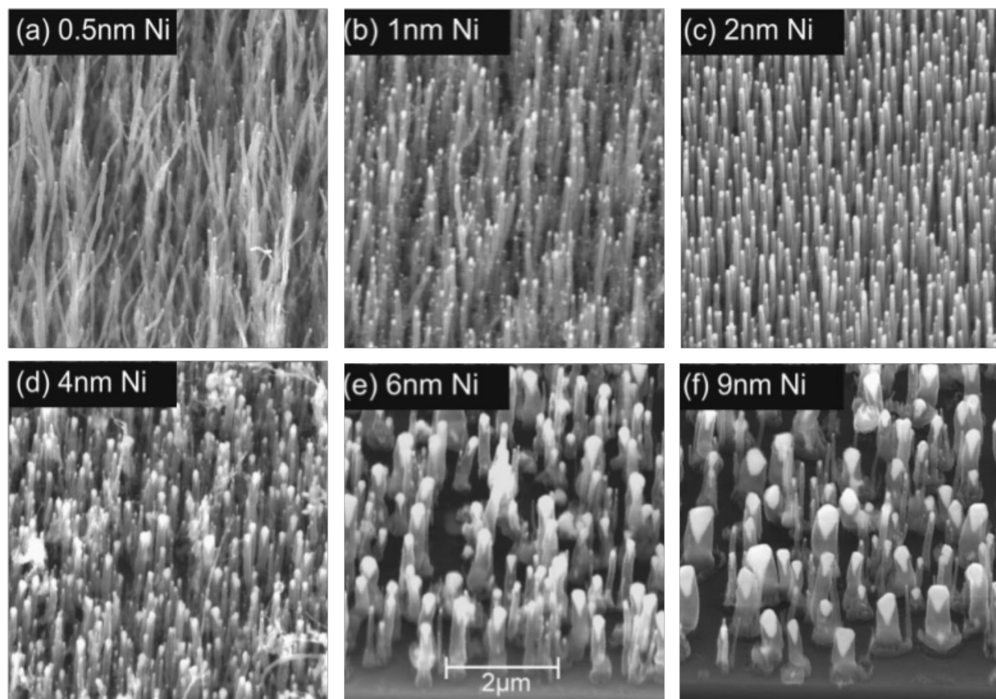


Figure 14: SEM image of CNT growth showing that catalyst thickness of 0.5 nm to 9 nm correlates to a CNT diameter of ~30 nm to ~400 nm, respectively. Note CNT length decreases as catalyst thickness increase [97].

As noted for root and tip CNT growth, the correct interaction of the catalyst with the substrate is crucial. This substrate interaction can be modified by adding additional layers of material under the catalyst. The surface energy of the catalyst needs to be such

that complete wetting does not occur with the substrate. Thus, surface energy is often modified for CNT synthesis in order to ensure that catalyst particles form. Oxides, such as SiO_2 and Al_2O_3, are commonly used as “support layers” to promote island formation of catalyst on various substrates, including Si [58].

In addition to preventing wetting, there needs to be little or no diffusion of the catalyst into the substrate at the elevated temperatures of CVD synthesis. Often “diffusion barrier” layers are used to prevent diffusion into substrates. One common example is Ni catalyst diffusion into Si. As shown in Figure 15, the diffusivity in Si becomes quite large at elevated temperatures for Ni, but not other catalysts. Without a diffusion barrier, Ni would diffuse into the Si and form a silicide, preventing CNT formation. Common diffusion barriers of Ni on Si include TiN, TaN, and Ti, which all have low diffusivity in Si (see Ti in Figure 15). At times, a single material can serve as a support and barrier layer. For example, many oxides have low diffusivity into Si and other metals, allowing them to be good diffusion barriers as well [58]. Occasionally, several materials may be needed to achieve the correct catalyst-substrate interaction, especially when only conductive materials can be used [99].

The nature of the surface interactions of the catalyst particle are not very well understood and are a source of debate. However, the surface instabilities can be related to similar systems such as crystal growth observed during molecular beam epitaxy deposition [5, 93]. There are several possible modes of growth for hetero-epitaxial film deposition which are dependent on the degree of lattice mismatch of the two layers [100]. The formation of wetting layers creates a layer-by-layer growth (Frank-van der Merwe process) due to an overall reduction of the interfacial energy. In this case, the substrate’s

interfacial energy is greater than the film's interface plus the over layer interfacial energy, thus promoting film growth. This process is analogous to the wetting of the catalyst material on the substrate, preventing CNT synthesis

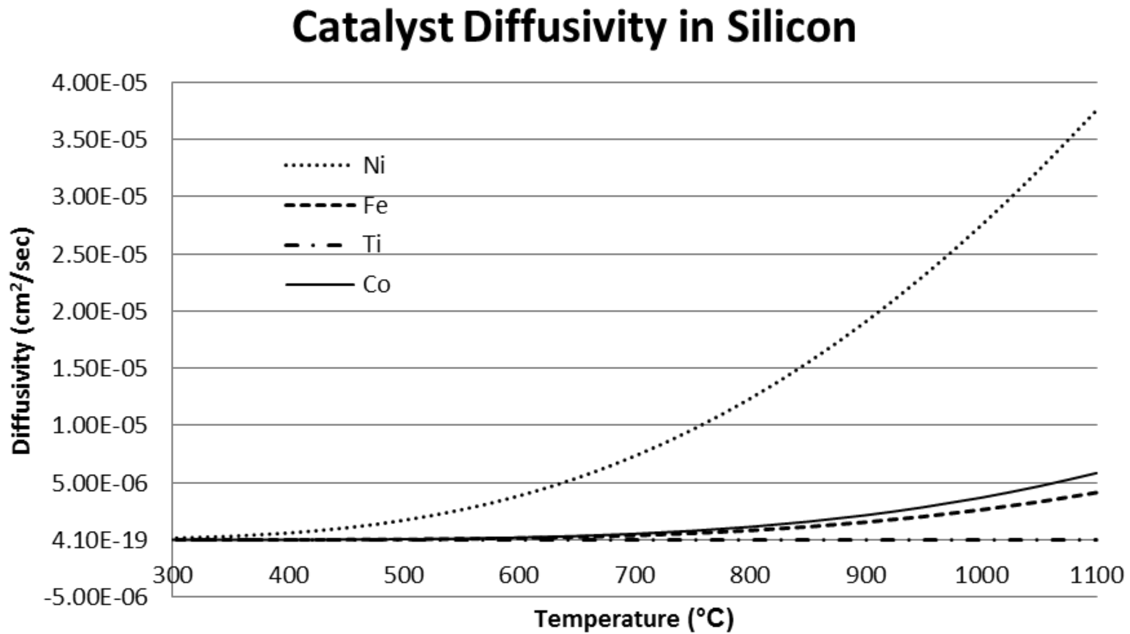


Figure 15: Diffusion in Si for CNT catalysts and Ti (a common diffusion barrier). Generated from [101].

Alternatively, non-wetting deposition can occur that forms islands on the substrate surface (Volmer Weber process) due to an increase in total interfacial energy. The substrate's interfacial energy is less than the film's interface plus over layer interfacial energy, which causes the deposition layer to repel the substrate and form islands of growth [100, 102]. This process is similar to the formation of catalyst particles on the surface of the substrate [5, 93]. In all of these cases, the catalyst surface instability is governed by two controlling themes, the first of which is the surface energy and the

second is the synthesis parameters: temperature, ramp rates, anneal times, and gas concentrations.

2.3 Carbon Nanotubes for Field Emission

CNTs have been heavily researched as FE sources due to their many desirable properties, such as an atomically sharp tip, whisker-like geometry, chemical inertness, and thermal stability, as discussed in Section 2.2 [1]. Necessary considerations for FE applications will be discussed, such as vertical alignment, effects on CNT field enhancement factor, and device configuration. In addition, the performance and failure of CNTs as field emitters as well as their potential applications in devices will be reviewed.

2.3.1 Vertical Alignment

Vertical alignment of individual CNTs or CNT bundles has been aggressively pursued due to the many industrial applications that would benefit from vertical alignment. These applications include 3-dimensional and organic photovoltaic devices [103], FE displays, and gas sensors. Alignment is important for FE applications because CNT tips in the same vertical position experience the same electric field and will produce more uniform emission. In addition, an electric field focused on CNT tips will have much greater field enhancement than CNT walls. Vertically aligned CNTs (VACNTs) were first synthesized by using Fe catalyst nanoparticles on porous silicon substrates [104]. In this work, tubes grew from pores directed in various directions, but VACNT were achieved because only CNT growing from vertically directed pores were not sterically

hindered by neighboring CNTs. Aligned growth directly onto substrates is only possible using the CVD technique and can occur via two different mechanisms [39].

The first mechanism achieves the alignment of CNTs in dense “forests” using thermal CVD synthesis and a lithography or similar method to pattern the catalyst on the substrate [105]. The aligned growth is achieved through Van der Waals forces and steric hindrance within dense arrays of CNTs (Figure 16). As the CNTs grow, the attractive Van der Waals forces between the CNTs cause alignment. In addition, any non-vertical CNTs are sterically hindered by other CNTs and forced to align [86]. Although the CNTs may exhibit curvature on the nanoscale, macroscopically they all have vertical alignment. This mechanism implies that there is a critical density needed for aligned growth, and unfortunately, it does not work for sparsely grown CNTs, which is needed for the best field enhancement of CNT tips for FE.

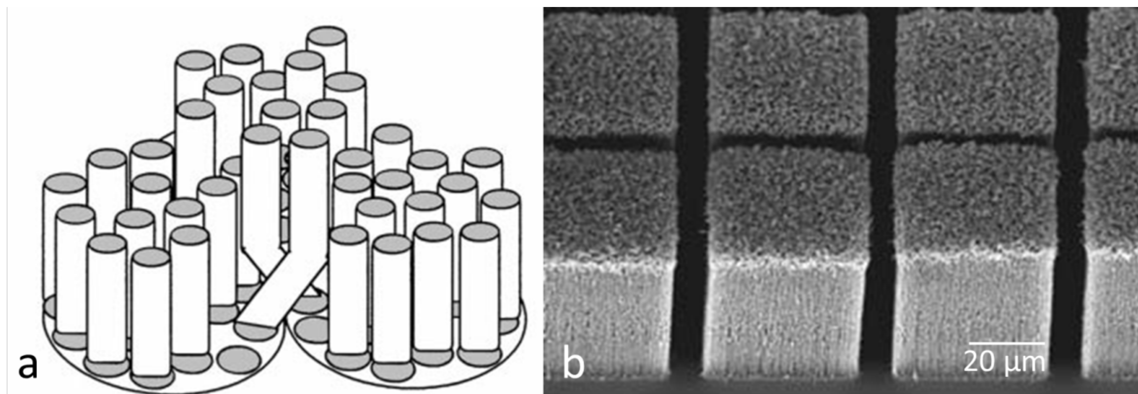


Figure 16: (a) Schematic for the alignment of densely packed CNT growth [86] and (b) SEM of rigid VACNT arrays achieved through lithography patterning of the catalyst [103].

In order to achieve sparse and aligned CNT growth, the second alignment mechanism uses PECVD synthesis, which synthesizes CNTs aligned to the electric field. Since the mechanism of alignment is an externally applied electric field, the CNTs don't necessarily need to be densely packed. Normally PECVD produces less dense arrays that can be patterned using a variety of techniques (Figure 17). The use of high resolution patterning, such as electron beam lithography, can create isolated spots of catalyst about 200 nm in diameter. At this size, only one CNT grows from each spot, thus creating arrays of aligned single CNTs as shown in Figure 17 (a).

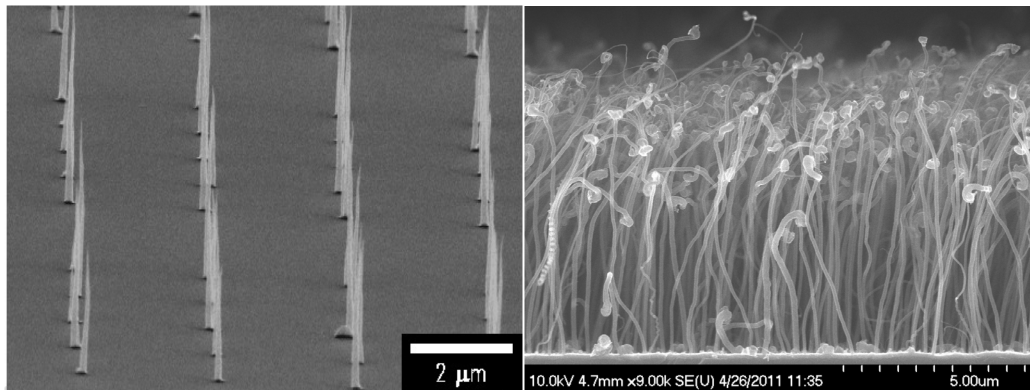


Figure 17: (a) Aligned CNT growth by PECVD of individual CNTs [106] and (b) arrays of aligned PECVD grown CNTs.

2.3.2 Field Enhancement

A major factor affecting CNT FE is the field enhancement of an electric field, which was introduced in Section 2.1.3. Careful consideration of several factors that affect field enhancement are necessary, including the high dependence on the radius of curvature, aspect ratio, and electrostatic screening. CNTs can achieve large field

enhancements due to their atomically sharp tip and a radius of curvature of less than 100 nm, which can give them enormous aspect ratios, exceeding 10^7 [46]. This geometry causes higher field concentration at the CNT tips, and hence significant reduction of the extraction voltage needed for FE. Utsumi, et al. evaluated the enhancement factors for common FE tip shapes shown in Figure 18, and concluded that the best field enhancement comes from whisker-like shapes, where the aspect ratio and degree of curvature are maximized [107]. This shape is essentially the shape of a CNT and gives more evidence on the benefit of its geometry. This prediction also explains why metal field emitter tips are often chemically etched to provide sharpened pyramid shapes [1].

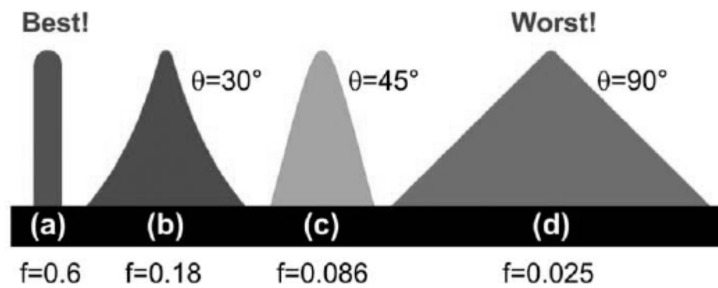


Figure 18: Geometries proposed by Utsumi: (a) whisker (b) sharpened pyramid (c) hemi-spheroidal and (d) pyramidal where f is a geometric factor [107].

Theoretical studies show that the field enhancement factor of single CNTs can be approximated by

$$\beta \approx 0.7 \frac{h}{r} \tag{18}$$

when h/r is between 4 and 4,000 and where the CNT height is h and radius is r [108]. Thus, the field enhancement will increase as the aspect ratio increases. This approximation determines that the field enhancement of a CNT is roughly two times that of a metal FE tip [5]. CNTs have also been shown to align in the direction of an applied electric field, which can provide more uniform field enhancement for an array of emitters [1, 50].

In addition to having a highly favorable whisker geometry, CNTs do not suffer the same resistive heating issues as metal emitters at high fields. Since the resistance, R, of metals increases with temperature, increased heat (Q) is produced when higher currents (I) are drawn through the material ($Q=I^2R$). Furthermore, the combination of high electric fields and temperatures causes surface diffusion at the metal tip, which results in a self-sharpening phenomenon. Although this field-sharpening increases the field enhancement and thus FE, it also increases the amount of resistive heating. This reinforcing cycle of heating and sharpening results in a thermal runaway reaction that destroys the emission tip over time [1, 2]. In contrast to metals, the resistance of CNTs reduces as temperature increases, which limits field induced heat generation at the tip and can prevent the thermal runaway reaction [1]. This attractive property could produce increased lifetimes of CNT field emitters over metal tips, and allows higher emitter density over larger areas since overheating is easier to prevent.

In order to have a complete understanding of CNT field enhancement, it is necessary to consider enhancement for many CNTs together in addition to individual CNTs. The height and separation of an array or bundle of emitters affects field enhancement. Multiple emitters that are densely packed will electrostatically screen each

other, causing a reduction in the enhancement of the electric field at the tips. As seen in Figure 19, when CNTs are randomly oriented and poorly separated, the equipotential lines show little field penetration between CNTs and no increased gradients at the CNT tips, meaning no significant field enhancement is achieved. However, when the CNTs are well separated and aligned, there is field penetration and high field gradients at the tips, causing increased field enhancement.

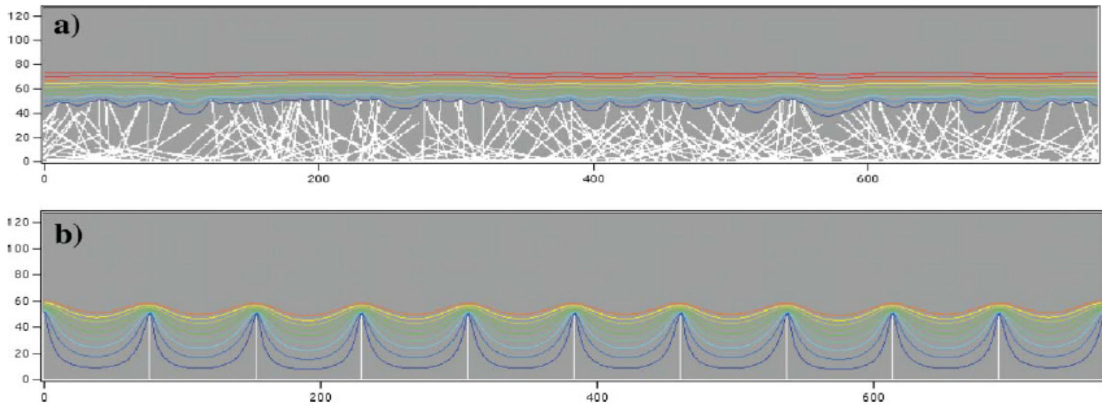


Figure 19: A schematic showing the equipotential lines of (a) poorly aligned and densely packed CNTs and (b) well aligned and spaced CNTs [1].

Studies have shown that closely packed CNT arrays are not good field emitters because field enhancement from the geometry of the CNTs is lost due to screening [109]. Therefore, it is important to have emitters that are well separated. Various theoretical calculations show that field screening effects are minimized while optimizing current density for separation distances ranging from 0.5-3 times the CNT height [1, 109-112]. Randomly oriented films of CNT field emitters have been commercially produced for low current and low current density applications, such as X-ray sources and FE displays.

However, research shows that in randomly oriented CNT films, as little as 0.1% of CNTs emit simultaneously, revealing that the design is highly inefficient and significantly more emission could be achieved [113, 114]. For applications that need high current and high current densities, such as high power/frequency amplifiers and spacecraft electric propulsion, a better design must be utilized [1, 115].

2.3.3 CNT Field Emission

Electron emission experiments on individual CNTs have demonstrated their remarkable FE properties. The first FE from CNTs was reported in 1994 [8]. In the years following this work, the amount of papers on this topic quickly increased and thousands of papers have been published ever since [9]. Most single CNT emitters are able to emit over a very large current range, roughly following F-N behavior and showing a maximum current of 200 μA for a single CNT [10-12]. This single CNT current demonstrates the tremendous current density that is possible from many CNTs if the same field enhancement can be maintained. Of the figures of merit discussed in Section 2.1.1, current density (J), turn-on field (E_{to}) and threshold field (E_{th}) are most commonly reported for CNT FE. If one extrapolates the current density for a single CNT to a large array of CNTs, the effect of screening becomes apparent. Unrealistic current densities result on the order of 10^7 A/cm^2, but this will never be achieved due to electrostatic screening and the unrealistic assumption of 100% packing density. Another important metric for CNT FE is total bias at E_{to} or E_{th}. Due to the large variation in electrode spacing and field enhancement, this value will vary greatly. The total voltage input

needed will give an idea of the efficiency of the device design for achieving the cited electric fields.

There are numerous methods to evaluate FE of CNTs. Emission tests are conducted on films of randomly oriented emitters, arrays of CNTs, or a single CNT as well as on different types of CNTs such as multi or single walled, capped or uncapped CNTs, and doped CNTs. The many different types of emitters that are tested have led to a wide variety of emission results for CNTs, some of which contradict other results [5]. For example, the field enhancement factor has been experimentally measured to be anywhere from 30,000 to 50,000 for individual CNTs and 100 to 3,000 for films of CNTs [11]. The record low threshold field reported is 0.4 V/μm [116], but often much higher fields are reported on the order of several V/μm [9]. These variations can also be attributed to the strong dependence of field enhancement on test setup, emitter geometry, height, and separation. Small changes in CNT geometry from sample to sample or even during emission can induce a large change in emission behavior [5]. In addition, the emission characteristics are dependent on the testing methods and specific setup of the testing apparatus, such as anode geometry and separation distance [4]. Therefore, direct comparison of emission results is often difficult. A survey of FE results from 2001 in Table 1 shows the large range of favorable data for various CNT films [5, 117]. A more recent review can be found in [9].

The type of CNTs has an effect on the electron emission behavior. Electron emission from MWNTs has been shown to be much more robust than SWNTs, even though SWNTs have larger field enhancement since they have a smaller diameter. Some studies find they degrade up to 10 times faster than MWNTs [117]. In addition, most

MWNTs are considered to be conductors [44]. Thus, a vast majority of FE work is conducted with MWNTs, especially since they are much easier to synthesize.

Table 1: Emission characteristics of CNT films (note: references correspond to the source references) [117].

Reference	Emitter	d (μm)	S (cm^{-2})	E_{to} (V/μm)	E_{thr} (V/μm)	J_{max} ($A\ cm^{-2}$)	Remarks
[22]	MWNT	10–40	0.002	n.a.	<25*	1	Very dense "tubulene" film
[153]	MWNT	15	0.003	n.a.	~15*	10	Very dense "tubulene" film
[24]	Arc MWNT	20	0.008	n.a.	20*	0.1	
[154]	Arc MWNT	30	0.007	4.0	6.5		
[113]	Arc MWNT	125	0.07	2.6	4.6		
[79]	Arc MWNT	125	0.07	1.1	2.2		Purified sample with closed caps
[124]	Arc MWNT	20–100	2.5×10^{-5}	7.5*	10*	0.4	Open tubes dispersed in epoxy
[155]	Arc MWNT	80	0.025	0.9*	4*		O_2 plasma treated tubes dispersed in epoxy
[126]	Arc MWNT	200	0.02	n.a.	1.5		Tubes dispersed in epoxy
[120]	SWNT	125	0.07	1.5	3.9		
[156]	SWNT	10–300	0.002	n.a.	4–7	4	
[157]	SWNT	150	3.1	2.1*	n.a.		
[91]	CVD MWNT	n.a.	0.001	1.7*	n.a.		
[93]	CVD MWNT	70	n.a.	n.a.	4.8–6.1		Aligned MWNTs, 15 emitters
[158]	CVD MWNT	150	3.1	n.a.	2.1*		Large amount of graphitic fragments
[134]	CVD MWNT	n.a.	0.0003	4.8	6.5	0.1–1	
[159]	CVD MWNT	600	0.07	n.a.	⩾ 5		
[160]	CVD MWNT	150	0.2	3	6.6*		Si substrate
[99]	CVD MWNT	500	0.1	1.6	5*		Steel substrate
[99]	CVD MWNT	500	0.1	3	5.6*		Ni substrate
[161]	CVD MWNT	10–300	0.002	0.75	1.6	1–3	Catalyst supplied in gas phase
[162]	Graphitic fibers	300	1–10	2.1	n.a.	0.2	

d is the interelectrode distance, S the emission area, E_{to} and E_{thr} are the turn-on and threshold fields needed to produce an integrated current density of 10 μA/cm² and 10 mA/cm², and J_{max} is the maximal current obtained without destruction of the emitter. n.a. means that the value is not indicated or could not be deduced from the figures, and * indicates that the value was estimated or extrapolated from the presented data.

FE from CNTs is achieved using one of two general electrode configurations: diode and triode (Figure 20) [5]. In the diode configuration there are only two electrodes: the cathode, which is electrically connected to the CNTs through the substrate, and the anode, which is above the cathode to collect emitted electrons. The diode configuration is very simple and compatible for nearly every type of process. It is widely used, especially

for experiments that are initial investigations of FE behavior. Although the diode is convenient, it is not ideal for efficiency because the electrode separation is much larger than the triode configuration, requiring a much larger voltage input to achieve the same electric field.

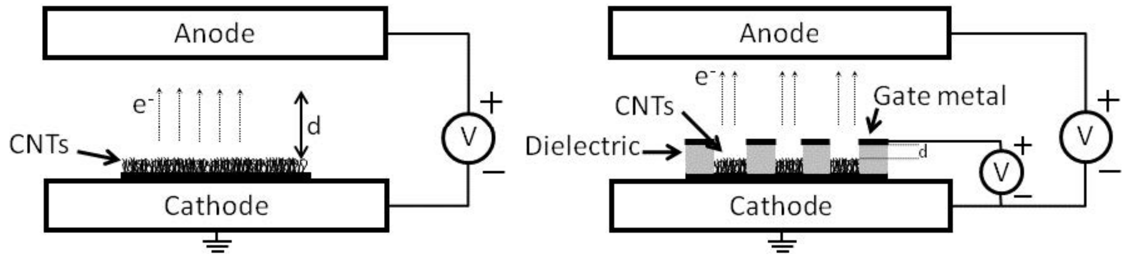


Figure 20: Schematic of (left) diode and (right) triode configurations for field emission testing [118].

In the triode configuration, a gate electrode between the anode and cathode is used to drive the electron emission. The gate is normally separated from the cathode only by a thin dielectric isolating layer. Through thin film deposition techniques, this method allows electrode separations that are less than 10 µm. Thus, much larger electric fields are achieved for a given input voltage than in the diode configuration, where the separation is on the order of 100 µm or more. In the triode, control and modulation of the electron emission is much easier because the low voltage gate controls emission. Unfortunately, only certain fabrication techniques are compatible with this setup, where the CNTs must only be on the cathode. In addition, the gate must remain electrically isolated from the cathode, which can be difficult to achieve during fabrication, CNT synthesis, and testing.

In the triode configuration, the gate will have a finite current consisting of field emitted electrons that go to the gate and/or leakage current through the insulator between the cathode and gate. A common metric is the ratio of anode to gate current, where an ideal emitter would have most of the current go to the anode, as emission to the gate causes a drop in efficiency. Triode type structures have shown favorable gate currents that are 25% to less that 1% of the total emission current [119-121].

2.3.4 Spindt Cathode Design

An understanding of the ways to improve field enhancement and FE has led to extensive research on sharp tip microstructures in the past 50 years. The most famous triode array device is the Spindt cathode, which was first developed in 1968 [15]. The Spindt arrays consist of a triode structure where arrays of metal cones, whose tips are etched to a few hundred nanometers in diameter, are recessed below the gate (Figure 21). Lithography techniques are used to create micron sized arrays of these tips, which are made of high melting temperature metals, such as molybdenum or tungsten. This design minimizes the electrode spacıng down to a few microns and achieves field enhancement by fabricating an emitter geometry similar to Figure 18(b).

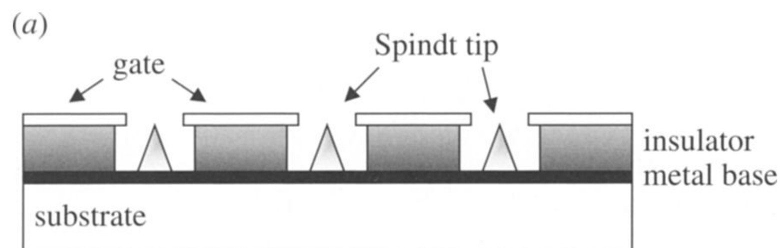


Figure 21: Cross section schematic showing the triode design of the Spindt cathode [2].

The Spindt cathode design has been successfully demonstrated in small FE displays, but never reached commercial availability due to drawbacks in the device. These cathodes were plagued by short lifetimes and unstable emission due to resistive heating failure (discussed in Section 2.3.2) and desorption of contaminants [1]. These drawbacks have limited the type of Spindt cathodes that can be produced based on their thermal management. Emitters with very large current density must be made very small (μm^2) so that the resistive heating can be dissipated. On the other hand, high current emitters (on the order of 10 mA) can be made only if they are spread out over a large area (several ft^2) with a low current density so that the heating can adequately dissipate. Due to these limitations, it has proven very difficult to produce a small area emitter that also produces large currents using traditional metallic emitters [1, 2, 122].

Although the performance of a Spindt cathode has shortcomings, the design of the cathode provides optimal emission and field enhancement because the emitter contains a large number of electrostatically isolated emitting elements [4]. For this reason, some of the CNT FE work has mimicked this design such that CNTs are grown within electrostatically isolated pits [6, 13, 14]. Even though this triode design causes a lower emitter density, it is offset by higher efficiency as higher field enhancement and less screening is achieved. Some research uses electron beam lithography to create the smallest possible pits, so that single or very few CNTs are within each pit [1, 13, 14, 106, 123-126]. It is generally accepted that the smaller the pit, the better the emission due to decreased CNT screening and electrode separation. Conversely, little is known about the effect of pit shape (for the case of multiple emitters within a single pit) and separation

distances of the pits [127-130]. This work will focus on a Spindt type design for its efficiency benefits.

2.3.5 Failure During Field Emission

The degradation and failure of CNTs from FE has been well studied, but mostly as individual CNTs or mats of randomly oriented CNTs [131]. Little is currently known about the FE lifetime and failure mechanisms of CNTs in Spindt based cathodes. Long term FE of a single CNT has been demonstrated at a low current of 0.4 μA for more than two months with no degradation [132]. In addition, emission of a film of CNTs showed an 11% increase in the applied field to maintain emission of 10 mA/cm^2 for 8,000 hours [133]. Recently, work was published on the FE of screen printed CNTs at 1.27 mA/cm^2 for over 45,000 hours (5.1 years) at a 10% duty ratio [134]. These lifetime data show that single CNTs and arrays of CNTs are a viable material for long term electron sources.

Although the exact mechanism of FE failure in CNTs is not completely understood, several factors have an important role [5]. Failure can occur gradually or very abruptly. Gradual degradation can be caused by electrostatic deflection or mechanical stresses which can cause small changes in the emitter geometry and lead to a decrease in field enhancement. Another strong influence on CNT emission is the presence of residual gases during electron emission. The emitter can be bombarded by gas molecules that are ionized by emitted electrons, causing irreversible damage and/or a decrease in field enhancement [5, 10]. Modeling has shown that degradation from ion sputtering is highly dependent on the applied voltage in the apparatus, showing that a low voltage Spindt type design is beneficial [135].

FE at high currents can quickly degrade the structure of a CNT. In-situ observations of CNT emission via TEM showed segment by segment shortening of the CNT [12, 136, 137]. This process involves a sharpening of the CNT tip as the length of the CNT is reduced. Although this process improves the geometry at the CNT tip, the distance to the gate is increased and the CNT will eventually be destroyed. Unlike metal Spindt tips, as the emitter is shortened the geometric field enhancement is maintained because of the whisker like geometry.

Others have proposed a string by string high current degradation of CNTs where strings of carbon atoms or entire outer walls peel off the CNT [138]. Although different processes for high current CNT failure are proposed, all of the cases involve a strong decrease in the emission current that requires a large increase in field to maintain current. This degradation could be due to either the electrostatic forces of the high electric fields on the CNT, or due to locally high temperatures from the flow of current out of the CNT tip, which effectively "burns off" parts of the CNT [5, 10, 136].

Abrupt failure of the emitter often occurs through a failure of the electrical circuit in the cathode design. An individual CNT can become disconnected at the cathode substrate during emission, which suggests mechanical failure due to tensile loading and/or resistive heating. At high emission currents, tensile loading may be a failure mechanism, whereas failure at lower emission currents could be due to resistive heating causing weakening of the CNT-substrate bond [5, 136, 139]. An additional and very catastrophic failure mechanism is a result of arcing between the anode and cathode during FE. Dielectric breakdown between the electrodes from high emission currents,

anode outgassing, and/or local evaporation of the cathode creates a conduction channel between the anode and cathode that generates an arc that can destroy the emitter [4, 5].

There are much fewer studies on the damage and failure modes of CNTs from FE testing in a Spindt-based structure. The failure modes include those for individual CNTs or CNT mats, but the cathode design is especially susceptible to arcing and electrical shorting due to the small electrode separation distance. Electrical shorting of the gate to the substrate is a common and problematic failure mode that prevents the production of commercializable CNT electron sources [13, 140, 141]. Understanding their failure will help produce more reliable and robust Spindt-based CNT electron sources. Spindt, *et al.* found that damage and failure in their metal based emitters was primarily due to arcing [142]. In CNT Spindt-based structures, failure and damage have been observed due to disconnection of the CNTs from the substrate and arcing in the emission pits [6, 143].

The mechanisms of thin film dielectric failure are not well understood, but several possible explanations exist [144]. Due to the nature of thin films, very small leakage currents flow through "weak" parts of the dielectric. These weak areas are always present because there is a finite conductivity for any insulator. In thermal breakdown, strong electric fields will locally increase heating at these leak sites which increases the concentration of point defects. At room temperatures, the equilibrium point defect concentration is normally low due to the minimization of entropy. As temperatures increase, entropy increases, causing point defects to be much more favorable [145]. As point defect concentration increases, ionic conductivity in the dielectric increases which allows more current flow and heating. A chain reaction of increasing current flow and localized heating can increase to the point of thermal breakdown [4, 146].

Avalanche breakdown is a thin film dielectric failure mechanism that arises from the fact that even the best insulators contain some free electrons. These electrons can be from the non-zero probability of electrons in the conduction band or from defects which create charge carriers. In large electric fields these charge carriers are accelerated and, above a critical value, they can achieve enough kinetic energy to remove electrons from adjacent atoms. These new electrons can ionize more atoms and a chain reaction called ensues that quickly increases current flow through the dielectric to the point of failure [5]. The lifetime of the dielectric can be increased by minimizing the electric field and maximizing film quality by minimizing the number of defects and impurities in the film. Thus, the use of quality materials and films, and operation at low fields is imperative to a Spindt type cathode lifetime [4, 5, 146].

2.3.6 Applications

The production of a successful CNT field emitter in a triode design would have a potential application in any technology which would benefit from low-power, light weight electron sources. These specifications are due to the compact triode design and the relatively low total emission current abilities for CNT electron sources. This dissertation is focused on the application of CNT FE for spacecraft electric propulsion systems, but the device could also be implemented in a variety of electronic devices, including portable x-ray sources and flat panel displays.

Spacecraft often use electric propulsion systems to provide thrust during long duration maneuvers or station keeping because they are much more efficient than conventional combustion thrusters. Electric propulsion systems operate by ionizing

gaseous propellants (typically Xenon) and electrostatically accelerating the ions, thus creating thrust. A thermionic source is normally used to emit the electrons necessary for ionizing the gas. Current cathodes are bulky, must be heated and can consume up to 10% of the propellant. These factors cause an increase in spacecraft weight and fuel needed. Weight is a significant consideration since it is estimated to cost $20,000 for each pound of material sent into orbit [147]. A CNT based electron source's efficiency and reduced weight would lower costs and increase spacecraft lifetime.

In the field of spacecraft electron sources, Busek Co. has a commercially available CNT cathode developed for spacecraft neutralization that has a sustained output of 1 mA and an approximate current density of 0.2 mA/cm^2 [148]. The Busek electron source contains an external gate electrode with a random mat of CNTs, so electrode spacing and field enhancement are far from idealized. Since total output and weight are important factors for electric propulsion, a CNT triode emitter that has an equivalent current density at a lower voltage input would be considered highly superior.

Although the competitive advantage of a CNT based cathode for electric propulsion is apparent, an internal industry analysis revealed that the industry is not large enough to support a successful business venture [149]. The US satellite market is valued at about $14 billion but the relevant segments of the industry are much smaller. The satellite thruster sub-industry is estimated to be less than $100 million and the thruster cathode sub-industry is estimated to be only $2 million. A sub-industry of this size would not be worth the investment of a dedicated venture without substantial government assistance.

A very fitting application for Spindt type CNT electron sources is in electrodynamic space tethers. These systems are currently in development by Tethers Unlimited, Inc. and are designed to interact with the Earth's magnetosphere to generate power or propulsion without consuming propellant. Differing from propellant based thrusters, these tethers generate thrust through Lorentz-force interactions with a planetary magnetic field and eliminate the need to launch large quantities of propellant (Figure 22). Spindt type CNT electron sources are well suited to this technology due to their lightweight, low power operation and no need for propellant. The electron source, mounted at one end of the tether, can magnify the propulsive or power generating effect of the system.

CNT field emitters also have potential applications as X-ray sources, since electron bombardment is needed to produce X-rays. Typical thermionic electron sources are heavy and bulky. In addition, field emitted electrons from CNTs have a much more uniform energy distribution than thermionic sources. This characteristic enables much higher X-ray resolution [150]. Researchers have already produced X-ray sources and images using a CNT based electron source, although in a diode design [151-153]. A low power and compact CNT electron source could enable portable X-ray sources for the medical, security, and non-destructive testing industries. An internal industry review for X-ray systems showed the potential market for each of these areas is significant, with a $140 million, $37 million, and $88 million size for the medical, security, and non-destructive testing markets, respectively [154]. The value proposition for a CNT based X-ray source comes from the possibility of increased portability, enhanced resolution, and the potential for new markets with a miniaturized device.

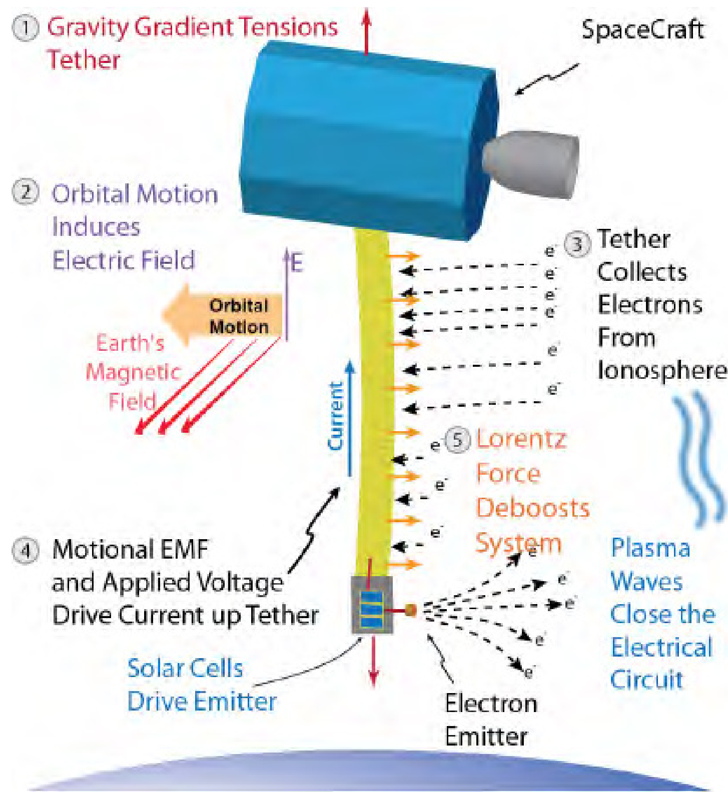


Figure 22: Schematic describing the electron emission enhanced electrodynamic space tether for enhancing the electrodynamic drag.

Finally, a thin film electron source could be applied to flat panel displays, where each pixel contains its own electron source. Many electronics companies have heavily pursued "FE displays" as a new display technology since the 1960s, but have yet to produce a commercial product. The first CNT based FE display was reported in 1998 in a 32 x 32 pixel matrix using a randomly oriented CNT source in a diode configuration [9, 155]. For FE display applications, a current density of 10 mA/cm^2 is needed for pixel saturation (from the definition of E_{th}). Although this technology has been heavily developed, the voltage input for this current density must be minimized in order to make the FE displays commercially feasible. In addition, lifetime and cost issues have hampered development [2].

CNT FE is a rapidly changing field with a great amount of research on many aspects of the science. This work shows that CNTs have outstanding performance as field emitters and, at the very least, potential for many applications. CNTs have ideal electrical and mechanical properties along with a truly nanoscale structure with a large aspect ratio. They can be synthesized in an aligned manner with a great deal of precision that enables divided arrays of even single CNTs. Due to these properties, a heavy interest in CNT FE emerged soon after their pioneering discovery and continues today.

CHAPTER 3

EXPERIMENTAL PROCEDURES

This chapter details the final experimental procedures that were developed for this dissertation. The silicon fabrication procedures for the CFEAs are fully detailed along with their electronic packaging and characterization techniques. Chip resurrection techniques developed to improve chip yield are also described. Next, the experimental setup for the Hall effect thruster exposure to the CFEAs are covered. Finally, details are given about a CubeSat developed to test CFEA performance in the space environment.

3.1 Silicon Fabrication Procedures

3.1.1 Emission Pit Fabrication

The fabrication procedures for the CFEAs involve standard CMOS processes including thin film deposition, ultra violet lithography, and a combination of wet and dry etching (Figure 23). The emission pit fabrication and CNT synthesis have been reported in manuscript [156].

The starting substrate is a 100 mm diameter Si wafer with (100) orientation, n-type arsenic doping, a resistivity of 0.001-0.005 Ωcm, and 500 μm thickness. Immediately prior to processing, each substrate is cleaned of organic residue using a standard 'piranha etch' bath of 3:1 H_2SO_4:H_2O_2 at 110 °C for 10 minutes. The substrate is rinsed and dried with nitrogen in a Semitool Spin Rinse Dryer.

Thermally grown SiO_2 synthesized in a Tystar tube furnace at 1,100 °C for ~24 hours is used as the insulator (Figure 23a). The process combines a 4 hour dry oxidation followed by a 20 hour wet oxidation. A final thickness of 3.2 μm is achieved. The SiO_2 film thickness is measured with a Nanometrics NanoSpec 3000 reflectometer.

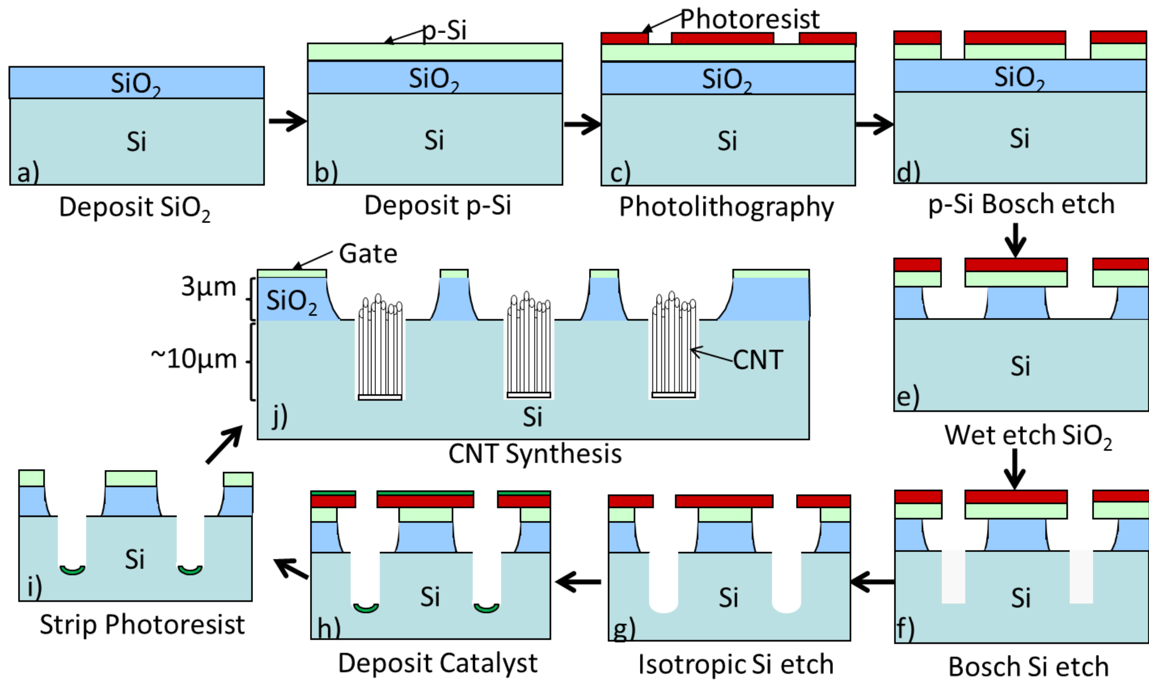


Figure 23: Fabrication process flow for the internally gated CNT FE design: (a) SiO_2 deposition, (b) p-Si deposition, (c) photolithography, (d) p-Si etch, (e) SiO_2 etch, (f) Si trench etch, (g) Si isotropic etch, (h) catalyst deposition, (i) liftoff, (j) CNT synthesis.

Doped polycrystalline silicon (p-Si) is deposited as the gate electrode (Figure 23b). A Tystar CVD tube furnace is used to deposit the 500 nm p-Si at 588 °C and 250 mTorr with a silane flow of 100 standard cubic centimeters per minute (sccm) for 90 minutes. Film thickness is measured with the NanoSpec reflectometer. The p-Si is doped in a Tystar tube furnace with Techneglas (Perrysburg, OH) PhosPlus TP-470 solid source

dopant by heating to 1,050 °C for 1 hour followed by a drive-in anneal at 1,100 °C for 30 minutes. These particular gate and dielectric materials are chosen to maximize film quality and compatibility while maintaining ease of fabrication.

The SiO_2 and p-Si are deposited on both sides of the wafer (not shown in Figure 23). The backside p-Si is removed so that the Si backside can be used as an electrical contact. To protect the layers on the top side of the wafer, S1818 photoresist (Dow Chemical Company) is spin coated at 3,000 rpm for 30 seconds using a Karl Suss RC-8 Spin Coater and baked at 95 °C for 8 minutes. The native oxide layer present on the p-Si from doping is etched in a buffered oxide etch (BOE) solution (6:1) for 30 seconds. Complete etching is noted by a change in color and a hydrophobic p-Si surface. An Advanced Vacuum (Lomma, Sweden) Vision reactive ion etch (RIE) tool is used at 90 W and 100 mTorr with 25 sccm of SF_6 and 5 sccm of O_2 for 3 minutes to etch the backside p-Si. Complete etching is noted by a change in color and a hydrophilic surface. Photoresist is removed by an acetone soak and solvent rinse. The backside SiO_2 is removed concurrently with the wet etching of the front side SiO_2.

Standard ultraviolet lithography is used to pattern the substrate instead of higher resolution methods, such as electron beam lithography, in order to maintain scalable fabrication methods (Figure 23 (c)). The native oxide layer on the front side p-Si is removed in BOE for 30 seconds. This step also removes any residue from the photoresist coating. Sufficiently low sheet resistance of the p-Si, typically ~10^{-4} Ω/sq, is now tested with a Signatone Four-point probe system. Hexamethyldisilazane (HMDS) is applied to the wafer using the RC-8 spin coater at 3,000 rpm for 30 seconds to increase photoresist adhesion. S1813 photoresist (Dow Chemical Company) is immediately spin coated at

4,000 rpm for 40 seconds with a 4 second ramp, and soft baked in an oven at 110 °C for 8 minutes. The photoresist is exposed in a Karl Suss MA-6 mask aligner under 365 nm light. The exposure dose is normally about 150 mJ/cm^2, which requires an 8.6 second exposure at an energy density of 17.3 mW/cm^2. The photoresist is developed in MF-319 (Rohm and Haas Electronic Materials LLC) developer for 60 seconds. Confirmation of the patterning is achieved using optical microscopy (OM). The patterned wafer is hard baked in an oven at 110 °C for 20 minutes to cure the photoresist for subsequent processing.

The patterned wafer consists of 64 die that are 11.75 x 11.75 mm. Each die has an array of 4 µm diameter circles across an ~8.6 x 8.6 mm square. The hexagonal patterned pitch of the circles varies: 16 die have a 200 µm pitch, 32 have a 100 µm pitch, and 16 have a 50 µm pitch. Depending on pitch, a die will have between ~1,800 – 29,000 circles. An OM image of the patterned array with a 50µm pitch is shown in Figure 24.

A Bosch etch process in an SPTS (Newport, UK) Deep RIE tool anisotropically etches the p-Si gate (Figure 23(d)). The wafer is first exposed to a brief oxygen plasma to remove any remaining photoresist scum from the lithography process. The descum is performed in the Vision RIE using a 50 W plasma of 50 sccm O_2 at 60 mTorr for 90 seconds. For the Bosch etch, the etch step is 5 seconds with SF_6 at 130 sccm and O_2 at 13 sccm, a pressure of 10 mTorr, and a coil power of 600 W with a platen power of 30 W. The passivation step is 4 seconds with C_4F_8 at 50 sccm and a coil power of 600 W with a platen power of 0 W. Both the platen and the coil power are radio frequency generated. Approximately 13 cycles are needed to completely etch the p-Si. Complete etching is confirmed with OM and the NanoSpec reflectometer.

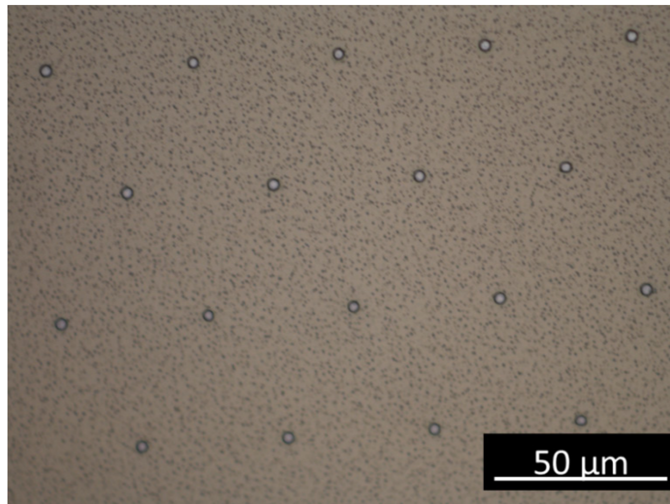


Figure 24: Optical micrograph of a photolithographically patterned array of circles.

Standard isotropic plasma etching of p-Si does not achieve uniform etching due to the disparate etch rates of the crystal grains, which results in jagged sidewalls and loss of feature definition. The Bosch process is mainly used for its sidewall passivation, which results in smoother etched sidewalls. The process has short cycle times to minimize sidewall roughness and achieve an anisotropic etch.

Prior to the SiO_2 etch, the standard descum process is used to remove any residual passivation material from the Bosch etch and to improve the hydrophilic nature of the photoresist for better wetting. The SiO_2 is isotropically etched for 35 minutes in a BOE solution (6:1) using a magnetic stir bar (Figure 23(e)). The wafer is placed in a custom made Teflon mount and submerged upside-down in the BOE solution. The upside-down position and stir bar promote uniform etching across the wafer. The SiO_2 etch rate is 100 nm/min and the SiO_2 is intentionally over etched so that the exposed Si substrate in each pit is larger than the photoresist aperture. Complete etching is again confirmed with OM and the NanoSpec reflectometer.

A second Bosch etch using the SPTS tool and same etch recipe is used to deepen the pits by etching into the Si substrate. The process uses an 8 second etch and 7 second passivation step for ~20 cycles (Figure 23(f)). This step increases the pit depth by 5-10 μm without significant removal of photoresist or increasing the insulation layer thickness. Interestingly, the Si pit diameter is determined by the size of the photoresist aperture and not by the amount of Si surface exposed, as shown by the unetched Si surface in Figure 25(a). Etching is inspected initially with OM and then with a WYKO 3300NT optical profilometer to confirm the depth of the silicon pits.

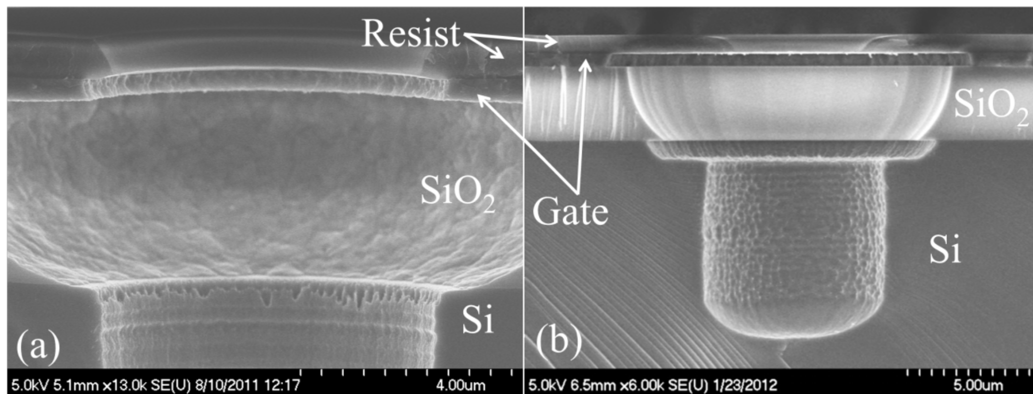


Figure 25: SEM cross section of etch geometry a) after Si Bosch etch, showing the over etch of SiO2, undercut p-Si gate, and a Si aperture that is defined by the photoresist aperture; and b) after the isotropic SF_6 etch, showing the Si pit and lateral etch of the p-Si causing an overhang of the photoresist over the Si pit.

The standard descum process is again used to remove any residual material from the SiO_2 etch. The isotropic SiO_2 etch causes an undercut of the gate layer by several microns. An RIE process is used to simultaneously remove this undercut p-Si and increase the diameter of the Si pit by isotropically etching all silicon exposed in the pit (Figure 23(g)). The Vision RIE is used at 70 W and 100 mTorr with 25 sccm of SF_6 and 5

sccm of O_2 for 3 minutes. Wafers are placed on glass slides in the Vision to isolate it from the chuck, which promotes isotropic etching by removing the directionality from the bias in an RIE etch. OM is used to confirm complete etching; often 1-2 more minutes of etching is needed, but care must be taken not to over etch the p-Si, causing the p-Si aperture to be too large. Typically the p-Si is etched about 100-200 nm past the p-Si/SiO_2 interface (Figure 25(b)). This etch also increases the depth of the Si pit by ~2 μm, shown by the curved base of the pit in Figure 25(b).

The isotropic Si etch ensures that catalyst cannot subsequently deposit on the gate, and results in a ~3 μm lateral buffer zone between CNT growth and the gate sidewall, thus preventing an electrical short between the two. The Si pit is also widened to prevent catalyst deposition on the Si sidewalls and is consequently deepened to achieve a total pit depth of 10-20 μm.

Prior to catalyst deposition, the standard descum process is used to remove any residual material from the silicon etch. This step is critical for having a clean catalyst-substrate interface for quality CNT growth. The etch geometry allows a line-of-sight path for deposition of the 4 nm Fe catalyst directly on the base of the pit (Figure 23(h)). An Angstrom Engineering (Kitchener, Canada) EvoVac system is used to deposit catalyst at $< 5 \times 10^{-7}$ Torr by electron beam evaporation. The photoresist is removed by a solvent rinse and soaking in Baker (Phillipsburg, NJ) PRS 2000 photoresist stripper at ~80 °C, leaving catalyst only in the Si pits (Figure 23(i)).

3.1.2 Electrical Contact Deposition

Metal contacts are deposited on the p-Si gate and Si backside of each die to create a quality electrical contact. A simple shadow mask process is used to pattern the contacts on the p-Si. A machined mask shadows deposition of material everywhere except a small 300 μm wide L-shaped region at the edge of each die (Figure 26). The Si wafer edges are taped to an Al mount that has a groove fit for the wafer and a large hole exposing the backside of the wafer. The shadow mask is aligned to the wafer using a stereoscope to line up alignment marks on the wafer and mask, and is mechanically secured to the mount with screws.

A Denton Explorer (Moorestown, NJ) electron beam evaporator is used to deposit metal at $< 8 \times 10^{-7}$ Torr. For the gate contact, a 50 nm layer of Ti is deposited as an adhesion layer, followed by 300 nm of Au. The Denton Explorer has the capability to flip the mount without venting the system. Thus, the backside of the wafer is subsequently deposited with 300 nm of Al for the cathode contact. After deposition, the shadow mask is disassembled and the wafer is inspected by OM followed by a solvent clean. A picture of a wafer with the gate contacts is shown in Figure 27.

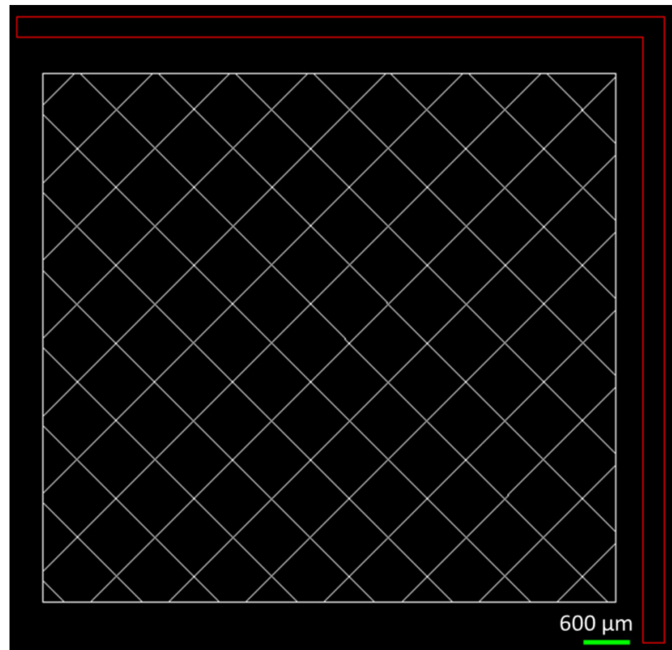


Figure 26: Illustration of gate contact pattern on a die. The pit array area is white and the 300 µm wide gate contact is red.

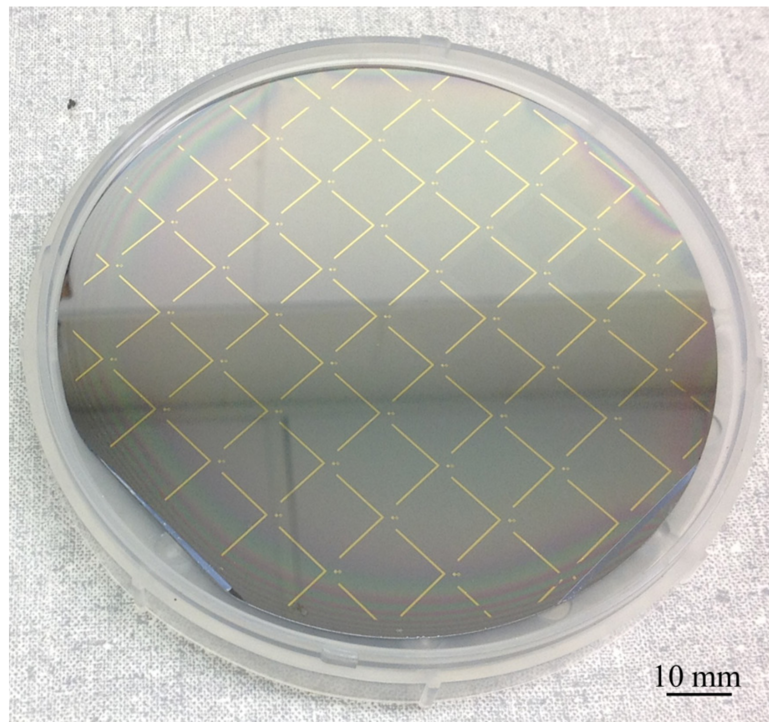


Figure 27: Picture of a 100 mm wafer with a Au L-shaped gate contact on each die.

3.1.3 Dice Channel Etching and Dicing

The p-Si gate material around the edge of each die must be removed to prevent the possibility of the gate smearing to the Si during wafer dicing and handling, thus creating an electrical short. Standard ultraviolet photolithography is used to pattern channels around each die. AZ 3312f photoresist (AZ Electronic Materials) is spin coated at 4,000 rpm with a 4 second ramp for 30 seconds and soft baked in an oven at 95 °C for 5 minutes to partially dry. A second coat of photoresist is spin coated with the same parameters and oven baked for 8 minutes. The two layer process is necessary to ensure the etch pits are completely covered and any air pockets in the pits will not escape, exposing the array to unwanted etching and debris from dicing.

The photoresist is exposed in a Karl Suss MJB4 mask aligner under 365 nm light. The exposure dose is normally about 170 mJ/cm^2, which requires a 19.5 second exposure at an energy density of 8.7 mW/cm^2. The photoresist is developed in AZ 300MIF (AZ Electronic Materials) developer for 15-30 seconds. Patterning is confirmed using OM.

The exposed p-Si around each die is removed by RIE. The standard descum process is used to remove any residual photoresist in the channels. The Vision RIE is used at 90 W and 100 mTorr with 25 sccm of SF_6 and 5 sccm of O_2 for 3 minutes to etch the p-Si. Complete etching is confirmed with OM and the reflectometer. The photoresist is left on the wafer to protect the etch pits during dicing. A picture of the wafer at this stage is shown in Figure 28.

The wafer is diced into individual die using a Kulicke and Soffa (Singapore) 982-10 dicing saw. The wafer backside is mounted on 100µm thick dicing tape so that the saw

can cut completely through the wafer. The wafer is aligned in the dicing saw and cut with a 10 μm thick diamond composite blade at 30,000 rpm with a feed rate of 2.5 in/sec.

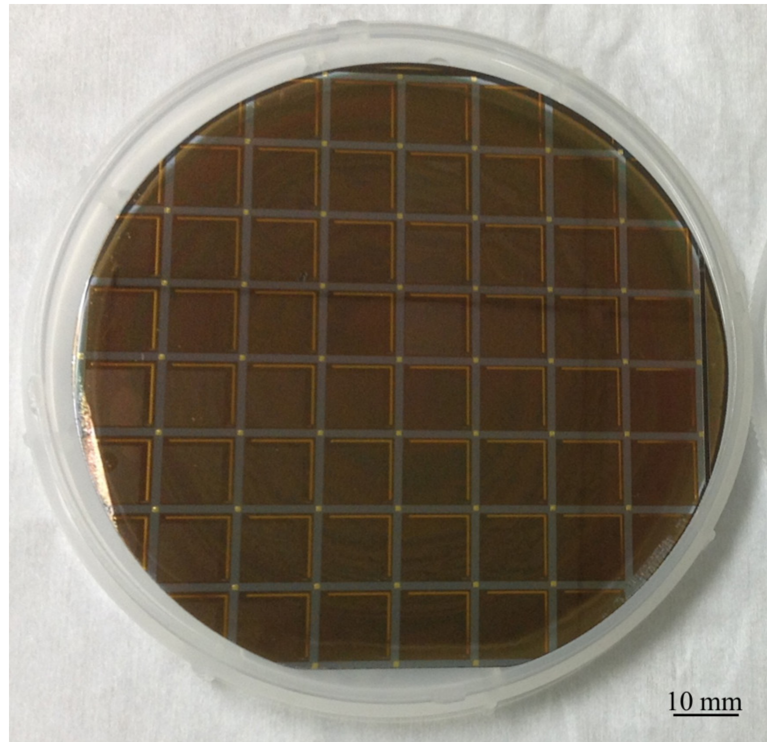


Figure 28: Picture of a 100 mm wafer with photoresist and dice channels etched.

After dicing, each chip is removed from the dicing tape and thoroughly cleaned. A solvent rinse removes most of the photoresist and debris from dicing. Chips are soaked in AZ 400T or Baker PRS 2000 photoresist stripper at ~80 °C for up to 4 hours. While in the warm photoresist stripper, the chips are sonicated to completely remove any photoresist residue. The sonication is very important because photoresist residue can remain even with soaking in the stripper. All chips are inspected by OM and separated from partial die or die with major defects. Figure 29 shows a labeled picture of a fully fabricated die that is ready for CNT synthesis.

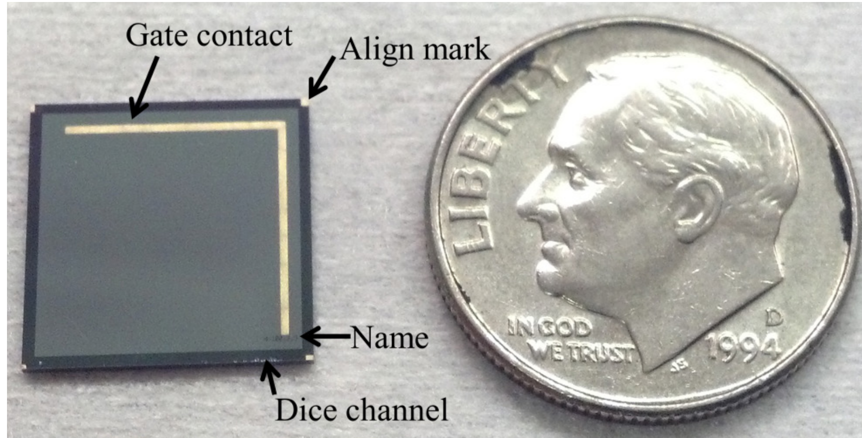


Figure 29: A fully fabricated die with components labeled. The pit array comprises a majority of the open space and is not visible.

3.2 CNT Synthesis and Oxygen Plasma Resurrection

All chips are electrically tested prior to CNT synthesis. The resistance between the Si substrate and the Au gate contact is measured with a Keithley (Cleveland, OH) 2400 sourcemeter measuring resistance up to 200 MΩ at a 21 V input. Resistance is measured by placing a chip on a piece of Al foil so that there is an electrical contact between the metallized backside of the chip and the Al foil. One contact is made with the Al foil, and other is placed on the Au gate contact. Chips are separated based on the resistance measured: shorted (<1 MΩ), high resistance (1-200 MΩ), and infinite resistance (>200 MΩ). This resistance test process is repeated throughout the assembly and testing process.

An Aixtron (Herzogenrath, Germany) Black Magic plasma enhanced CVD (PECVD) system is used for all CNT synthesis. A low pressure CVD (LPCVD) process without plasma is used for CNT synthesis [156]. The recipe heats the samples to 650 °C

at a rate of 100 °C/min under 200 sccm of N_2 and 700 sccm of H_2 at a pressure of 5 mbar. The catalyst is annealed at 650 °C for 15 minutes at 10 mbar to ensure catalyst particle formation is uniform across the wafer. Chips are then heated to 700 °C at a rate of 150 °C/min. The temperature is stabilized at 700 °C for 1 minute. C_2H_2 is introduced at 120 sccm for up to 3 minutes to grow the CNTs. Growth time is precisely tuned so that CNT close to the gate (~15 μm) is achieved. A change in growth of as little as 15 seconds can create a large change in CNT length. After growth, gas flow is suspended, heaters are turned off, and the chamber is pumped to 0.20 mbar to quickly terminate growth. The chamber is then cooled under N_2 flow until the temperature is less than 200 °C. The SEM images in Figure 30 shows that the CNT growth can be precisely controlled, remains aligned past the Si pit, and is uniform across many pits.

CNT synthesis is initially characterized with OM to determine the presence, length, and uniformity of CNTs across the now fabricated CFEA. All chips are again tested for resistance using the 2400 sourcemeter. The same separations are made for shorted (<1 MΩ), high resistance (1-200 MΩ), and infinite resistance (>200 MΩ) chips. Chips that have an infinite resistance are ready for packaging after SEM analysis to confirm CNTs. Chips that have a lower resistance are analyzed by SEM to determine CNT quality. A Hitachi (Tokyo, Japan) S4700 SEM is used for all analysis. CNT growth time is adjusted based on the SEM results.

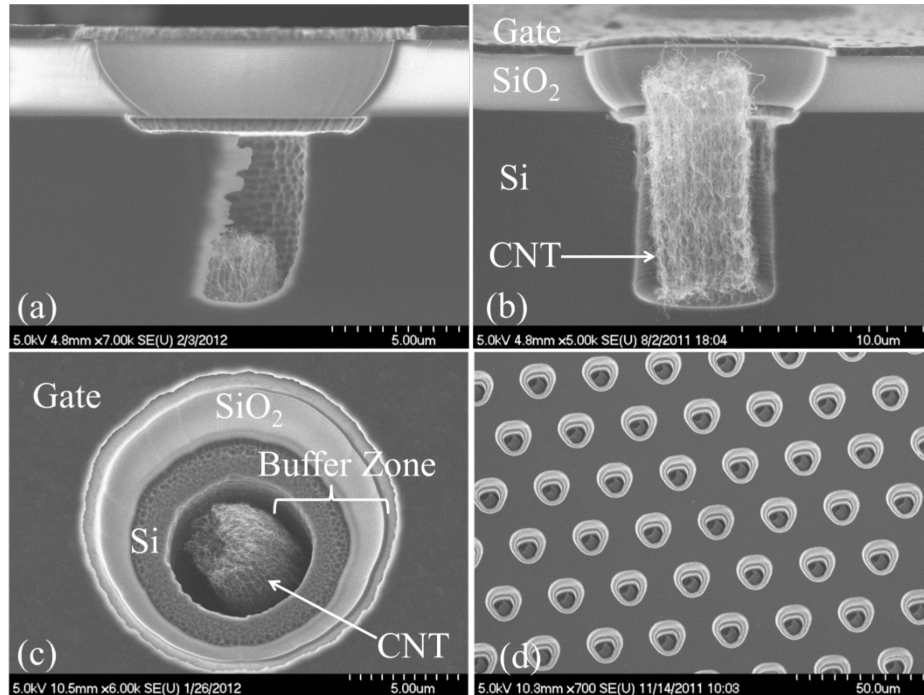


Figure 30: SEM of CNT synthesis. Cross section image for (a) 20 seconds and (b) 60 seconds of CNT growth. A 15° angle view of (c) a single etch pit showing the buffer zone between CNTs and gate, and (d) relative uniformity across many pits.

Chips that have good CNT growth confirmed by SEM but don't have an infinite resistance are treated to an oxygen plasma "resurrection" etch. This step is similar to a standard descum process. The Vision RIE is used at 50 W and 60 mTorr with 50 sccm of O_2 for up to 3 minutes. Chips are placed on a glass slide to prevent a bias and arcing between the gate and substrate in the plasma. An image of a sample before and after etching in Figure 31 shows the minimal morphological effect on the CNTs. Chip resistance is measured after each minute of etching as care is taken not to etch more than necessary because the process etches the CNTs. After etching, if the chip measures an infinite resistance and CNTs are again confirmed by SEM, then the chip is ready for packaging.

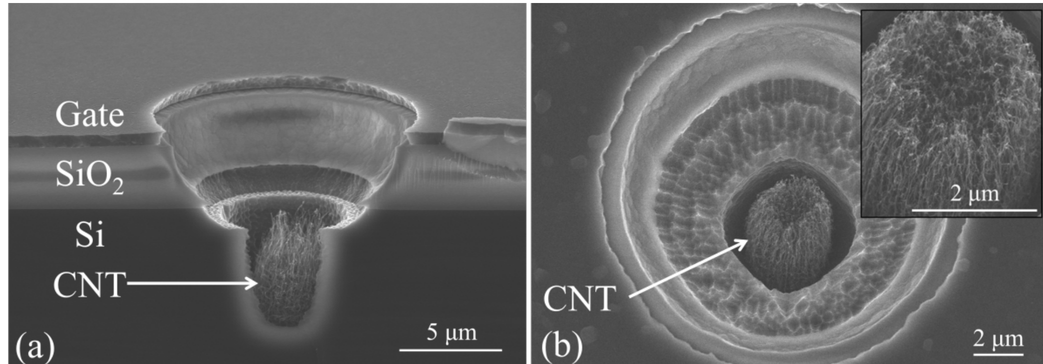


Figure 31: SEM images of CFEA etch pits. Image of the same CFEA (a) before plasma etching and (b) after a 75 second etch with magnification of CNTs inset.

3.3 Electronic Assembly

3.3.1 Electronic Package

An electronic package is used as a platform to make high quality electrical connections to the CFEA, and to be easily inserted and removed from a circuit board. A Kyocera plug in hybrid bathtub type package (PB125125EC122) from Chelsea Technology Inc. is used. It has 24 pins, is gold plated, and has an ASTM F-15 alloy (Kovar) body that is electrically isolated from the pins. A schematic of the package is shown in Figure 32.

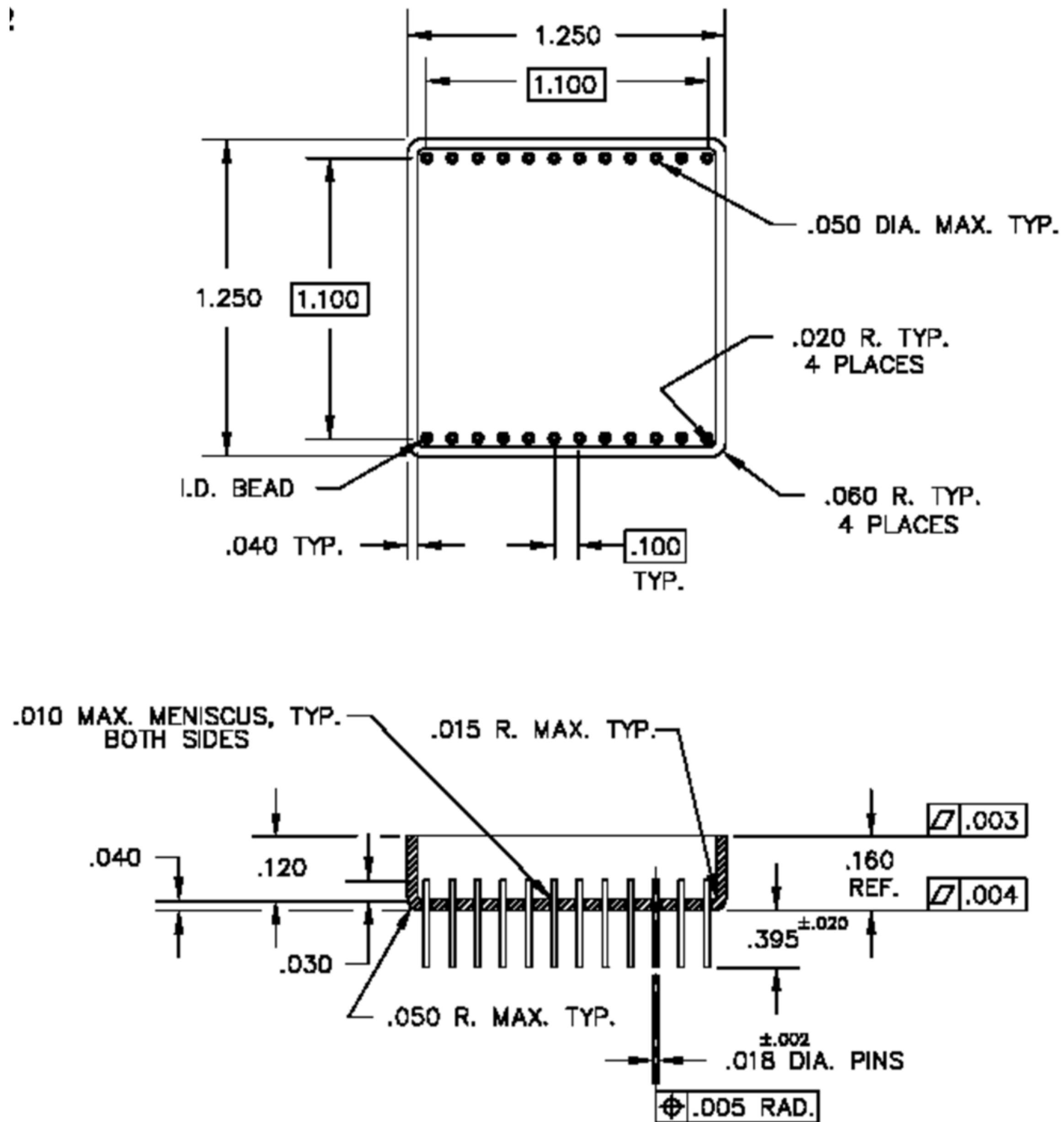


Figure 32: CAD schematic of the whole electronic package. Units are in inches.

Since the package is large enough to comfortably fit four CFEA chips, the package is cut in half to be more economical and so that more chips are able to be independently tested. A custom made Teflon holder surrounds and protects the pins during cutting. A picture of the cut package is shown in Figure 33. The package pins are also cut to about half their original length so that the package fits flush against sockets in the circuit board. A Teflon guide that fits over the pins against the package body is used. The remaining part of the pin protruding from the guide is cut, allowing all the pins and packages to have uniformly cut pins.

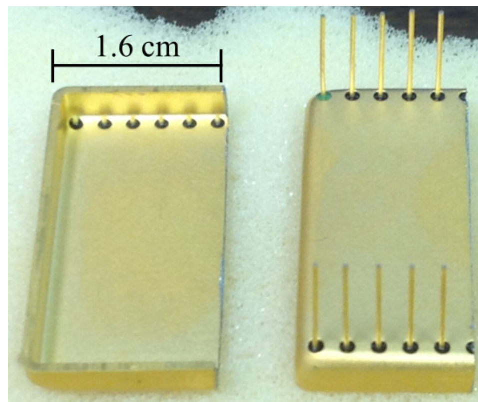


Figure 33: Top (left) and bottom (right) view of the electronic package cut in half.

3.3.2 Chip Mount and Wire Bonding

The CFEA chip is mounted to the cut package with Ablebond 84-1LMI heat cure silver epoxy. This epoxy provides a secure connection that is thermally and electrically conductive. It serves as the electrical connection from the metallized silicon backside to the package body. A small amount of the epoxy is applied to the package and the chip is

massaged into the epoxy, then the entire package is heat cured in a 150 °C oven for 1 hour.

Au wire bonds are used to make high quality electrical connections between the package pins and the CFEA. Wedge type wire bonds are applied at 150 °C with 300 W ultrasonic power and 32 g of force. Each chip has three redundant contacts for the gate and cathode (Si wafer) contacts, utilizing all 6 pins on one side of the package. The gate bonds are made directly between the gate contact line and three of the pins. The cathode bonds are made between the package body adjacent to the pin and the 3 remaining pins, completing the electrical connection through the backside of the chip. A picture and SEM image of the mounting and wire bonding is shown in Figure 34. Electrical resistance is measured through each pin to confirm the chip is an open circuit and that each wire bond has low resistance connections.

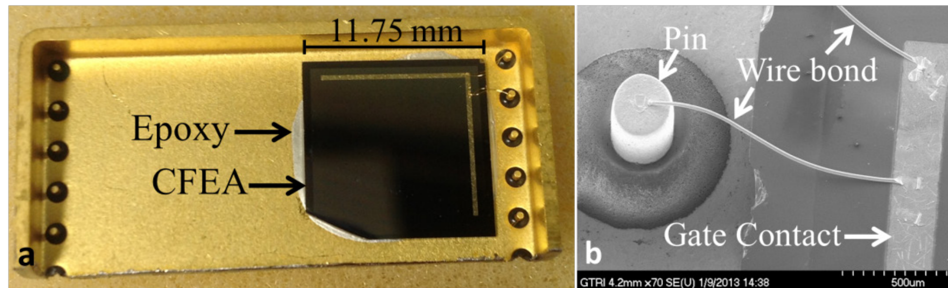


Figure 34: (a) Picture of a CFEA chip bonded to a package with the two top right pins wire bonded to the gate. (b) SEM image of a wire bond between a pin and the gate.

3.3.3 Circuit Board

A custom circuit board was designed in house and made by Innovative Circuits, Inc. The boards are made of Kapton for vacuum compatibility and high temperature

resistance. Au pads under each package, shown as the squares in Figure 35, are incorporated so that it would be possible to incorporate heat sinks that contact the back of the packages to the circuit board in future uses. The entire backside of the board is gold plated as a common ground and heat sink. The board was designed such that each cut package has three gate and three cathode pin connections on each end, following the wire bonding. The gate connections are all common because the gate is the ground in the electrical test circuit. Each individual package has an independent cathode line so that current from each package can be measured, even during testing of all packages at once. Each board is designed to hold 20 packages, with each cathode line going to a DB-25 connection on the tab of the board.

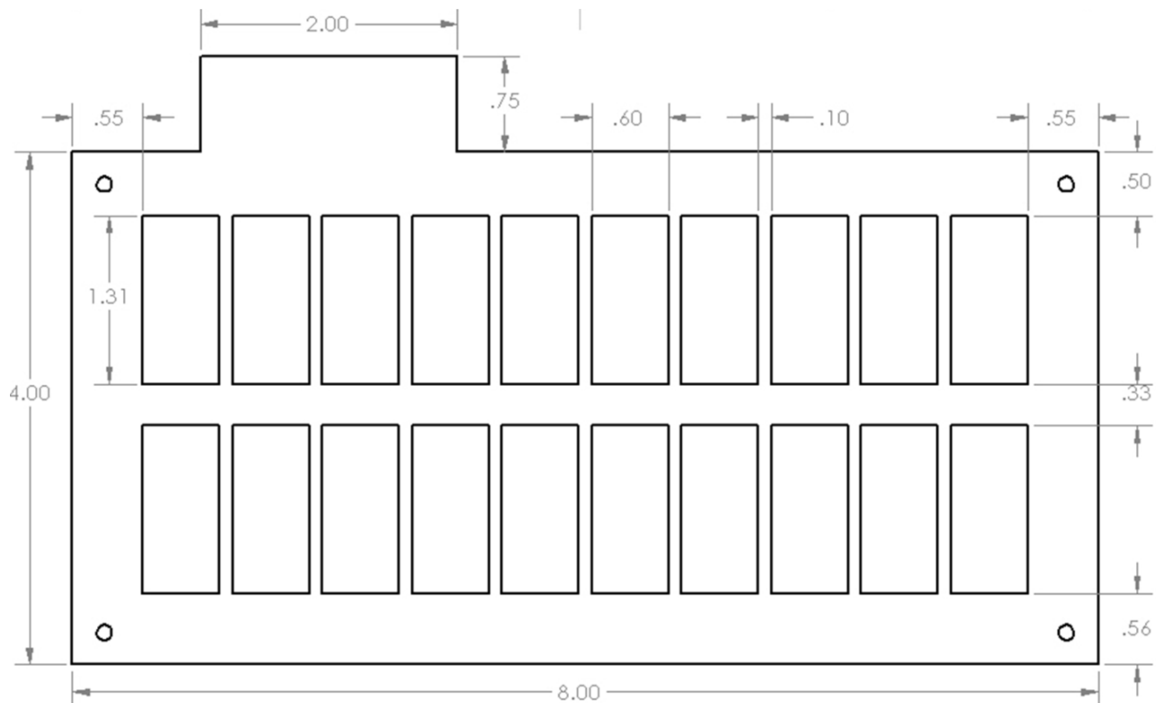


Figure 35: Schematic of the top of the circuit board with units in inches. Each square is a Au pad where each package will be placed.

Sockets and DB-25 connectors are soldered on to the board with Sn/Ag/Cu (96.5/3.0/0.5) lead free solder from Digi-Key (SMDSWLF.031). Lead free was chosen for the higher melting temperature (221 °C) and vacuum compatibility (lead has a relatively high vapor pressure at elevated temperatures). Andon sockets, shown soldered on the circuit board in Figure 36, are type 303 series, snappable, and with high temperature insulator (303-012-01S-R27-Y10). A picture of the top and bottom of the board with sockets soldered is shown in Figure 36.

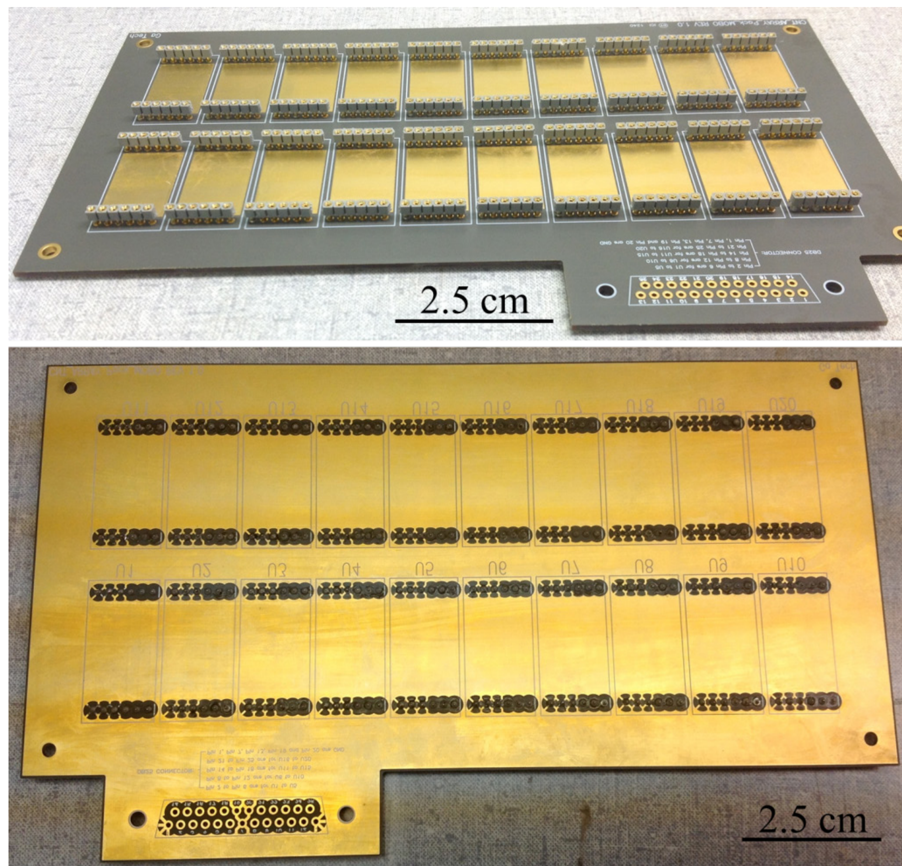


Figure 36: Picture of the top (upper) and bottom of the circuit board with sockets soldered on.

The packages are carefully inserted into the sockets on the circuit boards. Careful attention must be made to insert the packages level without touching the chips or wire bonds. After board assembly, another electrical resistance test is made to confirm independent contacts and open circuit CFEAs. During package cutting, the pins were cut too short, causing them to be able to be pushed too far into the sockets, and create an electrical short between the socket and package body. Simply shifting the package up slightly removes this electrical short. A picture of a fully assembled circuit board with a G-10 clamp over it is shown in Figure 37. At this stage, the circuit board, electronic package, and CFEA assembly is ready to be integrated with a test apparatus for FE testing.

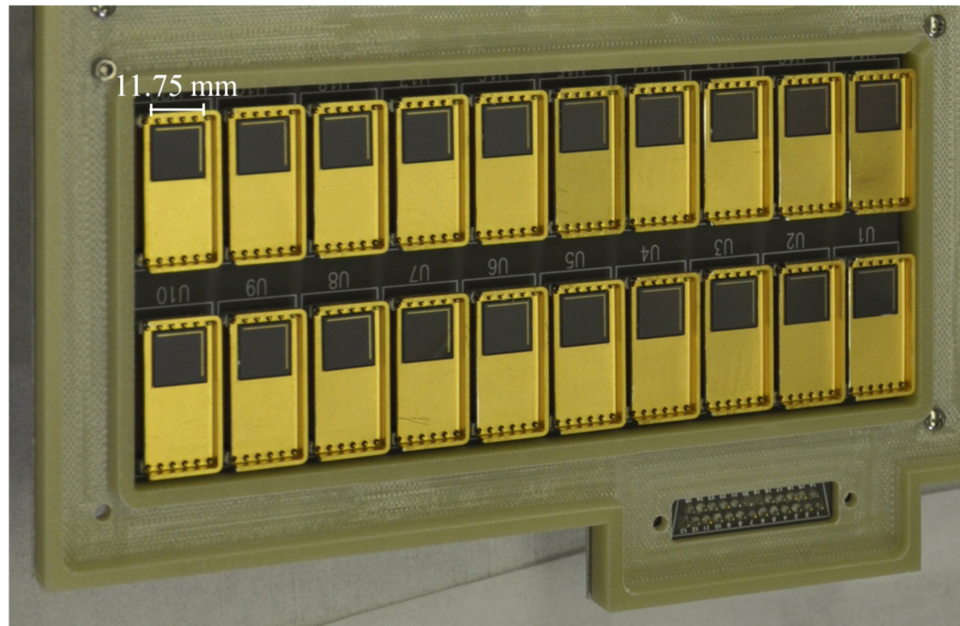


Figure 37: A fully assembled circuit board with 20 packages, each containing one CFEA, and a G-10 clamp around the edges of the board.

3.4 Characterization Techniques

3.4.1 Field Emission Test Apparatus

A variety of methods are used to test field emission for this dissertation, however all tests use the same basic electrical setup shown in Figure 38. The anode, normally an aluminum plate, is physically separated a few cm from the CFEA and biased positively anywhere from 25-100 V to attract electrons. The gate is always grounded in the circuit, which allows for there to be a constant potential difference between the gate and anode as FE is tested. The cathode (Si wafer and CNTs) controls the FE test by biasing negatively 100-300 V to create the electric field between the CNTs and gate to cause FE. Current can be independently measured on the gate, cathode, and anode to inform where emitted electrons or leakage current is and the percentage of current that reaches the anode. The only time the electrical setup in Figure 38 is not used is for the HET exposure test, which is detailed in Section 3.5.

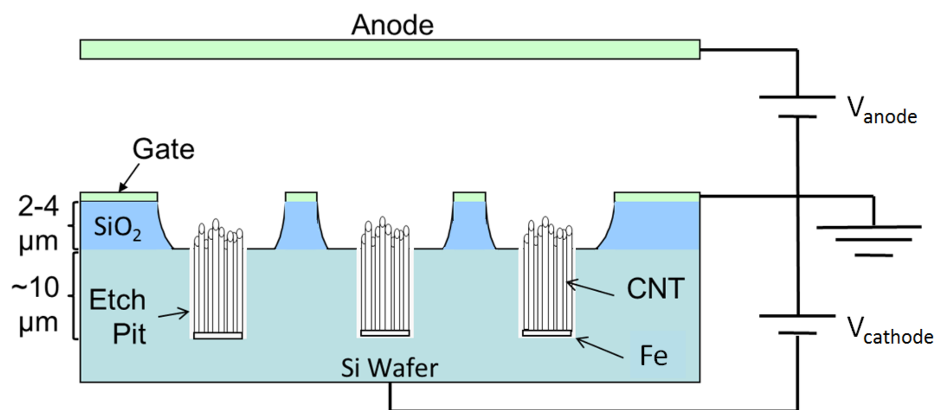


Figure 38: Electrical schematic for all field emission testing on the CFEAs showing the gate grounded, anode biased positively, and the CNTs (cathode) biased negatively.

FE testing is conducted in collaboration with the Georgia Tech High Power Electric Propulsion Laboratory (HPEPL) or the Air Force Institute of Technology (AFIT), who have the test facilities, electrical equipment and expertise for FE testing. The FE testing conducted at AFIT was on a limited basis and conducted in a different electrical assembly, the details of which are in Section 3.6.

The most basic FE test can be conducted on a single chip in a package. Contacts must be made through the package to the gate and cathode, and an anode can be placed above the package. The entire setup must be placed into a vacuum chamber, and connected to source meters or power sources through feedthroughs. Since this setup is only able to test one CFEA at a time, it is generally only used as an initial test of a CFEA or apparatus design.

Cathode Array Apparatus

The circuit boards were developed to be able to test many CFEAs individually for a single chamber pump down, or to test emission on many CFEAs simultaneously. A complete mount apparatus was designed with HPEPL to incorporate 4 circuit boards, which is able to independently test up to 80 packages at once. This apparatus is termed the “cathode array”. The cathode array is designed to fit a BHT-200 HET in its center and to be compatible with exposure to an electric propulsion plasma for the HET exposure test described in Section 3.5.

The cathode array performs the function of a mechanical and electrical integration point for the CFEAs on electrical packages. The cathode array provides rigid but non-permanent electrical and mechanical connections. For the HET testing, the array must

also be capable of surviving plasma conditions, provide a thermally isolated mechanical connection between the circuit boards and HET, and be light enough to not require additional support when fixed to the HET.

At the center of the cathode array are four circuit boards arranged in a square (Figure 39). Each circuit board provides a connection from the 20 packages to a DB-25 male connector located on the bottom of the board. The size and shape of the boards reduces the cost of fabrication over a single large board and reduces the cost of circuit board failure by allowing a single quadrant to be replaced.

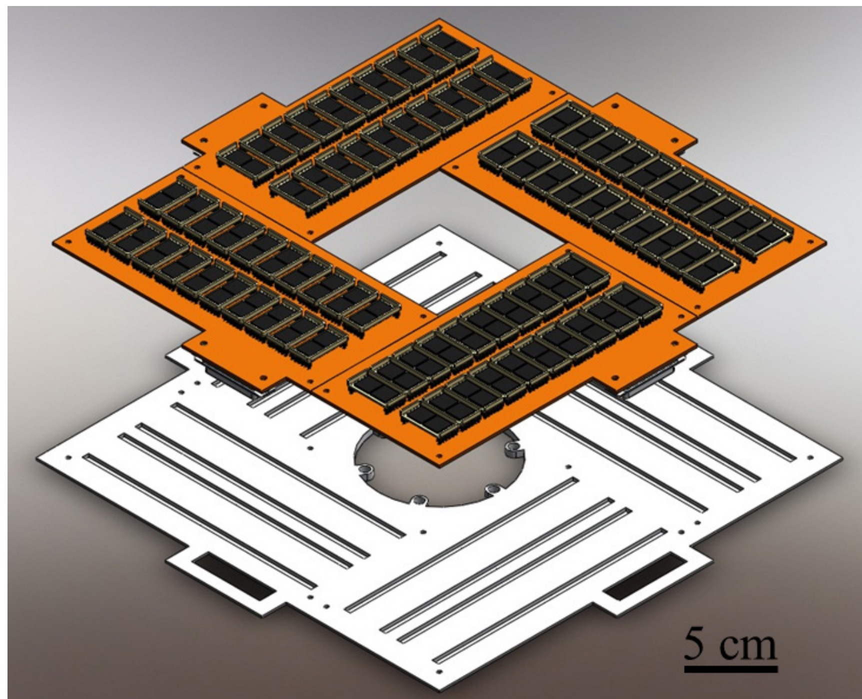


Figure 39: The back plate (white) and 4 package filled circuit boards arranged in a square. The grooves in the back plate line up with the socket solder connections on the back of the boards.

A back plate, shown in white in Figure 39, sits under the circuit boards as the structural foundation of the cathode array, electrical contact for the ground plane on the back of the boards, and a heat sink. It is machined from 3/16” Aluminum 6061, and its outer dimensions are 14 x 14”. Channels are cut into the top side of the back plate to prevent the socket solder connections on the circuit boards from contacting the back plate. The reverse side of the back plate is machined and thinned in between the channels to reduce the weight of the plate, and anodized to insulate it from plasma during the HET test.

A board clamp is used to rigidly fasten the circuit boards to the back plate, which also maintains electrical contact between the ground plane on the circuit boards and the back plate (Figure 40). The installed board clamp preserves easy access to the packages and acts as a spacer between the front shield and the sockets and packages, which are raised up from the circuit boards. The board clamp is machined from 3/8” G-10 (also known as FR4) fiberglass, which is a rigid and light weight electrical insulator. Most of the top side of the board clamp is hollowed out to reduce its mass, and vent holes are installed in the corners of the circuit board openings to vent trapped air during pump down.

For FE testing, no other cathode array components are necessary, but for the HET exposure test the circuit boards require additional protection. A front shield, shown in white in Figure 41, protects the circuit boards from the plasma environment and only exposes the packages. It is machined from 1/16” Aluminum 6061 and is anodized so that its surface is electrically insulating and will not interact with plasma.

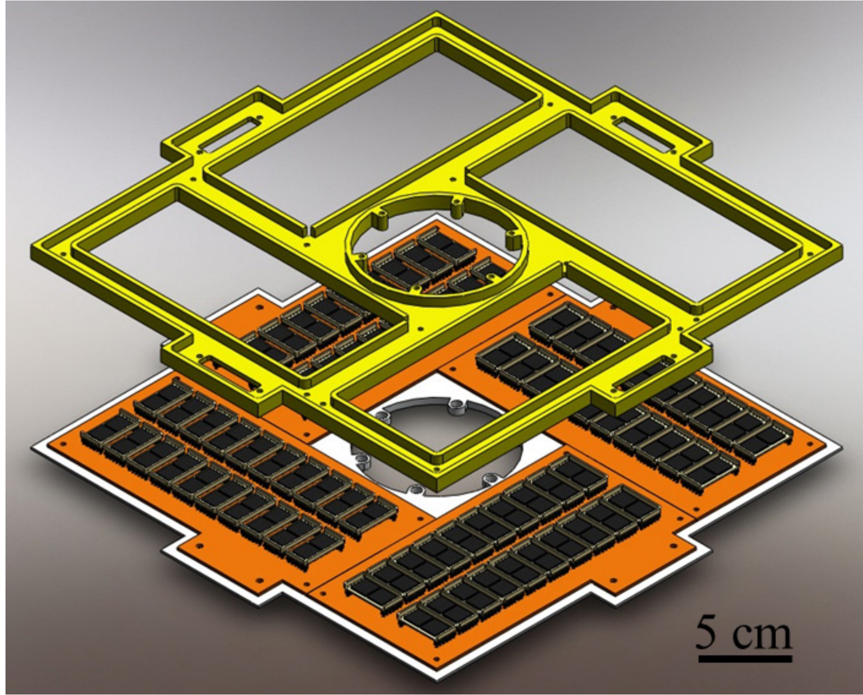


Figure 40: The board clamp (yellow) above the circuit boards on the back plate.

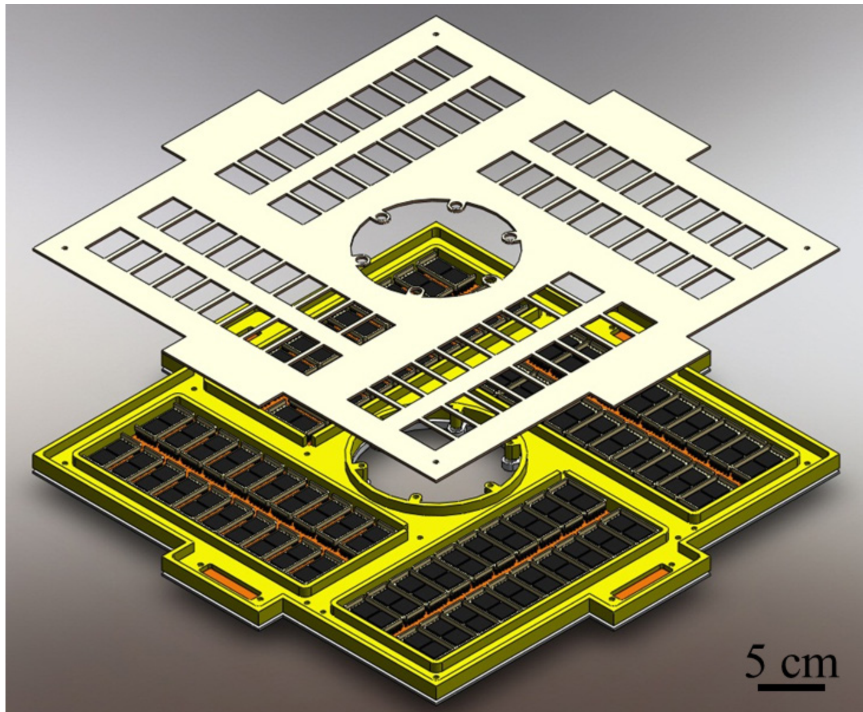


Figure 41: The front shield (white) above the assembled board clamp, circuit boards, and back plate.

The front shield comprises the last major component of the cathode array. However, a few additional parts are needed. Four hex supports that attach to the bottom of the back plate raise up the cathode array so that it does not rest on the DB-25 connections. These supports make the array easier to handle during installation and removal of packages. To thermally and electrically isolate the BHT-200 HET from the cathode array, alumina spacers are installed above and below the connection points to the array. Figure 42 shows an exploded view of the full cathode array apparatus with a HET, and Figure 43 shows pictures of the array with and without the front shield.

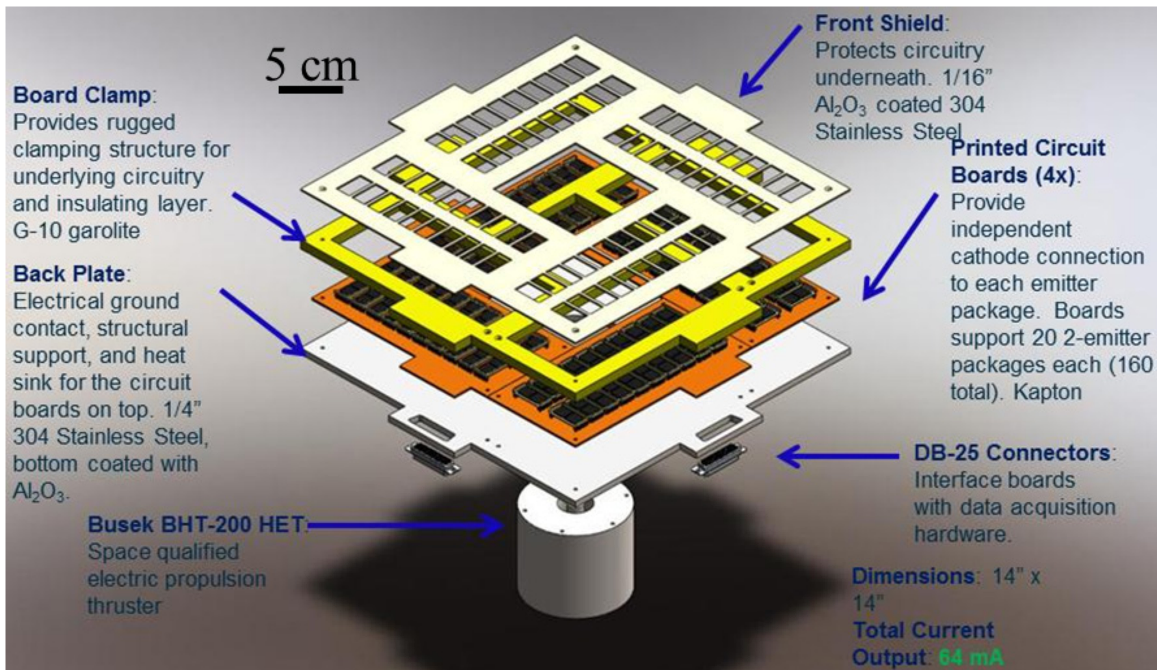


Figure 42: An expanded and labeled view of the full cathode array with a HET.

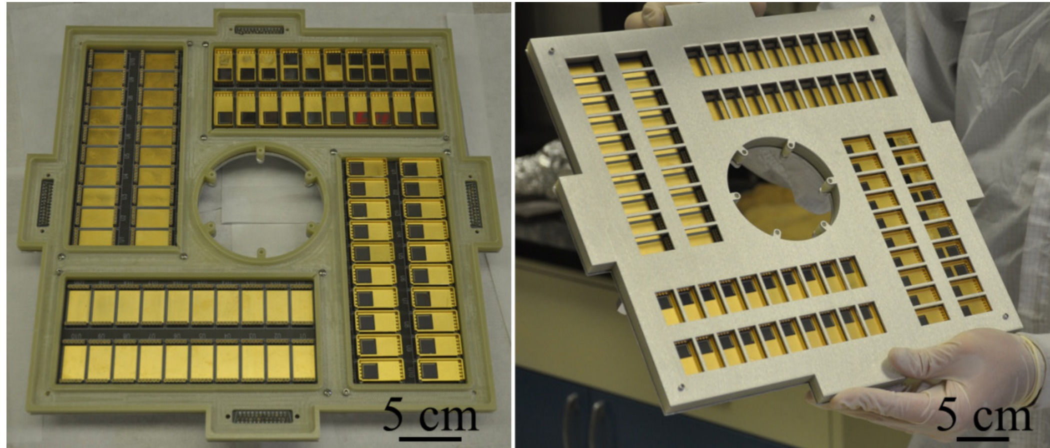


Figure 43: Picture of the cathode array that has partially filled circuit boards with (right) and without (left) the front shield.

3.4.2 Experimental Setup

FE testing was conducted at the Bell Jar 2 facility at the Georgia Tech HPEPL. The facility is a 0.5 m diameter by 0.7 m tall stainless steel chamber, evacuated by a CVC PMC-4B diffusion pump with a pump rate of 700 l/s. An Adixen 2021-SD rotary vane pump with a pump rate of 6.9 l/s backs the diffusion pump. A Bayard Alpert 571 ion gauge in connection with a SenTorr ion gauge controller monitors chamber pressure. It is able to achieve a minimum base pressure of 3×10^{-7} Torr.

Figure 44 is an electrical schematic of the system used for FE testing, designed to be able to test a fully loaded cathode array with 80 packages. Since the fully loaded array requires 82 independent channels (80 cathode, 1 gate, and 1 anode), the system has several integrating components.

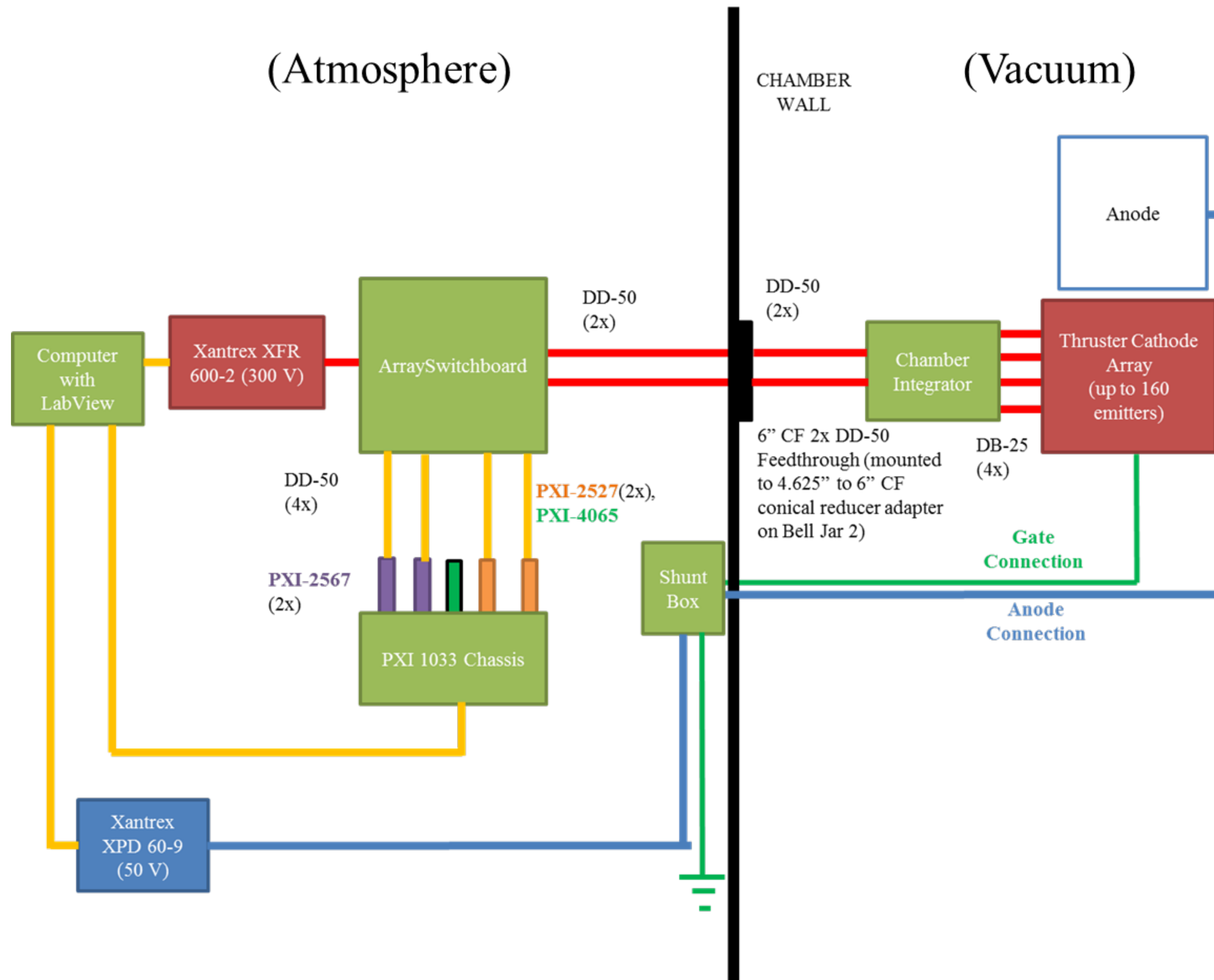


Figure 44: An electrical schematic of the FE test setup with the cathode array at the HPEPL Bell Jar 2 facility.

One DB-25 cable connects to each of the four independent circuit boards from the cathode array to a circuit board located inside the chamber, termed the "chamber integrator", where they are integrated into two DD-50 cables for transmission through the vacuum chamber. The chamber integrator, shown in Figure 45, is protected within a G-10 enclosure to improve its ruggedness and protect it from a plasma environment. The cables are integrated into two DD-50 cables to be compatible with a 6" CF 2 x DD-50 feedthrough on the bell jar.

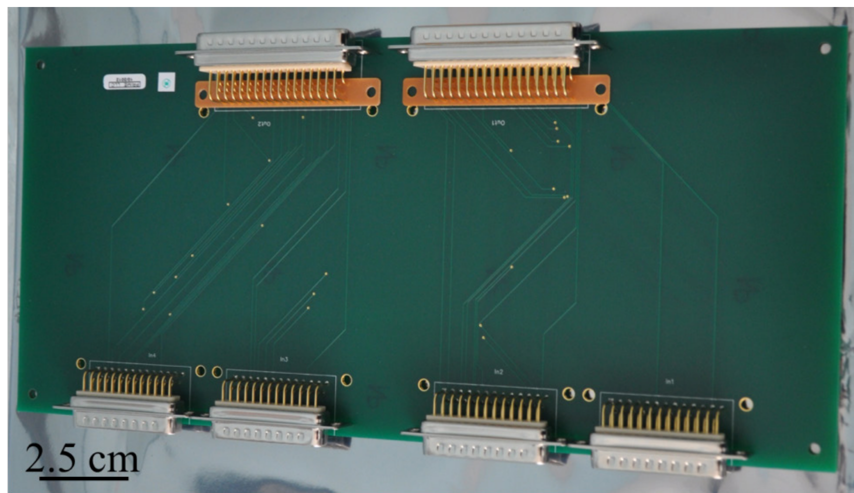


Figure 45: The chamber integrator circuit board integrates 4 DB-25 cables from the bottom into 2 DD-50 cables at the top.

Two DD-50 cables from the chamber feedthrough lead to a circuit board, termed the "array switchboard", which controls the power to each channel in the cables (Figure 46). The array switchboard consists of an array of electronic switches to control the power to each package inside the chamber. This allows the power to be automatically or manually turned ON or OFF to a package at any time during a FE test. Each switch is

controlled by connection to a NI PXI-2567 64-channel external relay driver card through two DD-50 cables. The array switchboard also contains current shunts across each channel which allows the cathode current of each package to be independently measured by measuring the voltage drop across the resistor. This data is measured via two DD-50 cables to two PXI-2527 64-channel (1 wire) multiplexer switches. The multiplexer switches then connect to a PXI-4065 digital multimeter. A PXI-1033 unit provides a control interface between a LabView program and the switches and multiplexers. The multiplexers communicate via the PXI-1033 bus with a NI PXI-4065 digital multimeter.

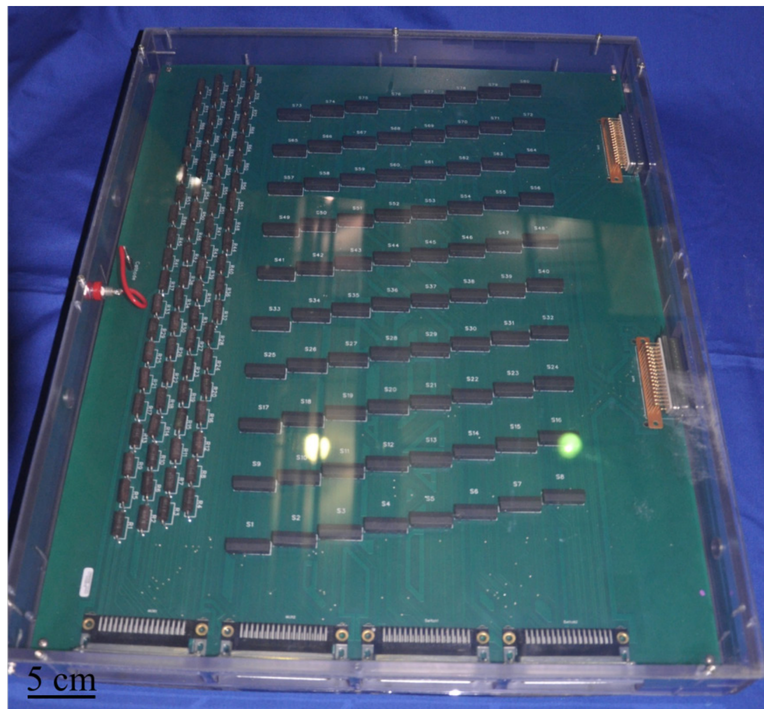


Figure 46: The array switchboard, which contains electronic switches for power and current shunts for each of the 80 channels to the cathode array packages.

The cathode array is biased up to -300 V via a Xantrex XFR 600-2 DC programmable power supply controlled via GPIB by LabView. In this configuration, all "ON" cathode channels are biased to the same potential. The cathode power supply connects to the Array Switchboard with a banana jack input connection. The anode is biased to a constant +50 V via a Xantrex XPD 60-9 DC programmable power supply controlled via GPIB by LabView. A current shunt box passes the gate (ground) and anode channels through resistors to determine current through the voltage drop. The current shunts connect to an Agilent 34970a DAQ connected via GPIB to LabView.

A LabView program virtual instrument (VI) consists of an interface for actuating the switches automatically (all at once) and manually (Figure 47). The interface has entries for cathode potential, cathode current, gate current, anode potential, and anode current. Most of the interface consists of indicators for each switch, each of which has a cathode current readout, an indicator for switch state, and a toggle to manually actuate the switch. Pressure measurement through a SenTorr ionization gauge control head is included on the interface, connected via RS-232. Cathode current, gate current, anode current, and pressure are automatically saved to .xls files. All channels can be sampled as few as once every three seconds.

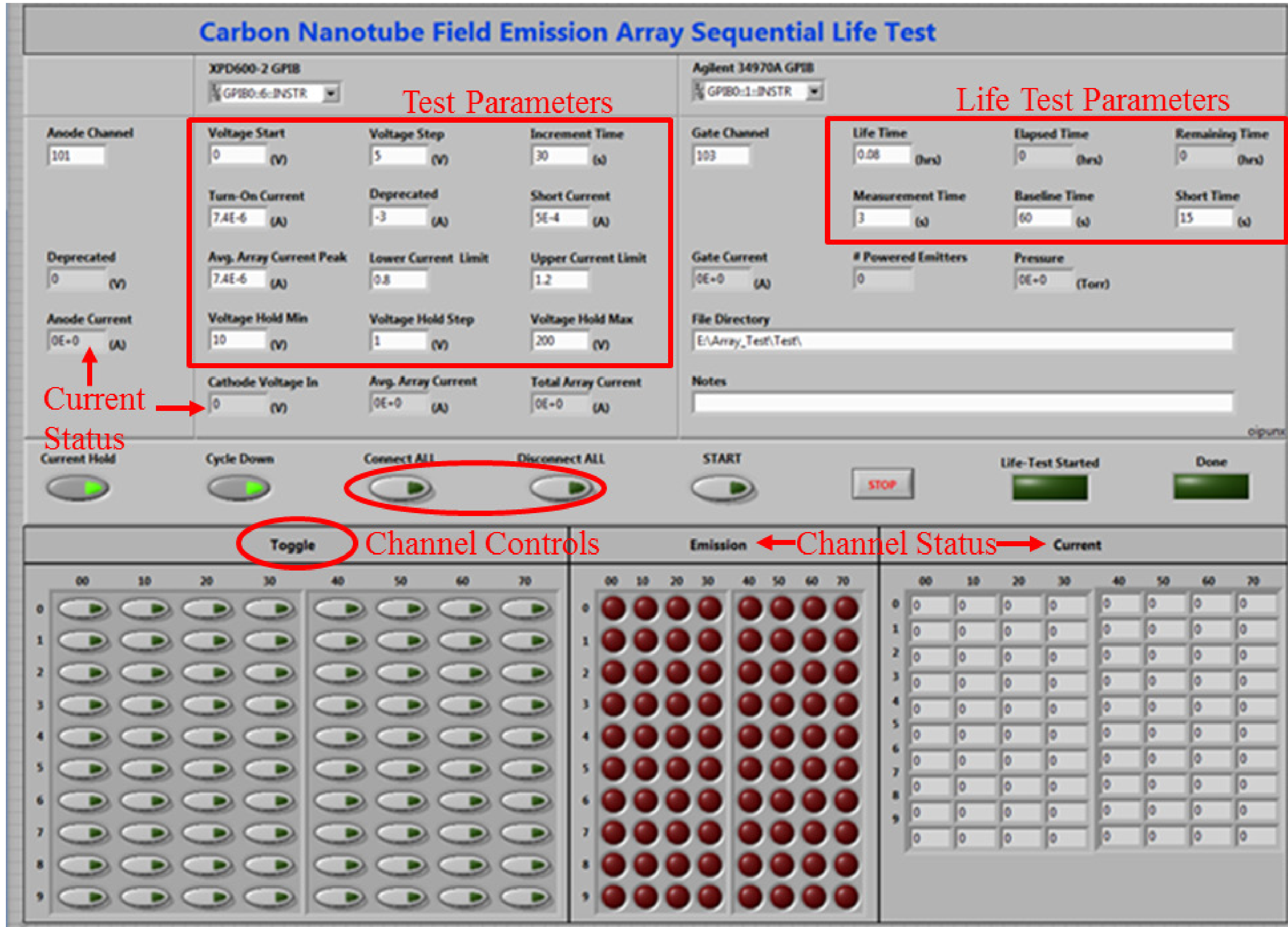


Figure 47: The LabView VI interface for FE testing of the cathode array. Areas of interest are annotated in red.

Bell Jar Mount

Since space is limited in the Bell Jar 2 facility, a mounting structure was designed to contain each component in a compact system. This bell jar mount integrates the chamber integrator circuit board, the cathode array, a UV photodesorption system, and the anode. It places each component in a tower configuration, allowing each component to utilize the entire footprint of the bell jar.

The bottom component in the mount is the chamber integrator circuit board protected within a G-10 enclosure, which rests on a stainless steel mounting plate secured to the base. Four G-10 posts provide support for a 1/16" thick G-10 plate to rest above the chamber integrator and hold the cathode array. A schematic of this mount is shown in Figure 48.

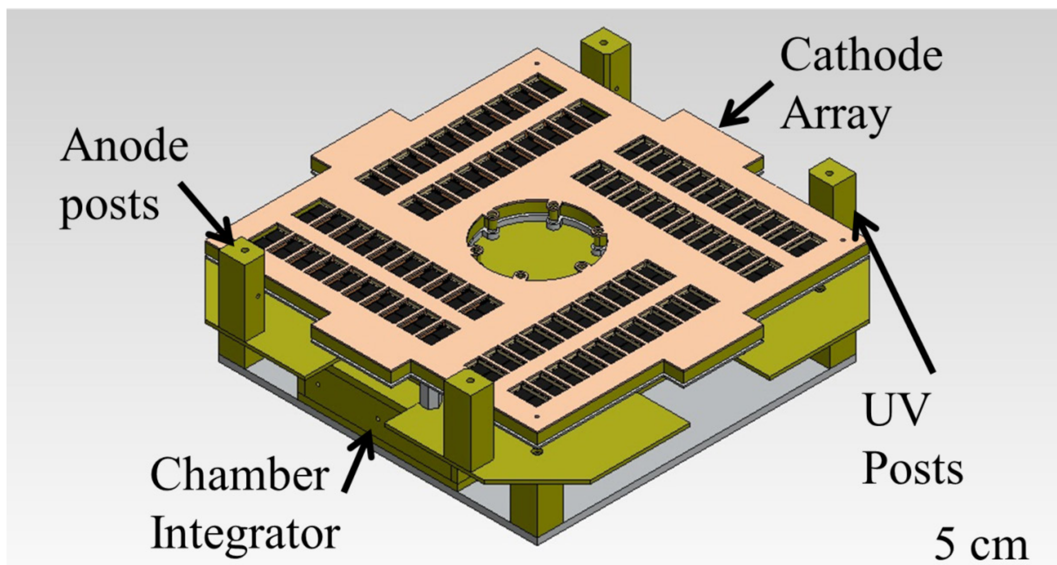


Figure 48: The Bell Jar mount showing (from bottom to top) the bottom stainless steel mounting plate, the chamber integrator circuit board in a G-10 enclosure, a G-10 plate, the cathode array, and posts for holding the UV photodesorption system and anode.

A UV photodesorption system is incorporated into the system to improve FE, pump down times, and base pressure. The literature has shown that desorption of field emitters, including CNTs, during pump down can improve FE stability and performance [119, 157]. UV lamps mounted to the side of the cathode array disperse UV light throughout the chamber and in the cathode array during pump down to desorb molecules, mainly moisture, trapped in the chamber. The lamp is cycled on and off several times during pump down to prevent overheating of the lamp. This system is a pragmatic alternative to desorption by heating, because the complex mount and cathode array would have to incorporate materials and thermal management for high temperatures and cooling.

The UV photodesorption system is mounted on two posts located on one side of the cathode array. The UV bulb is secured electrically and mechanically at one end via four custom aluminum screw connectors. At the other end, the UV bulb rests on a support which is fastened to another post. A side view of the mount in Figure 49 shows the UV system. Two posts on the other side of the cathode array provide support for the anode electrode, which completes the top of the setup. The anode is a 1/16” thick Aluminum 6061 mirror finish plate. The anode side facing the cathode array is mirror finished to reflect the UV light into the cathode array and CFEAs to improve photodesorption. The fully assembled bell jar mount is shown in Figure 50.

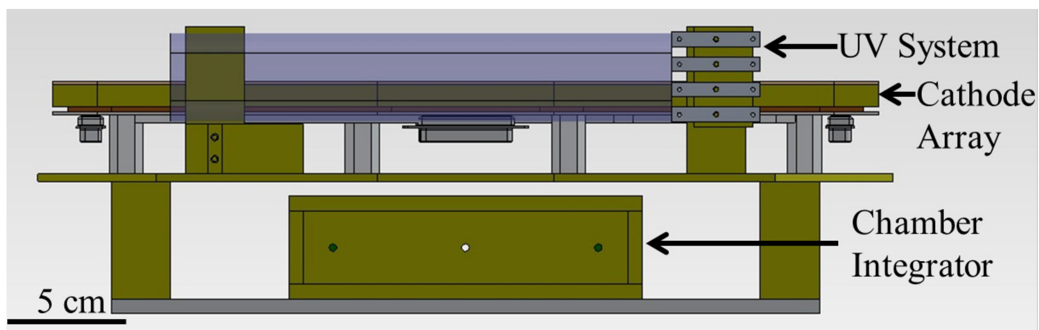


Figure 49: A side view of the bell jar mount showing the UV photodesorption system (lamps are transparent blue), cathode array, and chamber integrator.

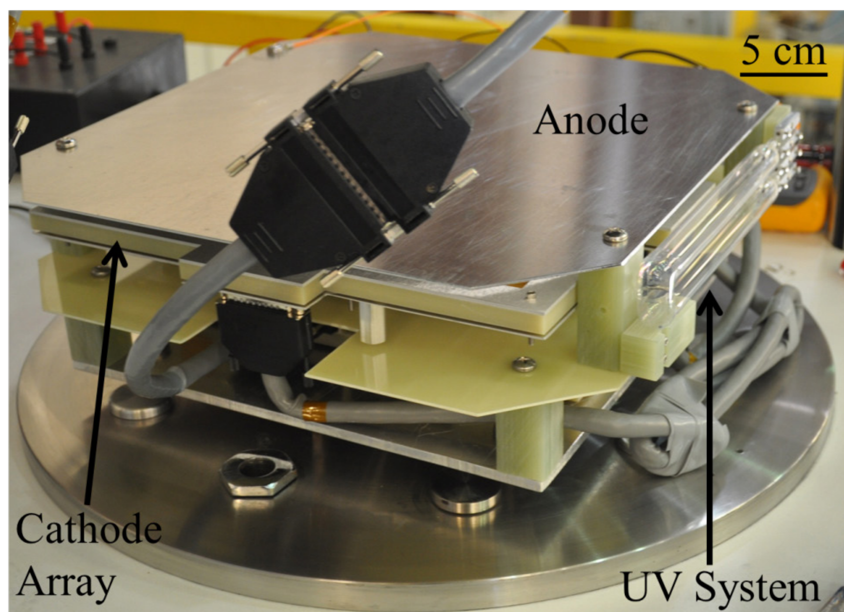


Figure 50: The fully assembled bell jar mount showing the anode, UV photodesorption system, and cathode array.

3.4.3 Characterization Procedures

A majority of FE testing was conducted in collaboration with the HPEPL at Georgia Tech. All testing was conducted at vacuums of at least 1 x 10^{-6} Torr. FE testing with the cathode array used the UV photodesorption system to remove moisture, and enabled test pressures as low as 3 x 10^{-7} Torr.

The LabView VI, introduced in Section 3.4.2, enables extensive flexibility in FE testing. For cathode voltage sweeps, it enables control over the initial and final voltage, the voltage step size and time, and the hold time at the maximum voltage before sweeping down. During a sustained emission test, the VI can run in voltage controlled or emission current controlled mode. Thus, in current controlled mode, the cathode voltage is automatically changed to maintain a constant current. This testing mode is favorable for variable or slowly changing emission performance.

The VI also allows automatic termination of testing due to specified low or high emission current conditions. For the low emission condition, if the emission is below a specified threshold current at a maximum voltage, then emission is assumed to have degraded and the test will terminate. For the high emission condition, if the emission is above a specified threshold current at a minimum voltage, then an electrical short is assumed (causing an unrealistic current) and the test will terminate. For both of these cases, a time period for the failure condition can be specified before the test is terminated.

All CFEA chips undergo an initial characterization FE test to determine performance. This test is a quick voltage sweep with a ~5 minute hold at either the maximum voltage or, in current controlled mode, once the emission reaches the specified current. After the ~5 minute hold the voltage step goes back down. Typical

characterization parameters include: initial voltage 0 V, maximum voltage 200 V, voltage step 5 V, step time 15 seconds, current hold time 300 seconds, current hold set 7.4 μA (which is E_{to}, 10 μA/cm^2). The characterization process can also help to remove any adsorbed gas molecules or impurities from the CNT that can cause instabilities in the emission. This need for conditioning CNT field emitters is commonly cited in the literature, although the procedure and understood purpose varies [2, 130, 158-160].

After successful characterization, subsequent characterizations may be run with different parameters, such as higher voltages or emission current set points. Often a lifetime test is conducted after initial characterization to determine performance degradation. This test can be considered an extended voltage sweep with similar ramp parameters. However, the maximum voltage, or current setpoint (for current controlled mode) is maintained for an extended period of time, often until failure.

The VI and experimental setup allows for simultaneous FE testing of up to 80 CFEAs. In this setup, all CFEAs are tested at the same cathode voltage, cumulative anode and gate currents are recorded, and individual cathode currents are recorded. The same type of characterization or lifetime emission tests can be conducted with multiple CFEAs. Individual CFEAs can be turned on or off during testing depending on the specified failure conditions so that the test can continue if single CFEAs fail. The full FE test procedure can be found in Appendix A.

Electrical Burnout

The inconsistent performance of the CFEA chips often resulted in electrical shorting ranging from 10-10^7 Ω. A "burnout" technique was developed during FE testing to reverse electrical shorting after a FE test. This technique can be conducted in air or

vacuum. The vacuum technique is preferred because it can be performed within the test chamber and prevents the possibility of arcing. A voltage limited current is manually applied to the CFEAs with a reverse bias to prevent FE (cathode positively biased). The voltage limit is slowly increased (up to 250V) until a current spike occurs, shortly followed by a drop in current. This current drop embodies an increase in resistance and a burnout of the electrical short. For the burnout in air, the procedure is the same, however a maximum of only 20-30 V can be applied. This limitation is necessary as it prevents the possibility of arcing due to dielectric breakdown in the small 2-3 μm gate-to-CNT air gap [101].

Infrared Imaging

An infrared (IR) camera test is performed to determine if a single location or emitter pit with an electrical short could be spatially located on a chip. The IR test electrically connects to a shorted CFEA and passes a current through it with a reversed polarity from FE testing, much like the burnout procedure. The gate is negatively biased and the cathode is positively biased. The CFEA must have a resistance < 10 kΩ to allow a sufficient current density to cause heating that can be picked up by the IR camera. In addition, since the IR test is run at atmospheric pressures, the potential applied during the test must not be more than 20-30 V to prevent arcing. Another complication from this test is that the resistance of a CFEA is often dynamic. The electrical current can, and often does, burn out the short and result in a higher resistance.

A preliminary IR test was conducted in a simple setup in collaboration with AFIT. An electronic package with clips to the appropriate pins is used to connect to the chip. No magnification is available on the IR camera. The current setup allows observation of

about ¼ of the chip at a time, and the package can be moved to scan across the chip. The package sits on an aluminum block that raises the pins from the ground and acts as a thermal interface to a heater at 45 °C to get a baseline on the IR camera. Voltage limited current is applied to prevent arcing and to allow the current to fluctuate with the resistance of the chip. Voltage is slowly increased to take note of current, subsequent chip resistance (which can change), and any temperature fluctuations on the CFEA.

A second IR test was conducted internally with a higher end camera. A similar setup was used, except thermal grease was applied between the Al block and heater. The system was a Quantum Focus Instruments (Vista, CA) Infrascope II. This camera can achieve up to 15x magnification for better special resolution. In addition, the camera takes an emissivity background image to zero out the temperature. This provides more accurate temperature readings across the sample.

3.5 Hall Effect Thruster Exposure Setup

The HET plasma exposure test of CFEAs in the cathode array was conducted in a dedicated thruster test facility at the HPEPL. This facility, Vacuum Test Facility 2 (VTF-2), is 9.2 meters long and 4.9 meters in diameter (Figure 51). One 3,800 CFM Oerlikon RA 5001 blower and one 495 CFM Oerlikon Sogevac SV630B rotary-vane pump evacuate the facility to moderate vacuum around 30 mTorr. To reach high-vacuum, the facility employs 10 liquid nitrogen (LN_2) cooled CVI TMI-1200i reentrant (nude) cryopumps that give the facility a nominal pumping speed of 350,000 l/s on xenon and a base pressure of 8.4 x 10^{-10} Torr; this is the highest xenon pumping speed at any University in the nation.

Figure 51: The VTF-2 vacuum facility at the Georgia Tech HPEPL with the walk-in door shown on the right.

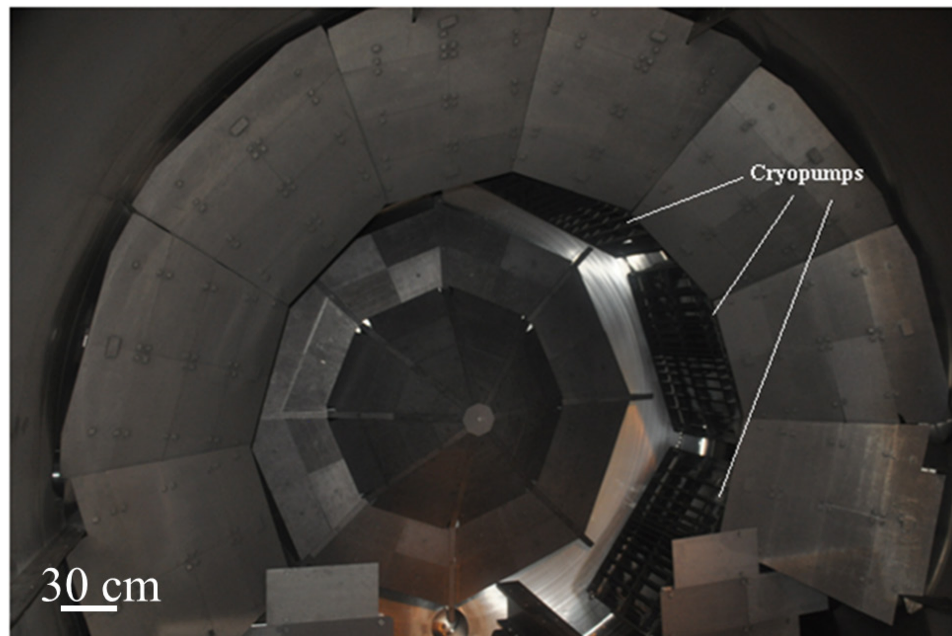


Figure 52: The graphite beam dumps and three of the ten cryopumps in VTF-2.

A Bayard Alpert 571 and UHV-24 (nude) ionization gauge connect to a Varian XGS-600 reader to measure system pressure at high vacuum. MKS Mass Flo 1179A mass flow controllers precisely control the flow of gases and propellants into the system. A camera system and viewports allow for viewing of ongoing experiments. A graphite beam dump designed in house prevents sputtering of the chamber wall and the resulting metallic coating of objects in the chamber during thruster testing. Figure 52 shows the beam dump and three of the six shielded cryopumps, which sits at the opposite end of the chamber from the door.

For economical operation, the facility utilizes a Stirling Cryogenics SPC-8 RL Special Closed-Looped Nitrogen Liquefaction System with a reservoir capacity of 1,500 liters of LN_2. A gravity feed allows phase separation of the N_2 so that LN_2 freely flows in through the supply line and gaseous waste N_2 flows out the return line. A reservoir has connections to the nitrogen loop out to the cryopumps, and to two Stirling Cryogenics SPC-4 cryogenerators capable of approximately 5.4 kW of cooling at 94 K each.

The HET test circuit, shown in Figure 53, is an integration of the cathode array circuit laid out in Figure 44 and a standard HET circuit with a hot cathode running the thruster. The discharge power supply biases the anode of the HET and establishes the floating low potential of the full system circuit. A second power supply (HET coil) supplies current to generate the magnetic field needed for HET operation. Sharing the discharge low potential with the discharge power supply for the HET, the hollow cathode heater and keeper power supplies drive the operation of the thermionic cathode. The low side of the HET circuit (discharge negative) is connected to the cathode side of the cathode array.

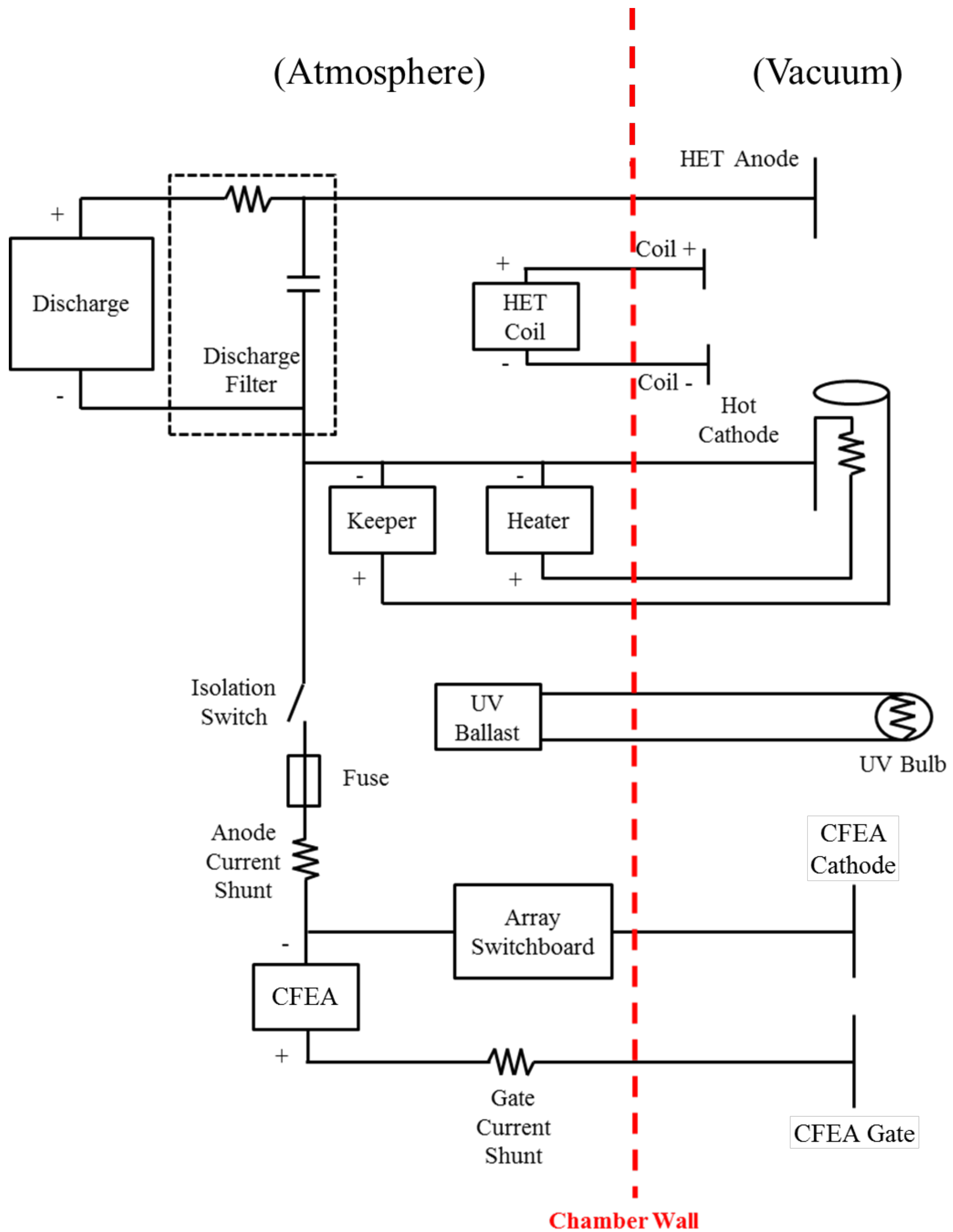


Figure 53: Schematic of the HET exposure test circuit which integrates the cathode array circuit and a standard HET circuit.

Two additional components are added to the system to guarantee HET transients in operation do not damage the cathode array or its circuitry. The first component is a normally open switch (labeled "Isolation Switch") that is only closed once the HET is operating in steady-state and the test is ready to begin. The second component is a 315 mA fuse (labeled "Fuse"), which will blow and isolate the cathode array circuit if an over current condition develops. In this circuit configuration, the gate electrode is biased positively with respect to the cathode electrodes, which float at the HET negative discharge potential. The anode of the HET serves as the anode electrode component for the triode configuration, and is biased above both the gate and cathode electrodes. Positive cathode current is defined to be electrons emitting from the electrode, whereas positive gate current is defined to be electrons arriving to the electrode. Positive anode current is defined to be electrons arriving at the anode of the HET, signified by electrons traveling from the HET sub-circuit to the CFEA sub-circuit.

3.5.1 HET Exposure Procedures

A single HET exposure test was conducted with a total thruster exposure time of 40 minutes and a biased CFEA exposure time of 8 minutes. The HET exposure test was conducted using the same equipment and electronics as the cathode array FE tests described in Section 3.4.3, so much of the testing procedures are the same. The tested cathode array consisted of a total of 41 CFEAs placed at the farthest array locations from the thruster on the circuit boards (Figure 54). Two of the CFEAs were electrically non-functional and were imaged under SEM in a repeatable way to capture the effects of the HET plasma on the same CNTs. One of these imaged CFEAs was placed at a proximal position as close as possible to the HET, and the other at a distal position from the HET.

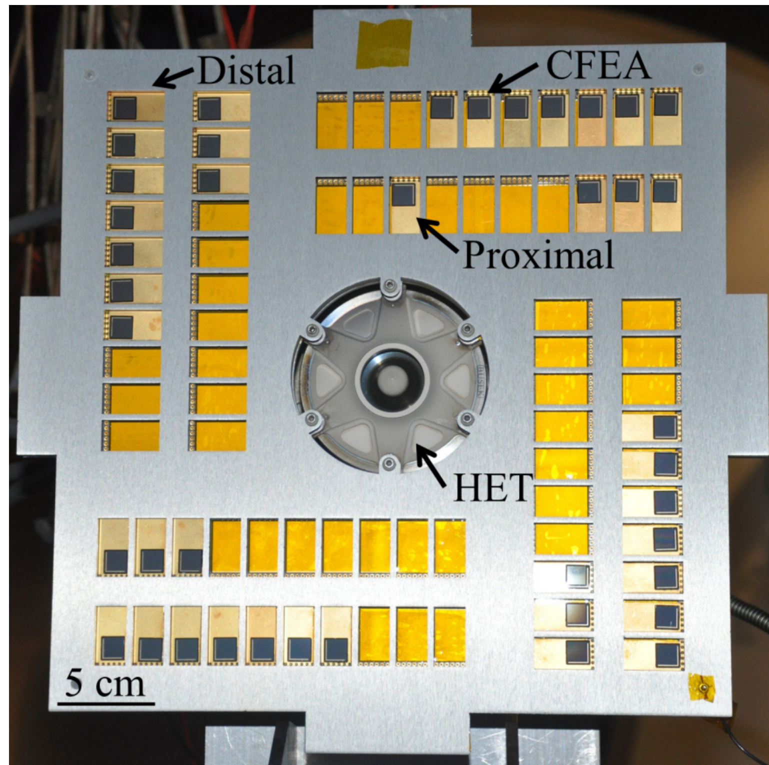


Figure 54: The cathode array loaded with 41 CFEAs for the HET exposure test and with the HET, proximal and distal CFEA labeled.

A Busek BHT-200 HET (Figure 55) is connected to the cathode array. The BHT-200 is a proven system with flight heritage on the TacSat-2 and FalconSat-5 missions and is the first US designed and manufactured HET to operate in space. Nominal performance specifications of the BHT-200 thruster include 200 W input power, 250 V discharge voltage, 800 mA discharge current, 13 mN thrust, 1,375 seconds specific impulse, and a 43% propulsive efficiency. The primary reason for using the BHT-200 is the relatively low discharge current compared to other HETs. The BHT-200 unit used is fully flight-qualified and originally had potted bolts on the front face. In order to integrate with the cathode array, the potting was removed so that the bolts which secure the front face of the BHT-200 could also be used to connect the cathode array.

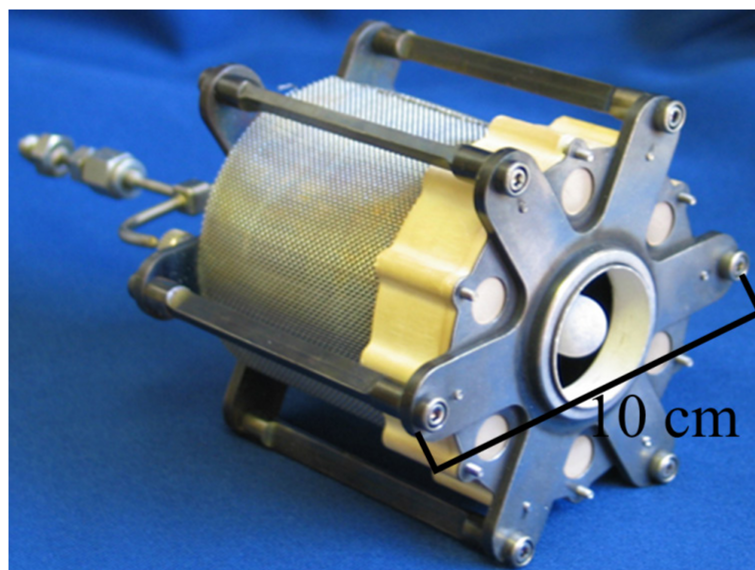


Figure 55: A BHT-200 HET with potted bolts (front face diameter is 3.98 in).

Also visible in Figure 53 is a UV photodesorption system. An 18-W lamp placed 0.75 meters away from the array is used prior to testing inside the vacuum chamber. The VTF-2 facility was pumped a base pressure of 1 x 10^{-9} Torr before starting the HET test. The chamber maintains a pressure of 1.1 x 10^{-6} Torr (corrected for xenon) near the chamber wall during HET operation.

A standard characterization test was run on all of the CFEAs individually before HET exposure. The HET was turned on with the cathode array system isolated from the HET circuit. Once steady operation was established, the cathode array system was connected with the HET circuit and the CFEAs were biased in an attempt to measure FE. The full HET exposure procedures can be found in Appendix A.

3.6 ALICE CubeSat Collaboration

A second effort to study CNT field emitters for applications in spacecraft propulsion is a collaboration with AFIT. CFEAs were provided to AFIT to test their emission performance in the space environment and compare it to that on earth. AFIT has internally developed a CubeSat, called ALICE, to run the experiments with the CFEAs as the payload. The FE tests on earth and in space are conducted in identical setups developed at AFIT. ALICE has passed all flight testing and is awaiting launch scheduled for December 2013. ALICE stands for the AFIT LEO (low earth orbit) iMESA (integrated miniaturized electrostatic analyzer) CNT Experiment.

The CFEAs are bonded to fitted J-hook packages with wire bonds to the gate and cathode. The test setup uses a specialized anode called an iMESA, which uses several different slotted plates to measure electron energy distribution. The electrical setup for FE testing with the iMESA is shown in Figure 56. The setup is a standard triode configuration similar to what is normally used in this work. The iMESA comprises a series of plates that alternate between anode potential and iMESA potential, which is normally ground. The slots in the anode plates are staggered, so that electrons must weave between the plates to reach the final anode plate. By modulating the potential difference between the anode and iMESA plates, the proportion of current that reaches the iMESA versus the anode plates changes. Plotting this variation will give a distribution of the emitted electron’s energies. The iMESA allows for additional analysis of the FE from the CFEAs. For example, the energy spectrum for different emission potentials or over time at constant potential can be determined.

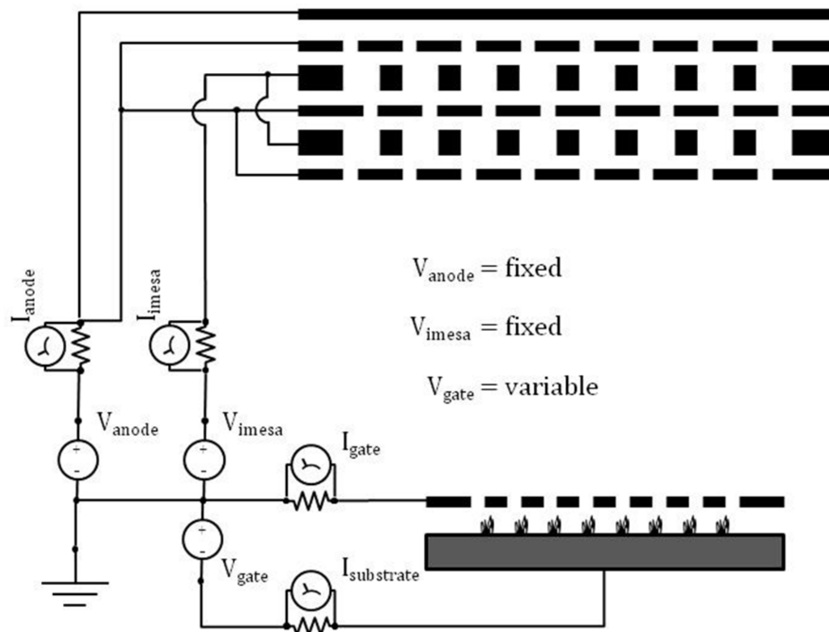


Figure 56: Electrical schematic for FE testing on ALICE showing a standard triode configuration with the iMESA anode (top).

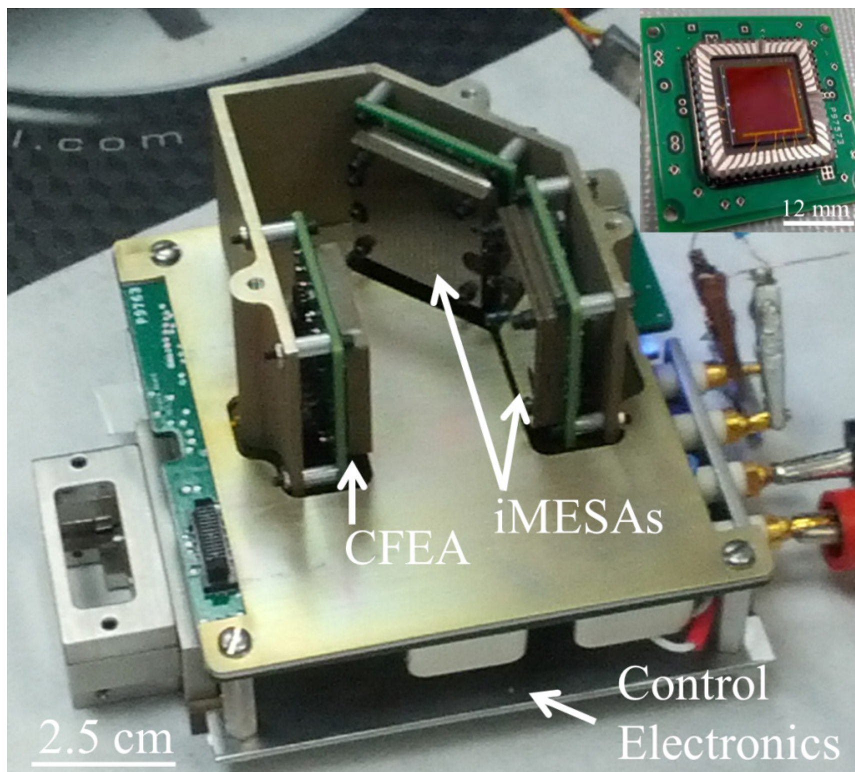


Figure 57: The ALICE FE testbed showing the mounts for the CFEA, iMESA anodes, and the control electronics below the mount. Inset shows the front of the CFEA.

The ALICE CubeSat uses custom made circuit boards and integrated electronics to test FE. The packages are either held in J-hook sockets bonded to circuit boards, or bonded directly to a circuit board. The test bed integrates two iMESA anodes, one directly in front of the CFEA and one shifted 45° from the CFEA, in order to characterize the spread in electron emission. An image of the full testbed is shown in Figure 57. This setup integrates all electronics needed for FE testing except a power source, which is either provided by the ALICE solar cells, or external power sources for laboratory testing. Aside from the iMESA anode tests and the addition of a second anode, the FE testing is the same. CFEAs are tested by voltage sweeps to characterize FE and constant voltage emission to determine lifetime.

The ALICE CubeSat contains two of the testbeds shown in Figure 57. One is fully enclosed within the CubeSat (but still at vacuum), and the other has small holes in its shielding to make it more exposed to the space environment. The purpose of these two setups is to compare the effect of the space environment on the CFEAs in a shielded and exposed configuration to differentiate the effects of the space vacuum from the effects of space plasma and particles.

ALICE, show in Figure 58, is a 3 unit CubeSat with dimensions of 10 x 10 x 30 cm. The upper portion contains the payload, or the two CFEA testbeds. The attitude determination and control systems (ADCS) module is below the payload. This module is able to detect the CubeSat's orientation relative to earth, and change its attitude for solar cell positioning and communications by the use of accelerometers, magnetorquers, and momentum transfer hardware. The last component below the ADCS is the Bus, which

contains all other hardware for communications and operation. The CubeSat also contains four deployable solar cells and antennas that fold up against the sides of the spacecraft.

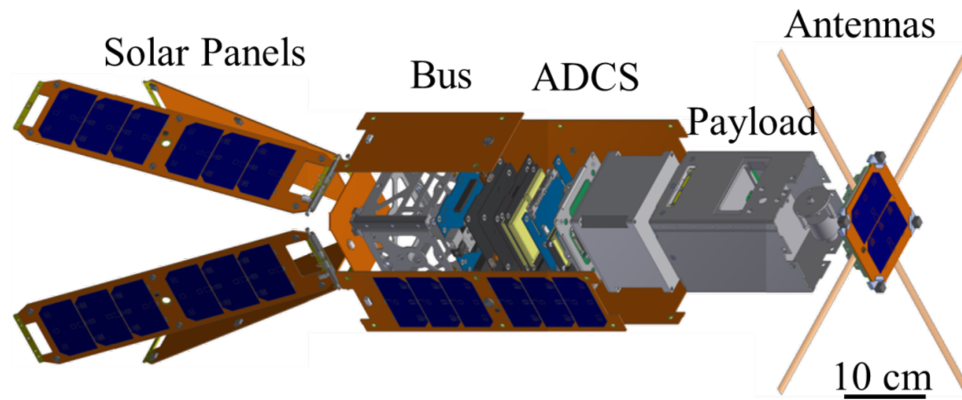


Figure 58: Schematic of the ALICE CubeSat, showing the deployable solar panels and antennas, CubeSat bus, ADCS, and payload.

CHAPTER 4

RESULTS AND DISCUSSION

This chapter follows a similar organization to the Experimental Procedures Chapter. The first sections include discussions on the process development that led to the final procedures presented in the previous chapter. This includes the major improvements and changes made to the CFEA fabrication to achieve the novel pit geometry. In addition, the PECVD CNT synthesis process initially developed, problems with arcing during PECVD, and a change to a LPCVD process are discussed.

The rest of this chapter presents the results and discussions of work using the final procedures and characterization techniques. The yield of wafer scale fabrication with the final procedures and the effect of an oxygen plasma resurrection are given. Various FE characterization data from internal work, AFIT collaborations, and then the cathode array are discussed, in addition to the analysis of FE damage observed. Next, the results from the HET exposure test are discussed. Last, a manufacturing readiness level assessment of the developed CFEA technology is summarized.

4.1 Fabrication Improvements

This section discusses the major improvements made during fabrication development and benefits of the final fabrication procedures. During initial fabrication work, it quickly became evident that electrical shorts were developing between the gate and cathode layers. Unfortunately, it proved quite difficult to determine when and where electrical isolation was lost. Electrical testing during fabrication is difficult while photoresist is still present and a single electrical short (such as in an etch pit) will short an

entire wafer. Several changes to the initial fabrication procedures, described below, were made to stop and prevent electrical shorting to enable a more robust CFEA.

Early work found that wafer dicing through the gate can cause electrical shorts along the dice cuts. A lithography mask, detailed in Section 3.1.3, is now used to expose and etch the gate material around each die where dicing occurs. This method prevents shorting from dicing and shorting during die handling as it removes gate material around the edge of each die. In addition, the photoresist from patterning protects the etch pits from debris during dicing.

4.1.1 Oxide and Gate Layers

Initial fabrication procedures used CVD or ion assisted deposition (IAD) SiO_2 and a Cr gate. In order to maximize film quality, the layers were optimized to thermal oxide and doped p-Si. Reasons for using these materials include film quality, ease of fabrication, and compatibility with each other. Thermal oxide deposits the best quality SiO_2 in terms of density, uniformity, purity, and dielectric breakdown. Thermal oxide has a dielectric breakdown of about 1,000 V/μm, which is about ten times higher than CVD SiO_2 [146]. Thus, even though the oxide cannot be deposited as thick as CVD or IAD oxide, with an upper limit of ~4 μm, the film's breakdown strength is still much greater. High dielectric breakdown prevents degradation of the device during operation.

The thermal oxide is deposited using a combined dry and wet process. Initially, ~250 nm dry oxide is deposited using diatomic oxygen in order to have the highest quality oxide surface. The rest of the oxide is deposited using a wet oxide process, where water vapor is used as the oxygen source and much faster growth rates are achieved.

The p-Si is used for its robustness and high temperature stability with SiO_2, preventing degradation during high temperature fabrication and operation. It is very compatible with the thermal oxide because they have similar coefficients of thermal expansion. Both materials use scalable furnace processes and can be deposited directly after one another with very little handling, reducing defects.

The p-Si deposition achieves uniform films across the wafer with some surface roughness due to the CVD growth mechanism. Silane decomposes at the high furnace temperatures, depositing intrinsic Si at a rate of ~5 nm/min. The deposited p-Si does not have a low enough sheet resistance, so the p-Si is heavily n-type doped with phosphorous using a solid source ceramic dopant wafer. In a "pre-deposition" step, ~10 nm of a P_2O_5 glassy oxide is sublimed on the p-Si surface. Doping occurs during a "drive-in" anneal at ~1,100°C, which allows P from the glassy oxide to diffuse into the p-Si. Since only high doping is needed, as opposed to a specific dopant concentration, this method is convenient and sufficient.

4.1.2 Pit Geometry

The etched pit geometry is specifically designed to prevent electrical shorting by increasing the separation between CNT growth and the gate, while still allowing growth of longer, more reproducible CNTs. A Bosch etch process is used to anisotropically etch the p-Si and is mainly used for its sidewall passivation. Standard isotropic plasma etching of p-Si does not achieve uniform etching due to the disparate etch rates of the crystal grains, which results in jagged sidewalls and loss of feature definition. The Bosch process uses short cycle times to minimize sidewall roughness and achieve the anisotropic etch. A

quick descum etch is needed afterwards to remove any residual polymer from the Bosch process, which also helps wetting in later processing.

A BOE wet etch process isotropically etches the SiO_2. The wafer is placed in a custom made Teflon mount that holds the wafer upside-down submerged in the BOE solution with a magnetic stir bar, which promote uniform etching across the wafer. The etch rate is 100 nm/min and the SiO_2 is intentionally over etched so that the exposed Si substrate in the pit is larger than the photoresist aperture. This over etch allows the photoresist aperture, and not the SiO_2 aperture, to remain as the mask for subsequent Si etching.

A standard Bosch etch is used to extend the pits into the Si substrate, thus creating a larger electrode separation than would be possible by just using an oxide layer. This deeper pit allows for fabrication of a larger CNT-to-gate separation to prevent shorting while still allowing growth of longer, more reproducible CNTs. The etch increases the pit depth by 5-10 μm without significant removal of photoresist or increasing the insulation layer thickness. Interestingly, the Si pit diameter is determined by the size of the photoresist aperture and not by the amount of Si surface exposed, thus, the photoresist remains the mask, as shown by the unetched Si surface in Figure 59. Even though the p-Si in the pit is exposed, it is masked by the photoresist and is not significantly etched.

The isotropic SiO_2 etch causes an undercut of the gate layer by several microns, as shown in Figure 59. An RIE process is used to simultaneously remove this undercut and increase the diameter of the Si pit by isotropically etching all exposed silicon. Wafers are placed on glass slides in the RIE to isolate it from the electrode, which promotes isotropic etching by removing the directionality from the bias in an RIE etch. Typically

the p-Si is etched about 100-200 nm past the p-Si/SiO_2 interface. This etch increases the diameter of the gate aperture without increasing photoresist aperture and thus, the CNT catalyst spot size. The size difference effectively creates a lateral buffer zone between CNT growth and the gate sidewall, preventing electrical shorting. The etch also increases the depth of the Si pit by ~2 μm, indicated by the curved base in Figure 60, and widens the Si pit to prevent any catalyst deposition on the Si sidewalls.

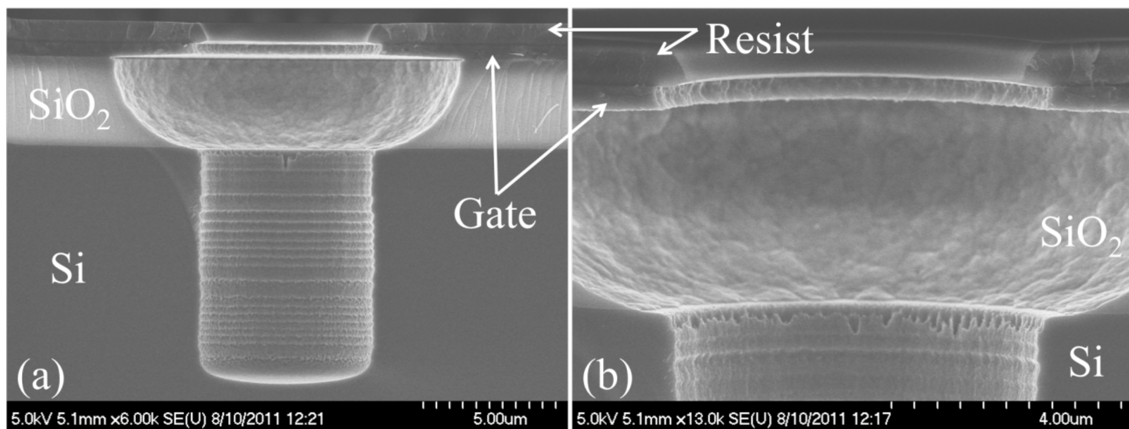


Figure 59: SEM cross section of the etch pit design after the Si Bosch etch. Scalloping from the Bosch etch of the Si trench is visible in. The unetched Si surface in (b) indicates the Si trench is masked by the photoresist aperture.

It was found that the omission of a standard oxygen plasma descum etch after the isotropic RIE Si etch greatly effects LPCVD CNT growth and quality. Without the descum, quality CNT growth cannot be achieved. However, with the descum the growth is greatly improved and is highly uniform. It is presumed that the etch provides a high quality support for the catalyst on the Si by removing any scum or debris from the RIE etch.

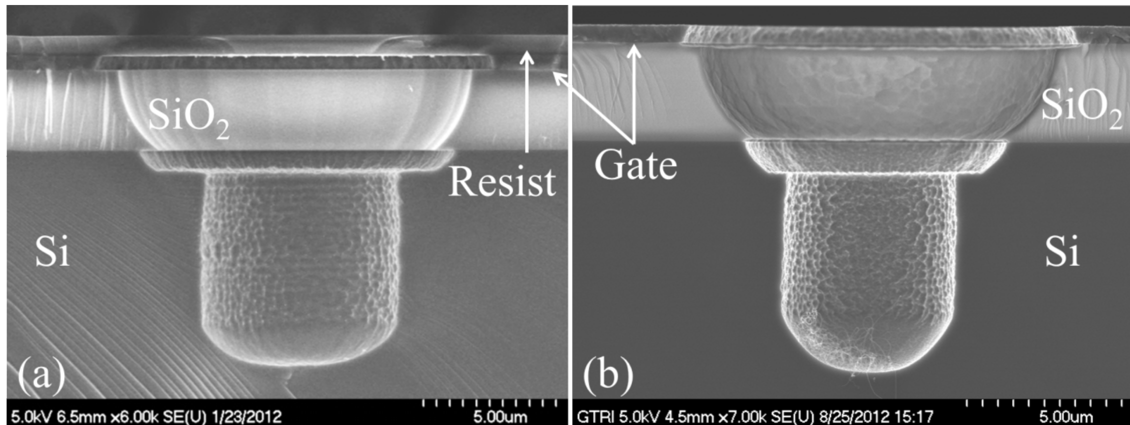


Figure 60: SEM cross section of the final etch geometry showing the undercut p-Si removed (a) with and (b) without photoresist. The curved Si pit and undercut SiO_2 is from the isotropic Si etch.

This finalized etch geometry in Figure 60 is highly beneficial since the many thousands of pits per CFEA increase the chances of having an abnormally long CNT that can short the entire sample by contacting the gate. The etch geometry prevents electrical shorting by increasing the horizontal and vertical separation between CNT growth and the gate, while still allowing growth of longer CNTs, which are more uniform and reproducible than short (< 1μm) CNTs.

4.1.3 CNT Catalyst Deposition

During initial fabrication development, it was found that a majority of samples would electrically short after CNT catalyst deposition, even without CNT synthesis. At times, catalyst deposition on the pit sidewalls was noticed in the SEM, which could cause an electrical short by connecting the gate and Si. As shown in Figure 61, sidewall deposition was especially evident when a short BOE dip was used to try to reverse an electrical short, which caused the catalyst to peel off of the sidewalls. This evidence confirms that catalyst was depositing on the sidewalls, which can be caused by either

photoresist defects exposing the sidewalls or misalignment in the electron beam evaporator.

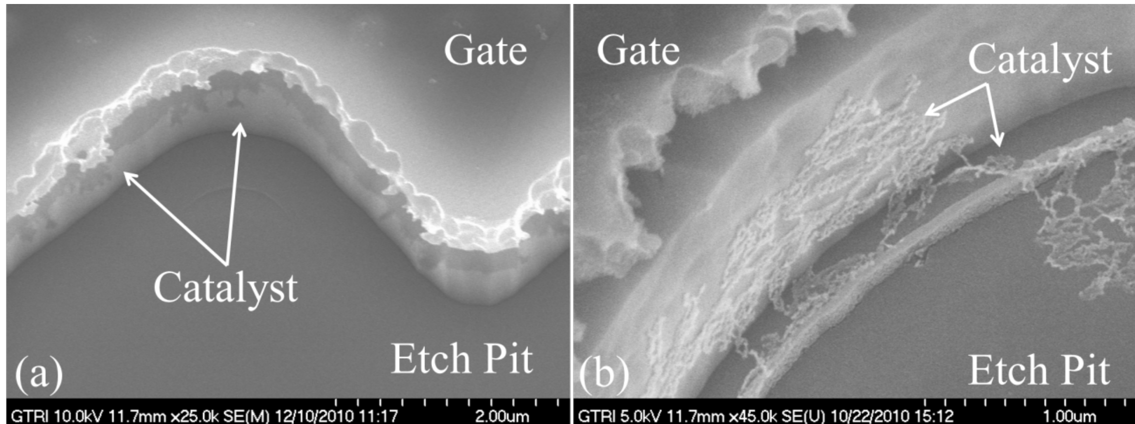


Figure 61: SEM at a 20° view of an etch pit showing catalyst deposition peeling off the SiO_2 sidewalls (a) before and (b) after a BOE etch.

The catalyst is deposited by electron beam evaporation, which is a line-of-sight deposition process. Investigation of the Angstrom Engineering EvoVac tool used to deposit catalyst revealed that samples were significantly off center from the source. This occurred because the tool has two electron beam sources, which are both aligned about 2 inches from center of the sample holder so that the flux from both sources to the center is the same. However, as shown in Figure 62, the off center source causes an angle of deposition to the center of the sample holder, which correlates to a flux of material on the pit sidewalls, especially during sample rotation. The tool has a standard separation of 45 cm between the source and sample holder, and can have samples that are off center by up to 6 cm, which gives a deposition angle of 7.6°. Assuming no overhang of the photoresist or gate causing shadowing, this angle causes a 13% flux of material onto the sidewalls, which could easily electrically short the gate.

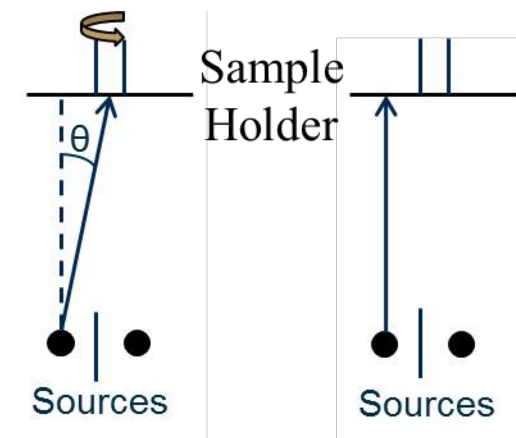


Figure 62: Schematic of the deposition angle in electron beam evaporation when (a) a sample isn't centered over a source with sample rotation, and (b) when the sample is centered without rotation.

Following the geometry shown, the angle of deposition was reduced in two ways. The distance from the source to the sample holder was increased to 75.5 cm using the adjustable height on the sample holder. Increasing the separation distance also reduces the variation in angle across a large sample. The sample was also moved directly over the source by using a plumb line to accurately center samples over the source. A small, centered 4 cm sample results in a maximum off center of 2 cm, a greatly reduced maximum deposition angle of 1.5° and a 2.6% flux onto the sidewall. Sample rotation cannot be used with the sample centered over one source because the center of rotation is between the two sources, causing the variation of angle with rotation to be large. Tests with the deposition angle minimized revealed that sidewall deposition was significantly reduced. Figure 63, which is an early pit geometry that has little overhang to cause shadowing, shows that the catalyst deposition is well centered onto the exposed Si.

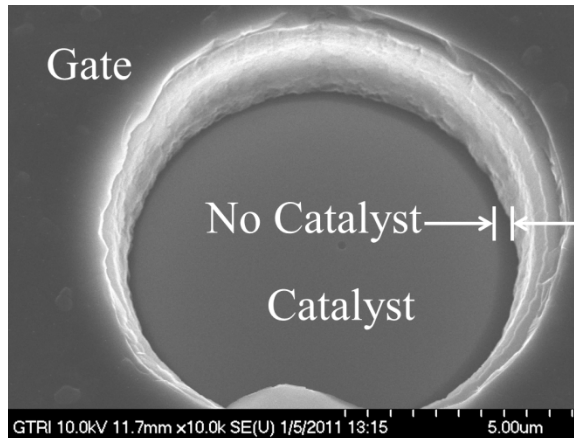


Figure 63: SEM image of an etch pit with catalyst deposited at a minimized deposition angle showing the catalyst is well centered.

The combination of this low angle deposition with the final pit geometry that has a photoresist aperture smaller than the gate, oxide, and Si pit apertures ensures that there is no possibility of catalyst deposition on anything but the Si pit. The photoresist overhang ensures that any small angle of deposition is shadowed. For a worst case example, a centered 10 cm (4 in) wafer will have a maximum off center of 5 cm, corresponding to a deposition angle of 3.8°. In the extreme case that a pit is 15 μm deep, only a 1.0 μm photoresist overhang is required to shadow deposition on the Si sidewalls, let alone on to the gate or SiO_2. As shown in Figure 59 and Figure 60, the overhang is close to the 1 μm needed. Tests on samples with this pit geometry and minimized deposition angle remained an open circuit after catalyst deposition.

Two types of catalysts were during the development of CNT synthesis. Early stage work used a Ni catalyst for PECVD synthesis, while most work used a Fe catalyst for LPCVD synthesis. The Fe catalyst used a standardized process with 3 nm of Fe deposited at 0.5 Å/s at a pressure < 1.0 x 10^{-6}. The Ni catalyst required significant development for new PECVD synthesis processes.

Early Ni catalyst work showed that Ni alone was insufficient for uniform and consistent CNT synthesis on Si because, as mentioned in Section 2.2.5, Ni has a significant diffusion rate in Si at synthesis temperatures. Therefore an electrically conductive diffusion barrier is used, excluding the use of common oxide barrier layers. Ti was determined to be the best diffusion barrier for Ni as it has been demonstrated as a high quality barrier for CNT synthesis [161, 162]. Unfortunately, CNT growth tests produced inconsistent growth. Incorporation of a thin Al layer between the Ti and Ni produced greatly improved growth because the Al layer acts as a support for Ni particle formation. All three layers were concurrently deposited without breaking vacuum to minimize oxidation. An optimized growth recipe was achieved with Ti, Al, and Ni at a 20, 2, and 10 nm thickness, respectively.

4.2 Carbon Nanotube Synthesis

This section briefly discusses the PECVD CNT synthesis process initially developed for this work, and methods to prevent arcing observed during PECVD. Next, reasons for switching to and details of the final LPCVD CNT synthesis process are discussed, and Raman spectroscopy is presented.

4.2.1 Plasma Enhanced CVD Synthesis

For CNT growth in this particular triode design, the PECVD synthesized CNT growth was considered to be superior and was initially pursued. PECVD CNT growth is preferred partially due to the precise height control, achieved by the driving force for CNT growth, a plasma, which can be instantly terminated. In thermal methods, growth is terminated by other less immediate methods. PECVD can also produce CNTs that are

very well aligned at densities lower than thermal CVD, whose alignment mechanism depends on dense growth [86]. PECVD CNTs typically have a larger diameter, reducing field enhancement relative to thermal CVD. However, the lower PECVD density reduces the field screening, and may overshadow the increased diameter [89].

The optimized PECVD growth recipe for the Ti/Al/Ni catalyst achieves well aligned growth. The Black Magic PECVD uses N_2 for purging and cooling, C_2H_2 as the carbon source, and NH_3 as the reducing gas. For growth, a DC power input is used to strike the plasma, quickly followed by a 30 W and 15 kHz input. An example of the CNT growth in a CFEA pit is shown in Figure 64.

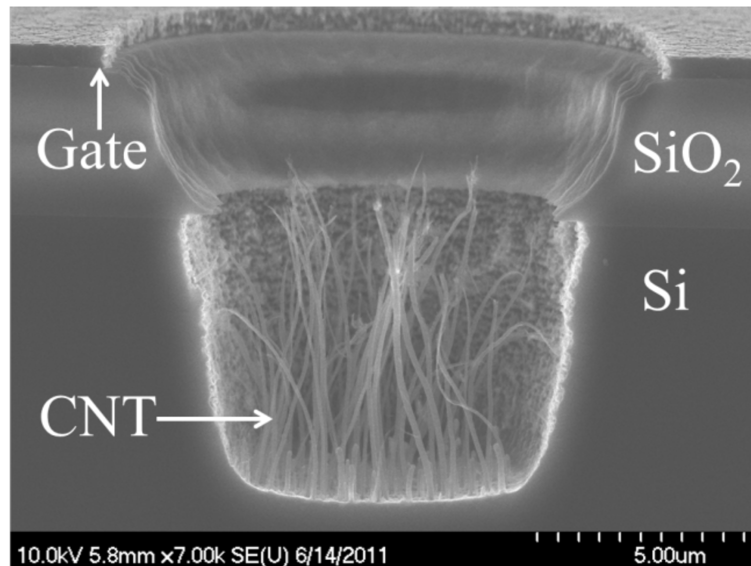


Figure 64: SEM cross section of PECVD growth in a CFEA etch pit.

It was found that all samples ended up shorted after PECVD growth. Testing on un-catalyzed samples with and without plasma suggested that plasma is a cause of shorting. OM and SEM revealed some of the shorted samples contained damage to the etch pits, shown in Figure 65. This damage is very similar to what is seen from FE

testing, which is discussed in Section 4.6. The evidence suggests that the plasma causes arcing and shorting of the gate due to the high potential (up to 700 V) of the plasma.

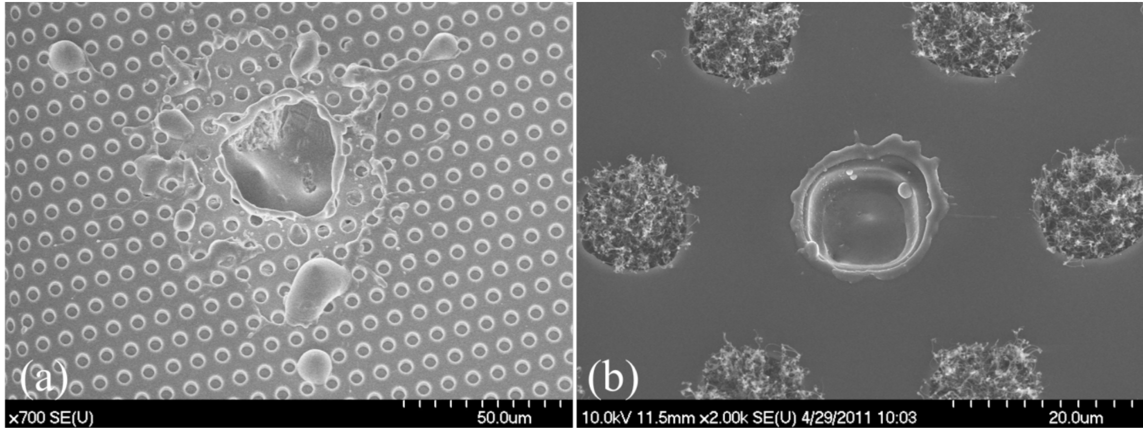


Figure 65: SEM of the typical damage seen from PECVD synthesis showing melting and spallation of the surface.

Significant effort was devoted to temporarily ground the gate to the Si cathode to prevent arcing. Material limitations made it difficult to form low resistance contacts in the extreme PECVD environment. Colloidal carbon paint and strips of graphite were used to ground the samples, but these methods only achieved a resistance of 1 kΩ. An evaporated metal strip was used to ground the samples by masking with photoresist. A strip of metal connecting the exposed Si to the gate was deposited so that the strip could be opened by scraping through it after PECVD. However, tests showed that samples still shorted, suggesting there is another shorting mechanism other than arcing, or the metal line could be sputtering in the plasma. Several other unsuccessful methods were tried in conjunction with each other with no success. At this point, all pragmatic ideas for preventing shorting were exhausted. Since shorting was isolated to the plasma step, efforts were focused on using LPCVD synthesis, which does not use a plasma step.

4.2.2 Low Pressure CVD Synthesis

To avoid arcing, LPCVD synthesis is used in this work. It is much more difficult to uniformly synthesize short CNTs using LPCVD because the growth rate is much faster and there is no immediate removal of growth species as there is in PECVD. To mitigate these challenges, the Black Magic system with precisely controlled process parameters and recipe steps is used to produce uniform and consistent CNT growth. The low pressure process is used because it allows better height control and uniformity than atmospheric methods for high surface area samples. Due to the fast growth rate, the final etch geometry, which etches into the Si to form deeper pits, was developed in parallel with the LPCVD process to accommodate longer CNTs.

In this work, a standard Fe catalyst and optimized LPCVD recipe from a standard process are used [90]. The recipe uses N_2 for purging and cooling, C_2H_2 as the carbon source, and H_2 as the reducing gas. Growth is at 700 °C and 10 mbar. Temperature control above 500 °C uses an IR sensor aimed at a piece of Si scrap in the chamber. The scrap is used to simulate the p-Si surface temperature because the IR sensor is calibrated for Si and the emissivity of p-Si can vary significantly from Si and from sample to sample with small changes in the p-Si thickness [163, 164]. This method ensures accurate and consistent temperature profiles independent of sample variation. A 15 minute anneal at 650 °C was used to ensure catalyst particle formation is uniform across all samples.

After annealing, the top heater is set to 700 °C with a 30% power limit, allowing it to reach 700 °C during growth. Power levels above 30% cause interference with the IR temperature sensor, which reads surface temperature through the middle of the top heater. The substrate temperature is ramped to 700°C and held for 90 seconds to ensure

temperature uniformity across samples to achieve uniform growth. The growth step follows for up to 3 minutes, depending on the pit depth. This short growth time shows how precise the recipe must be to achieve the correct CNT length. A change in growth of as little as 15 seconds can create a large change in CNT length, showing precision is required. Figure 66 shows that the CNT growth can be precisely controlled, remains aligned past the Si pit, and is uniform across many pits.

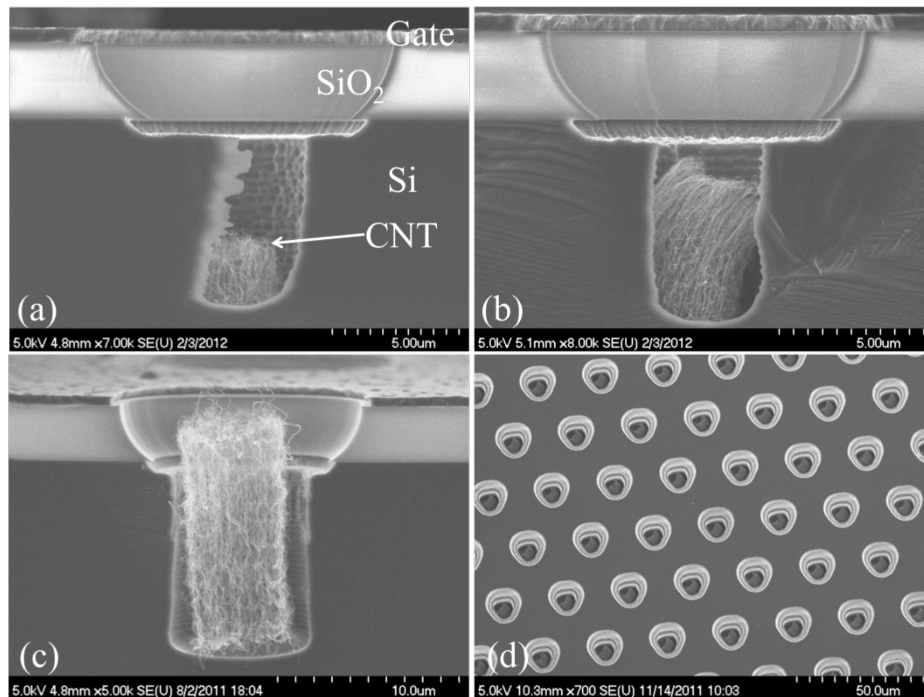


Figure 66: SEM of CNT synthesis. (a-c) Cross section images showing controllability of CNT length. (d) Image showing CNT uniformity across many pits.

4.2.3 Raman Spectroscopy

Raman spectroscopy is commonly used to characterize the quality of CNTs. A Thermo Almega XR Micro Analysis System with a 488 nm laser was used. The spectra in Figure 67 focus on the features that are particularly useful for CNTs. The D line,

located around ~1,340 cm^{-1}, corresponds to disordered graphitic material in the CNTs and can give an idea of the amount of defects present. The G band, which contains a group of peaks ranging from ~1,550-1,600 cm^{-1}, correlates to tangential mode vibrations of the carbon atoms in the graphene walls of CNTs [44]. A ratio of the relative intensities of these two features gives an idea of the relative quality of the CNTs. This ratio is called the D/G ratio and is commonly cited in the literature [165, 166]. The spectra in Figure 67 have a D/G ratio of 0.83 and 1.00 for the LPCVD and PECVD synthesized CNTs, respectively. Generally, a ratio of less than one is preferred and high quality CNT are indicated by ratios less than 0.3.

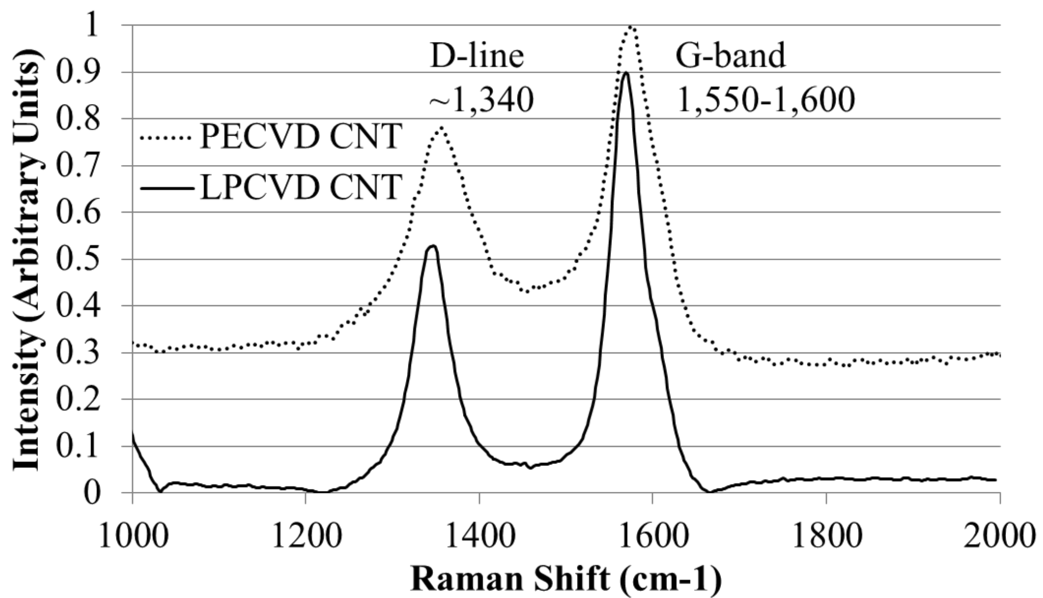


Figure 67: Raman spectra of PECVD and LPCVD synthesized CNTs.

4.3 CFEA Fabrication

The optimized LPCVD process is favorable for the triode design, demonstrating uniform growth close to the gate. Initial tests with the final fabrication procedures still

produced electrically shorted samples. This shorting was originally remedied by growing shorter CNTs that stopped below the Si surface. Subsequent improvements in fabrication and reduction in defects helped to prevent shorting, and allowed CNT synthesis close to the gate. The initial high failure rate is attributed to fabrication defects and CNT non-uniformity. The growth must be extremely uniform since one CNT of the billions of CNTs in a sample can short the entire device. In addition, any scratches and defects in the photoresist can allow catalyst and growth on the gate, which can short the device. This defect mechanism has been directly observed in the SEM. As wafer fabrication improved and CNT uniformity increased, the sample yield increased.

4.3.1 CFEA Yield

A review of the fabrication of 13 wafers with the final fabrication procedures shows considerable improvement in final CFEA yield, defined as the percentage of CFEAs produced with an open circuit and good CNT growth. Table 2 summarizes the wafer yield of chips before and after CNT synthesis. The shaded wafers were fully fabricated to CFEAs while others suffered from some sort of fabrication failure. The fabrication results are presented here, and fully exhaustively detailed elsewhere [167].

The second column in Table 2 denotes the number of chips what were suitable for CNT growth, meaning that the chip was a full die (not partial from the edge of a wafer), had no major defects, and had a resistance > 50 MΩ. Note that this “fabrication yield” is consistently high and close to the maximum of 41 chips from the lithography mask. The most common chip failure was due to a major defect from wafer handling and not electrical shorting. This high fabrication yield shows that the fabrication process was very effective in producing open circuit chips up to CNT synthesis at a high yield.

Table 2: Summary of wafer yield before and after CNT synthesis with successfully fabricated CFEAs shaded.

Wafer Name	Fabrication Yield (pre CNTs)	CFEA Packaged	CFEA Yield
SMC-001	34	12	35.3%
SMC-002	32	2**	6.30%
SMC-003	30	0**	0**
SMC-004	0†	0†	0†
SMC-005	0†	0†	0†
SMC-006	38	0††	0††
SMC-007	38	0††	0††
SMC-008	39	21	53.8%
SMC-009	34	16	47.1%
SMC-010	0‡	0‡	0‡
SMC-011	0‡	0‡	0‡
SMC-012	37	12	32.4%
SMC-013	39	28	71.8%
**Most of 002 and all of 003 CNT growth was incompatible for testing			
†004 and 005 were contaminated with Au from a contact patterning error			
††006 and 007 had insufficient CNT growth for testing			
‡010 and 011 were abandoned after etch processing errors			

The third column in Table 2 denotes the number of fully fabricated CFEAs that were packaged. This value represents full CFEA yield and only includes chips that are electrically open (> 200 MΩ) with sufficient CNT growth and successfully packaged for FE testing. The fourth column gives the percent CFEA yield calculated from the previous two columns. This number only takes into account losses from CNT synthesis and packaging, which does not account for losses during chip fabrication. The CFEA yield from successfully fabricated wafers varies significantly, ranging from 32-72%. Small changes and improvements in the wafer fabrication process helped to increase fabrication yield and gradually increase CFEA yield. It should be noted that most wafers used an

oxygen plasma resurrection technique after CNT synthesis to reverse shorting and improve yield, the results of which are reported in Section 4.3.2

Wafer SMC-001, denoted hereafter as 001, had good initial fabrication results, with a CFEA yield of 35%. As the initial wafer, it was fabricated slowly and carefully to confirm procedures and maintain quality. After this wafer, attempts were made to scale fabrication, which is where errors and small fabrication changes reduced wafer yield.

Wafers 002 and 003 were fabricated in parallel to accelerate production. These wafers had a variety of fabrication problems that caused failure. They had heterogeneous photolithography processing, resulting in areas with photoresist still present in the features, and incomplete etching in later fabrication. In addition, due to problems with the shared facility Vision RIE, the isotropic Si etch to remove the undercut p-Si took up to 5 times longer than normal. Both of these problems resulted in a heterogeneous and improper etch geometry, as shown in Figure 68.

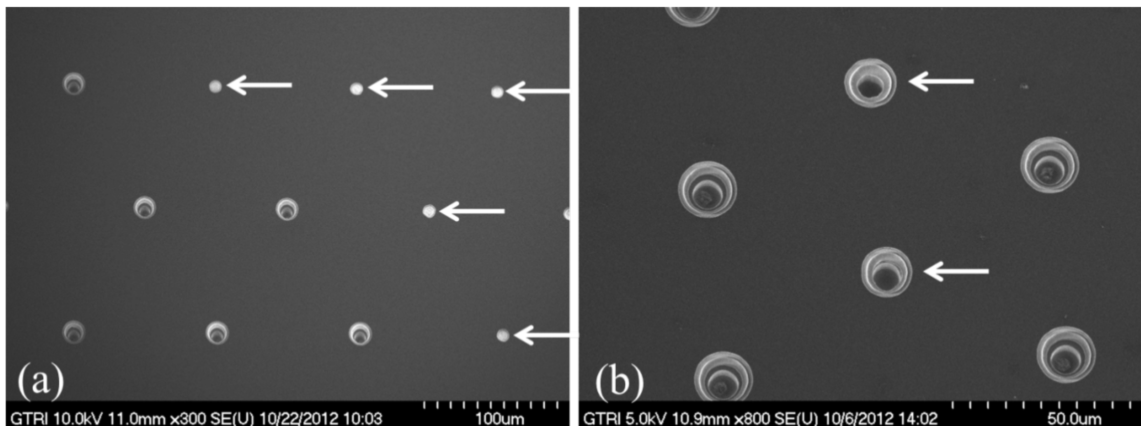


Figure 68: SEM of wafer SMC-002 showing inconsistent etching. Arrows indicate (a) unetched and (b) poorly etched pits.

In addition, prior to catalyst deposition on wafers 002 and 003, a standard descum etch and 8 minute BOE etch that was used in 001 to remove undercut SiO_2 away from the Si pit opening was abandoned because no significant etching was observed. It wouldn't be noticed until after wafer 007 that the descum step is pivotal for having a clean catalyst-substrate interface for quality CNT growth. This step omission caused inconsistent and poor CNT growth.

Wafers 004 and 005 were also fabricated together, but both wafers were abandoned before dicing because the wafers were insecurely fastened to the shadow mask for Au contact deposition, allowing the wafers to shift and metal to deposit in the etch pits. Photolithography and etch problems observed in wafers 002 and 003 were resolved. In wafer 004 a different tool was used to deposit catalyst, and in wafer 005 the deposition tooling factor was tuned on the original EvoVac tool. However, both of these methods did not improve CNT growth because they had the same aforementioned descum step omitted.

Wafers 006 and 007, fabricated in parallel, were successfully fabricated up to CNT synthesis without any significant problems, but still suffered from poor CNT growth. Measures were taken to securely fasten the Au contact shadow mask to prevent the wafer movement seen in wafers 004 and 005. Both wafers had a high fabrication yield, each producing 38 chips that were suitable for CNT synthesis.

At this point, since three sets of wafers had produced poor CNT growth even with attempts to improve catalyst deposition, a cumulative fabrication analysis was made on wafers 001-007. It was noted that the only major difference between the good CNT growth in wafer 001 and the rest of the wafers was that 001 had the extra descum and 8

minute BOE etch added before catalyst deposition. In addition, the catalyst and CVD tool were eliminated as causes of bad growth. The catalyst was eliminated as a cause of bad growth because normal growth still occurred in wafer defects where catalyst was deposited on exposed SiO_2. The Black Magic CVD was eliminated as a cause because standardized catalyst samples showed good growth.

These observations seemed to support a theory that the poor CNT growth is due to a poor support layer under the catalyst, and performing the extra descum and possibly the BOE etch on wafer 001 properly treats the silicon as a support. Thus, this descum and BOE etch step was re-introduced in subsequent wafers.

Wafers 008 and 009 had a successful fabrication yield of 39 and 34 chips, respectively, and finally achieved good CNT growth. This result confirms that the extra descum and/or the BOE etch is needed for good CNT growth. Wafers 008 and 009 achieved a CFEA yield of 54% and 47%, respectively, showing similar yield and a greater than 12% improvement over wafer 001.

Wafers 010 and 011, fabricated in parallel, succumbed to another fabrication error that resulted in unusable wafers. A protective photoresist layer was spin coated to prevent front side etching during backside p-Si etching. The photoresist left a small amount of material on the front side, which wasn't adequately removed before further processing. This material caused poor adhesion of the lithography photoresist, which caused it to strip off during BOE etching.

In wafer 012 and 013, the protective photoresist layer used in wafers 010 and 011 was utilized, but full removal was ensured with a standard descum etch prior to lithography. These wafers achieved successful fabrication and good CNT synthesis.

Wafer 012 achieved a fabrication yield of 37 chips and a CFEA yield of 32%, showing a lower CFEA yield but still successful completion. Wafer 013 achieved a fabrication yield of 39 chips and a record high CFEA yield of 72%.

The evolution of results from wafer 001 through wafer 013 shows that small changes or errors during silicon fabrication can have significant effects and even make entire wafers unusable. The successfully fabricated wafers showed a consistently high fabrication yield and a gradual increase in CFEA yield throughout the process development.

4.3.2 Oxygen Plasma Resurrection

Even though CNT FE in this Spindt type design is well studied, electrical shorting of the gate to the substrate is still a common and problematic failure mode [13, 140, 141]. This work developed the use of an oxygen plasma etch to dramatically improve CFEA yield by reversing shorting of the gate after CNT synthesis – a common time for shorts to develop [168]. The use of different plasma treatments on CNTs are commonly used to improve FE performance [169-171], by introducing defects as FE sites [172] and reducing screening by neighboring CNTs [173, 174]. However, no published work seems to detail the use of a plasma etch to reverse shorting of a Spindt type CNT electron source. This oxygen plasma resurrection was used on the aforementioned wafers 008-013 to improve CFEA yield.

Chips that have good CNT growth confirmed by SEM but are not an open circuit (> 200 MΩ) are exposed to the oxygen plasma etch, which is similar to a standard descum process. Chips are etched in the Vision RIE tool on a glass slide to isolate the cathode from the chuck and prevent a bias and arcing between the gate and substrate in

the plasma. After etching, if the chip measures an open circuit and CNTs are confirmed present by SEM, then the chip is ready for FE testing.

A total of 78 different CFEAs from four wafers were subjected to the developed resurrection technique. The results of the etching are summarized in Table 3. Etching is considered successful if the CFEA is an open circuit and there are still ample CNTs present in the etch pits. From the four different wafers, the yield ranged from 44-83% with a 71% average yield. Even though there is a large variation between wafers, the oxygen plasma etching still drastically increases the yield of each wafer since the samples would otherwise be useless. Thus, this method is a very simple and effective process to improve chip yield by reversing electrical shorting from CNT synthesis.

Table 3: The number of CFEAs etched and their yield from oxygen plasma etching.

Wafer	Plasma Etched	Open Circuit Due to Plasma Etch	Open Circuit + has CNTs	Yield (w/CNTs)
SMC-08	17	14	12	70.6%
SMC-09	20	16	16	80.0%
SMC-12	18	10	8	44.4%
SMC-13	23	20	19	82.6%
Total	78	60	55	70.5%

SEM is used to confirm presence of CNTs after the CFEAs are etched. As noticed by Juan et al. [173], over time the CNTs are etched and their density is reduced by the plasma. Figure 69 shows the effect of etching on the CNTs. For around 1 minute of etching, there is minimal effect on the CNTs, as shown by the images of the same sample before (Figure 69a) and after (Figure 69b) etching. Figure 69c is a cross-section image of an etch pit after 3 minutes etching, showing a significant reduction in CNT density from

the longer etch time. The etch rate for different chips or tool runs varies, so a serial process is followed where chips are etched in 60-90 second intervals until the chip measures an open circuit or for a total of 3 minutes. This serial process helps minimize excess etching of the CNTs after the chip is an open circuit. Figure 69d shows an etch pit where the CNTs have been almost completely etched away after 4 minutes of etching. As shown in the fourth column in Table 3, only 1-2 CFEAs per wafer are lost due to over etching of CNTs.

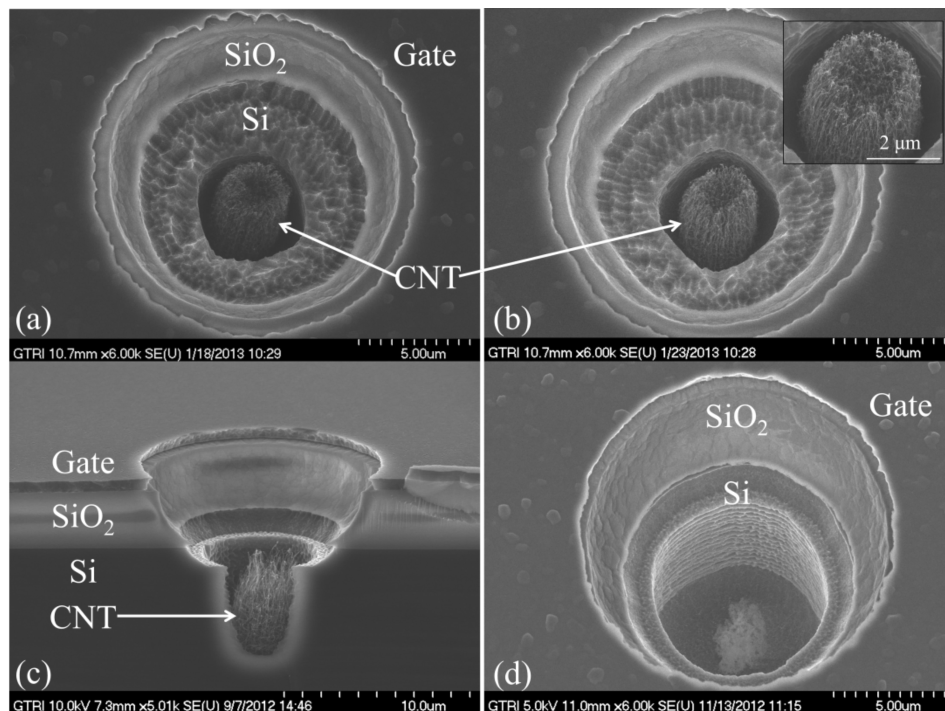


Figure 69: SEM images of CFEA etch pits. Image of the same CFEA (a) before plasma etching and (b) after a 75 second etch with magnification of CNTs inset, (c) cross-section SEM image after a 3 minute etch, (d) CNTs completely etched away after a 4 minute etch.

As mentioned earlier, each wafer contains chips with one of 3 different pit spacings: a 50, 100, or 200 µm pitch. Analysis of the oxygen plasma etch yield versus pitch and wafer are summarized in Table 4. These data show there is a large variation in yield for each pitch, ranging from 29-100%. There is also no consistent trend for pitch yield between each wafer, but on average there is a higher yield (~80%) for the 100 and 200 µm pitch versus the 50 µm pitch (64%). The lower yield on the 50 µm pitch samples could be due to the increased probability of having irreversible defects that would short the entire chip due to the higher density of etch pits. Again, even though there is a large variation in yield, the plasma etch still significantly increases the fabrication yield of all pitch types. This analysis shows that the oxygen plasma etch is a simple and highly effective method to reverse shorting from CNT synthesis and greatly increase yield of Spindt type CNT electron sources.

Table 4: Summary of oxygen plasma etch yield for chip pitch of 50, 100, and 200 µm.

Wafer	100 µm Open Circuit	100 µm yield	200 µm Open Circuit	200 µm yield	50 µm Open Circuit	50 µm yield
SMC-08	8	100.0%	3	75.0%	3	60.0%
SMC-09	7	63.6%	4	100.0%	5	100.0%
SMC-12	5	83.3%	3	60.0%	2	28.6%
SMC-13	11	84.6%	5	100.0%	4	80.0%
Total	**31**	**81.6%**	**15**	**83.3%**	**14**	**63.6%**

4.4 Field Emission Testing

In this section, the various tested field emission metrics will be discussed. These topics include emission results that were conducted at various times in the CFEA development. Emission achievements from simple I-V tests at various stages will be discussed. Throughout the FE testing in the work, reversible and non-reversible electrical shorting during FE testing was a concern. The use of an electrical burnout technique to reverse and prevent this shorting is also analyzed. Finally, lifetime emission achievements are presented and discussed.

4.4.1 Emission Measurements

FE testing was initially conducted in the finalized CFEA design by growing CNTs that were very short and recessed well below the gate. These methods were not ideal, but produced the first open circuit CFEAs and allowed initial testing. The first field emission achieved was from wafer 133, which is from the generation before the "SMC" wafers described in Section 4.3, but still has the final etch geometry. The sample tested was "4t100d", meaning 4 μm diameter triangles with a 100 μm pitch. The letter "d" indicates this is the 4th identical chip on the wafer. Pit shapes were initially proposed to be studied, but were later removed in the lithography mask developed for the "SMC" wafers.

Figure 70 shows this first FE achieved, with the inset SEM displaying the very short CNT growth. This data shows turn-on (10 μA/cm^2) at a very low 115 V. The electric field shown is only approximate since the CNTs are within the Si pit. It is calculated from an assumed 10 μm gate to CNTs separation, which is based on cross section images of similar samples. The sample produced a peak cathode current of 55 μA/cm^2 at 285 V with very unstable emission.

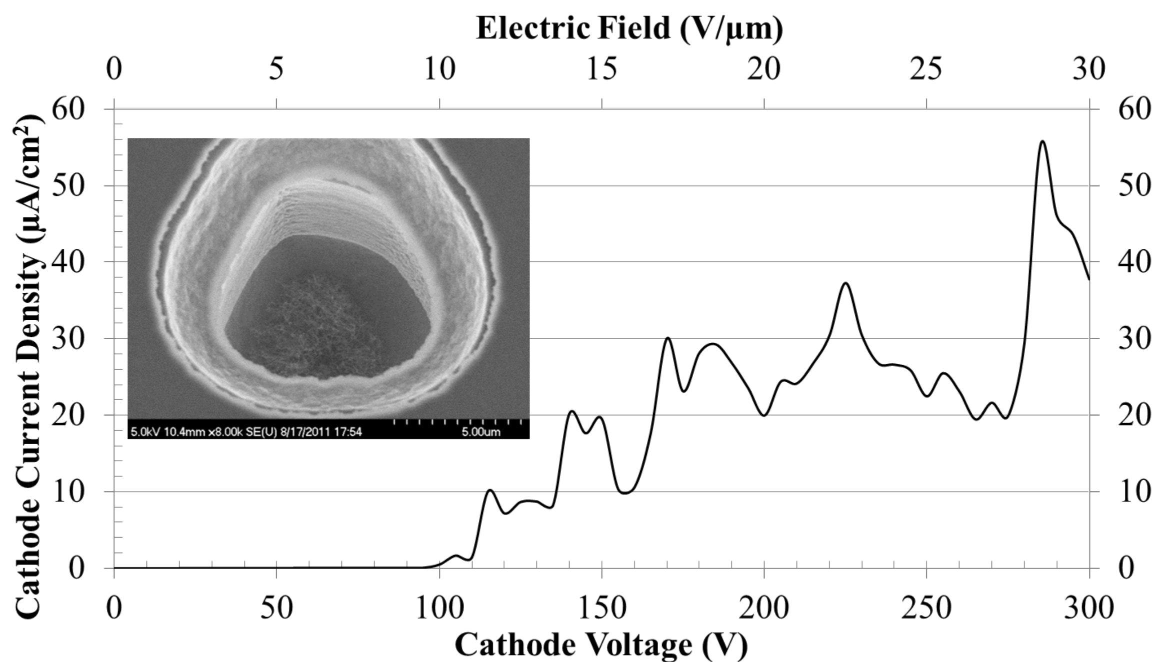


Figure 70: The first FE achieved. Sample W133 4t100d showing 55 μA/cm^2 of cathode current at 285 V. SEM showing very short CNT growth is inset.

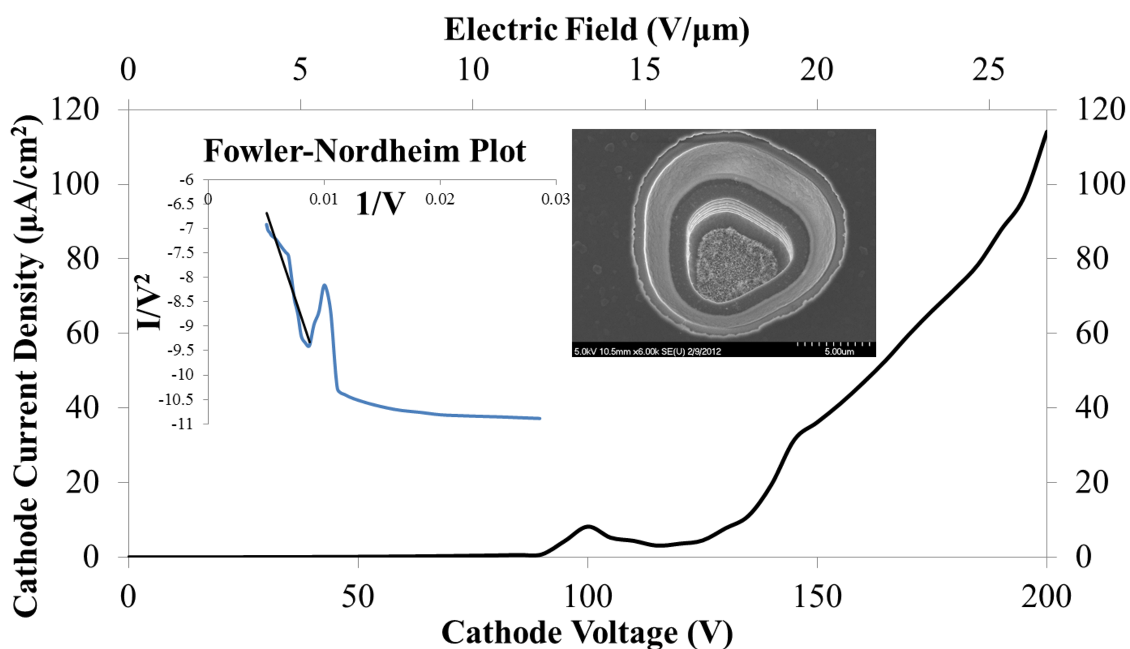


Figure 71: Sample W134 4t50a showing 114 μA/cm2 of cathode current at 200 V. SEM of the CNT growth and a Fowler-Nordheim plot are inset.

The second successful emission, shown in Figure 71, achieved more stable emission. This sample, 4t50a, again had very short CNT growth, as shown by the inset SEM. Turn-on was achieved at a slightly higher 135 V, but a much improved maximum of 114 μA/cm^2 was achieved at 200 V. This much more stable data shows a smooth increase in emission with cathode voltage. The characteristic FE behavior is indicated by the inset Fowler-Nordheim plot. The linear plot in the high field region (small 1/V) correlates with common FE behavior. These first tests demonstrate the capabilities of the CFEA design, showing a relatively low voltage is needed for FE turn-on.

In addition to these simple cathode I-V tests, most testing was conducted with the ability to simultaneously measure cathode, anode, and gate current. This allowed for redundancy in the test setup, but also gave information about when shorting occurs and how much emission current reaches the anode. The proportion of gate current to anode current is a common comparison. Generally, a higher proportion of anode current means a more efficient device. In addition, gate plus anode current should equal the cathode current. At times, there can be small deviations between these values, where some cathode current is lost to another object in the vacuum chamber. However, if the entire chamber is connected to a common ground, then any differences between the gate plus anode current and cathode current points to an electrical component problem.

The sporadic emission seen in the FE results presented in this work can partially be attributed to the need of a “conditioning” process to stabilize emission. Conditioning CNT field emitters is commonly cited in the literature, although the procedure and understood purpose varies. The conditioning mechanism has been proposed as removing adsorbed gas molecules or impurities from the CNTs that can cause instabilities in the

emission [2, 159, 160]. Common condition processes involve baking in vacuum, sustained emission, or repeated I-V tests [130, 158, 159]. All of the FE data shown here, unless otherwise noted, is the first emission of the samples without conditioning. The I-V test process could contribute to the conditioning process, but a standard process has yet to be developed. For the cathode array work, a UV photodesorption system was developed to remove moisture in vacuum without baking. This process is further discussed in Section 4.5.

Various other I-V tests were made during the CFEA development process and 81 samples were tested multiple times for the cathode array work, reported in Section 4.5. The best emission metrics were achieved in collaboration with the Air Force Institute of Technology (AFIT) where slightly different testing parameters were used. Normally emission tests are controlled using the cathode current so that when there are extremely high cathode currents or there is cathode current at unrealistically low voltages for field emission (< 20 V), the sample is considered shorted and the test is terminated. The testing at AFIT was controlled using anode current. The presence of anode current is the only way to definitively confirm FE because the anode is physically separated from the CFEA. For the AFIT testing, as long as anode current was achieved, testing continued, even if large cathode currents were observed. This difference of testing at AFIT allowed tests while a large proportion of emission current is going to the gate or if there is a sustained high resistance short between the gate and cathode causing constant leakage current.

The best FE results, shown in Figure 72**,** demonstrate *anode* turn-on at 140 V at an electric field of 16 V/μm. In order to prevent electrical shorting, this sample has a short CNT length that is ~9 μm from the gate. The electric field is approximated from this

spacing. The sample produced a much higher maximum anode current density of 293 μA/cm^2 at 250 V with a CFEA active area of 0.347 cm^2. The maximum current density at the cathode is more than 5 times higher than the anode, producing 1.68 mA/cm^2 at 250 V.

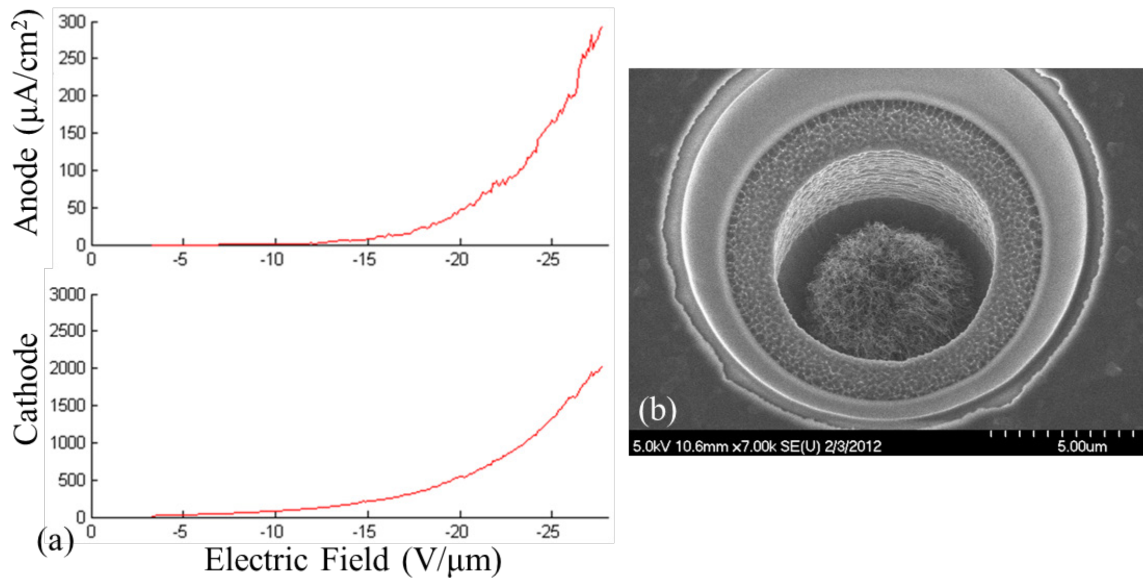


Figure 72: Sample W135 4c75b showing the best FE achieved. (a) I-V test to 250 V with anode and cathode current density on top and bottom, respectively. (b) SEM of the sample showing CNT growth.

Analysis shows that on average 89% of the current goes to the gate, 8% to the anode, and 3% is lost (electrons not collected at the anode or gate). Thus, a majority of the electrons that make it past the gate are captured by the anode, but most of the electrons are captured by the gate. Since FE is occurring, it is assumed a majority of the gate current is from field emitted electrons with a small contribution of leakage current. The high proportion of gate current is attributed to the very short CNT growth, which gives a longer distance for the electrons to disperse and collide with the gate. Typically, Spindt based cathodes that are fabricated with the emitter parallel to the gate have a much

higher proportion of electrons captured by the anode [119]. If a higher proportion of anode current can be achieved, then a superior CNT triode electron source may be realized, especially considering the pitch could be much smaller than the 75 μm feature pitch of this sample.

It should be noted that current density is reported in terms of actual area of the array, not the total area of CNT growth, in order to give a realistic estimation of the current density. However, this does not allow for comparison of the turn-on field to other planar CNT electron sources. For the sake of comparison, current density calculated using just the CNT growth area gives an anode turn-on at ~5 V/μm with a maximum anode current density of 136 mA/cm^2. This turn-on field is slightly high compared to the 1-4 V/μm that is observed in the literature for other CNT FE devices [97, 117, 175]. This difference could be due to the very short CNT growth and electrostatic screening of the electric field by the walls of the Si pit.

Other CNT field emitters have a turn-on potential that is normally much higher, ranging from ~150-2000 V, due in part to larger electrode separations (such as in diode configurations) [117, 128, 175, 176]. These FE tests exhibit the capabilities of this triode design, demonstrating a low voltage turn-on (140 V) and sufficient current densities compared to other devices.

4.4.2 Electrical Burnout

As mentioned earlier, electrical shorting during FE testing is a common occurrence, but it is often difficult to tell when an electrical short develops and even depends on how an electrical short is defined. In this type of triode design, it is expected that some current will be lost to the gate, but what isn't known is what proportion of this

current is from field emitted electrons or leakage current. There is often a small amount of current to the gate that has an ohmic response, meaning there is a linear response from voltage input. This current can be considered leakage because FE has an exponential response. However, this leakage is often equivalent to having a 10–100 MΩ resistor between the gate and cathode. Thus, an electrical short isn't an entirely accurate description and FE can still occur during this short. Given the design of the CFEA with CNTs below the gate, it also isn't unexpected that some field emitted electrons will be lost to the gate.

An alternative way to plot the standard I-V tests shown previously is to plot current versus time, with the cathode potential co-plotted on the y-axis. This kind of plot provides much more information, as the emission response is dynamic, even at a constant potential. The plot will also show both the upward and downward potential sweep, along with any current controlled modulation.

An example of this plot is shown in Figure 73. The plot shows a stair step voltage ramp to 220 V held for 3 minutes, and then ramped down (no current controlled potential). Both the anode and cathode current are very unstable, even during constant potential, but the current quickly increases once a turn-on potential is reached. Similar to past tests, the anode current is only a small proportion of the total cathode current. At the end of the test the anode and cathode current degrades, and there is an ohmic response in the cathode current, circled in black. This cathode response isn't entirely linear, but the stair step response could indicate an ohmic portion, potentially from a high resistance electrical short, especially since there is current below the original turn-on from the start of the test.

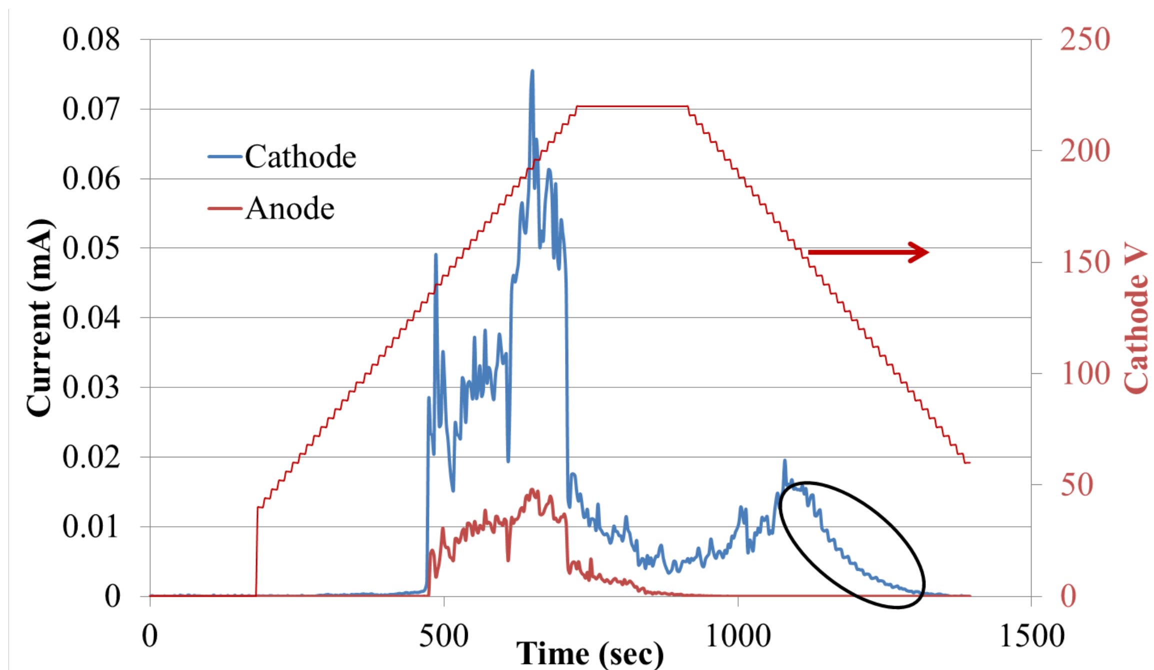


Figure 73: An alternative plot of the I-V test for sample W135 4s200b. Note the sporadic emission over time, and the ohmic current response circled in black.

This electrical shorting during FE testing can range from the high resistance short seen at the end of Figure 73, to a spontaneous low resistance short in the middle of a test, indicated by a current spike. An electrical burnout procedure was developed that proved to be quite successful in reversing this shorting to allow for more FE testing. From the cathode array testing of batch I discussed in Section 4.5, 32 individual burnout tests were conducted on 26 different CFEAs with a success rate of 69%. The burnout was not permanent, as more FE testing often led to more shorting. In addition, the burnout procedure sometimes led to permanent shorting the sample. However, the process is still highly effective, as it drastically reduces the failure rate of CFEA since the samples would otherwise be useless. It is proposed that resistive shorts in the chip are burned out because they are very small, such as from a CNT. Thus, there is an extremely high current density in the short which causes enough heating to remove it.

4.4.3 Lifetime Measurements

One electronic package was lifetime tested while the cathode array was being manufactured. Two chips were tested simultaneously on a single package: SMC-001 50.3.2 and 50.3.1. After an initial I-V test, the lifetime test shown in Figure 74 was performed. This experiment also served as a test of the current controlled software, where once a threshold current was reached the cathode voltage would automatically be modulated to keep a constant current.

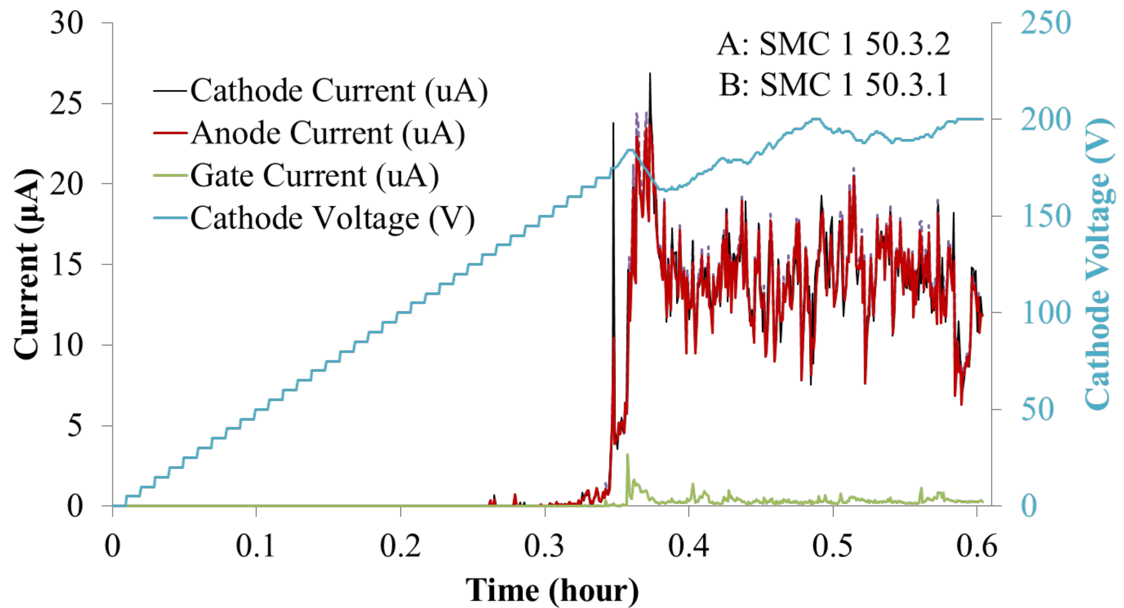


Figure 74: Lifetime test from two chips on one package showing sustained emission for 15 minutes and a large anode to gate current.

The cathode current was initially ramped to 15 µA (10 µA/cm^2) at 180 V, after which the voltage was software controlled up to 200 V. Emission was sustained for 15 minutes before current spiked due to a presumed short and the test was automatically stopped. The emission current is very sporadic, but produced the best proportion of anode

to gate current achieved than in any other test. This large ratio, up to 15 times the gate current, shows that most of the electron emission escaped the gate. It is unknown why these samples had a better anode current ratio than any other test, since the CFEA design and CNT growth did not significantly change.

Post test analysis showed that sample 50.3.2 remained an open circuit while 50.3.1 shorted to a 0.3 kΩ resistance during the test. Since both CFEAs shared the same contacts on the package, the short affected the entire package. On future testing, only one CFEA is mounted to each package so that each CFEA can be tested until it fails.

The longest continuous lifetime achieved was conducted at AFIT using their altered test procedures, and is shown in Figure 75. A constant emission of 25–50 $\mu A/cm^2$ at the anode and 1-1.5 mA/cm^2 at the cathode is achieved for over 167 minutes at a constant potential of 220 V. Significant instability is observed which makes it difficult to discern any gradual degradation. However, no sudden degradation is observed at the anode. In addition, large jumps in the cathode current are not reflected in the anode current. This data shows that FE in the CFEA can be sustained over extended periods of time.

Several other lifetime tests were conducted internally and at AFIT. The additional internal lifetime tests were conducted on the cathode array and are reported in the following section. The work conducted at AFIT includes multiple I-V and lifetime tests on the same CFEAs, and has shown cumulative emission longer than 100 hours on a single CFEA. This achievement demonstrates the potential continuous lifetime of the CFEAs.

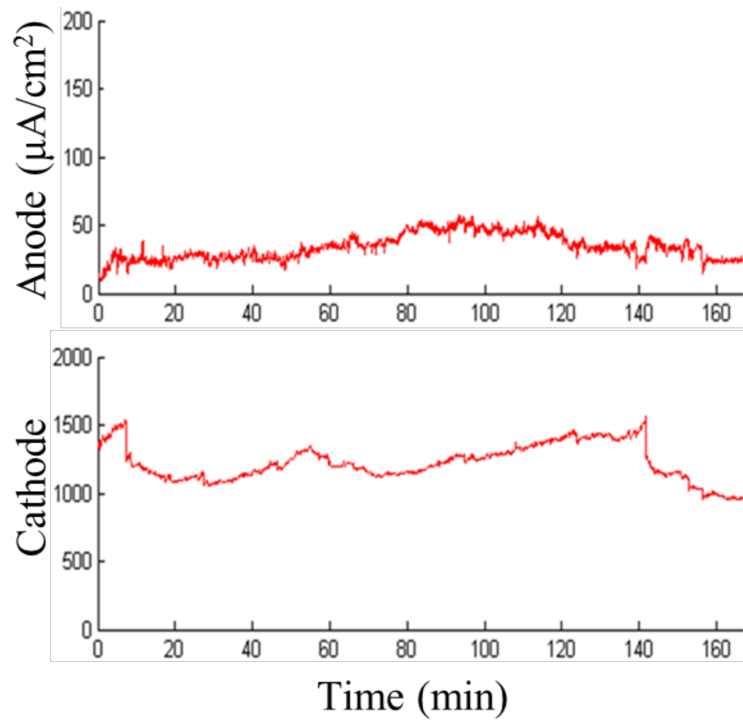


Figure 75: Constant voltage emission for W135 4c75b at a potential of 220 V over 167 minutes shows unstable yet constant field emission over time.

4.5 Cathode Array Emission

A total of 79 CFEAs were tested in two batches in the cathode array apparatus. In each batch, every CFEA was at least characterized in an I-V test, while open circuit samples were further tested with more I-V and/or lifetime tests. Burnout techniques were used throughout testing to reverse shorting that developed during a test. Notable FE and lifetime data metrics achieved.

4.5.1 Cathode Array Batch I

A total of 40 CFEAs (1 per package) were tested in batch I in the cathode array. The batch underwent an initial I-V test, followed by unloading, analysis of the chips, and a burnout of any shorted chips in air. All open circuit chips were I-V tested a second time, followed by a burnout in vacuum, and a third and fourth I-V test of all open circuit chips.

Each CFEA underwent an initial I-V test where each package was individually biased to a cathode current of 7.5 μA (10 μA/cm^2) or a maximum of 200 V. The result of the test is summarized in Table 5. After this test, it was found that 14 of the packages had a low resistance, metallic-like short before the test. This short was found to be due to a contact between the board socket and the bottom of the package when the package was pushed down too far (indicated by INF in the "loosen package" column). All of these packages changed to an open circuit by slightly moving the package up. There were also 7 packages that were an open circuit after the characterization test, giving 21 chips that are still open:

- 19 CFEAs electrically shorted after the I-V test
- 14 CFEAs had a contact short to the board socket before the I-V test
- 7 CFEAs are an open circuit after the I-V test (red data in Table 5)
    - 4 showed gate current without anode current
    - 2 showed no gate current (no current response)
    - 1 produced anode current (package 8, bolded)

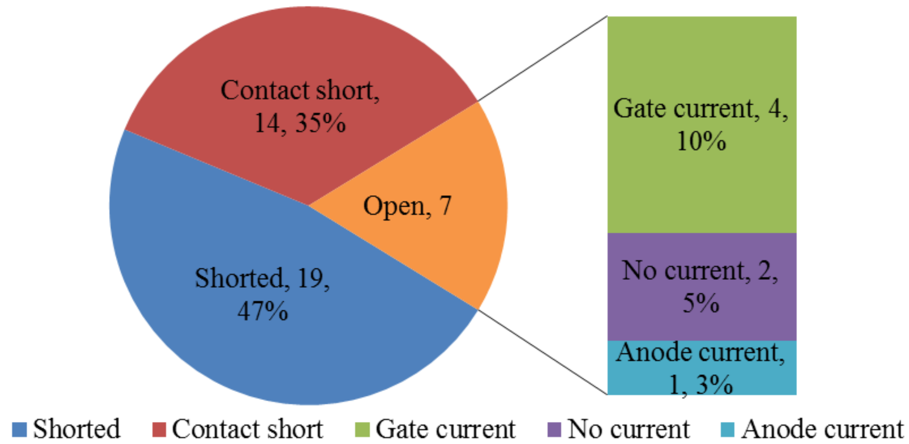


Figure 76: Schematic of the I-V test 1 results from cathode array batch I.

The naming convention used for the SMC wafers is based off of the pitch. The first number gives the pitch, either 50, 100, or 200 µm. The second and third numbers gives the row and column of the chip for that pitch on the wafer, respectively. Thus, sample "200.2.4" has a 200 µm pitch on the 2nd row and 4th column of the 200 µm samples.

Most of the data from the first I-V test are very similar, and include samples that have anode and gate current, only gate current, no current, and are shorted. Typical plots of a CFEA with only gate current and no current are shown in Figure 77 and Figure 78, respectively. For any shorted samples, the VI software quickly shuts down because it is set to terminate tests where emission occurs below a threshold voltage. The small amount of cathode current seen at all potentials is present in all data and is attributed to equipment noise. Figure 77 shows turn-on at 95 V with no anode current. Figure 78 shows no gate current even up to 200 V.

Table 5: Summary of the first I-V test from batch I. The 1st column indicates the package number. The 4th column gives the result of the I-V test, where a resistance value is given if the CFEA was shorted before the test. "INF" in the 6th column indicates that an open circuit after loosening the package on the circuit board.

Pkg #	CFEA Wafer	CFEA Sample	I-V Test 1 Results	Ω	Loosen Package	Comments
1	2	200.2.4	0.8 Ω	0.6	INF	
2	1	50.4.2	emit @ 10V	1M		
3	2	100.3.7	emit @ 17V	32M		rebond 100.3.7
4	8	100.2.7	0.8 Ω	0.4	INF	B: 5Mohm short - bond gate to package
5	8	50.4.2	0.8 Ω	0.5	INF	rebond
6	8	200.2.4	gate I, no short	INF		break 100.1.5, leave on 200.2.4 (heated)
7	8	100.2.6	emit at 10V	3.7M		short B to package
8	**8**	**100.1.8**	Anode I, no short	1.1M		short B to package
9	8	200.3.2	emit at 10V	3.4M		
10	8	200.4.4	gate I, no short	63M		
11	8	100.1.3	3.9M, mA at gate	5M		
12	8	100.3.7	anode I, short	2.4M		short reversed- rebond
13	8	50.3.1	Anode I, no short	26M		
14	8	50.2.2	emit at 12V	5.6M		
15	8	50.3.2	0.9 Ω	0.5	INF	
16	8	200.4.3	gate I, no short	149M		
17	8	200.3.3	INF, no gate I	0.4	INF	
18	8	100.1.6	1.1 Ω	0.4	INF	
19	8	100.2.4	1.1 Ω	0.4	INF	
20	8	100.2.5	1.2 Ω	0.4	INF	
21	8	100.3.3	1 Ω	0.4	INF	
22	8	100.3.4	gate I, no short	INF		
23	8	100.2.2	INF, no gate I	INF		
24	8	100.1.2	1 Ω	0.4	INF	
25	9	100.3.5	emit at 10V	2M		
26	9	200.4.3	emit at 13V	2.5M		
27	9	100.3.7	gate I, no short	INF		
28	9	100.1.2	INF, no gate I	INF		
29	9	200.2.4	INF, no gate I	INF		
30	9	200.3.3	1.2 Ω	0.4	INF	
31	9	100.2.3	Anode I, short	~160M		
32	9	100.2.7	Anode I, short	95M		
33	9	200.2.3	emit at 10V	1.7M		
34	9	50.4.1	1 Ω	0.4	INF	
35	9	200.3.4	1 Ω	0.4	INF	
36	9	100.1.6	emit at 15V	4.5M		
37	9	100.2.5	emit at 10V	.5M		
38	9	100.2.4	1.1 Ω	0.4	INF	
39	9	50.3.3	emit at 30V	2.4M		
40	9	100.3.4	emit at 5V	37k	0.2M	

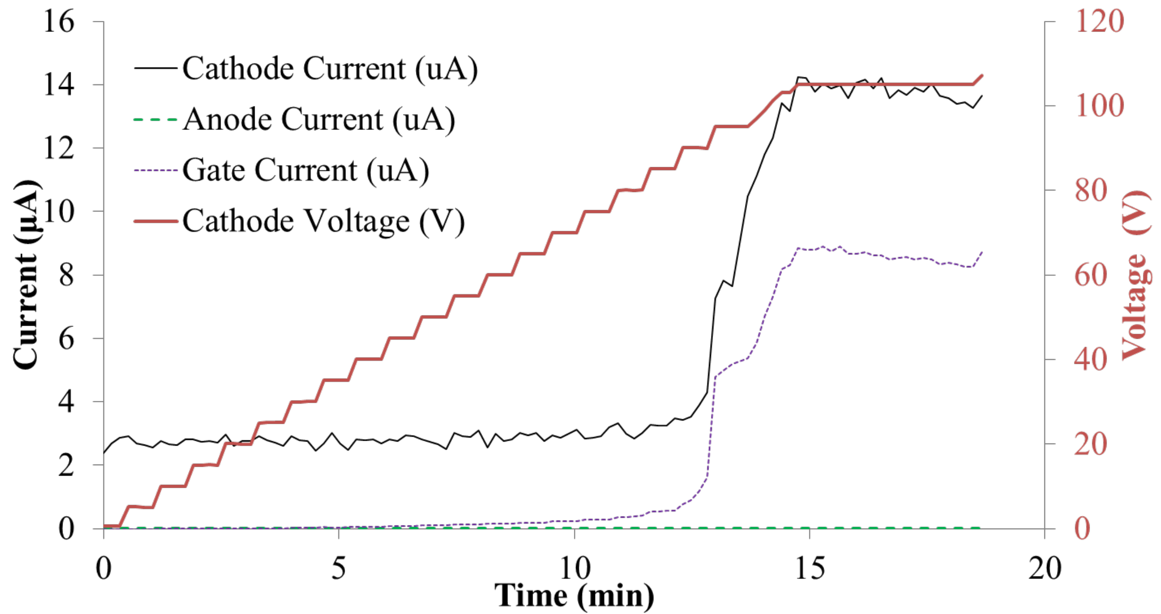


Figure 77: Typical plot of an I-V test showing only gate current on sample SMC-009 100.3.7. Cathode current before turn-on is attributed to equipment noise.

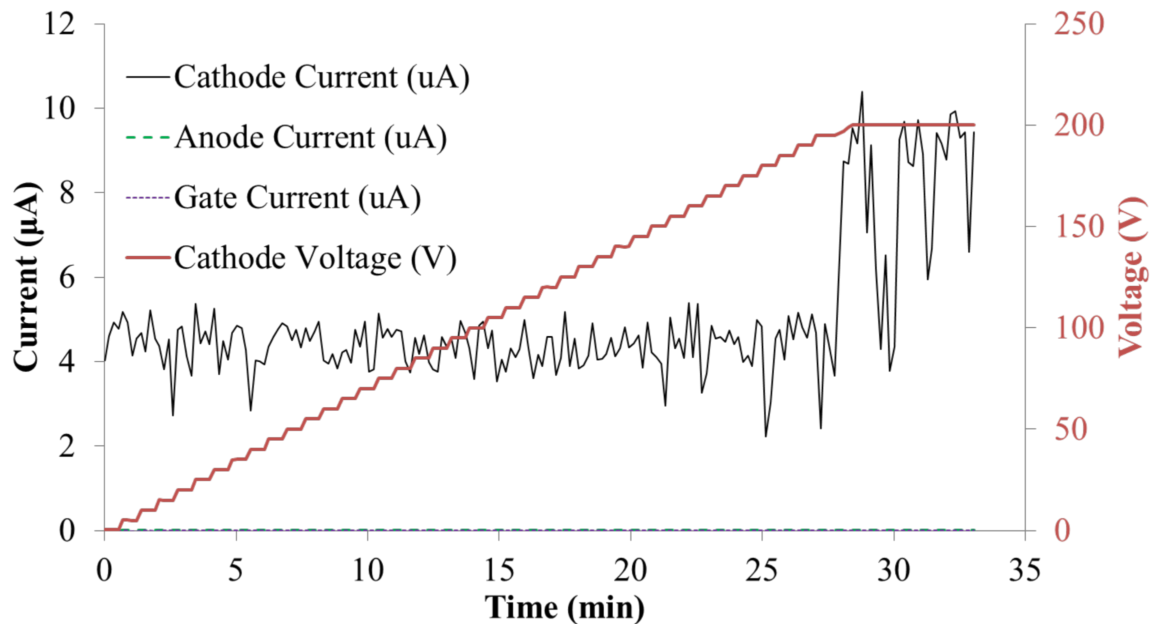


Figure 78: Typical plot of an I-V test showing no gate current on sample SMC-008 200.3.3. The constant cathode current is attributed to equipment noise.

A lifetime test was performed on package 8 (SMC-008 100.1.8), which is the only open circuit sample that produced anode current in the first I-V test. Plots of both the I-V and lifetime test are shown in Figure 79. This CFEA was not shorted after the characterization test, and showed the best emission of the batch. The I-V test produced gate current from 40-100 V with a maximum of 7.7 μA, and anode current from 95-100 V with a maximum of 7.7 μA.

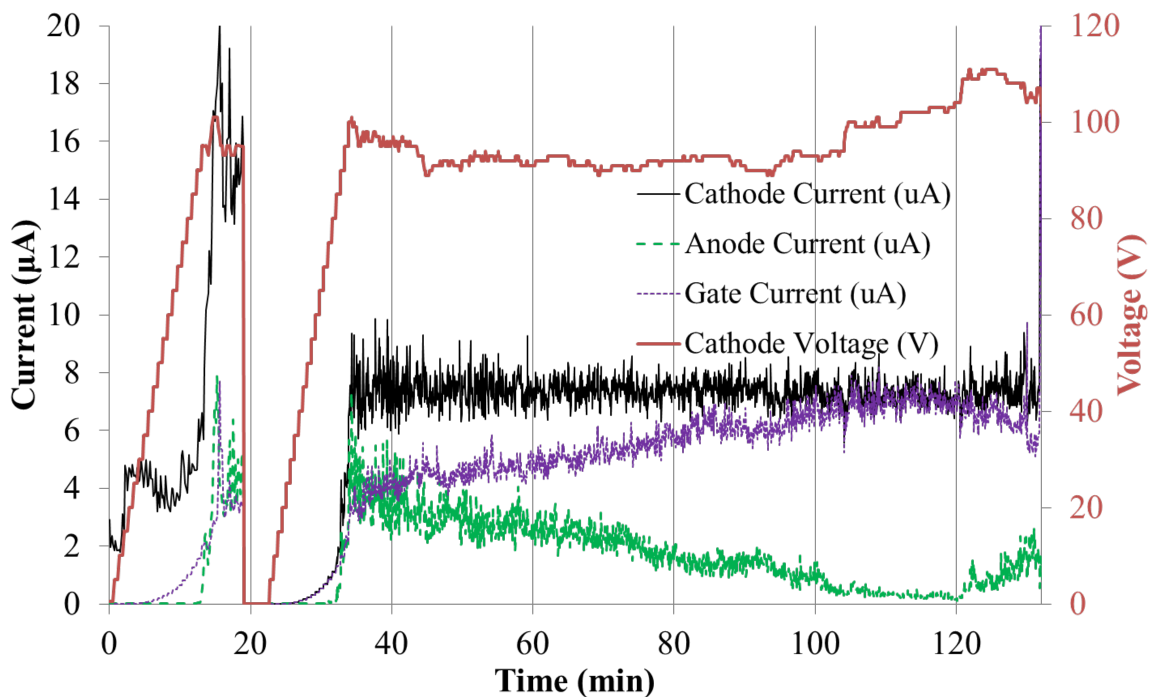


Figure 79: I-V and lifetime test of SMC-008 100.1.8 plotted together. About 7.5 μA of anode current was sustained for 100 minutes at 85-110 V.

This sample demonstrates very low potential emission and a higher proportion of anode current. During the lifetime test, the anode current is initially greater than the gate current and gradually degrades to a smaller proportion. The initial anode current proportion is favorable for efficient emission. The lifetime test shows degradation of the anode current over time, but little degradation in the total cathode current. The test

produced gate current from 70-110 V with a maximum of about 10 μA and anode current from 85-110 V with a maximum of 7.3 μA. Emission was sustained for about 100 minutes before electrically shorting.

A total of 20 CFEAs from the first I-V test and the above lifetime test were shorted with a resistance ranging from 0.2 MΩ to 150 MΩ. Table 6 contains a summary of the analysis performed on these 20 chips after they were unloaded. Different types of arcing and melting damage was observed in the etch pits on five of the chips (green comments in Table 6). This damage is discussed in the next section. A burnout procedure was conducted in air. Of the 20 chips:

- 3 CFEAs produced gate current without anode current
- 5 CFEAs produced anode current
- After burnout on 19 CFEAs (1 changed to an open circuit on its own):
    - 14 changed to an open circuit - 3 of which showed damage
    - 5 remained shorted (red data in Table 6) - 2 of which showed damage

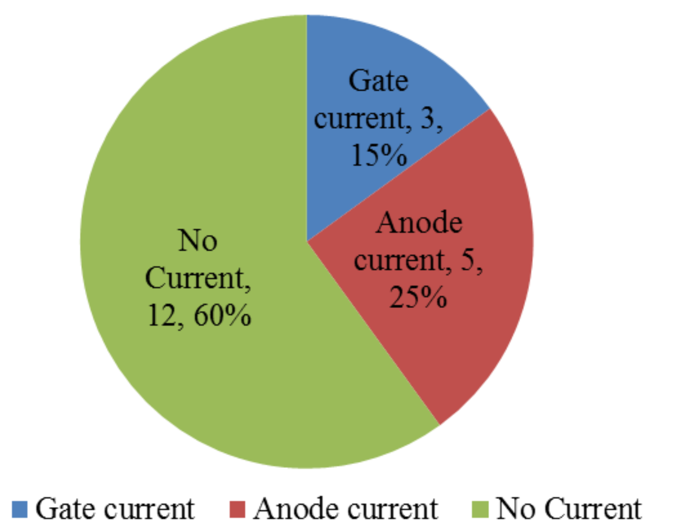


Figure 80: Schematic of the results from the 20 shorted CFEAs from I-V test 1.

Table 6: Summary of results and analysis of the 20 shorted chips from I-V test 1.

Pkg #	CFEA		I-V Test 1 Result	Resistance (Ω)	Anode I?	Gate I?	SEM	Burnout Result (Ω)	Comments
	Wafer	Sample							
2	1	50.4.2	emit @ 10V	1M				INF	2 bonds off, dirty, OM - good
3	2	100.3.7	emit @ 17V	32M				INF	OM- good
7	8	100.2.6	emit at 10V	3.7M				INF	OM- good
8	8	100.1.8	Anode I, no short	1.1M	Y		Y	INF	new looking arced pits, EDS normal
9	8	200.3.2	emit at 10V	3.4M			Y	INF	OM- arc at litho defect, 1 pit; SEM - melted pit
10	8	200.4.4	gate I, no short	INF		Y			OM- good; changed on own to INF
11	8	100.1.3	3.9M, mA at gate	5M				INF	OM- good
12	8	100.3.7	anode I, short	2.4M	Y		Y	100M	OM- good
13	8	50.3.1	Anode I, no short	26M	Y		Y	15M	OM- good
14	8	50.2.2	emit at 12V	5.6M				INF	OM- good
16	8	200.4.3	gate I, no short	149M		Y		170M	OM -good
25	9	100.3.5	emit at 10V	2M				INF	OM- good
26	9	200.4.3	emit at 13V	2.5M				INF	OM- good
31	9	100.2.3	Anode I, short	~160M	Y			115M	OM - ~10 arc pits, poly blown out
32	9	100.2.7	Anode I, short	95M	Y			INF, high I	high leakage, OM - ~8 arced pics, poly blown out
33	9	200.2.3	emit at 10V	1.7M				INF	OM- good
36	9	100.1.6	emit at 15V	4.5M				INF	OM- good
37	9	100.2.5	emit at 10V	.5M				INF	OM- good
39	9	50.3.3	emit at 30V	2.4M			Y	INF	OM- 2 arced pits SEM - arcs in pits
40	9	100.3.4	emit at 5V	.2M-INF				INF	IR test: low I, now INF, OM - good

After the burnout test, 35 of the 40 CFEAs from batch I were recovered as an open circuit. All of these 35 chips were reloaded in the cathode array for more testing. An initial 2nd I-V test was run again to a cathode current of 7.5 μA or a maximum of 200 V, followed by a burnout of shorted chips while still in vacuum. A summary of this testing is in Table 7. Of the 35 chips:

- 8 CFEAs remained an open circuit (red data in Table 7)
    - 3 had no current response (no gate current)
    - 5 produced gate current without anode current
- The remaining 27 CFEAs were electrically shorted
    - 10 produced anode current
    - 17 produced gate current without anode current
    - 13 of the 27 were high resistance and were burned out in vacuum
        - 8 changed to an open circuit
        - 3 had a resistance > 100 MΩ
        - 2 ended with a resistance < 1 kΩ (red data in Table 7)

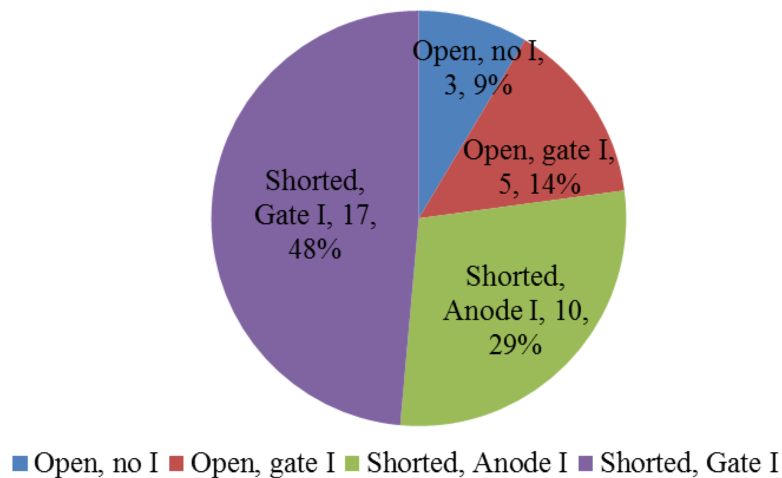


Figure 81: Schematic of the I-V test 2 results from cathode array batch I.

Table 7: Summary of the 2nd I-V test and burnout in vacuum conducted in the 35 remaining CFEAs from batch I.

Pkg #	CFEA Wafer	CFEA Sample	I-V Test 2 Results	Anode I?	Gate I?	Burnout (V, Ω)
1	2	200.2.4	gate spike/short	Y	Y	175V, INF
2	1	50.4.2	emit at 8			
3	2	100.3.7	emit at 5V			
4	8	100.2.7	emit at 10V			100V, INF
5	8	50.4.2	emit at 10V			
6	8	200.2.4	INF, low gate I		Y	
7	8	100.2.6	emit at 12V			125V, INF
8	8	100.1.8	anode, spike	Y	Y	
9	8	200.3.2	short 55V		Y	
10	8	200.4.4	emit 30 V- ok	Y		172V, short (32)
11	8	100.1.3	emit at 14	Y	Y	74V, INF
14	8	50.2.2	emit at 10			124V, INF
15	8	50.3.2	emit at 5			
17	8	200.3.3	INF, no gate I			
18	8	100.1.6	15M,gate I early		Y	90V, short (68)
19	8	100.2.4	short 55V			
20	8	100.2.5	short, 230uA	Y	Y	
21	8	100.3.3	emit at 5			30V, INF
22	8	100.3.4	gate short		Y	80V, 130M
23	8	100.2.2	INF, low gate I		Y	
24	8	100.1.2	emit at 10			95V, INF
25	9	100.3.5	anode, short	Y	Y	
26	9	200.4.3	emit at 10			
27	9	100.3.7	INF, gate leak		Y	
28	9	100.1.2	INF			
29	9	200.2.4	INF, low gate I		Y	
30	9	200.3.3	anode @ gate spike	Y	Y	60V, 120M
33	9	200.2.3	short			
34	9	50.4.1	emit at 10			45V, INF
35	9	200.3.4	INF, no gate I			
36	9	100.1.6	emit at 5			
37	9	100.2.5	emit at 10			
38	9	100.2.4	bad short, mA	Y	Y	
39	9	50.3.3	bad short	Y	Y	
40	9	100.3.4	emit at 24			70V, 145M

The successful burnout test in the vacuum chamber confirms that the process does not need to be performed in air. This process greatly saves time because the procedure can be run within the chamber without modification or a need to vent.

The emission results from the 2nd I-V test showed a variety of results, similar to what was observed in the first test. Figure 82 shows an emission plot different from Figure 77 and Figure 78 where low potential emission occurs and then the sample shorts. The sample shows ~1 µA of anode current starting at an incredibly low 55 V, followed by a large spike in gate current, and termination of the test.

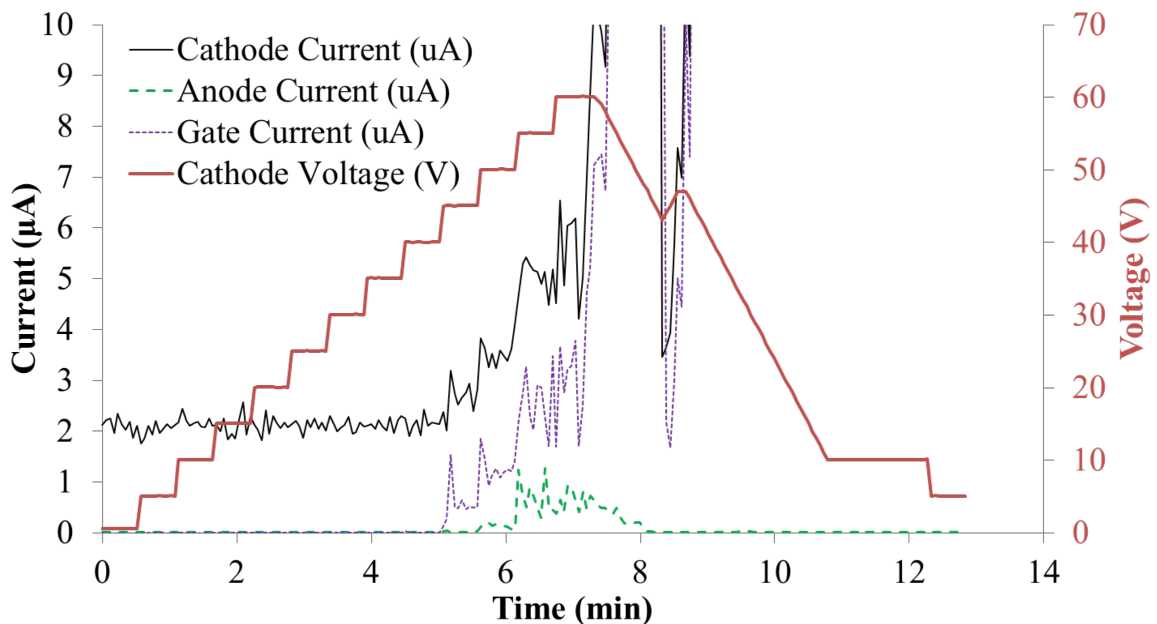


Figure 82: Emission plot from I-V test 2 (SMC-009 100.3.5) showing anode current starting at a very low 55 V, followed by a spike in gate current (up to 80 µA).

Sample SMC-008 100.1.8, which showed low potential anode current in the first test and was lifetime tested, again showed great emission in the 2nd I-V test, similar to Figure 82. Anode current starts at a very low 50 V (lower than in its 1st I-V test) and

reaches a maximum 3 μA at 95 V. Gate current starts at 50 V and spikes to 22 μA at 95 V. The anode current continued until the spike in gate current caused the software to drop the potential. The current spike may not have been due to an electrical short because anode current was still being produced.

After the 2nd I-V test and subsequent burnout in vacuum, 18 chips (16 open circuit and 2 high resistance burnouts) were subjected to a 3rd I-V test, as summarized in Table 8. This test resulted in:

- 8 CFEAs remained an open circuit (red data in Table 8)
    - 4 produced gate current without anode current
    - 2 produced anode current and gate current
    - 2 had no current response (no gate current)
- 2 CFEAs have a resistance > 100 MΩ with gate current
- 8 CFEAs were shorted
    - 2 produced anode current

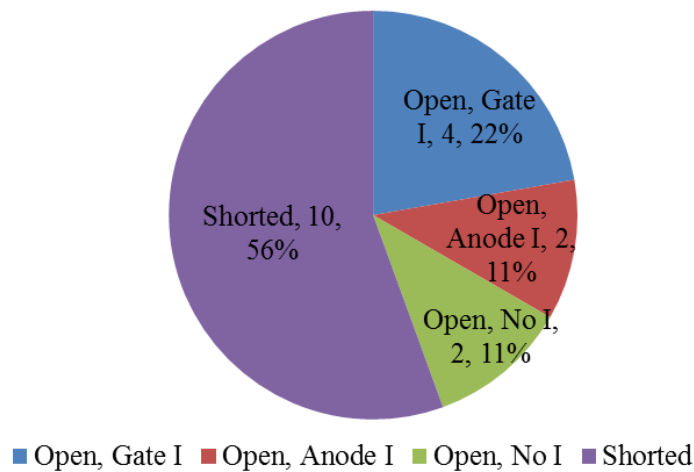


Figure 83: Schematic of the I-V test 3 results from cathode array batch I.

Again, a variety of results were obtained similar to the other I-V tests. After this test, it was noticed that many of the open circuit chips had very low or no emission current, even at the maximum 200 V potential. In order to induce more current, a final I-V test, summarized in Table 8, was conducted on 7 of the 8 open circuit chips with a maximum potential of 250 V. This test resulted with:

- 6 CFEAs still at an open circuit
    - 1 produced anode current
    - 5 still showed no current response
- 1 CFEA with a resistance of 77 MΩ produced gate current (Table 8 red data)

The high potential I-V test was unsuccessful in generating more current in the open circuit CFEAs. However, it did show that some chips can withstand the higher potential. Table 8 also includes general comments and optical microscopy comments from the 35 CFEAs that were tested after the 1st I-V test. These comments include any damage that was observed on the chips and is discussed in the following section.

All of the testing on the batch I CFEAs show very inconsistent emission data. A high proportion of anode current and a 100 minute lifetime was achieved in SMC-008 100.1.8. In addition, some samples showed very low potential anode current. The burnout procedure was shown to be highly successful in temporarily reversing shorting. Most samples did not achieve much field emission and quickly shorted. These deficiencies are further discussed in the next sections.

Table 8: Summary of the 3rd I-V test, high V test, and comments on the 35 remaining CFEAs from batch I.

Pkg #	CFEA Wafer	CFEA Sample	I-V Test 3 Results	Anode I?	Gate I?	High V Test (250V)	Ω @ GTRI	Comments	OM Comments
1	2	200.2.4	116M (65V emit)		Y		INF	AE 2nd burn 270V, 20M	Dozens of poly melt damaged pits.
2	1	50.4.2					2M		Lots of crud. Some distressed poly
3	2	100.3.7					40M		Minor poly scratches
4	8	100.2.7	22M (emit 7V)		Y		INF	good growth	4 pits with poly melt damage.
5	8	50.4.2					6.5M		One area btw 4 pits with arc damage
6	8	200.2.4	INF, low gate I		Y	INF, no I	INF	not emitting, good growth	5+ pits showing poly melting.
7	8	100.2.6	1.9M (5V emit)		Y		2.1M	short, good growth	2 pits with poly melt damage.
8	8	100.1.8	33M (15V emit)		Y		~46M	test 2: anode I @ 50V!!!!	arc damage from 1st test.
9	8	200.3.2					0.8M		pit & defect arc from 1st test.
10	8	200.4.4					INF	now ok?	2 processing defects arc damage. >12 pits poly damage.
11	8	100.1.3	2.9M (10V emit)		Y		3.7M	short, good growth	poly scratches and 1 large defect maybe damage
14	8	50.2.2	2.6M (10V emit)	Y	Y		3.2M		>2 pits poly melt damage. distressed poly regions
15	8	50.3.2					1.3M		Scratch connecting poly and contact
17	8	200.3.3	INF, no I			INF, no I	INF	no emission	
18	8	100.1.6					60	shorted on burnout	1 pit poly melt damage. Large poly scratch melt damage
19	8	100.2.4					2M		Some poly scratches.
20	8	100.2.5					0.8M		Processing defect arc damage near edge
21	8	100.3.3	INF, 50V anode	Y	Y		0.6M	why short?	Processing defect arc damage in array, Dicing damage
22	8	100.3.4	93M (20V emit)		Y		7M		3+ pits with 'poly melt' type damage.
23	8	100.2.2	INF, low gate I		Y	INF, no I	INF	no emission, descum but has CNTs	Some distressed looking poly regions around pits.
24	8	100.1.2	INF, I spike	Y	Y	INF, anode	105M	life test after 250V char - 280V, 47M	5+ pits poly melting. Appears along scratched area
25	9	100.3.5					2.8M		Some ply scratches and significant crud.
26	9	200.4.3					2M		Scratch connecting poly and contact near chip ID
27	9	100.3.7	INF, gate leak		Y	77M	150M	no emission, descum but has CNTs	One pit with 'poly melt' damage
28	9	100.1.2	INF, no I			INF, no I	INF	AE 2nd burn 40V, dec 5M; no emission	poly melt at precessing defect near edge, Au in damage
29	9	200.2.4	INF, low gate I		Y	INF, no I	INF	no emission, descum but has CNTs	
30	9	200.3.3	115M (15V emit)		Y		35M	AE 2nd burn 60V, dec 7M	Long scratch connecting contact and poly in feature area.
33	9	200.2.3					3M		
34	9	50.4.1	1.5M (10V emit)	Y	Y		~118M		dirty surface. large processing defect shows Au
35	9	200.3.4	why not?				INF		Some scratches in poly
36	9	100.1.6					INF		
37	9	100.2.5					INF	1 bond off	processing damage at contact/poly interface.
38	9	100.2.4					0.3M		
39	9	50.3.3					1.5M		Arc damag from 1st test
40	9	100.3.4	1.5M (10V emit)		Y		67M		

4.5.2 Cathode Array Batch II

A second batch of CFEAs were fabricated and packaged for FE testing and exposure to a Hall effect thruster (HET), which is discussed in Section 4.7. This batch contains 39 open circuit CFEAs for FE testing. The parameters of batch II were slightly different because of the integration with the HET test. The VTF-2 facility was used instead of the Bell Jar 2 facility. The VTF-2 facility uses a large cryogenically pumped chamber as opposed to a diffusion pumped chamber. The use of a different pump enabled comparison to see if diffusion pump oil backstreaming could be a cause of the periodic shorting and poor emission performance observed in batch I. The Bell Jar 2 facility uses the UV photodesorption system, which allows testing close to the base pressure of the diffusion pump, at about 3 x 10^{-7} Torr. At this pressure, diffusion oil backstreaming is a likely occurrence, causing oil from the diffusion pump to enter and contaminate the chamber [177]. This potential failure mechanism is further discussed in Section 4.6.5.

The I-V tests for batch II were conducted without an anode, which would normally be in front of the cathode array, because the HET serves as an anode in the HET test. Thus, only cathode and gate current were measured. This lack of an anode results in less data and the inability to decisively confirm FE, but allowed the I-V and HET tests to be conducted sequentially without venting.

The 39 CFEAs first underwent an initial I-V test to a cathode current of 7.5 µA (10 µA/cm^2) or a maximum of 200 V, summarized in Table 9. This test is the same as in batch I and was used to determine initial performance and to compare emission.

Interestingly, the I-V test showed a much lower shorting rate than in batch I, but emission performance metrics were about the same. The I-V test resulted in:

- 32 CFEAs still an open circuit
    - 9 had no emission response
    - 23 produced gate current
- 5 CFEAs had low voltage emission, indicating possible intermittent shorting
- 2 CFEAs shorted at 7.2 and 2.5 MΩ (red data in Table 9)

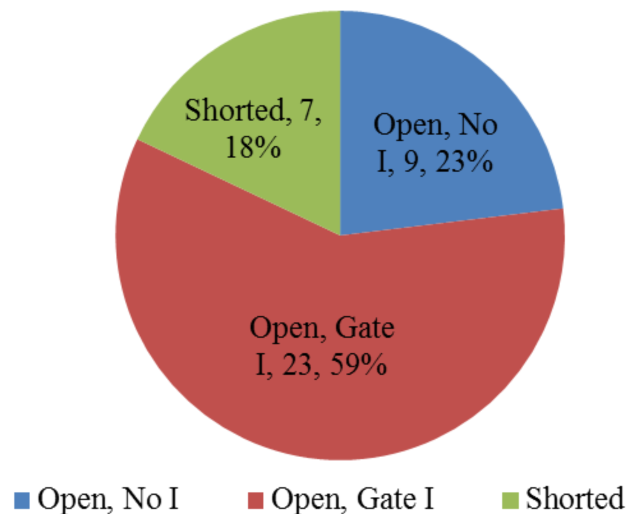


Figure 84: Schematic of the I-V test 1 results from cathode array batch II.

The emission data was much more consistent than the other I-V tests in batch I. This test had 82% of the CFEAs remain an open circuit as opposed to 23-44% from I-V testing in batch I. In addition, many CFEAs in batch II showed stabilized emission and a very low turn-on at 70-80 V. This greatly improved stability and reduced shorting could be attributed to the different high vacuum pump used in the VTF-2 facility.

Table 9: Summary of the I-V test conducted on the 39 CFEAs from batch II.

Pkg	CFEA		I-V Test	Gate	Resistance	Life Test
#	Wafer	Sample	Results	I	(Ω)	Attempt
41	12	50.2.3	7uA @ 50V	Y	INF	
42	12	50.3.1	8uA @ 70V	Y	INF	Y
43	12	50.3.2	10uA @ 140V	Y	INF	Y
44	12	50.3.3	<1uA @ 200V		INF	
45	12	100.1.4	7uA @ 70V	Y	INF	Y
46	12	100.1.5	N	Y	INF?, 10V emit	
47	12	100.1.6	N	Y	7.2M, 10V emit	
48	12	100.2.3	sporatic I	Y	INF	
49	12	100.2.4	8uA @ 80V	Y	INF	
50	12	100.3.5	7uA @ 70V	Y	INF	
52	12	200.2.4	~8uA @ 80V	Y	INF	
53	13	50.3.1	8uA @ 65V	Y	INF	
54	13	50.4.1	<1uA @ 200V		2.5M	
55	13	50.4.2	<1uA @ 200V		INF	
56	13	50.4.3	7uA @ 140V	Y	INF	Y
57	13	100.1.2	~6uA @ 160V	Y	INF	Y
58	13	100.1.3	8uA @ 110V	Y	INF	Y
59	13	100.1.4	~8uA @ 140V	Y	INF	
60	13	100.1.5	<1uA @ 200V		INF	
61	13	100.1.7	sporatic, low I	Y	INF, low gate I	
62	13	100.1.8	~8uA @ 160V	Y	INF	Y
63	13	100.3.2	<1uA @ 200V		INF	
64	13	100.3.3	8uA @ 100V	Y	INF	Y
65	13	100.3.7	~7uA @ 140V	Y	INF	Y
66	13	100.2.2	~8uA @150V	Y	INF	
67	13	100.2.6	~2uA @ 200V	Y	INF, low gate I	
68	13	200.1.4	no test	n/a	malfunction	
69	13	200.2.4	<1uA @ 200V		INF	
70	13	200.3.2	~9uA @ 170V	Y	INF	
71	13	200.3.4	<1uA @ 200V		INF	
72	13	200.4.4	8uA @ 65V	Y	INF, 60V emit	
73	13	50.2.1	8uA @ 60V	Y	INF, 60V emit	
75	13	100.1.6	6uA @ 115V	Y	INF	Y
76	13	100.2.4	8uA @ 115V	Y	INF	
77	13	100.2.7	<1uA @ 200V		INF	
78	13	100.3.4	8uA @ 140V	Y	INF	
79	13	100.3.5	<1uA @ 200V		INF	
80	13	100.3.6	8uA @ 35V	Y	INF, 31V emit	
81	13	200.4.3	8uA @ 38V	Y	INF 38V emit	

Many CFEAs had an abrupt current spike at initial turn-on that was subsequently stabilized by the current controlled software, and could be due to a lack of a conditioning process. A typical plot is shown in Figure 85, where turn-on starts at 80 V, and is stabilized for five minutes at 70 V.

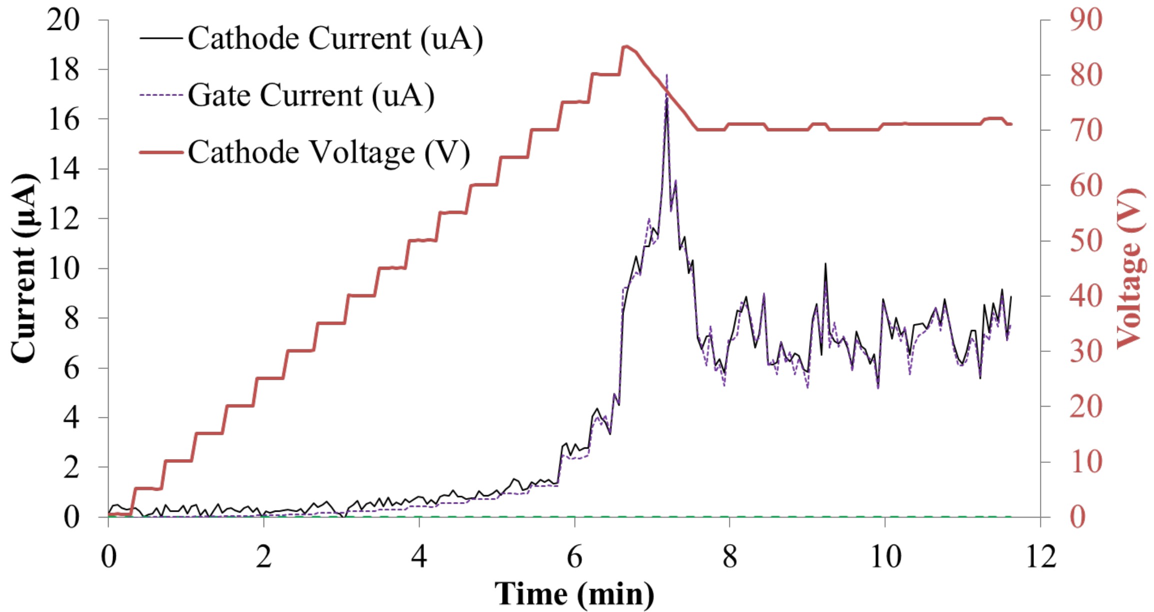


Figure 85: Typical plot from batch II (SMC-012 50.3.1) showing a turn-on spike at 80 V and stabilization for several minutes at 70 V.

As noted in a column in Table 9, a lifetime test was attempted on 10 of the open circuit CFEAs. This test was the first attempt at consecutively testing multiple chips at once (all at same bias, measuring cumulative gate current and individual cathode current). Unfortunately, problems with the software caused the test to be automatically terminated at the beginning of the test. No other FE testing was conducted on batch II because the subsequent HET test damaged the packages.

In conclusion, the cathode array emission tests demonstrated FE from 79 different CFEAs. The results, especially from batch I, indicate that the CFEAs do not easily emit large currents, which partially conflicts with AFIT test results, and could be due to the different test parameters used. In addition, the intermittent shorting observed in batch I may be due to backstreaming of diffusion pump oil contaminating the CFEAs. The CFEAs from batch II and some from batch I show particularly good performance at low potentials, demonstrating production of appreciable anode current at as little as 40 V. Lifetime measurements were achieved in excess of 100 minutes, which are significantly less than the > 100 hours achieved in the AFIT testing, and could also be potentially due to oil backstreaming or different test parameters used.

4.6 Field Emission Damage

The degradation and failure of CNTs from FE has been well studied, but mostly as individual CNTs or mats of randomly oriented CNTs [131]. FE at high currents can quickly damage the structure of a CNT and gradual degradation is often observed at low currents [12, 136-138]. CNTs can also become disconnected at the substrate during emission, suggesting mechanical failure due to tensile loading and/or resistive heating at the CNT-substrate interface [5, 136, 139]. A catastrophic failure mechanism occurs from arcing between electrodes during FE [4, 5].

There are much fewer studies on the damage and failure modes from FE testing in the Spindt-based structure. The failure modes include those for individual CNTs or CNT mats, but the cathode design is especially susceptible to arcing and electrical shorting due to the small electrode separation distance. Electrical shorting of the gate to the substrate

is a common and problematic failure mode [13, 140, 141]. Spindt, *et al.* showed melting from arcing in their metal based emitters [142]. In CNT Spindt-based structures, failure and damage have been observed due to disconnection of the CNTs from the substrate and arcing in the emission pits [6, 143]. Considering these few studies, more work is needed to understand and prevent the causes of damage in these Spindt-type emitters so their performance and reliability can be improved.

In this work, the 79 CFEAs from the cathode array testing are analyzed by optical microscopy (OM) and scanning electron microscopy (SEM) for any damage or changes to the CNT morphology [178]. This qualitative analysis is carried out on all tested chips, regardless of their emission performance. OM is used as a quick way to scan over an entire chip and inspect every emission pit to note any damage. Since the SEM is higher magnification, it is impractical to image all pits in a sample. As a result, SEM is used primarily to closely investigate any noted damage from OM, and to inspect portions of the chip.

Of the 79 CFEAs tested, 35 or about 43% show at least one type of damage after FE testing, whether or not the chip is electrically shorted. In most cases, the number of damaged etch pits is minimal – less than 15 pits per chip of the 1,800-29,000 total pits, depending on pitch. However, four chips show greater than 50 damaged pits, with a maximum amount of damage at about 5% of the pits. In addition, about half of the damaged chips were not electrically shorted, indicating that the chip design is very robust because the damage did not cause electrical shorting. From the optical and electron microscopy investigations of the CFEAs, three distinct damage modes were identified. The damaged observed is very similar to the damage seen during PECVD CNT synthesis.

4.6.1 Damage Mode I: Poly Silicon Melting

The first type of damage commonly observed is outward melting of the p-Si gate around an emission pit aperture. Figure 86 is an optical micrograph of an array of undamaged pits, with an arrow indicating one pit with the typical damage. Figure 87 shows an SEM image of a normal emission pit and a damaged pit from the same sample. In the normal emission pit, the gate and Si aperture are well defined, and the CNT bundle is unobstructed. With damage mode I, the p-Si area around the feature has quickly melted away from the pit and resolidified, causing the damage seen in Figure 87b.

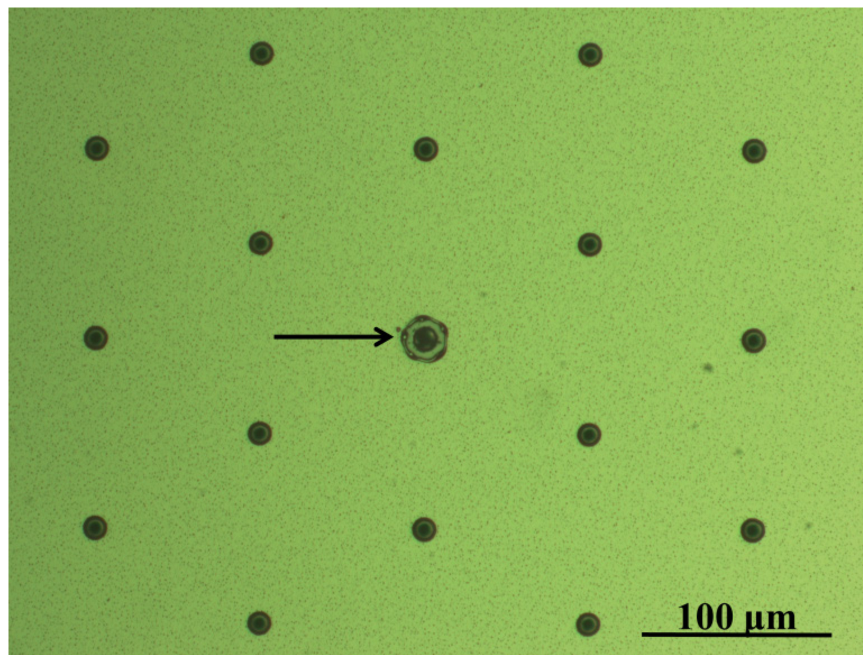


Figure 86: Optical micrograph of an array of emission pits in SMC-008 100.2.7 with an arrow indicating a damaged pit with p-Si melting away from the pit.

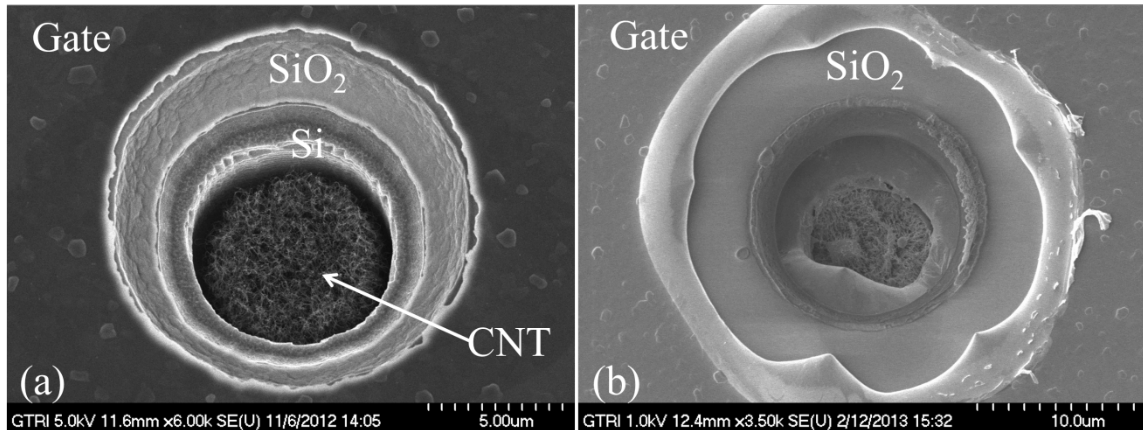


Figure 87: SEM of SMC-008 100.2.7 showing a (a) normal and (b) damaged emission pit with outward p-Si melting from damage mode I.

It is proposed that damage mode I occurs when a conductive species, such as a CNT, bridges between the silicon pit or CNT in the pit, and the p-Si gate surface, creating an electrical short. The resulting high current density of the short locally increases the temperature of the p-Si near the emitter pit opening past its 1,414 °C melting temperature. This local temperature increase causes the gate material to melt and flow. The p-Si can cool and resolidify as a result of (1) the movement of the melting material removing the short circuit, (2) the high current density burning out the short, or (3) when the electrical potential is removed. Observations of multiple damaged pits within the same sample indicate the third resolidification option is less likely.

It is possible that this type of damage could be a healing mode by removing an electrical short, especially since this damage has been observed on chips that are not shorted. The outward melting of the p-Si suggests this type of damage is a very fast, nearly explosive event, where the damage occurs almost instantly and either removes the short, or sustains a short on the entire chip.

4.6.2 Damage Mode II: Melting Within the Etch Pit

The second type of damage commonly observed is melting within the emission pit with limited damage to the p-Si. Figure 88 shows an SEM image of an emission pit with this type of damage. When compared to the undamaged pit in Figure 87a, the silicon aperture is no longer defined and the CNTs are obstructed. The SEM analysis suggests that the silicon pit melts and resolidifies around the CNT bundle. Oftentimes the CNTs are still visible within the melted material and look undamaged, indicating an electrical short is not directly through the CNT bundle. Figure 88 shows that the insulating layer has not melted, suggesting there is no breakdown of the oxide.

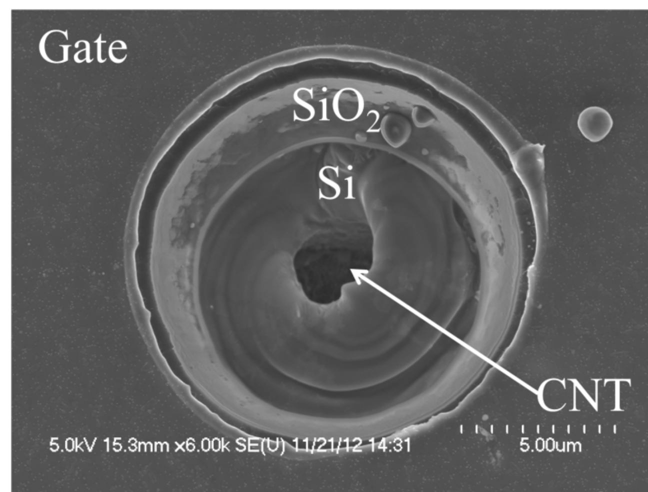


Figure 88: SEM image of an emission pit in SMC-001 50.3.1 with damage mode II.

Similar to damage mode I, it is proposed that damage mode II occurs when a conductive species bridges between the silicon or CNT in the pit, and the p-Si gate surface, creating an electrical short. The fact that the p-Si gate is not significantly damaged could be explained by having a lower current density around the p-Si, but a

higher current density through the silicon pit, which is high enough to cause melting. This situation could be possible, for example, by having a short with a larger contact area on the p-Si.

4.6.3 Combination of Damage Modes I & II

Although damage mode I and II are independently observed, there is often a combination of these two modes present in a damaged pit, where the amount of each damage mode varies. Figure 89 shows an SEM image of an emission pit where there is both significant melting to the silicon pit and outward melting to the p-Si gate. In this case, there is melted material covering the pit, so the presence of CNTs cannot be observed. Damage modes I & II are observed around emission pits, as well as around areas with processing defects, i.e. features that are inadvertently transferred to the surface due to lithography defects, particles, or damage to the photoresist.

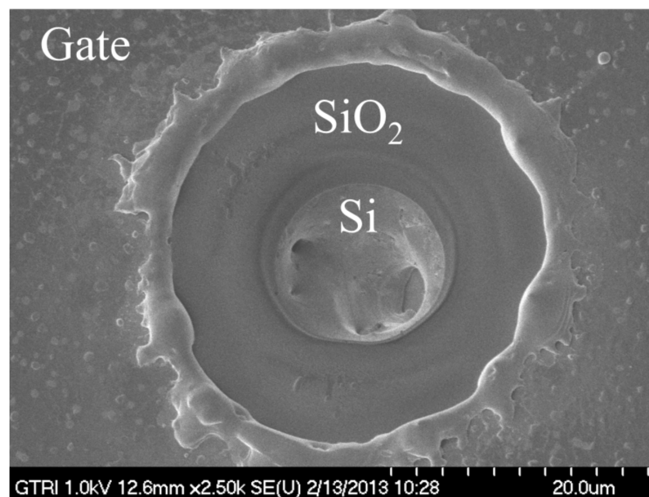


Figure 89: SEM image of an emission pit in SMC-008 200.4.4 with a combination of damage modes I & II.

4.6.4 Damage Mode III: Material Ejecta

A third type of damage is frequently observed where, in combination with the other two damage modes, there is a pattern of ejected material around the damaged pit. As seen in the optical and SEM images in Figure 90, the damage leads to discoloration and ejection of material in a radial pattern several millimeters from the damaged pit. The emission pits around the damaged pit appear to be undamaged and unaffected by the material ejecta. Like the other damage modes, this damage can also occur at the edge of a processing defect.

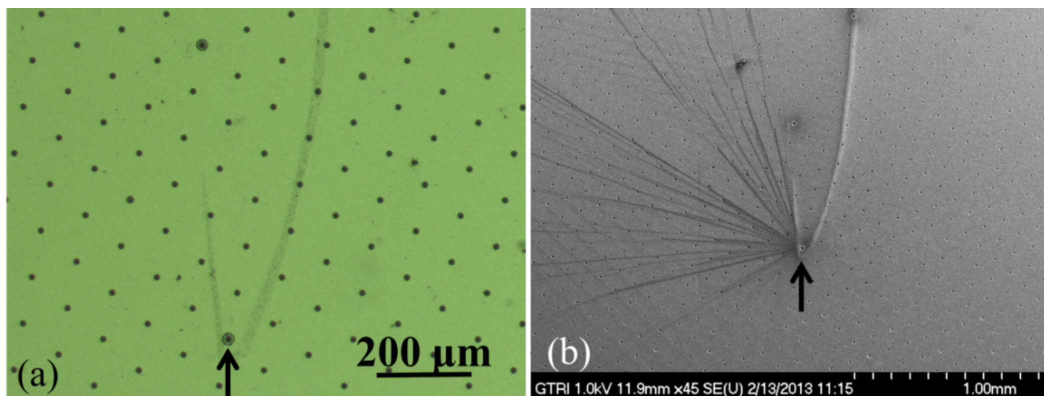


Figure 90: (a) Optical and (b) SEM images of the same damaged pit in SMC-008 100.1.2, showing how the damage mode III can look different between the two methods.

Comparison of the same damaged spot in Figure 90a and Figure 90b reveals that the damage does not always look the same in optical and electron microscopy. The arrow indicates the same pit, which is at the vertex of a line processing defect on the p-Si. In the optical image, there is no evidence of the ejecta observed in the SEM image. The presence of this pattern only in the secondary electron SEM image could be due to a change in the electrical conductivity of the ejected versus p-Si material, which would not

be observable in OM. Back-scatter electron imaging that was conducted on the same spot did not show the p-Si scratch nor the ejecta, indicating there is no elemental difference in these features.

Similar to the other damage modes, it is proposed that damage mode III occurs when a conductive species bridges between the silicon or CNT in the pit, and the p-Si gate surface, creating an electrical short. In this case, the electrical short is probably a particularly fast and explosive event, such that material around the shorted pit is ejected.

As mentioned earlier, the electrical short that causes the damage could be created between CNTs that become detached, or CNTs that are grown near the surface of the pit as a result of a processing defect. Figure 91b shows a magnified SEM image of this latter case, where CNTs are inadvertently grown close to the gate due to a processing defect. The damage mode III ejection pattern seen around the CNT defect in Figure 91a indicates that the CNT defect could be a cause of the damage. For example, during FE testing, some CNTs in the defect could have come in contact with the gate, causing a temporary short, destruction of the shorting CNT, and ejection of material.

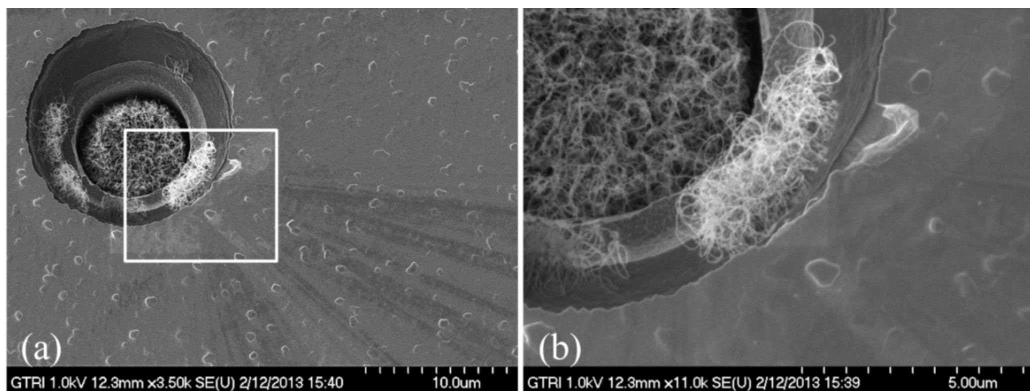


Figure 91: SEM images of damage mode III in SMC-008 100.2.7 caused by a CNT defect by the edge of the p-Si. Box in (a) indicates the magnified region (b).

4.6.5 Damage Mechanism

SEM analysis, such as the images shown in Figure 87-Figure 91, indicates that damage and melting is focused on the silicon and p-Si materials. When the CNTs are not completely covered by melted material, they are present and look unaffected. This observation suggests that the electrical short is mostly not occurring through the CNTs, except when the CNTs are part of a processing defect, e.g. Figure 91.

Energy-dispersive X-ray spectroscopy (EDS) was performed on each type of damage to determine if there is any foreign material present that could be a cause of the damage. This spectroscopy was used to detect any contamination around the damage, especially from heavier atoms, other than the carbon, silicon, and oxygen natively present on the samples. EDS analysis reveals that no unexpected materials were in or around the damaged regions.

Considering that EDS indicates contamination or deposition of unexpected heavy materials are probably not a cause for the damage, there are three general possible causes to the formation of an electrical short in the CNT emission pit. Even though only general mechanisms for the damage are proposed, the fact that there are distinct damage types observed in these structures indicates that there are different ways and possibly different mechanisms for the pits to be damaged.

The first cause could be due to a foreign body, such as metal catalyst or particles from handling, but is most likely due to stray CNTs or amorphous carbon from the CVD synthesis. The foreign body would not be detected by EDS, either because it is too sparse (catalyst) or has a low molecular weight, such as carbon. The electrical connection could also be made as a consequence of the large electric field between the electrodes during

FE testing, causing the “kinky” CNTs to physically straighten and move toward the gate. This phenomenon is difficult to confirm because the CNTs would likely revert back to their original coiled shape once the potential is removed. However, CNTs have been shown to move during FE and in the presence of strong electric fields [5, 136]. SEM comparison of the CNTs before and after field emission testing shows no significant changes or loss of CNTs, indicating that most CNTs are not being permanently pulled out or changed during testing. In order to prevent this type of electrical short, the CNTs are intentionally synthesized to a height several micrometers below the gate to provide a larger vertical separation between the two electrodes.

The second potential cause of an electrical short arises from the idea that increased localized pressures around the pits could provide enough gas molecules to form an arc from dielectric breakdown in the large electric field during testing. The literature shows that these Spindt-type structures can outgas significantly and often require baking because of the extremely large surface area of the pit/CNT geometry [5, 142, 179]. Thus, the outgassing could increase the localized pressure enough to allow an arc within the pit. The use of an *in vacuo* bake out or UV photodesorption could prevent damage in these emitters by driving out moisture and minimizing outgassing [5, 179]. The UV photodesorption used in the cathode array work had significant effects on pump down, but no significant prevention of damage.

About half, or 40, of the CFEAs analyzed were FE tested in a diffusion pumped vacuum chamber (cathode array batch I). At the test pressure of 3 x 10^{-7} Torr, diffusion oil backstreaming is a likely occurrence, allowing oil from the diffusion pump to enter and contaminate the chamber. This backstreaming may be a cause for arcing and the

intermittent shorting seen in the cathode array testing. If the 3.5 μm oxide thickness is used to calculate electric field, FE testing at 250 V results in fields greater than 70 V/μm between the electrodes. This field greatly exceeds the 10-25 V/μm dielectric strength of standard silicone oils used in diffusion pumps, such as the Dow Corning DC 705 oil used for this work [101]. Thus, if the oil deposits across the oxide in an etch pit, oil breakdown could be a cause of arcing and damage. Unfortunately, the EDS performed would be unable to differentiate diffusion pump oil contamination from the CFEA, as it is also mainly composed of carbon and silicon. High performance liquid chromatography and mass spectroscopy are techniques that could be used to confirm the presence of diffusion oil on the CFEA surface.

A comparison was made between the CFEAs from cathode array batch I, which were tested in a diffusion pumped chamber, to those from batch II, which were tested in a cryogenically pumped chamber. After the first I-V test without a burnout, 73% of the batch I CFEAs were electrically shorted and only 5% of the batch II CFEAs were shorted, indicating a significant change in shorting between pump methods. However, this shorting difference could also be due to other environmental or sample factors. For example, batch II CFEAs were from different, later generation wafers that could have better fabrication. After batch testing, 45% of the batch I CFEAs were found to contain damage, whereas 28% of the batch II samples contained damage. Unfortunately, a significant correlation between the damage observed in the two batches cannot be made because the diffusion pumped CFEAs were tested more times than batch II, and batch II was subjected to the HET exposure.

It is important to note that the damage modes observed do not always indicate an electrical short between the gate and cathode layers. About half of the damaged CFEAs were an open circuit and were observed with all three types of damage. In addition, the four chips that were observed with many damaged pits are all electrically open. This result indicates that the chips are able to survive for an extended period of time with significant damage. It is proposed that these highly damaged chips accumulate the damage over time as temporary individual shorts are eliminated by the damage.

This damage analysis indicates that there is a large degree of robustness in the CFEA design that allows for damage to reverse electrical shorting and for the accumulation of significant damage before failure from shorting. It is proposed that the horizontal and lateral separation of the CNTs from the gate in this particular CFEA design allows for this robustness, permitting damage and melting without causing an electrical short. In addition, this evidence substantiates the perceived enhanced reliability of CNT Spindt-based cathodes from the reduced possibility of single point failures in the arrayed pit design, a common failure mode in traditional electron sources. Likely causes of damage are electrical shorts caused by debris, outgassing, and diffusion pump oil backstreaming.

4.6.6 Infrared Imaging

An infrared (IR) camera test is performed to determine if a single location or emitter pit with an electrical short could be spatially located on a chip. This test method provides a unique opportunity to definitively determine where an electrical short is

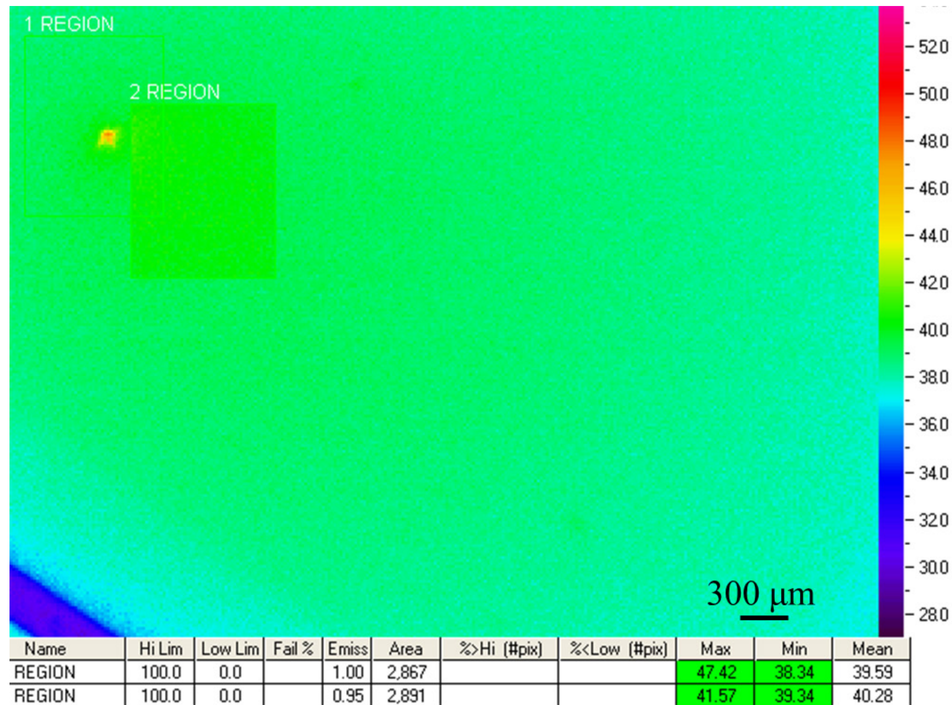
located, as all other characterization techniques do not give location specific electrical data. In addition, this test could provide insight into how and why shorting occurs.

The IR test passes voltage limited current through a shorted CFEA. The CFEA must have a low enough resistance to allow a sufficient current density to cause heating that can be picked up by the IR camera. In addition, since the IR test is run at atmospheric pressures, the potential applied during the test must not be more than 20-30 V to prevent arcing. Initial IR test attempts indicate that a resistance below 2 kΩ is needed. Another complication from this test is that the current can, and often does, immediately burn out the short and result in an open circuit. Thus, IR image acquisition can be difficult.

An initial IR test was performed at AFIT on SMC-1 50.3.1, which had a resistance of 300 Ω. At an applied 8 V and ~22 mA, a single hot spot (+10 °C versus remainder of chip), was observed on the lower right quadrant of the chip and is shown in Figure 92. An increase to 14 V caused a spike of ~31 mA and a temperature spike of +65 °C in the same spot before the current suddenly dropped to 11 mA. Potential was increased several times, which was followed by a short spike in current. Finally, at 20 V a spike of 50 mA and a temperature spike of +112 °C was observed, followed by a drop in current to $<$ 1 mA. The final chip resistance measured $>$ 50 MΩ, indicating a partial burnout of the short.

In this test, the camera resolution is low and the scale bar is approximate. The field of view is about ¼ of the CFEA and the blue line in the corner of Figure 92 is the 300 μm wide Au contact line. However, the initial data suggests that a shorted chip is due to a single area electrically shorting the entire chip with no other areas containing a short,

since burnout of the spot resulted in an open circuit CFEA. Optical microscopy of the shorted area showed no apparent damage that may be causing the short.



Name	Hi Lim	Low Lim	Fail %	Emiss	Area	%>Hi (#pix)	%<Low (#pix)	Max	Min	Mean
REGION	100.0	0.0		1.00	2,867			47.42	38.34	39.59
REGION	100.0	0.0		0.95	2,891			41.57	39.34	40.28

Figure 92: IR image of SMC-001 50.3.1 at 8V and 22mA showing a single hot spot. The blue line in the bottom left is the Au contact line. Scale bar is approximate.

A second IR test was performed on a higher end camera with better resolution and higher magnification to determine if electrical shorts are coming from a single etch pit. Again, voltage limited current was applied. Sample SMC-008 100.1.6 (package 18) with a resistance of 64 Ω was tested. The chip was first scanned at 0.7 V and 11 mA at 1x magnification, which identified a +5 °C hot spot in the upper left quadrant of the chip. At 5x magnification, where the individual pits can be resolved, the spot had a +9 °C temperature under the same current. At 15x magnification the spot could be identified from a single pit with a +40 °C temperature. Figure 93 shows an image at 15x

magnification, 1.5 V, and 16 mA with a +150 °C spot coming from the edge of a single pit. The camera takes a background emissivity image to zero out the thermal image. This figure is an overlay of the two images, allowing the hot spot to be correlated to position. A increase in potential to 2.0 V and 19 mA showed the spot at +240 °C. A further increase resulted in a brief current and temperature spike, followed by no current and an electrically open CFEA, demonstrating typical burnout behavior.

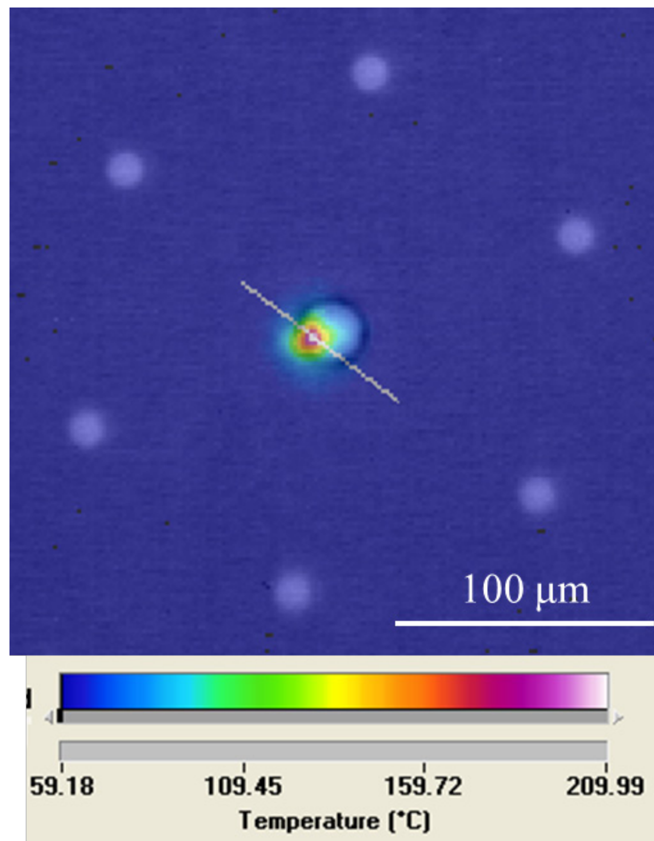


Figure 93: IR image overlaid an emissivity background image of SMC-008 100.1.6 showing a hot spot at +150 °C at the edge of an etch pit. White line is from the software tool to measure the maximum temperature.

This data shows that the electrical short can not only come from a single pit, but a portion of a pit. In addition, this sample likely had only one shorted pit, as its burnout resulted in an open circuit CFEA. This result indicates that shorted CFEAs could be due to single electrical shorts. The IR image indicates that the electrically shorted pit looks abnormal. OM investigation after the IR test, shown in Figure 94, reveals there is one damaged pit in the area that the hot spot came from. The damaged pit appears to be due to damage mode I. Notes on this sample after FE testing in batch I reveals that one damaged pit was observed after a burnout in vacuum shorted the chip to a low resistance, but no image is available before the IR test. These observations indicate that the electrical short could have come from the single noted damaged pit.

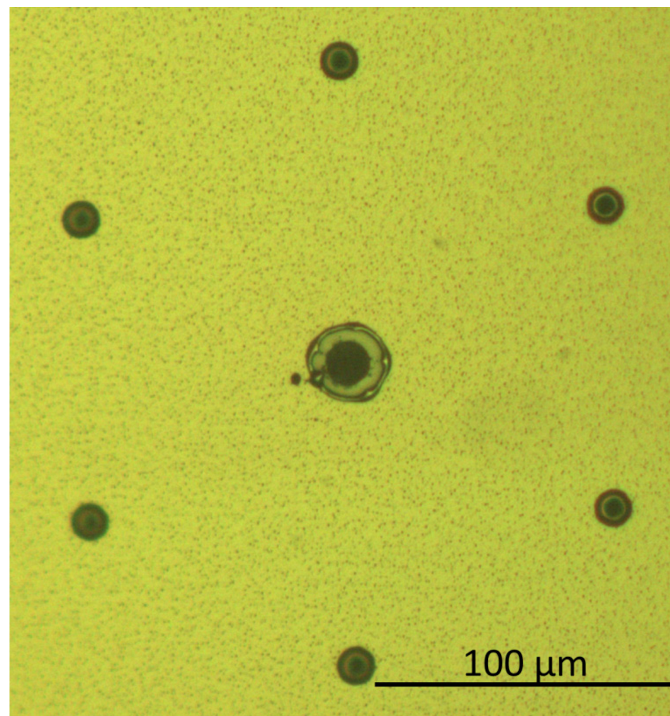


Figure 94: Optical micrograph of a damaged pit in SMC-008 100.1.6 after the IR test, which is in the vicinity of the shorted pit imaged in the IR test.

4.7 Hall Effect Thruster Exposure

Hall effect thrusters (HETs) have been used for several decades by space vehicles for station keeping and orbital maneuvering [180]. HETs ionize and accelerate propellant electrostatically, resulting in a high velocity beam of ions. The present state-of-the-art cathode used in HETs is the thermionic or hollow cathode, which emits electrons from a heated surface. Thermionic cathodes internally ionize propellant to amplify the number of electrons extracted from the cathode in order to achieve necessary emission currents. The cathode propellant flow is not accelerated by the thruster and can account for as much as 10% of the total propellant required by the thruster [181].

In contrast, FE cathodes do not consume propellant. The primary consequence of this benefit is up to a 10% increase in system specific impulse, a measure of propellant mass efficiency. A secondary consequence is a reduction in the spacecraft power requirements by reducing the power the cathode consumes. These benefits are enabling for CubeSat applications. In this test, the effect of the HET plume environment on CFEAs is examined to evaluate their potential as an alternative to the thermionic cathode on low-power HETs [182].

The HET exposure test was conducted immediately after the cathode array batch II FE testing. This batch contains 39 open circuit CFEAs, all distributed evenly in positions farthest away from the HET in an effort to capture the effects of the plume on the CFEAs while minimizing the risk of catastrophically damaging them. In addition, 2 CFEAs were included that were electrically shorted. These "dummy" chips underwent a gridded SEM analysis before testing in order to compare the effect of the plasma on the same exact pits after the test. These chips were not wire bonded and were placed in

positions furthest (distal, package 82) and closest (proximal, package 83) to the HET in order to compare the effect of the plasma at different positions.

4.7.1 HET Exposure Data

The CFEAs were exposed to a running HET for 40 minutes, which was operated with a typical hollow cathode. An attempt at CFEA FE testing was made in the last 8 minutes of exposure. However, a significant amount of unexpected electronic interaction between the CFEA circuit and the HET environment caused complications. Figure 95 shows the cathode array current and applied potential data as a function of time.

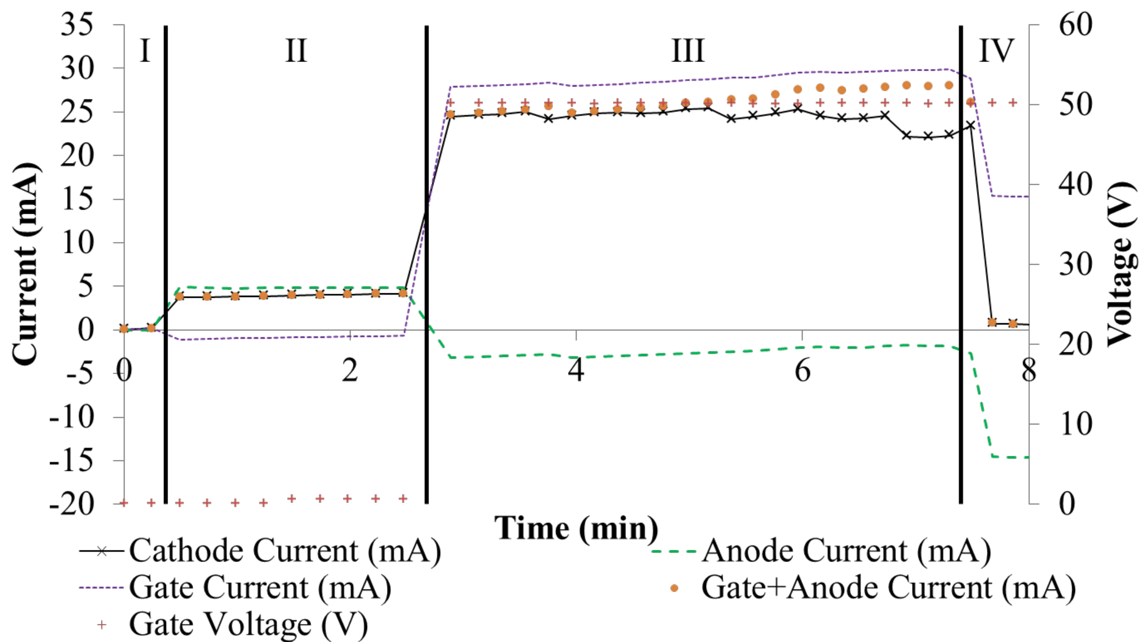


Figure 95: The cathode array current data for the HET test, indicating the 4 stages. Anode current represents current between the CFEA and HET circuits [182].

The collected data can be broken up into four distinct stages. Before data collection, the HET was brought to nominal operation with the isolation switch between

the HET and CFEA circuits open. Once the HET was stable, the data acquisition program began capturing data and the isolation switch was closed. The data acquisition system measured baseline data for the circuit with the CFEAs unbiased for 2 minutes. Once the CFEAs were biased, the system operated for five minutes before all CFEAs appeared to be shorted and data acquisition was terminated.

The first stage covers the first two data points, when the isolation switch is open. Consequently, no current travels between the CFEA and HET circuits (stated as anode current). There are 68-200 μA of gate and cathode current during this period. The HET was running at the beginning of the test, so the current is likely noise from the charge exchange (CEX) ion and hollow cathode electron collisions.

The second stage consists of the next 9 data points, where the isolation switch is closed and initially the CFEA power supply has no output. Power supply output starts during the middle of the second stage, as seen by the small jump in gate voltage from 0 V to 0.575 V. Negative gate current, and positive anode and cathode currents result from closing the switch. The currents detected correspond with CEX ions bombarding the CFEA surfaces, which are now set to the negative discharge potential on the HET circuit.

The third stage consists of the large positive plateau, where the experiment software interpreted the currents detected as the trigger to initiate a current-controlled test. At this point, the gate potential rises to + 50 V from the cathode potential, which is equal to the HET discharge negative potential (about -10 V). Previous FE testing has shown typical performance of the CFEAs with a limited cathode current density (< 50 $\mu A/cm^2$) at a bias of 50 V. In contrast, the measured cathode current from this test equates to a current density of roughly 650 $\mu A/cm^2$. This data suggests charged particles

from the plasma and electrical shorting are the primary contributions to the currents measured.

In the third stage there is a large positive gate current, which corresponds to electrons from the hollow cathode colliding with the positively biased gate. Enough electrons arrive at the gate that they reverse the desired direction of current between the HET and CFEA circuits. This effect is manifested as a negative anode current. There is also positive cathode current, which corresponds with CEX ions colliding with the CNTs and exposed package. The gate + anode current values diverge from the cathode current because the experiment software stopped measuring the cathode current data on some channels even though they were still active.

The fourth stage consists of three data points where the emitter channels are manually shut down. The experiment software had an error where it stopped measuring the cathode current on channels without disconnecting them from cathode bias. Unfortunately, even when the cathode bias is disconnected, the circuit still allows the common gate electrode to be biased by the power supply. The result is that the cathode on a disconnected channel floats to the plasma potential, maintaining an electric field between the cathode and gate. Since the anode and gate electrodes are common, the current from the disconnected channels is detectable on these electrodes despite the software error.

In conclusion, the electrical test data contained several complications due to the plasma ions, hollow cathode electrons, and software errors. The data gives insight into what constituents were bombarding the cathode array and suggests a significant flow of

electrons and CEX ions to the CFEAs and packages. This information is used in the following analysis.

4.7.2 Package Pin Electrical Shorting

A summary of the HET test on the 39 open circuit and 2 shorted "dummy" CFEAs is shown in Table 10. Resistance measurements were made after the HET test under vacuum through the circuit boards and packages ("HET Test" column in Table 10). This measurement in vacuum indicates electrical shorting outside of the CFEAs:

- Only 8 CFEAs *measure* an open circuit (red data in Table 10)
- 31 CFEAs *measure* electrically shorted
    - 13 have a resistance > 1 kΩ
    - 18 have a resistance < 1 kΩ
- Proximal and distal dummy *packages* (not CFEAs, which are not wire bonded) measure 12 Ω and 30 MΩ, respectively (green data in Table 10)

The electrical resistance of the dummy chips could not be measured since they did not have a wire bonded gate connections. The electrical shorting on the dummy packages and the < 1 kΩ resistance measured on 18 of the CFEAs indicate there is a metallic electrical short on the package or circuit boards. The cathode array was removed from the vacuum chamber and the packages were removed for further testing. Resistance measurements on the packages ("Post Ω" column) showed some changes in resistance, but still with 22 CFEAs indicating an electrical short.

Table 10: Summary from the HET test and microscopy analysis.

Pkg #	CFEA W	CFEA Sample	HET Test (Ω)	Post Ω	Stereoscope	Optical Microscope
41	12	50.2.3	17	40M	Au sputter, chip good	poor growth, no damage
42	12	50.3.1	21	22	worse than 41 Au sputter	poor growth, no damage
43	12	50.3.2	28	35	Au sputter, dirty chip	lots arc damage in clusters
44	12	50.3.3	82	60M	major Au sputter	irregular poly apertures but no damage
45	12	100.1.4	2.78k	~140k	major Au sputter	good, no damage
46	12	100.1.5	INF	INF	Au sputter, chip dirty	good, no damage
47	12	100.1.6	3.6M	INF	Au sputter	good, no damage
48	12	100.2.3	54	~4k	Au sputter, yellow spot on 3rd quad	3 poly melt pits spread out, spot
49	12	100.2.4	2.7M	INF	Au sputter, coupledefects on chip	good, no damage
50	12	100.3.5	INF	INF	Au sputter	good, no damage
52	12	200.2.4	7.4	~3	major Au sputter, scratches on L	good, no damage
53	13	50.3.1	40	~40M	Au sputter, chip dirty & defects	good, no damage, spots of discolored poly
54	13	50.4.1	21	20	major Au sputter, litho defects	CNT good, 1 poly melt pit, poly discolor
55	13	50.4.2	89	~15M	Au sputter, ohm inc to 110M	CNT good, poly/etch defects, no damage
56	13	50.4.3	24k	170k	maybe Au sputter, ohm inc to INF	CNT good, poly spots, no damage
57	13	100.1.2	16M	inf	Au sputter, scratched chip	CNT good, poly spots, no damage
58	13	100.1.3	INF	inf	little Au sputter, many pits damaged	lots damage- R side, many unetched pits
59	13	100.1.4	30	70	Au sputter, many damaged pits on L	L side pits not etched w/ lots damage
60	13	100.1.5	2.8M	inf	little Au sputter, many pits damaged	CNT good, no damage
61	13	100.1.7	8.8M	inf	little Au sputter	CNT good, no damage
62	13	100.1.8	8.4	5	major Au sputter	CNT good, 30+ arc pits, most on R side
63	13	100.3.2	INF	13	Au sputtering	CNT good, random unetched pits ~5%
64	13	100.3.3	41	37	Au sputter, chip scratched	CNT good, ~15 arced pits spread out
65	13	100.3.7	1.4k	90M	Au sputter, damaged pits	CNT good, unetched pits, ~12 damaged pits
66	13	100.2.2	634	inf	Au sputter, chip scratched	CNT good, ~47 damaged pits
67	13	100.2.6	970k	inf	little Au sputter, scratched chip	CNT good, no damage
68	13	200.1.4	832	inf	little Au sputter, scratched chip	poor growth, random unetched pits
69	13	200.2.4	INF	27	Au sputter, scratched chip	poor growth? (no emission), unetched parts
70	13	200.3.2	2.7M	inf	little Au sputter, 1 chip scratch	CNT good, ~8 arced pits,
71	13	200.3.4	INF	inf	little Au sputter, couple chip scratches	poor growth, 1 arced pit
72	13	200.4.4	3.9	4	major Au sputter	CNT good, no damage
73	13	50.2.1	13.5	~10M	major Au sputter	CNT good, ~6 arced pits
75	13	100.1.6	14	25	Au sputter	CNT good, no arc damage
76	13	100.2.4	16	15	major Au sputter	indiv. pit damage >100, ~5%. Good CNTs
77	13	100.2.7	700k	~150M	Au sputter	CNT good, no damage
78	13	100.3.4	7.1k	inf	Au sputter, chip little dirty, scratched	CNT good, ~48 arced pits w/clusters
79	13	100.3.5	INF	~inf	Au sputter, big scratch, dirty R side	no arc damage. CNTs good, normal
80	13	100.3.6	429k	inf	Au sputter, dirty spot in centerish	CNT good, no damage
81	13	200.4.3	INF	inf	little Au sputter	CNT good, no damage
82	13	50.1.1	30M	inf	little Au sputter, dirty, litho defects	CNT good, sporatic unetched pits
83	12	50.3.2	12	0.3k	Au sputter, scratched, litho defect	CNT good, no damage, all pits etched

The rest of Table 10 includes optical analysis of the CFEAs. This analysis showed an observation of sputtered Au onto the package pin insulation on all packages (circled in Table 10), which could possibly electrically short the pins to the package. The analysis also notes damage to etch pits, which is discussed in the following section.

Wire bonds on shorted packages were removed so that independent resistance measurements of each CFEA and each pin could be made. This analysis is summarized in Table 11. Twenty of the packages that had an electrical short and the two dummy chips were analyzed:

- 19 of the 20 CFEAs are an open circuit (shorted data is red in Table 11)
- A majority of the package pins are shorted to the package body
  - All of the top 4 pins are electrically shorted
  - The 5th pin is shorted in all but 3 packages (red data in Table 11)
  - The 6th pin is an open circuit in all but 3 packages (green data in Table 11)
- The proximal dummy package: all pins are shorted (bolded package numbers in Table 11)
- The distal dummy package: 1 pin is shorted

Table 11: Pin resistance measurements of packages from the HET test.

Pkg	CFEA		Pin/Chip status (remove bonds, Ω)							
#	W	Sample	chip	(top) 1	2	3	4	5	6	Comments/growth quality
41	12	50.2.3	inf	50M	50M	40M	49M	110M	inf	SEM: nonuniform growth
42	12	50.3.1	inf	34M	9Ω	10Ω	23Ω	81Ω	n/a	
43	12	50.3.2	inf	47Ω	7Ω	13Ω	116Ω	~30k	inf	roughly >100 pits, ~5% damaged
44	12	50.3.3	inf	100M -in	60M	15M	120M	100M	inf	
45	12	100.1.4	inf	30M	5k	30M	50k	inf	inf	
46	12	100.1.5	n/a							
47	12	100.1.6	n/a							
48	12	100.2.3	inf	40Ω	~40k	5M	48k	12M	5M	
49	12	100.2.4	n/a							
50	12	100.3.5	n/a							
52	12	200.2.4	inf	8Ω	2Ω	5Ω	4Ω	~5M	inf	
53	13	50.3.1	inf	50M	12M	120M	77M	75M	inf	
54	13	50.4.1	~inf	1M	8Ω	37Ω	1M	24k	inf	
55	13	50.4.2	inf	30M	18M	50M	140M	inf	inf	
56	13	50.4.3	n/a							
57	13	100.1.2	n/a							
58	13	100.1.3	n/a							damage but INF, bad chip- pits not etched
59	13	100.1.4	inf	10M	25Ω	12M	100M	32k	inf	bad chip, next to pkg 58 on wafer
60	13	100.1.5	n/a							no bottom gate bond
61	13	100.1.7	n/a							
62	13	100.1.8	30k	78Ω	9Ω	9Ω	5Ω	40Ω	60M	Irregular etching - some pits not etched
63	13	100.3.2	inf	1M	5M	11Ω	18Ω	7M	n/a	
64	13	100.3.3	inf	21Ω	16Ω	24Ω	0.6M	0.2M	inf	
65	13	100.3.7	inf	8M	7M	110M	110M	inf	inf	
66	13	100.2.2	n/a							last gate bond off gate
67	13	100.2.6	n/a							
68	13	200.1.4	n/a							not many CNTs pre test, last bond off
69	13	200.2.4	inf	11Ω	24Ω	69k	25k	29k	inf	short CNTs pre test
70	13	200.3.2	n/a							INF, good emission
71	13	200.3.4	n/a							pre-SEM - normal growth
72	13	200.4.4	inf	15Ω	5Ω	5Ω	4Ω	7Ω	1M	bottom bond off, low V emission
73	13	50.2.1	inf	7Ω	7Ω	8Ω	80M	150M	inf	
75	13	100.1.6	inf	7Ω	6Ω	8Ω	22k	170Ω	inf	
76	13	100.2.4	inf	80Ω	5Ω	6Ω	25Ω	3M	inf	
77	13	100.2.7	n/a							OM- now INF, no emission at 200V
78	13	100.3.4	n/a							last bond off gate (remove)
79	13	100.3.5	n/a							
80	13	100.3.6	n/a							
81	13	200.4.3	n/a							
82	13	50.1.1	1M	120M	80M	inf	inf	inf	inf	edge piece so prob why defects
83	12	50.3.2	100Ω	50M	110	110M	4Ω	60M	160M	

These surprising results show that the CFEAs were not electrically affected by the HET plasma, with 97% of the CFEAs remaining an open circuit. In addition, in almost all cases the top five package pins are electrically shorted, but the 6 pin is open in all but 3 cases. This trend indicates that the shorting is dependent on the pin location on the package, where the 6th pin may be coated by sputtered Au less because it is adjacent to the cut (open) edge of the package and is less confined. None of the pins opposite of the CFEA were shorted, nor was there and indication of sputtering on them or the CFEAs. This evidence suggests that the presence of the grounded CFEA has a significant effect on where the Au sputtered.

Since the dummy packages were biased by the cathode, but were not grounded at the gate, they cannot be directly compared to the other CFEAs. However, the closer dummy package had all pins shorted and the further one only had one pin shorted, indicating that position could have a drastic effect on pin shorting. This trend points towards a sputtering dependence on the ion density, which is highest close to the HET.

A positional analysis of the shorted packages was conducted on the circuit boards. The symmetry of the cathode array, which contains 4 circuit boards, allows for CFEAs placed in the same slot across different circuit boards to be treated together. Figure 96 maps the number of packages with shorting across the cathode array. The number on the top in each slot indicates the number of packages that shorted, and the number on the bottom indicates the number of CFEAs that contained arc damage. In this schematic, the HET lies beyond the lower left side of the figure.

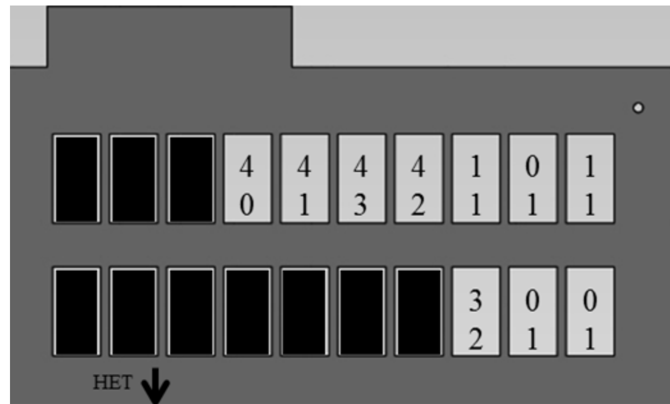


Figure 96: Schematic of one circuit board of the cathode array. The numbers on the top of each package location indicate the number of packages in this slot around the array that shorted from sputtered gold. The number on the bottom indicates the number of CFEAs that contained arc damage [182].

Plotting the shorting data in this manner reveals a clear trend of packages shorting due to sputtering more often at positions close to the HET (top number). The amount of material sputtered is a function of the incident energy of the ions, the binding energy of the sputtered material, the relative atomic masses, and the number of incident ions [183]. Of these factors, the two that vary with distance from the HET plume are the ion energy and the number of ions. Since sputtering still occurred on the farthest packages, it is likely that variation in the ion density rather than the ion energy is responsible for the noted trend. Also of note, the quadrant of the array which was closest to the hollow cathode did not have any observable differences compared with the other three quadrants. Thus, the shorting is dependent on distance from the HET as a result of variation in the ion density.

A series of tests were conducted on the packages to determine how and why the pins were electrically shorting. As noted in Table 10, optical microscopy showed a distinct Au coloring on the pin insulation, with a more pronounced coloration on the

upper pins. This observation, shown in different packages in Figure 97, was the first evidence of sputtered Au and correlates with the pin shorting noted in Table 11.

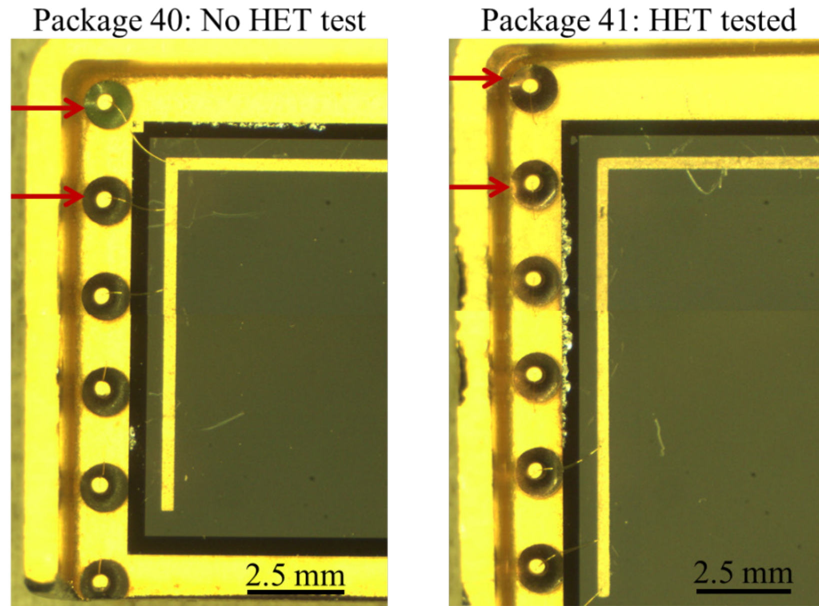


Figure 97: Stereoscope images of electronic packages with and without exposure to the HET. Arrows indicate upper pins for comparison of Au coloring.

SEM comparisons of package pins with and without HET exposure, an example of which is shown in Figure 98, indicate deposition of a conductive material. Insulation charging made clear image acquisition difficult, but a significant lack of charging was noted in the HET tested pins. In Figure 98, the pin with no HET exposure has insulation that charges all around the pin. In the HET exposed pin, charging only occurs on one side of the pin and surface texture can even be resolved in the higher magnification image, indicating a conductive surface.

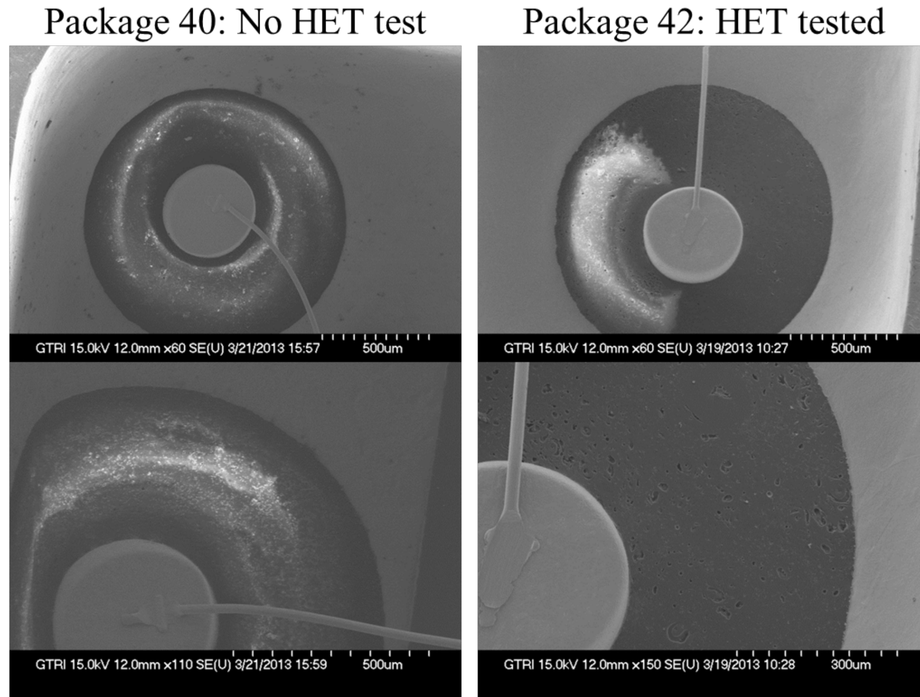


Figure 98: SEM comparison of package pins with and without exposure to the HET.

EDS was used to determine the elemental composition of the conductive coating observed in the stereoscope and SEM. Control EDS spectra on CFEAs with no exposure to the HET were taken. Areas with and with Au were measured to have a baseline spectra with and without Au. In addition, EDS line scans across HET exposed CFEAs showed no indication of Au in the pit array.

EDS line scans were conducted across the package pin and insulation in order to compare detected Au in the package pin (plated with Au) and the insulation. A control 10 point line scan of a package with no HET exposure is shown in Figure 99. The inset is the line scan across an SEM with counts of Au plotted in green across the line. EDS spectra are given for the indicated points in the insulation and the pin to show typical spectra. This data clearly indicates the detection of Au only on the pin.

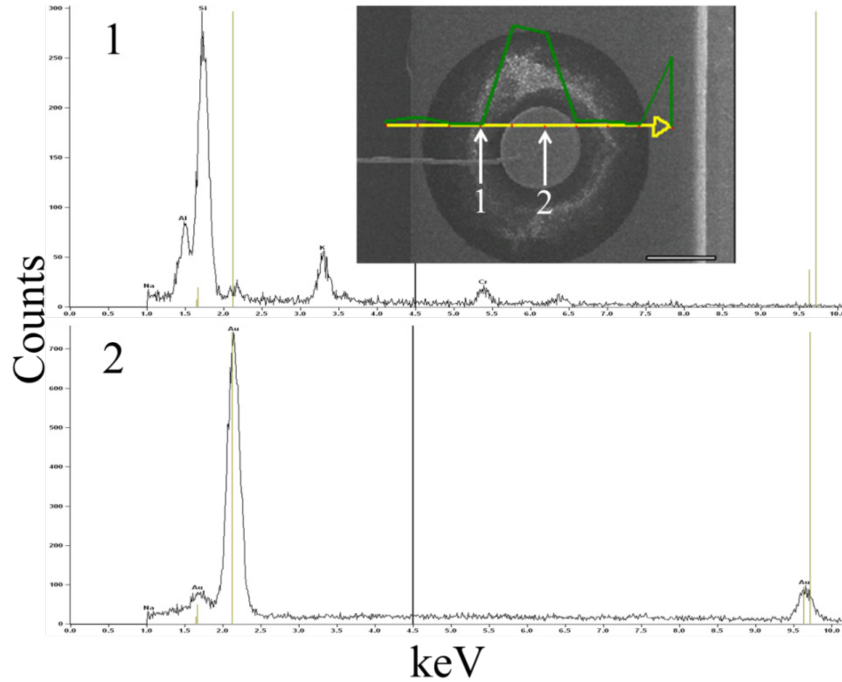


Figure 99: A control EDS line scan of a pin on SMC-009 100.3.4 without HET exposure showing no Au detection in the insulation. Gold lines indicate X-ray energies for Au.

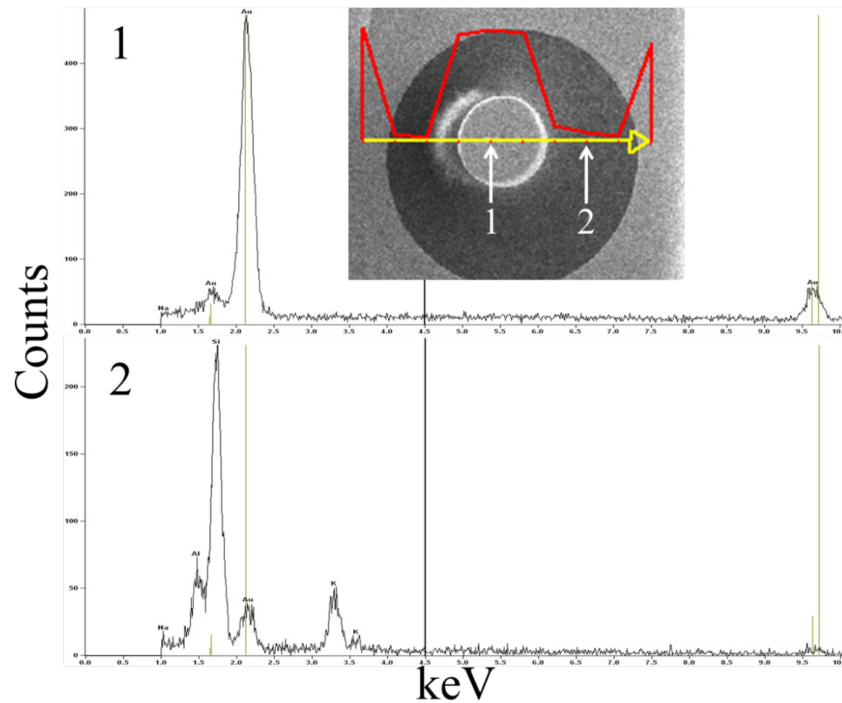


Figure 100: EDS spectra from the HET exposed pin. (1) is from the pin, and (2) is from the insulation to the right of the pin. Gold lines indicate X-ray energies for Au.

A similar EDS line scan of a HET exposed package pin that was electrically shorted is shown in Figure 100. Here, the counts for Au decrease in the insulation, but do not go completely down and actually tail off to the right of the pin. The indicated EDS spectra for the positions over the pin and to the right of the pin are shown in Figure 100. As expected, there are strong peaks for Au over the pin. In the spectra to the right of the pin, there are still weak peaks for Au, indicating that Au is present on the pin insulation.

Even though EDS cannot be considered a quantitative or even definitive technique, the use of control spectra and comparisons with different areas clearly indicates that Au is detected on the pin insulation. This evidence combined with the observations from the stereoscope and SEM give clear indication that a majority of the package pins electrically shorted because of Au sputtered onto the pin insulation.

4.7.3 CNT Analysis

The proximal and distal dummy CFEA samples underwent repeatable SEM imaging both prior to and after HET exposure. Figure 101 shows a single emission feature on the distal CFEA (SMC-13 50.1.1) before and after the HET test. Close examination reveals the overall structure to be identical between the two images, with two exceptions. The post-exposure image shows particulate debris present in the emission feature marked with arrows. Both the proximal and distal samples have several features with similar debris accumulation. This particulate debris could be from spallation of material from the cathode array during the HET test. The debris could also be from handling the devices between the two images when they were unavoidably transported outside of a cleanroom environment for testing.

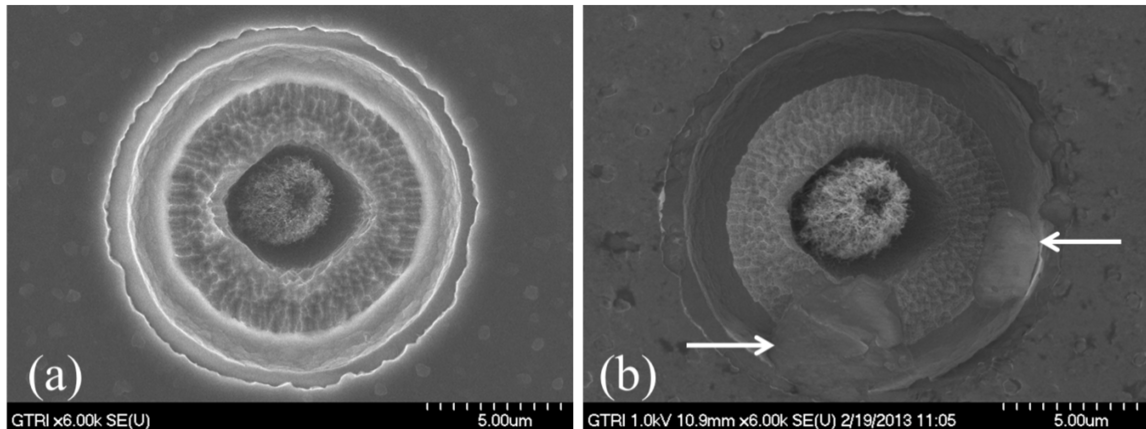


Figure 101: Before (a) and after (b) HET test SEM images of the same emission feature from the distal CFEA (SMC-13 50.1.1). Arrows point to particulate debris.

The before and after images in Figure 101 also show differences in contrast and charging. A difference in contrast could indicate topological changes on the surface, but the difference is most likely attributable to charging of the gate electrode and a change in the accelerating voltage on the SEM. The accelerating voltage is at 1 kV in Figure 101b as opposed to 10 kV because the CFEA is not removed from the electronic package after the test to avoid damage from removal. SEM images from before HET testing were taken without the package. The dummy sample was not wire bonded to the package, which made it very difficult to make a quality contact to the floating gate to ground it during imaging. The poor contact caused significant charging of the gate during imaging, even with a lower accelerating voltage. In addition, the magnetic package (Ni-based Kovar) can cause significant imaging problems due to its interactions with the imaging electron beam. All of the post HET test SEM images in this section contain this variation.

Figure 102 shows a fortuitously grown CNT on the gate edge of a pit on the distal CFEA before and after HET exposure. The presence and position of the CNT remains

largely unaffected between the two images, but some changes are present. In particular, the part of the CNT in the upper left of both images appears to have flipped or twisted, while the component of the CNT on the lower right of the image appears to have untwisted and dropped slightly. These changes in position could be due to HET exposure or to handling during the installation and removal of the distal sample. As noted earlier, studies have reported motion of CNTs under the presence of electric fields and during field emission [184, 185]. While this CNT could not have field emitted, it was exposed to the HET plasma and the electric field variations present at its length scale could be responsible for these positional changes.

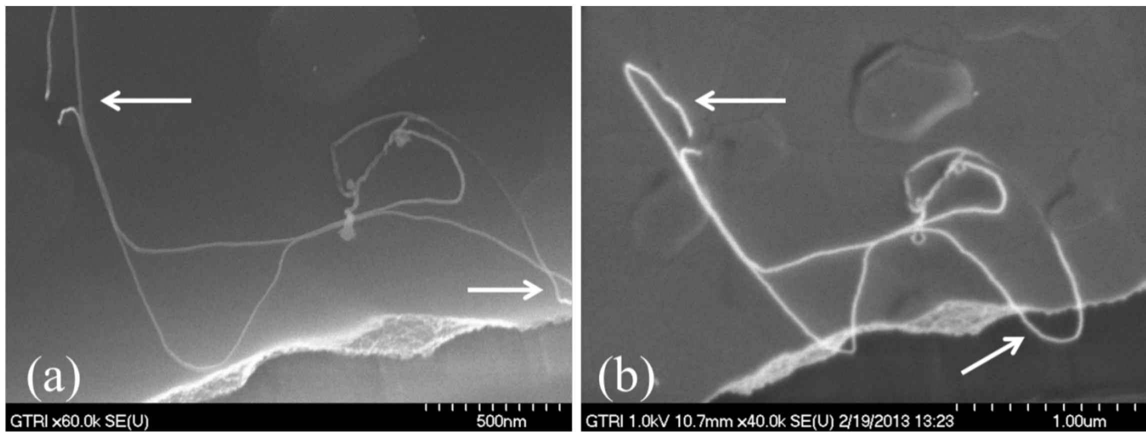


Figure 102: Before (a) and after (b) HET test SEM images of the same stray CNT on the p-Si edge of the distal CFEA. Arrows indicate where the CNT has moved slightly.

Figure 103 shows a single CNT bundle on the proximal CFEA (SMC-012 50.3.2) before and after HET exposure. Like most emission features observed on the CFEAs exposed to the HET environment, there are no observable changes in the emitter geometry after exposure. Close examination of these images reveals no observable

difference in the gate, insulation, Si, or CNTs. The remarkable similarity between the two images in Figure 103 demonstrates that CFEAs can survive close exposure to a HET environment when not biased. This result is extended when comparing etch pits of the functioning, biased CFEAs exposed to the HET. Comparisons of the same samples, but not the same exact pits of the biased samples also show no significant changes.

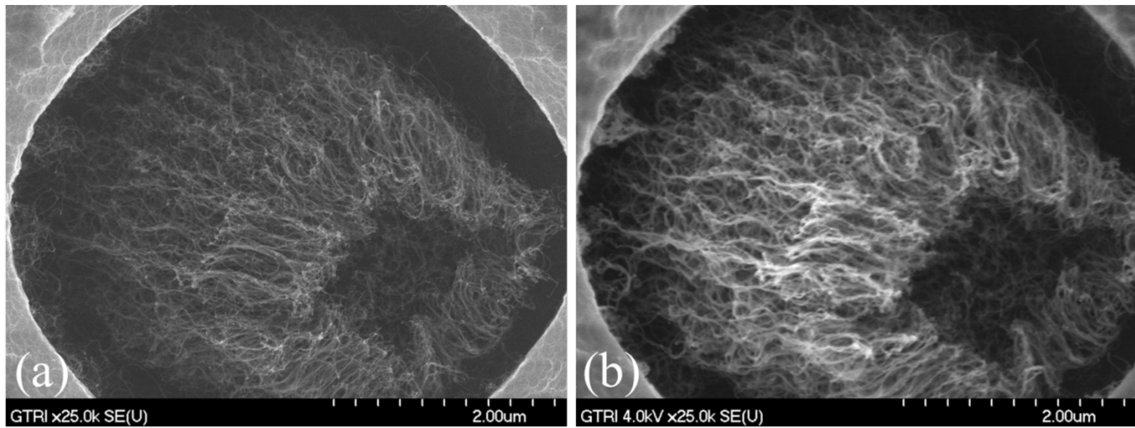


Figure 103: Before (a) and after (b) HET test SEM images of the same CNT bundle on the proximal sample (SMC-012 50.3.2), which appears to be unaffected.

In conclusion, the data gathered during the HET exposure test suggests a significant flow of electrons and CEX ions to the CFEAs and packages. CEX ions sputtered appreciable amounts of gold from the packages, causing electrical shorting of most pins. Despite this sputtering of gold, there is no evidence of sputtering on the CFEAs after 40 minutes of exposure to the HET environment. SEM imaging of the CFEAs indicates possible spallation from the cathode array, but the evidence is more likely due to contamination from handling the devices. No observable changes to the CNTs or etch pits are observed, except small positional changes in an isolated CNT, indicating the CFEA can withstand the HET environment. This effort is the first

experimental study of CNT field emitters in an operational HET environment, and the results are encouraging for future development.

4.8 Manufacturing Readiness Level

A manufacturing readiness level (MRL) assessment was performed on the CFEA technology using the Air Force manufacturing readiness assessment tool (2007 v10). The MRL assessment is a U.S. Department of Defense framework to assess and manage manufacturing risk, readiness, and manufacturability, and can be seen as a more detailed version of the Technology Readiness Level (TRL) assignments. The MRL for assignments 1-4 are described in Table 12. The results of the assessment are that the CFEA technology is in the MRL 4 regime, succinctly described as "capability to produce the technology in a laboratory environment." The full MRL report is in Appendix B.

Table 12: Description of the first 4 manufacturing readiness levels.

Phase (as specified by DoDI 5000.02)	**Leading to**	**MRL**	**Definition**	**Description**
Materiel Solutions Analysis	Materiel Development Decision review	1	Basic manufacturing implications identified	Basic research expands scientific principles that may have manufacturing implications. The focus is on a high level assessment of manufacturing opportunities. The research is unfettered.
		2	Manufacturing concepts identified	Invention begins. Manufacturing science and/or concept described in application context. Identification of material and process approaches are limited to paper studies and analysis. Initial manufacturing feasibility and issues are emerging.
		3	Manufacturing proof of concept developed	Conduct analytical or laboratory experiments to validate paper studies. Experimental hardware or processes have been created, but are not yet integrated or representative. Materials and/or processes have been characterized for manufacturability and availability but further evaluation and demonstration is required.
	Milestone A decision	4	Capability to produce the technology in a laboratory environment.	Required investments, such as manufacturing technology development identified. Processes to ensure manufacturability, producibility and quality are in place and are sufficient to produce technology demonstrators. Manufacturing risks identified for prototype build. Manufacturing cost drivers identified. Producibility assessments of design concepts have been completed. Key design performance parameters identified. Special needs identified for tooling, facilities, material handling and skills.

CHAPTER 5

SUMMARY AND FUTURE WORK

5.1 Summary of Contributions

This work fully developed, from initial concept to working prototype, a novel Spindt type CNT field emission array (CFEA). Its design follows after other Spindt type CNT electron sources in the literature, but incorporates a unique geometry designed to prevent electrical shorting of the gate and promote robustness during FE testing. The CFEA design is patent pending in the United States [186]. The development of the CFEA fabrication and testing processes also led to two original methods. First, an oxygen plasma resurrection technique was developed to reverse electrical shorting after CNT synthesis, which drastically increased open circuit CFEA yield by an average of 71% [168]. Second, during FE testing, an electrical "burnout" resurrection technique was developed to reverse CFEA shorting, which showed a 69% success rate of reversing electrical shorting.

A total of eighty CFEAs were fabricated for high volume FE testing. Extensive analysis of the 80 CFEAs identified three distinct damage modes, which do not necessarily correlate with electrical shorting [178]. Damage analysis indicates that there is robustness that allows for damage to reverse electrical shorting and for the accumulation of significant damage before failure from shorting. The unique CFEA

geometry, namely the horizontal and lateral separation of the CNTs from the gate, may allow for this robustness.

CFEA testing demonstrates FE with a current density of up to 293 μA/cm^2 at the anode and 1.68 mA/cm^2 at the gate, calculated from total area of the device [124]. For comparison to planar CNT sources, current density calculated using the CNT area gives a maximum anode current density of about 241 mA/cm^2. In addition, several microamps of anode current are achieved at as little as 40 V. Cumulative lifetimes are demonstrated in excess of 100 hours with a constant emission of slightly less than 50 μA/cm^2.

The high volume FE testing was also developed to explore the potential application of CFEAs as the cathode in HETs. Forty-one CFEAs were exposed to an operating HET for 40 minutes to determine the effect of the plasma environment on the CFEAs [182]. Despite sputtering of gold on the CFEA packages, there is no evidence of sputtering on the actual CFEAs after exposure. No significant changes to the CNTs or etch pits are observed, indicating the CFEA can withstand the HET environment. This effort is the first experimental study of CNT field emitters in an operational HET environment, and the results are encouraging for future development.

A collaboration with AFIT will further explore the utility of CNT electron sources in the space environment. CFEAs developed in this work were provided to AFIT to be integrated as the payload in an experimental CubeSat, called ALICE. The CubeSat objective is to test the CFEA emission performance in the space environment and compare it to that on earth. ALICE has passed all flight tests and is currently awaiting launch scheduled for December 2013. This work marks the first planned launch and operation of a CNT field emitter in space.

5.2 Future Work

The developments within this dissertation include the initial advancements of a laboratory prototype CNT electron source. Significant progress must be made to advance the TRL and achieve a commercially viable device. The objectives for future work can be broken down into three categories: (1) improve the CFEA emission metrics, (2) increase reliability by studying and preventing electrical shorting and damage, and (3) further explore the utility of the CFEAs, such as in the space environment.

First, the emission metrics (current density, anode:gate current ratio, lifetime) need to be improved. The easiest way to improve current emission performance could be to modify how I-V tests are run. The collaborative AFIT emission tests, which used anode controlled tests, demonstrated much higher currents and must be repeated internally. This testing is identical to the cathode current controlled tests, except the anode current provides the feedback for potential. Thus, with this method testing can continue even during current spikes or high gate currents, as long as anode current is present (confirming FE). Other methods to improve emission could be simultaneously achieved by the following methods to prevent shorting.

Second, efforts to prevent electrical shorting of the gate need to be continued by confirming the effect if diffusion oil backstreaming, fundamentally studying FE and shorting, and using novel design improvements to prevent shorting. Arcing and electrical shorting caused by oil backstreaming during FE testing has not been definitively confirmed in this work. A simple method to confirm the effect is to directly compare the performance of the same CFEAs in the two chambers. In addition, material investigations on diffusion pumped samples, such as high performance liquid chromatography or mass

spectroscopy, could be made to confirm the presence of diffusion oil on the CFEA surface.

The FE, damage, and shorting mechanism in the CFEA design needs to be carefully studied. Integrating new lithography masks could maintain the same pit design in a much smaller device area with many fewer pits. In this simplified design, small numbers of pits or even individual pits could be individually gated. This modification would make testing more difficult (each gate on an independent channel), but would allow the study of the emission and damage/shorting on individual or groups of pits. In addition, the small groupings would make locating a short much easier. Additionally, physical techniques should be used to determine the location of FE sites, such as by using a small scanning anode during diode testing, phosphor anodes, or field emission microscopy.

The IR testing of shorted samples should be continued on the CFEAs or the above simplified design. Of particular interest is to use the IR test to locate a shorted pit so that it can be imaged in the SEM. Then the electrical short can be burned out under the IR camera, and the same pit can be reimaged to determine the effect of burnout. This test could give insight into if damage occurs before or after burnout. In addition, modeling of the heat dissipated using finite element analysis could give insight to the properties of the electrical short and if the observed temperatures are realistic.

Other novel design improvements could be used to prevent electrical shorting. For example, work by Wang, et al. demonstrated controllable vapor densification of CNT bundles using solvents [187]. This method is highly controllable and could prevent electrical shorting caused by moving or detached CNTs. Another potential improvement

uses atomic layer deposition to conformally coat the CNTs in a few nanometer thick Al_2O_3. The main benefit of the coating would be to provide mechanical strength to the CNTs to prevent movement and detachment. In addition, the coating could facilitate heat transfer away from the CNTs during FE, as Al_2O_3 is a good thermal conductor (30 W/mK) and is a significant improvement over vacuum [101].

Third, applications of CNT electron sources need to be further explored, especially in the space environment. The planned ALICE CubeSat test with AFIT will advance our understanding of CNT FE performance in the space environment. In another application, feasibility tests should be conducted for the utility of CFEAs with electrodynamic space tethers, which CFEAs are uniquely suited for.

For the CFEA work with HETs, longer duration testing needs to be conducted since the initial test showed no degradation of the CFEA. Other tests and significant improvements in the CFEA performance are needed before operation of a HET can be achieved. Of particular interest is high pressure FE testing to simulate performance in the high pressure region (~10^{-4} Torr) around the HET. For improvements, the proportion of anode current needs to be maximized to minimize power requirements, and current density needs to be greatly increased. Table 13 shows the parameters for running the tested Busek HET compared to the current and projected CFEA performance. Considerable real estate is available to the CFEAs since they can be placed radially around the thruster. However, given recent anode current densities, an area of a quarter meter is needed to meet the 800 mA discharge current. If the recent cathode current density achieved is completely from FE and if all the current can be directed to the anode, then a much smaller CFEA area is needed. Reaching goals of 5-10 mA/cm^2 would

require more feasible CFEA areas. This proposed testing and improvements could culminate in operating a HET exclusively with CFEAs.

Table 13: Comparison of the metrics needed for operating a Busek BHT-200 HET and the current and future CFEA emission metrics with their necessary required emitter areas.

	Discharge Current	**Input Power**	**Discharge Voltage**	**Emitter Area**
BHT-200	800 mA	200 W	250 V	n/a
CFEA Anode	0.3 mA/cm^2	200 W	250 V	>2600 cm^2
CFEA Cathode	1.7 mA/cm^2	200 W	250 V	>470 cm^2
CFEA Goal 1	5 mA/cm^2	200 W	250 V	160 cm^2
CFEA Goal 2	10 mA/cm^2	200 W	250 V	80 cm^2

APPENDIX A

TEST PROCEDURES

Field Emission Test Procedures

Phase 1 (at GTRI)

1. Remove the front shield from the cathode array and set aside.
2. Install electronic packages with CFEAs into cathode array circuit boards. The circuit boards will already be connected to the back plate of the cathode array. Record package identification with board channel for post-test analysis.
3. Record list of populated slots in the array for delivery to HPEPL
4. Check each package for contact with the circuit board by contacting a multimeter to the package and corresponding output pin on the circuit board.
5. Affix the front shield of the cathode array onto the back plate and circuit board assembly.
6. Take pictures
7. Place cover onto assembly and secure in transport container.
8. Deliver cathode array and the list of populated slots to HPEPL.

Phase 2 (at HPEPL)

Installation in Vacuum Facility:

1. Remove from transport container and remove cover.

2. Take pictures of received cathode array.
3. Place cathode array onto the insulating G-10 base of the bell jar mount.
4. Connect DB-25 cables from the chamber integrator board to each of the circuit boards through the back plate interface. Verify correct connection by referencing indicators on back plate interface and DB-25 cable connectors.
5. Connect the gate connection to the back plate interface.
6. Take Pictures
7. Affix the anode above the cathode array, making sure to electrically connect the anode connection via a screw terminal.
8. Lower Bell Jar chamber top until it is 3” away from the base.
9. Connect DD-50 cables from the chamber integrator board to the DD-50 cables connecting to the 4.5” CF port located on the chamber top. Verify correct connection by referencing indicators on the cable connectors.
10. Verify electrical connections
11. Finish lowering the Bell Jar chamber top onto the base of the facility.
12. Evacuate Bell Jar 2 by following standard HPEPL procedure and hold at $<10^{-5}$ Torr for 48 hours to allow for out-gassing.
13. Record vacuum facility leak rate

UV Gas Desorption

1. Make sure all view ports are covered.
2. Notify other lab personnel of UV process start. Personnel should use UV safety glasses while in the area.

3. Record the pressure on the SenTorr ionization gauge reader.
4. Turn on the UV system and run for 60 minutes.
5. Turn off the UV system. Record the pressure on the SenTorr.
6. Wait 60 minutes and repeat the procedure from Step 3 of this section.
7. When complete, notify lab personnel of the conclusion of the process.

Initial Characterization:

1. Initiate the characterization LabView VI.
2. Turn on power supplies (0 V, 0 A)
3. Enter in a test file directory where data from the test will be saved.
4. Enter the desired voltage ramp parameters. An example of the parameters is: Maximum Cathode Voltage – 200 V, Cathode Voltage Step – 5 V, Step Time – 15 sec.
5. Enter the desired cathode current target. With the current CFEA design, this value is 14.8 μA for 10 μA/cm^2.
6. Enter the desired anode bias voltage (+50 V).
7. Check that each piece of electronics is referenced correctly by the VI. This is done by checking hardware port names in the Measurement and Automation Explorer tool provided by National Instruments.
8. Enter the sampling period. Minimum time period is approximately 3 seconds to avoid system sync errors.
9. Enter the desired hold time at the current target required to qualify the CFEAs. An example time is 5 minutes (300 seconds).

10. Toggle the switches on the VI interface corresponding to the populated positions on the cathode array to ON.
11. Press “run” once all test parameters have been entered and double checked. The VI will record which emitters meet the turn-on voltage requirement without electrical shorting.
12. Review the output file for a list of successfully emitting array positions.
13. Close the LabView program

Testing:

1. Initiate the lifetime test LabView VI.
2. Enter in a test file directory where data from the test will be saved.
3. Enter the desired voltage ramp parameters. An example of the parameters is: Maximum Cathode Voltage - 295 V, Cathode Voltage Step - 5 V, Step Time - 15 sec.
4. Enter the desired maximum voltage hold time of 200 hours.
5. Enter the desired anode bias voltage (+50 V).
6. Check that each piece of electronics is referenced correctly by the VI. This is done by checking hardware port names in the Measurement and Automation Explorer tool provided by National Instruments.
7. Enter the minimum current over which the emitter package is considered to have shorted (3 mA)
8. Enter the sampling period. Minimum time period is approximately 3 seconds to avoid system sync errors.

9. Toggle the switches on the interface corresponding to the populated (and successfully characterized) positions on the cathode array to ON.
10. Press “run” once all test parameters have been entered and double checked. If the minimum cathode current over which the emitter package is considered to have shorted is reached on any channel, the VI will automatically turn off power to that channel and log the event.
11. Every four hours, check the status of the cathode array channels, which is displayed on the VI front interface. Record all channels which have been automatically turned off. Any channels which are automatically switched off can be manually switched back on to check if the issue resolved itself. Record if any channels which were automatically turned off stay on when manually switched back on.
12. The test is complete when the indicator labeled “Done” on the VI front interface turns on.
13. Turn off the power supplies (0 V, 0 A)
14. Close the LabView program.

Shutdown and Removal:

1. Shut down and vent the chamber following standard HPEPL procedure.
2. Hoist the Bell Jar top off of the base by 3”.
3. Disconnect the DD-50 cables connecting to the 4.5” CF port on the chamber top from the DD-50 cables connecting to the chamber integrator board on the bottom of the chamber.

4. Hoist the Bell Jar top up as high as necessary to remove the cathode array.
5. Take Pictures
6. Remove the anode plate from the test setup and set aside.
7. Take Pictures
8. Disconnect the gate connection from the back plate interface.
9. Disconnect the DB-25 cables from the back plate interface.
10. Carefully lift the cathode array from the test assembly and remove from the chamber.
11. Take Pictures
12. Install cover on cathode array and secure in storage container.
13. Return the cathode array assembly to GTRI for post-test disassembly.

Phase 3 (GTRI)

1. Remove from storage container and remove cover.
2. Take Pictures
3. Remove the front shield from the cathode array and set aside.
4. Take Pictures
5. Remove each emitter package, double checking the accuracy of the record of emitter package identification number and channel placement.
6. Take Pictures
7. Reinstall front shield for array storage.
8. Reinstall cover and place in storage container.

HET Exposure Procedures

Phase 1 (at GTRI)

1. Remove the front shield from the cathode array and set aside.
2. Install electronic packages with CFEAs into cathode array circuit boards. The circuit boards will already be connected to the back plate of the cathode array. Record package identification with board channel for post-test analysis.
3. Record list of populated slots in the array for delivery to HPEPL
4. Check each package for contact with the circuit board by contacting a multimeter to the package and corresponding output pin on the circuit board.
5. Affix the front shield of the cathode array onto the back plate and circuit board assembly.
6. Take pictures
7. Place cover onto assembly and secure in transport container.
8. Deliver cathode array and the list of populated slots to HPEPL.

Phase 2 (HPEPL)

Installation in VTF-2

1. Install the BHT-200 onto the thrust stand following documented lab procedure.
2. Install modified hot cathode mount.
3. Install Moscow Aviation hot cathode following documented lab procedure.
4. Carefully remove the standard 4-40 bolts on the front face of the BHT-200.
5. Remove cathode array from transport container and remove cover.

6. Take pictures of received cathode array.
7. Install alumina spacers and pre-thread 4-40 bolts used for securing the cathode array to the BHT-200 by threading each 4-40 bolt through a 3/16" spacer, then through a HET mounting bolt hole on the array, then through a 3/8" spacer.
8. Carefully mount the cathode array onto the BHT-200. One researcher should hold the array in place on the front of the BHT-200 while another lightly tightens the bolts.
9. Connect strain relieved DB-25 cables from the chamber integrator board to each of the circuit boards through the back plate interface. Verify correct connection by referencing indicators on back plate interface and DB-25 cable connectors.
10. Connect the gate connection to the back plate interface.
11. Take Pictures
12. Verify electrical connections
13. Evacuate VTF-2 by following standard documented lab procedure.

UV Gas Desorption

1. Make sure all view ports are covered.
2. Notify other lab personnel of UV process start. Personnel should use UV safety glasses while in the area.
3. Record the pressure on the SenTorr ionization gauge reader.
4. Turn on the UV system and run for 60 minutes.
5. Turn off the UV system. Record the pressure on the SenTorr.
6. Wait 60 minutes and repeat the procedure from Step 3 of this section.

7. When complete, notify lab personnel of the conclusion of the process.

Characterization:

1. Initiate the characterization LabView VI.
2. Turn on power supplies (0 V, 0 A)
3. Enter in a test file directory where data from the test will be saved.
4. Enter the desired voltage ramp parameters. An example of the parameters is: Maximum Cathode Voltage – 200 V, Cathode Voltage Step – 5 V, Step Time – 15 sec.
5. Enter the desired cathode current target. With the current emitter chip/package design, this value is 7.4 μA.
6. Check that each piece of electronics is referenced correctly by the VI. This is done by checking hardware port names in the Measurement and Automation Explorer tool provided by National Instruments.
7. Enter the sampling period. Minimum time period is approximately 3 seconds to avoid system sync errors.
8. Enter the desired hold time at the current target required to qualify the emitters. An example time is 5 minutes (300 seconds).
9. Toggle the switches on the interface corresponding to the populated positions on the array to ON.
10. Press "run" once all test parameters have been entered and double checked. The VI will record which emitters meet the turn-on voltage requirement without shorting.

11. Review the output file for a list of successfully emitting array positions.
12. Close the LabView program

Testing:

1. Initiate the lifetime test LabView VI.
2. Enter in a test file directory where data from the test will be saved.
3. Enter the desired voltage ramp parameters. An example of the parameters is: Maximum Cathode Voltage - 295 V, Cathode Voltage Step - 5 V, Step Time - 15 sec.
4. Enter the desired maximum voltage hold time of 200 hours.
5. Enter the desired anode bias voltage (50 V).
6. Check that each piece of electronics is referenced correctly by the VI. This is done by checking hardware port names in the Measurement and Automation Explorer tool provided by National Instruments.
7. Enter the minimum current over which the emitter package is considered to have shorted (3 mA)
8. Enter the sampling period. Minimum time period is approximately 3 seconds to avoid system sync errors.
9. Start the BHT-200 and hot cathode by following documented lab procedures. Ensure stable operation before moving forward.
10. Toggle the switches on the interface corresponding to the populated (and successfully characterized) positions on the array to ON.

11. Press “run” once all test parameters have been entered and double checked. If the minimum cathode current over which the emitter package is considered to have shorted is reached on any channel, the VI will automatically turn off power to that channel and log the event.
12. After pressing “run”, close the isolation switch between the HET and cathode array circuits.
13. The test is complete when the indicator labeled “Done” on the VI front interface turns on.
14. Turn off the power supplies (0 V, 0 A)
15. Close the LabView program.
16. Shut down the BHT-200 and hot cathode by following documented lab procedures.

Shutdown and Removal:

1. Shut down and vent the chamber following standard HPEPL procedure.
2. Open the chamber door.
3. Take Pictures
4. Disconnect the gate connection from the back plate interface.
5. Disconnect the DB-25 cables from the back plate interface.
6. Carefully loosen the bolts connecting the BHT-200 and cathode array.
7. Remove the array and remove the spacers.
8. Take Pictures
9. Install cover and secure in storage container.

10. Return the cathode array assembly to GTRI for post-test disassembly and imaging.

Phase 3 (GTRI)

1. Remove cathode array from storage container and remove cover.
2. Take Pictures
3. Remove the front shield from the cathode array and set aside.
4. Take Pictures
5. Remove each emitter package, double checking the accuracy of the record of emitter package identification number and channel placement.
6. Take Pictures
7. Reinstall front shield for array storage.
8. Reinstall cover and place in storage container.

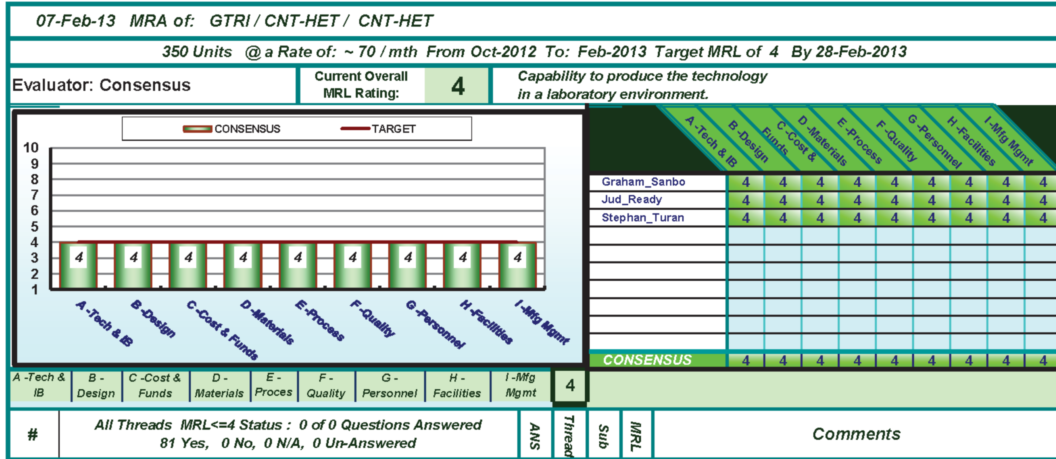
APPENDIX B

MANUFACTURING READINESS LEVEL ASSESSMENT

07-Feb-13 MRA of: GTRI / CNT-HET / CNT-HET

350 Units @ a Rate of: ~ 70 / mth From Oct-2012 To: Feb-2013 Target MRL of 4 By 28-Feb-2013

Evaluator: Consensus | Current Overall MRL Rating: **4** | *Capability to produce the technology in a laboratory environment.*



#	*All Threads MRL<=4 Status : 0 of 0 Questions Answered 81 Yes, 0 No, 0 N/A, 0 Un-Answered*	ANS	Thread	Sub	MRL	Comments
1	Is the Technology Readiness at TRL 1 or greater?	Yes	A -Tech & IB	Tech Maturity	1	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
2	Is the Technology Readiness at TRL 2 or greater?	Yes	A -Tech & IB	Tech Maturity	2	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
3	Is the Technology Readiness at TRL 3 or greater?	Yes	A -Tech & IB	Tech Maturity	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
4	Is the Technology Readiness at TRL 4 or greater?	Yes	A -Tech & IB	Tech Maturity	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
5	Is the Technology Readiness at TRL 5 or greater?	Yes	A -Tech & IB	Tech Maturity	5	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
6	Is the Technology Readiness at TRL 6 or greater?	No	A -Tech & IB	Tech Maturity	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
7	Is the Technology Readiness at TRL 7 or greater?	No	A -Tech & IB	Tech Maturity	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
8	Is the Technology Readiness at TRL 7 or greater?	No	A -Tech & IB	Tech Maturity	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
9	Is the Technology Readiness at TRL 9?	No	A -Tech & IB	Tech Maturity	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
10	Is the Technology Readiness at TRL 9?	No	A -Tech & IB	Tech Maturity	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
11	Have potential manufacturing sources been identified for technology needs (Understand state of the art)?	Yes	A -Tech & IB	A 1 - Transition	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion

350 Units @ a Rate of: ~ 70 / mth From Oct-2012 To: Feb-2013 Target MRL of 4 By 28-Feb-2013

Evaluator: Consensus | Current Overall MRL Rating: 4 | *Capability to produce the technology in a laboratory environment.*

#	Question	Answer	Thread	Sub-thread	MRL	Comments
12	Have industrial base capabilities and gaps/risks been identified for key technologies, components, and/or key processes?	Yes	A -Tech & IB	A 1 - Transition	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
13	Has the industrial base assessment been initiated to identify potential manufacturing sources to produce the required capability?	No	A -Tech & IB	A 1 - Transition	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
14	Have sole/single/foreign source vendors been identified?	No	A -Tech & IB	A 1 - Transition	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
15	Has planning begun to minimize the risks associated with sole/single/foreign source vendors?	No	A -Tech & IB	A 1 - Transition	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
16	Has the Industrial Capability Assessment (ICA) for MS B been completed?	No	A -Tech & IB	A 1 - Transition	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
17	Is the industrial capability in place to support the manufacturing of development articles?	Yes	A -Tech & IB	A 1 - Transition	6	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
18	Are the plans to minimize sole/single/foreign sources complete?	No	A -Tech & IB	A 1 - Transition	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
19	Has the need for sole/single/foreign sources been justified?	No	A -Tech & IB	A 1 - Transition	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
20	Have potential alternative sources been identified?	No	A -Tech & IB	A 1 - Transition	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
21	Has the industrial capability to support production been analyzed?	Yes	A -Tech & IB	A 1 - Transition	7	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
22	Is the stability of all sole/single/foreign sources being assessed/monitored?	No	A -Tech & IB	A 1 - Transition	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
23	Are the necessary alternates to sole/single/foreign sources being developed?	No	A -Tech & IB	A 1 - Transition	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
24	Has the Industrial Capability Assessment (ICA) for Milestone C been completed?	No	A -Tech & IB	A 1 - Transition	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
25	Is the industrial capability in place to support Low Rate Initial Production (LRIP)?	Yes	A -Tech & IB	A 1 - Transition	8	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
26	Are all necessary sources available including multi-sourcing where cost-effective or necessary to mitigate risk?	No	A -Tech & IB	A 1 - Transition	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
27	Is the industrial capability in place to support the start of Full Rate Production (FRP)?	No	A -Tech & IB	A 1 - Transition	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments

350 Units @ a Rate of: ~ 70 / mth From Oct-2012 To: Feb-2013 Target MRL of 4 By 28-Feb-2013

Evaluator: Consensus	Current Overall MRL Rating: 4	*Capability to produce the technology in a laboratory environment.*				
28	Does the industrial capability support Full Rate Production (FRP)?	Yes	A -Tech & IB	A 1 - Transition	10	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
29	Has the industrial capability been assessed to support modifications, upgrades, surge, and other potential manufacturing requirements?	No	A -Tech & IB	A 1 - Transition	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
30	Have new manufacturing concepts and potential solutions been identified?	Yes	A -Tech & IB	A 2 - Mfg Tech Dev	2	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
31	Have manufacturing technology concepts been identified through experiments/models?	Yes	A -Tech & IB	A 2 - Mfg Tech Dev	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
32	Have pertinent Manufacturing Science (MS) and Advanced Manufacturing Technology requirements been identified?	Yes	A -Tech & IB	A 2 - Mfg Tech Dev	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
33	Have the required manufacturing technology development efforts been initiated as applicable?	No	A -Tech & IB	A 2 - Mfg Tech Dev	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
34	Are the necessary manufacturing technology development efforts continuing?	Yes	A -Tech & IB	A 2 - Mfg Tech Dev	6	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
35	Have the required manufacturing technology development solutions been demonstrated in a production relevant environment?	Yes	A -Tech & IB	A 2 - Mfg Tech Dev	6	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
36	Are the necessary manufacturing technology development efforts still continuing?	Yes	A -Tech & IB	A 2 - Mfg Tech Dev	7	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
37	Have the required manufacturing science and manufacturing technology development solutions been demonstrated in a production representative environment?	Yes	A -Tech & IB	A 2 - Mfg Tech Dev	7	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
38	Are the primary manufacturing technology efforts concluding and some improvement efforts continuing?	No	A -Tech & IB	A 2 - Mfg Tech Dev	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
39	Have the required manufacturing technology development solutions been validated on a pilot line?	No	A -Tech & IB	A 2 - Mfg Tech Dev	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
40	Have the required manufacturing technology process improvement efforts been initiated for Full Rate Production (FRP)?	No	A -Tech & IB	A 2 - Mfg Tech Dev	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
41	Are manufacturing technology continuous process improvements ongoing?	No	A -Tech & IB	A 2 - Mfg Tech Dev	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
42	Have relevant materials/processes been evaluated for manufacturability using experimental results?	Yes	B -Design	B 1 - Producibility	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
43	Are initial producibility and manufacturability assessments of preferred systems concepts completed?	Yes	B -Design	B 1 - Producibility	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion

350 Units @ a Rate of: ~ 70 / mth From Oct-2012 To: Feb-2013 Target MRL of 4 By 28-Feb-2013

Evaluator: Consensus	Current Overall MRL Rating: 4	Capability to produce the technology in a laboratory environment.				
44	Are the results of the producibility and manufacturability assessment being considered in the selection of preferred design concepts?	Yes	B -Design	B.1 - Producibility	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
45	Are the results of the producibility and manufacturability assessment being reflected in the Technology Development Strategy key components/technologies?	Yes	B -Design	B.1 - Producibility	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
46	Have producibility & manufacturability assessments of key technologies and components been initiated as appropriate?	Yes	B -Design	B.1 - Producibility	5	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
47	Do ongoing design trades consider manufacturing processes and industrial base capability constraints?	No	B -Design	B.1 - Producibility	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
48	Have the manufacturing processes been assessed for capability to test and verify in production and their influence on Operations and Support (O&S)?	No	B -Design	B.1 - Producibility	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
49	Have producibility assessments and producibility trade studies (performance vs. producibility) of key technologies/components been completed?	No	B -Design	B.1 - Producibility	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
50	Are the results of the producibility assessments and trade studies being used to shape the Acquisition Strategy, Systems Engineering Plan (SEP), Manufacturing and Producibility plans, and Planning for Engineering and Manufacturing Development (EMD) or technology insertion programs?	No	B -Design	B.1 - Producibility	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
51	Are the preliminary design choices assessed against manufacturing processes and industrial base capability constraints?	No	B -Design	B.1 - Producibility	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
52	Are the producibility enhancement efforts (e.g. Design For Mfg Assembly (DFX)) initiated?	No	B -Design	B.1 - Producibility	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
53	Are the detailed producibility trade studies using detailed knowledge of key design characteristics and related manufacturing process capabilities completed?	No	B -Design	B.1 - Producibility	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
54	Are the producibility enhancement efforts (e.g. Design For Mfg Assembly) ongoing for an optimized integrated system?	No	B -Design	B.1 - Producibility	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
55	Are manufacturing processes re-assessed as needed for capability to test and verify potential influence on Operations & Support?	No	B -Design	B.1 - Producibility	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
56	Have the producibility improvements been implemented on the system?	Yes	B -Design	B.1 - Producibility	8	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
57	Have the known producibility issues been resolved and pose no significant risk for Low Rate Initial Production (LRIP)?	No	B -Design	B.1 - Producibility	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
58	Have prior producibility improvements been analyzed for effectiveness during Low Rate Initial Production (LRIP)?	No	B -Design	B.1 - Producibility	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
59	Have the producibility issues/risks discovered in Low Rate Initial Production (LRIP) been mitigated and pose no significant risk for Full Rate Production (FRP)?	No	B -Design	B.1 - Producibility	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments

350 Units @ a Rate of: ~ 70 / mth From Oct-2012 To: Feb-2013 Target MRL of 4 By 28-Feb-2013

Evaluator: Consensus | Current Overall MRL Rating: 4 | *Capability to produce the technology in a laboratory environment.*

#	Question	Answer	Thread	Sub-thread	MRL	Comments
60	Have design producibility improvements been demonstrated in Full Rate Production (FRP)?	No	B -Design	B 1 - Producibility	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
61	Are process producibility improvements ongoing?	Yes	B -Design	B 1 - Producibility	10	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
62	Are all modifications, upgrades, Diminishing Mfg Sources & Material Shortages (DMSMS), and other changes assessed for producibility?	No	B -Design	B 1 - Producibility	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
63	Have manufacturing research opportunities been identified?	Yes	B -Design	B 2 - Dsgn Maturity	1	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
64	Have applications been defined?	Yes	B -Design	B 2 - Dsgn Maturity	2	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
65	Have broad performance goals been identified that may drive manufacturing options?	Yes	B -Design	B 2 - Dsgn Maturity	2	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
66	Have top level performance requirements been defined?	Yes	B -Design	B 2 - Dsgn Maturity	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
67	Have trade-offs in design options been assessed based on experiments?	Yes	B -Design	B 2 - Dsgn Maturity	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
68	Are product lifecycle requirements and technical requirements being evaluated?	Yes	B -Design	B 2 - Dsgn Maturity	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
69	Do the Systems Engineering Plan (SEP) and the Test and Evaluation Strategy recognize the need for the establishment/validation of manufacturing capability and management of manufacturing risk for the product lifecycle?	Yes	B -Design	B 2 - Dsgn Maturity	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
70	Have initial potential Key Performance Parameters (KPPs) been identified for the preferred systems concept?	Yes	B -Design	B 2 - Dsgn Maturity	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
71	Are system characteristics and measures to support required capabilities identified?	Yes	B -Design	B 2 - Dsgn Maturity	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
72	Are form, fit, and function constraints and manufacturing capabilities identified for the preferred systems concepts?	Yes	B -Design	B 2 - Dsgn Maturity	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
73	Are lower level performance requirements sufficient to proceed to the preliminary design?	No	B -Design	B 2 - Dsgn Maturity	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
74	Are all enabling/critical technologies and components identified?	No	B -Design	B 2 - Dsgn Maturity	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
75	Do enabling/critical technologies and components consider the product lifecycle?	No	B -Design	B 2 - Dsgn Maturity	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments

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#	Question	Answer	Thread	Sub-thread	MRL	Comments
76	Have the evaluation of design Key Characteristics (KC) been initiated?	No	B -Design	B 2 - Dsgn Maturity	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
77	Have product data required for prototype component manufacturing been released?	No	B -Design	B 2 - Dsgn Maturity	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
78	Has a system allocated baseline been established?	No	B -Design	B 2 - Dsgn Maturity	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
79	Are the system and subsystem preliminary design sufficient for Engineering and Manufacturing Development (EMD)?	Yes	B -Design	B 2 - Dsgn Maturity	6	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
80	Have all enabling/critical technologies/components been demonstrated?	Yes	B -Design	B 2 - Dsgn Maturity	6	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
81	Have preliminary design Key Characteristics (KC) been defined?	No	B -Design	B 2 - Dsgn Maturity	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
82	Are the product requirements and features well enough defined to support critical design review even though design change traffic may be significant?	Yes	B -Design	B 2 - Dsgn Maturity	7	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
83	Has all the product data essential for component manufacturing been released?	No	B -Design	B 2 - Dsgn Maturity	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
84	Have potential Key Characteristic risk issues been identified?	No	B -Design	B 2 - Dsgn Maturity	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
85	Is a mitigation plan in place for potential Key Characteristic risk issues?	No	B -Design	B 2 - Dsgn Maturity	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
86	Is the detailed design of product features and interfaces complete?	No	B -Design	B 2 - Dsgn Maturity	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
87	Has all the product data essential for system manufacturing been released?	No	B -Design	B 2 - Dsgn Maturity	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
88	Does the design change traffic have minimal impact on Low Rate Initial Production (LRIP)?	No	B -Design	B 2 - Dsgn Maturity	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
89	Are the Key Characteristics attainable based upon pilot line demonstrations?	No	B -Design	B 2 - Dsgn Maturity	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
90	Are the major product design features and configuration stable?	No	B -Design	B 2 - Dsgn Maturity	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
91	Has the system design been validated through operational testing of Low Rate Initial Production (LRIP) items?	No	B -Design	B 2 - Dsgn Maturity	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments

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#	Question	Answer	Thread	Sub-thread	MRL	Comments
92	Is the Physical Configuration Audit (PCA) or equivalent complete as necessary?	No	B -Design	B.2 - Dsgn Maturity	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
93	Is the design change traffic limited to minor configuration changes?	No	B -Design	B.2 - Dsgn Maturity	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
94	Are all Key Characteristics controlled in Low Rate Initial Production (LRIP) to appropriate quality levels?	No	B -Design	B.2 - Dsgn Maturity	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
95	Is the product design stable (i.e. design changes are few and generally limited to those required for continuous improvement or in reaction to obsolescence)?	No	B -Design	B.2 - Dsgn Maturity	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
96	Are all Key Characteristics controlled in Full Rate Production (FRP) to appropriate quality levels?	No	B -Design	B.2 - Dsgn Maturity	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
97	Has the cost model approach been defined?	Yes	C -Cost & Funds	C.1 - Cost Modeling	2	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
98	Have initial cost targets and risks been identified?	Yes	C -Cost & Funds	C.1 - Cost Modeling	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
99	Has a high level process chart model been developed?	Yes	C -Cost & Funds	C.1 - Cost Modeling	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
100	Have technology cost models been developed for new process steps and materials based on experiments?	Yes	C -Cost & Funds	C.1 - Cost Modeling	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
101	Have key manufacturing, material and specialized requirement cost drivers been identified?	Yes	C -Cost & Funds	C.1 - Cost Modeling	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
102	Are detailed process chart cost models driven by process variables?	Yes	C -Cost & Funds	C.1 - Cost Modeling	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
103	Has cost driver uncertainty been quantified?	Yes	C -Cost & Funds	C.1 - Cost Modeling	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
104	Do prototype components produced in a production relevant environment, or simulations drive end-to-end cost models?	No	C -Cost & Funds	C.1 - Cost Modeling	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
105	Is there a realistic cost model that includes materials, labor, equipment, tooling/Special Test Equipment (STE), setup, yield/scrap/rework, Work In Progress (WIP), and capability/capacity constraints?	No	C -Cost & Funds	C.1 - Cost Modeling	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
106	Have cost models been updated with design requirements, material specifications, tolerances, integrated master schedule, results of system/subsystem simulations and production relevant prototype demonstrations?	No	C -Cost & Funds	C.1 - Cost Modeling	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
107	Are cost models updated with the results of systems/sub-systems produced in a production representative environment, production plant layout and design, and obsolescence solutions?	No	C -Cost & Funds	C.1 - Cost Modeling	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments

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#	Question	Answer	Thread	Sub-thread	MRL	Comments
108	Have cost models been updated with results of the pilot line build?	No	C -Cost & Funds	C 1 - Cost Modeling	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
109	Has the Full Rate Production (FRP) cost model been updated with the result of the Low Rate Initial Production (LRIP) build?	No	C -Cost & Funds	C 1 - Cost Modeling	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
110	Has the cost model been validated against actual Full Rate Production (FRP) cost?	No	C -Cost & Funds	C 1 - Cost Modeling	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
111	Have manufacturing cost implications been identified?	Yes	C -Cost & Funds	C 2 - Cost Analysis	1	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
112	Have cost elements been identified?	Yes	C -Cost & Funds	C 2 - Cost Analysis	2	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
113	Has a sensitivity analysis been conducted to define cost drivers and production development strategy (i.e. lab to pilot to factory)?	Yes	C -Cost & Funds	C 2 - Cost Analysis	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
114	Have producibility cost risks been assessed?	Yes	C -Cost & Funds	C 2 - Cost Analysis	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
115	Do initial cost models support Analysis of Alternatives (AoA) and Alternative Systems Review (ASR)?	Yes	C -Cost & Funds	C 2 - Cost Analysis	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
116	Are costs analyzed using prototype component actuals to ensure target costs are achievable?	No	C -Cost & Funds	C 2 - Cost Analysis	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
117	Are decisions regarding design choices, make/buy, capacity, process capability, sources, quality, key characteristics, yield/rate, and variability influenced by cost models?	No	C -Cost & Funds	C 2 - Cost Analysis	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
118	Are costs analyzed using prototype system/sub-system actuals to ensure target costs are achievable?	No	C -Cost & Funds	C 2 - Cost Analysis	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
119	Have cost targets been allocated to subsystems?	No	C -Cost & Funds	C 2 - Cost Analysis	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
120	Have cost reduction and avoidance strategies been developed?	No	C -Cost & Funds	C 2 - Cost Analysis	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
121	Have the manufacturing costs been rolled up to the system/sub-system level and been tracked against targets?	No	C -Cost & Funds	C 2 - Cost Analysis	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
122	Are detailed trade studies and engineering change requests supported by cost estimates?	No	C -Cost & Funds	C 2 - Cost Analysis	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
123	Are cost reduction and avoidance strategies underway?	No	C -Cost & Funds	C 2 - Cost Analysis	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments

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#	Question	Answer	Thread	Sub-thread	MRL	Comments
124	Are costs analyzed using pilot line actuals to ensure target costs are achievable?	No	C -Cost & Funds	C 2 - Cost Analysis	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
125	Does manufacturing cost analysis support proposed changes to requirements or configuration?	No	C -Cost & Funds	C 2 - Cost Analysis	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
126	Are the cost reduction initiatives ongoing?	No	C -Cost & Funds	C 2 - Cost Analysis	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
127	Have Low Rate Initial Production (LRIP) cost goals been met and has the learning curve been analyzed with actual data?	No	C -Cost & Funds	C 2 - Cost Analysis	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
128	Are the cost reduction initiatives still ongoing?	No	C -Cost & Funds	C 2 - Cost Analysis	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
129	Has touch labor efficiency been analyzed to meet production rates?	No	C -Cost & Funds	C 2 - Cost Analysis	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
130	Have elements of inefficiency for touch labor been identified with plans in place for reduction?	No	C -Cost & Funds	C 2 - Cost Analysis	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
131	Have Full Rate Production (FRP) cost goals been met?	No	C -Cost & Funds	C 2 - Cost Analysis	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
132	Are the cost reduction initiatives continuing?	Yes	C -Cost & Funds	C 2 - Cost Analysis	10	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
133	Have potential investments been identified?	Yes	C -Cost & Funds	C 3 - Mfg Invst Bdgt	1	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
134	Do the program/projects have reasonable budget estimates for reaching MRL 3 through experiment?	Yes	C -Cost & Funds	C 3 - Mfg Invst Bdgt	2	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
135	Do the program/projects have reasonable budget estimates for reaching MRL 4 by Milestone A?	Yes	C -Cost & Funds	C 3 - Mfg Invst Bdgt	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
136	Have manufacturing technology initiatives been identified to reduce costs?	Yes	C -Cost & Funds	C 3 - Mfg Invst Bdgt	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
137	Does the program have a reasonable budget estimate to reach MRL 6 by Milestone B?	Yes	C -Cost & Funds	C 3 - Mfg Invst Bdgt	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
138	Does the cost estimate include capital investment for production-relevant equipment?	Yes	C -Cost & Funds	C 3 - Mfg Invst Bdgt	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
139	Are all outstanding MRL 4 risk areas understood with approved mitigation plans in place?	Yes	C -Cost & Funds	C 3 - Mfg Invst Bdgt	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion

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#	Question	Answer	Thread	Sub-thread	MRL	Comments
140	Does the program have an updated budget estimate for reaching MRL 6 by Milestone B?	No	C -Cost & Funds	C 3 - Mfg Invst Bdgt	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
141	Are all outstanding MRL 5 risk areas understood with approved mitigation plans in place?	No	C -Cost & Funds	C 3 - Mfg Invst Bdgt	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
142	Does the program have a reasonable budget estimate for reaching MRL 8 by Milestone C?	No	C -Cost & Funds	C 3 - Mfg Invst Bdgt	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
143	Does the cost estimate include capital investment for production-representative equipment by CDR and pilot line equipment by Milestone C?	No	C -Cost & Funds	C 3 - Mfg Invst Bdgt	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
144	Are all outstanding MRL 6 risk areas understood with approved mitigation plans in place?	No	C -Cost & Funds	C 3 - Mfg Invst Bdgt	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
145	Does the program have an updated budget estimate for reaching MRL 8 by Milestone C?	No	C -Cost & Funds	C 3 - Mfg Invst Bdgt	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
146	Are all outstanding MRL 7 risk areas understood with approved mitigation plans in place?	No	C -Cost & Funds	C 3 - Mfg Invst Bdgt	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
147	Does the program have a reasonable budget estimate for reaching MRL 9 by the Full Rate Production (FRP) decision point?	No	C -Cost & Funds	C 3 - Mfg Invst Bdgt	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
148	Does the cost estimate include investment for Low Rate Initial Production (LRIP) and Full Rate Production (FRP)?	No	C -Cost & Funds	C 3 - Mfg Invst Bdgt	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
149	Are all outstanding MRL 8 risk areas understood with approved mitigation plans in place?	No	C -Cost & Funds	C 3 - Mfg Invst Bdgt	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
150	Does the program have a reasonable budget estimate for Full Rate Production (FRP)?	No	C -Cost & Funds	C 3 - Mfg Invst Bdgt	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
151	Are all outstanding MRL 9 risk areas understood with approved mitigation plans in place?	No	C -Cost & Funds	C 3 - Mfg Invst Bdgt	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
152	Are the production budgets sufficient for production at the required rates and schedule to support the funded program?	No	C -Cost & Funds	C 3 - Mfg Invst Bdgt	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
153	Have material properties been identified for research?	Yes	D -Materials	D 1 - Mtrl Maturity	1	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
154	Have material properties and characteristics been predicted?	Yes	D -Materials	D 1 - Mtrl Maturity	2	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
155	Have material properties been validated and assessed for basic manufacturability using experiments?	Yes	D -Materials	D 1 - Mtrl Maturity	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion

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156	Has a survey been completed to determine if the projected material has been produced in a laboratory environment?	Yes	D -Materials	D.1 - Mtrl Maturity	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
157	Have all materials been manufactured or produced in a prototype environment (may be in a similar application/program)?	Yes	D -Materials	D.1 - Mtrl Maturity	5	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
158	Are maturity efforts in place to address new material production risks for technology demonstration?	Yes	D -Materials	D.1 - Mtrl Maturity	5	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
159	Has the material maturity been verified with technology demonstration articles?	Yes	D -Materials	D.1 - Mtrl Maturity	6	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
160	Are preliminary material specifications in place?	Yes	D -Materials	D.1 - Mtrl Maturity	6	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
161	Have material properties been adequately characterized?	Yes	D -Materials	D.1 - Mtrl Maturity	6	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
162	Is the material maturity sufficient for a pilot line build?	Yes	D -Materials	D.1 - Mtrl Maturity	7	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
163	Have the necessary material specifications been approved?	Yes	D -Materials	D.1 - Mtrl Maturity	7	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
164	Have the materials been proven and validated during Engineering and Manufacturing Development (EMD) as adequate to support Low Rate Initial Production (LRIP)?	Yes	D -Materials	D.1 - Mtrl Maturity	8	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
165	Are material specifications stable?	Yes	D -Materials	D.1 - Mtrl Maturity	8	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
166	Have all necessary materials been proven and controlled to specification in Low Rate Initial Production (LRIP)?	No	D -Materials	D.1 - Mtrl Maturity	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
167	Have all necessary materials been proven and controlled to specification in Full Rate Production (FRP)?	No	D -Materials	D.1 - Mtrl Maturity	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
168	Has material availability been assessed?	Yes	D -Materials	D.2 - Mtrl Availability	2	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
169	Have material scale-up issues been identified?	Yes	D -Materials	D.2 - Mtrl Availability	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
170	Have projected lead times been identified for all difficult to obtain, difficult to process, or hazardous materials?	Yes	D -Materials	D.2 - Mtrl Availability	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
171	Have material quantities and lead times been estimated?	Yes	D -Materials	D.2 - Mtrl Availability	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion

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#	Question	Answer	Thread	Sub-thread	MRL	Comments
172	Have material availability issues been addressed for the prototype build?	Yes	D -Materials	D 2 - Mtrl Availability	5	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
173	Have significant material risks been identified for all materials?	Yes	D -Materials	D 2 - Mtrl Availability	5	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
174	Has planning begun to address scale-up issues?	No	D -Materials	D 2 - Mtrl Availability	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
175	Have material availability issues been addressed to meet Engineering and Manufacturing Development (EMD) build?	No	D -Materials	D 2 - Mtrl Availability	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
176	Have potential obsolescence issues been identified?	Yes	D -Materials	D 2 - Mtrl Availability	6	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
177	Have material availability issues been addressed to meet Engineering and Manufacturing Development (EMD) builds?	Yes	D -Materials	D 2 - Mtrl Availability	7	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
178	Have long lead procurements been identified/planned for Low Rate Initial Production (LRIP)?	No	D -Materials	D 2 - Mtrl Availability	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
179	Is an obsolescence plan in place?	No	D -Materials	D 2 - Mtrl Availability	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
180	Have long lead procurements been initiated for Low Rate Initial Production (LRIP)?	No	D -Materials	D 2 - Mtrl Availability	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
181	Are material availability risk issues minimized for Low Rate Initial Production (LRIP)?	No	D -Materials	D 2 - Mtrl Availability	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
182	Have long lead procurements been initiated for Full Rate Production (FRP)?	No	D -Materials	D 2 - Mtrl Availability	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
183	Are availability risk issues minimized for Full Rate Production (FRP)?	No	D -Materials	D 2 - Mtrl Availability	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
184	Are all significant Full Rate Production (FRP) material availability risk issues resolved?	No	D -Materials	D 2 - Mtrl Availability	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
185	Has an initial assessment of potential supply chain capability been completed?	Yes	D -Materials	D 3 - Sply Chain Mgmt	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
186	Has a survey for potential supply chain sources been completed?	Yes	D -Materials	D 3 - Sply Chain Mgmt	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
187	Have potential supply chain sources been identified?	No	D -Materials	D 3 - Sply Chain Mgmt	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments

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#	Question	Answer	Thread	Sub-thread	MRL	Comments
188	Are supply chain plans (e.g., teaming agreements, etc.) in place leading to an Engineering and Manufacturing Development (EMD) contract award?	No	D -Materials	D.3 - Sply Chain Mgmt	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
189	Is there an effective supply chain management process in place?	No	D -Materials	D.3 - Sply Chain Mgmt	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
190	Has an adequate assessment of the first tier supply chain been completed?	No	D -Materials	D.3 - Sply Chain Mgmt	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
191	Is the supply chain adequate to support Low Rate Initial Production (LRIP)?	No	D -Materials	D.3 - Sply Chain Mgmt	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
192	Has an adequate assessment of the critical second and lower tier supply chain been completed?	No	D -Materials	D.3 - Sply Chain Mgmt	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
193	Is the supply chain stable and adequate to support Full Rate Production (FRP)?	No	D -Materials	D.3 - Sply Chain Mgmt	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
194	Are long term agreements in place where practical?	No	D -Materials	D.3 - Sply Chain Mgmt	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
195	Has the supply chain been proven to support Full Rate Production (FRP) requirements?	No	D -Materials	D.3 - Sply Chain Mgmt	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
196	Has an initial evaluation of potential regulatory requirements and special handling concerns been completed?	Yes	D -Materials	D.4 - Spcl Handling	2	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
197	Has a list of hazardous materials been identified?	Yes	D -Materials	D.4 - Spcl Handling	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
198	Have potential special handling procedures been applied in the lab?	Yes	D -Materials	D.4 - Spcl Handling	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
199	Have special handling concerns been assessed?	Yes	D -Materials	D.4 - Spcl Handling	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
200	Has a list of hazardous materials been updated?	Yes	D -Materials	D.4 - Spcl Handling	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
201	Have special handling requirements been identified?	Yes	D -Materials	D.4 - Spcl Handling	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
202	Have the special handling procedures been applied in the lab?	Yes	D -Materials	D.4 - Spcl Handling	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
203	Have special handling procedures been applied in a production relevant environment?	Yes	D -Materials	D.4 - Spcl Handling	5	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments

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#	Question	Answer	Thread	Sub-thread	MRL	Comments
204	Have all special handling requirement gaps been identified?	Yes	D -Materials	D.4 - Spcl Handling	5	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
205	Have new special handling processes been demonstrated in lab environment?	Yes	D -Materials	D.4 - Spcl Handling	5	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
206	Have special handling procedures been applied in a production relevant environment?	Yes	D -Materials	D.4 - Spcl Handling	6	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
207	Have the plans to address the special handling requirement gaps been completed?	No	D -Materials	D.4 - Spcl Handling	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
208	Have special handling procedures been applied in a production representative environment?	Yes	D -Materials	D.4 - Spcl Handling	7	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
209	Have special handling procedures been developed and annotated on work instructions?	No	D -Materials	D.4 - Spcl Handling	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
210	Have special handling procedures been applied in a pilot line environment?	Yes	D -Materials	D.4 - Spcl Handling	8	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
211	Have special handling procedures been demonstrated in Engineering and Manufacturing Development (EMD) or technology insertion programs?	No	D -Materials	D.4 - Spcl Handling	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
212	Have the special handling risk issues been minimized for Low Rate Initial Production (LRIP)?	No	D -Materials	D.4 - Spcl Handling	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
213	Do all work instructions contain special handling provisions as required?	N/A	D -Materials	D.4 - Spcl Handling	8	[Graham_Sanbo]: N/A. No Comments [Jud_Ready]: N/A. No Comments [Stephan_Turan]: N/A. No Comments
214	Have special handling procedures been applied in a Low Rate Initial Production (LRIP) environment?	N/A	D -Materials	D.4 - Spcl Handling	9	[Graham_Sanbo]: N/A. No Comments [Jud_Ready]: N/A. No Comments [Stephan_Turan]: N/A. No Comments
215	Have the special handling procedures been demonstrated in Low Rate Initial Production (LRIP)?	No	D -Materials	D.4 - Spcl Handling	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
216	Have the special handling risk issues been minimized for Full Rate Production (FRP)?	N/A	D -Materials	D.4 - Spcl Handling	9	[Graham_Sanbo]: N/A. No Comments [Jud_Ready]: N/A. No Comments [Stephan_Turan]: N/A. No Comments
217	Have the special handling procedures been effectively implemented in Full Rate Production (FRP)?	No	D -Materials	D.4 - Spcl Handling	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
218	Have initial models been developed, if applicable?	Yes	E -Process	E.1 - Modeling & Sim	2	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
219	Have proposed manufacturing concepts or producibility needs been identified based on high-level process flow chart models?	Yes	E -Process	E.1 - Modeling & Sim	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion

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#	Question	Answer	Thread	Sub-thread	MRL	Comments
220	Have production modeling and simulation approaches for process or product been identified?	Yes	E -Process	E.1 - Modeling & Sim	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
221	Have the initial simulation models (product or process) been developed at the component level?	Yes	E -Process	E.1 - Modeling & Sim	5	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
222	Have the initial simulation models been developed at the technology sub-system or system level?	No	E -Process	E.1 - Modeling & Sim	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
223	Have the simulation models been used to determine system constraints and identify improvement opportunities?	Yes	E -Process	E.1 - Modeling & Sim	7	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
224	Have the simulation models been verified by the pilot line?	No	E -Process	E.1 - Modeling & Sim	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
225	Have the results of the simulation models been used to improve processes and determine that Low Rate Initial Production (LRIP) requirements can be met?	No	E -Process	E.1 - Modeling & Sim	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
226	Have the simulation models been verified by Low Rate Initial Production (LRIP) build and used to assist in management of Low Rate Initial Production (LRIP)?	No	E -Process	E.1 - Modeling & Sim	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
227	Have the results of the simulation models been used to determine if Full Rate Production (FRP) requirements can be met?		E -Process	E.1 - Modeling & Sim	9	
228	Have the simulation models been verified by Full Rate Production (FRP) build?		E -Process	E.1 - Modeling & Sim	10	
229	Have the production simulation models been used as a tool to assist in management of Full Rate Production (FRP)?	No	E -Process	E.1 - Modeling & Sim	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
230	Have material and/or process approaches been identified?	Yes	E -Process	E.2 - Process Maturity	2	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
231	Have high level manufacturing processes been documented?	Yes	E -Process	E.2 - Process Maturity	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
232	Have critical manufacturing processes been identified through experimentation?	Yes	E -Process	E.2 - Process Maturity	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
233	Has a survey been completed to determine the current state of critical processes?	Yes	E -Process	E.2 - Process Maturity	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
234	Has process maturity been assessed on similar processes in production?	Yes	E -Process	E.2 - Process Maturity	5	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
235	Have process capability requirements been identified for pilot line, Low Rate Initial Production (LRIP) and Full Rate Production (FRP)?	No	E -Process	E.2 - Process Maturity	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments

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#	Question	Answer	Thread	Sub-thread	MRL	Comments
236	Have the key manufacturing processes been demonstrated in a production relevant environment?	No	E -Process	E 2 - Process Maturity	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
237	Has collecting or estimating process capability data from prototype build begun?	No	E -Process	E 2 - Process Maturity	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
238	Have the manufacturing processes been successfully demonstrated in a production representative environment?	No	E -Process	E 2 - Process Maturity	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
239	Has collecting or estimating process capability data continued?	No	E -Process	E 2 - Process Maturity	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
240	Have the manufacturing processes for Low Rate Initial Production (LRIP) been verified on a pilot line?	No	E -Process	E 2 - Process Maturity	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
241	Does capability data from the pilot line meet the target?	N/A	E -Process	E 2 - Process Maturity	8	[Graham_Sanbo]: N/A. No Comments [Jud_Ready]: N/A. No Comments [Stephan_Turan]: N/A. No Comments
242	Are the manufacturing processes stable, adequately controlled, capable, and have the manufacturing processes achieved program Low Rate Initial Production (LRIP) objectives?	No	E -Process	E 2 - Process Maturity	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
243	Have variability experiments been conducted to show Full Rate Production (FRP) impact and potential for continuous improvement?	No	E -Process	E 2 - Process Maturity	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
244	Are the manufacturing processes stable, adequately controlled, capable, and have the manufacturing processes achieved program Full Rate Production (FRP) objectives?	No	E -Process	E 2 - Process Maturity	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
245	Have initial estimates of yields and rates based on experiments or state of the art been completed?	Yes	E -Process	E 3 - Yields & Rates	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
246	Has a yield and rates assessment on proposed/similar processes been completed?	Yes	E -Process	E 3 - Yields & Rates	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
247	Has a yield and rates assessment on proposed/similar processes been applied within the Analysis of Alternatives (AoA)?	Yes	E -Process	E 3 - Yields & Rates	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
248	Have target yield and rates been established for the pilot line, Low Rate Initial Production (LRIP), and Full Rate Production (FRP)?	No	E -Process	E 3 - Yields & Rates	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
249	Have yield and rate issues been identified?	Yes	E -Process	E 3 - Yields & Rates	5	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
250	Have yield and rate improvement plans been developed/initiated?	Yes	E -Process	E 3 - Yields & Rates	5	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
251	Are yields and rates from the production relevant environment being evaluated against targets?	No	E -Process	E 3 - Yields & Rates	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments

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252	Are results from the yields and rates from the production relevant environment being fed into an improvement plan?	No	E -Process	E 3 - Yields & Rates	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
253	Are yields and rates from the production representative environment being evaluated against pilot line targets?	No	E -Process	E 3 - Yields & Rates	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
254	Are results from the yields and rates from the production representative environment being fed into improvement plans?	No	E -Process	E 3 - Yields & Rates	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
255	Have pilot line yield and rate targets been achieved?	No	E -Process	E 3 - Yields & Rates	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
256	Have yields and rates required to begin Low Rate Initial Production (LRIP) been verified using pilot line articles?	No	E -Process	E 3 - Yields & Rates	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
257	Are yield and rate improvement plans ongoing and being updated?	No	E -Process	E 3 - Yields & Rates	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
258	Have the Low Rate Initial Production (LRIP) yield and rate targets been achieved?	No	E -Process	E 3 - Yields & Rates	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
259	Are yield improvements on-going?	Yes	E -Process	E 3 - Yields & Rates	9	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
260	Have the Full Rate Production (FRP) yield and rate targets been achieved?	No	E -Process	E 3 - Yields & Rates	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
261	Are yield improvements on-going?	Yes	E -Process	E 3 - Yields & Rates	10	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
262	Has a quality strategy been identified as part of the Technology Development Strategy (TDS)?	Yes	F -Quality	F 1 - Quality Mgmt	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
263	Is a quality strategy included in the System Engineering Plan (SEP)?	Yes	F -Quality	F 1 - Quality Mgmt	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
264	Has the quality strategy been updated to reflect Key Characteristic identification activities?	No	F -Quality	F 1 - Quality Mgmt	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
265	Is there an initial Quality Plan (QP) and a Quality Management System (QMS) in place?	No	F -Quality	F 1 - Quality Mgmt	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
266	Have quality risks and adequate metrics been identified?	No	F -Quality	F 1 - Quality Mgmt	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
267	Have the quality targets been established?	No	F -Quality	F 1 - Quality Mgmt	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments

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268 Has the ability to collect and analyze quality data (process and system) been demonstrated in the production representative environment?	No	F -Quality	F 1 - Quality Mgmt	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
269 Has quality targets been demonstrated on the pilot line?	No	F -Quality	F 1 - Quality Mgmt	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
270 Is continuous quality improvement on-going?	Yes	F -Quality	F 1 - Quality Mgmt	8	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
271 Have supplier products completed qualification testing and first article inspection?	No	F -Quality	F 1 - Quality Mgmt	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
272 Have supplier products passed acceptance testing at a rate adequate to begin Low Rate Initial Production (LRIP)?	No	F -Quality	F 1 - Quality Mgmt	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
273 Have quality targets been verified on the Low Rate Initial Production (LRIP) line?	No	F -Quality	F 1 - Quality Mgmt	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
274 Is continuous quality improvement on-going?	Yes	F -Quality	F 1 - Quality Mgmt	9	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
275 Have supplier products passed acceptance testing at a rate adequate to transition to Full Rate Production (FRP)?	No	F -Quality	F 1 - Quality Mgmt	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
276 Have the quality targets been verified on the Full Rate Production (FRP) line?	No	F -Quality	F 1 - Quality Mgmt	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
277 Is continuous quality improvement on-going?	Yes	F -Quality	F 1 - Quality Mgmt	10	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
278 Have new manufacturing skills been identified?	Yes	G -Personnel	G 1 - Mfg Personnel	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
279 Have manufacturing skill sets been identified?	Yes	G -Personnel	G 1 - Mfg Personnel	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
280 Have production workforce requirements (technical and operational) been evaluated as part of AoA?	Yes	G -Personnel	G 1 - Mfg Personnel	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
281 Has the availability of process development workforce for the Technology Development Phase been determined?	Yes	G -Personnel	G 1 - Mfg Personnel	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
282 Have the necessary workforce skill sets been identified to meet prototype production needs?	Yes	G -Personnel	G 1 - Mfg Personnel	5	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
283 Have plans for the identified skill sets been developed to meet prototype production needs?	No	G -Personnel	G 1 - Mfg Personnel	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments

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#	Question	Answer	Thread	Sub-thread	MRL	Comments
284	Have special skills certification and training requirements been established?	Yes	G -Personnel	G.1 - Mfg Personnel	5	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
285	Are the manufacturing workforce skills available for production in a relevant environment?	Yes	G -Personnel	G.1 - Mfg Personnel	6	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
286	Have resources (quantities and skill sets) been identified to achieve requirements for pilot line and production?	No	G -Personnel	G.1 - Mfg Personnel	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
287	Have initial plans for the identified resources (quantities and skill sets) been developed to achieve requirements for pilot line and production?	No	G -Personnel	G.1 - Mfg Personnel	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
288	Have the manufacturing workforce resource requirements been identified for the pilot line?	No	G -Personnel	G.1 - Mfg Personnel	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
289	Have plans been developed to achieve pilot line requirements?	No	G -Personnel	G.1 - Mfg Personnel	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
290	Have plans been updated to achieve Low Rate Initial Production (LRIP) workforce requirements?	No	G -Personnel	G.1 - Mfg Personnel	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
291	Has the pilot line workforce been trained in the representative environment?	No	G -Personnel	G.1 - Mfg Personnel	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
292	Have manufacturing workforce resource requirements been identified for Low Rate Initial Production (LRIP)?	No	G -Personnel	G.1 - Mfg Personnel	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
293	Have plans been developed to achieve Low Rate Initial Production (LRIP) requirements?	No	G -Personnel	G.1 - Mfg Personnel	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
294	Have plans been updated to achieve Full Rate Production (FRP) workforce requirements?	No	G -Personnel	G.1 - Mfg Personnel	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
295	Have Low Rate Initial Production (LRIP) personnel been trained on the pilot line where possible?	No	G -Personnel	G.1 - Mfg Personnel	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
296	Have Low Rate Initial Production (LRIP) personnel requirements been met?	No	G -Personnel	G.1 - Mfg Personnel	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
297	Has a plan been implemented to achieve Full Rate Production (FRP) workforce requirements?	No	G -Personnel	G.1 - Mfg Personnel	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
298	Have Full Rate Production (FRP) personnel requirements been met?	No	G -Personnel	G.1 - Mfg Personnel	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
299	Are production workforce skill sets being maintained due to attrition of the workforce?	No	G -Personnel	G.1 - Mfg Personnel	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments

350 Units @ a Rate of: ~ 70 / mth From Oct-2012 To: Feb-2013 Target MRL of 4 By 28-Feb-2013

Evaluator: Consensus	Current Overall MRL Rating: 4	*Capability to produce the technology in a laboratory environment.*

#	Question	Answer	Thread	Sub-thread	MRL	Comments
300	Are tooling/Special Test Equipment (STE)/Special Inspection Equipment (SIE) requirements being considered as part of AoA?	Yes	H -Facilities	H 1 - Tools/STE/SIE	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
301	Have tooling and STE/SIE requirements been identified?	No	H -Facilities	H 1 - Tools/STE/SIE	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
302	Have supporting rationale and a schedule been provided for the tooling and STE/SIE requirements?	No	H -Facilities	H 1 - Tools/STE/SIE	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
303	Have prototype tooling and STE/SIE concepts been demonstrated in production relevant environment?	No	H -Facilities	H 1 - Tools/STE/SIE	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
304	Have production tooling and STE/SIE requirements been developed?	No	H -Facilities	H 1 - Tools/STE/SIE	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
305	Are production tooling and STE/SIE design and development efforts underway?	No	H -Facilities	H 1 - Tools/STE/SIE	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
306	Has a manufacturing equipment maintenance strategy been developed?	No	H -Facilities	H 1 - Tools/STE/SIE	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
307	Have all tooling, test, and inspection equipment been proven on the pilot line?	No	H -Facilities	H 1 - Tools/STE/SIE	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
308	Have all tooling, test and inspection equipment requirements been identified for Low Rate Initial Production (LRIP)?	No	H -Facilities	H 1 - Tools/STE/SIE	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
309	Has manufacturing equipment maintenance been demonstrated on pilot line?	No	H -Facilities	H 1 - Tools/STE/SIE	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
310	Have all tooling, test, and inspection equipment been proven in the Low Rate Initial Production (LRIP)?	No	H -Facilities	H 1 - Tools/STE/SIE	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
311	Have all tooling, test, and inspection equipment requirements been identified for Full Rate Production (FRP)?	No	H -Facilities	H 1 - Tools/STE/SIE	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
312	Has a manufacturing equipment maintenance schedule been demonstrated?		H -Facilities	H 1 - Tools/STE/SIE	9	
313	Is proven tooling, test, and inspection equipment in place to support maximum Full Rate Production (FRP)?	No	H -Facilities	H 1 - Tools/STE/SIE	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
314	Has a planned equipment maintenance schedule been achieved?	No	H -Facilities	H 1 - Tools/STE/SIE	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
315	Have specialized facility requirements/needs been identified?	Yes	H -Facilities	H 2 - Facilities	3	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion

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Evaluator: Consensus | Current Overall MRL Rating: **4** | *Capability to produce the technology in a laboratory environment.*

#	Question	Answer	Thread	Sub-Thread	MRL	Comments
316	Has the availability of manufacturing facilities for prototype development and production been evaluated as part of the Analysis of Alternatives (AoA)?	Yes	H -Facilities	H.2 - Facilities	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
317	Have manufacturing facilities been identified to produce prototypes?	Yes	H -Facilities	H.2 - Facilities	5	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
318	Have plans for the identified manufacturing facilities been developed to produce prototypes?	Yes	H -Facilities	H.2 - Facilities	5	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
319	Have manufacturing facilities been identified to produce the pilot line build?	Yes	H -Facilities	H.2 - Facilities	6	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
320	Have plans for the identified manufacturing facilities been developed to produce the pilot line build?	Yes	H -Facilities	H.2 - Facilities	6	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
321	Have manufacturing facilities been identified to produce the Low Rate Initial Production (LRIP) build?	No	H -Facilities	H.2 - Facilities	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
322	Have plans for the identified manufacturing facilities been developed to produce the Low Rate Initial Production (LRIP) build?	No	H -Facilities	H.2 - Facilities	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
323	Have pilot line facilities been demonstrated?	Yes	H -Facilities	H.2 - Facilities	8	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
324	Are manufacturing facilities adequate to begin Low Rate Initial Production (LRIP)?	No	H -Facilities	H.2 - Facilities	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
325	Are plans in place to support the transition to Full Rate Production (FRP)?	No	H -Facilities	H.2 - Facilities	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
326	Have manufacturing facilities been demonstrated in Low Rate Initial Production (LRIP)?	No	H -Facilities	H.2 - Facilities	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
327	Are capacity plans adequate to support Full Rate Production (FRP)?	No	H -Facilities	H.2 - Facilities	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
328	Are the production facilities in place to meet Full Rate Production (FRP) requirements?	No	H -Facilities	H.2 - Facilities	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
329	Has the capacity of the production facilities been demonstrated to meet Full Rate Production (FRP) requirements?	No	H -Facilities	H.2 - Facilities	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
330	Has a manufacturing strategy been developed and integrated with an acquisition strategy?	Yes	I -Mfg Mgmt	I.1 - Mfg Plan & Schdl	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
331	Have prototype schedule risk mitigation efforts been incorporated into the Technology Development Strategy (TDS)?	Yes	I -Mfg Mgmt	I.1 - Mfg Plan & Schdl	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion

350 Units @ a Rate of: ~ 70 / mth From Oct-2012 To: Feb-2013 Target MRL of 4 By 28-Feb-2013					
Evaluator: Consensus	Current Overall MRL Rating: 4				*Capability to produce the technology in a laboratory environment.*
332 Has the manufacturing strategy been refined based upon the preferred concept?	No	I -Mfg Mgmt	I.1 - Mfg Plan & Schdl	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
333 Have prototype schedule risk mitigation efforts been initiated?	No	I -Mfg Mgmt	I.1 - Mfg Plan & Schdl	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
334 Has the initial manufacturing approach been developed?	Yes	I -Mfg Mgmt	I.1 - Mfg Plan & Schdl	6	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
335 Are all system design related manufacturing events included in the Integrated Master Plan/Schedule (IMP/S)?	No	I -Mfg Mgmt	I.1 - Mfg Plan & Schdl	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
336 Has the manufacturing risk mitigation approach for the pilot line or technology insertion programs been defined?	No	I -Mfg Mgmt	I.1 - Mfg Plan & Schdl	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
337 Has the initial manufacturing plan been developed?	No	I -Mfg Mgmt	I.1 - Mfg Plan & Schdl	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
338 Has manufacturing planning required to achieve MRL 8 been included in the Integrated Master Plan/Schedule (IMP/S)?	No	I -Mfg Mgmt	I.1 - Mfg Plan & Schdl	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
339 Have manufacturing risks been integrated into risk mitigation plans?	No	I -Mfg Mgmt	I.1 - Mfg Plan & Schdl	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
340 Have initial work instructions been developed?	Yes	I -Mfg Mgmt	I.1 - Mfg Plan & Schdl	7	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. No Comments
341 Is an effective production control system in place to support the pilot line?	No	I -Mfg Mgmt	I.1 - Mfg Plan & Schdl	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
342 Has the manufacturing plan been updated for Low Rate Initial Production (LRIP)?	No	I -Mfg Mgmt	I.1 - Mfg Plan & Schdl	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
343 Have all key manufacturing risks been identified and assessed with approved mitigation plans in place?	No	I -Mfg Mgmt	I.1 - Mfg Plan & Schdl	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
344 Have work instructions been finalized?	No	I -Mfg Mgmt	I.1 - Mfg Plan & Schdl	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
345 Is an effective production control system in place to support Low Rate Initial Production (LRIP)?	No	I -Mfg Mgmt	I.1 - Mfg Plan & Schdl	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
346 Has the manufacturing plan been updated for Full Rate Production (FRP)?	No	I -Mfg Mgmt	I.1 - Mfg Plan & Schdl	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
347 Have all manufacturing risks been tracked and mitigated?	No	I -Mfg Mgmt	I.1 - Mfg Plan & Schdl	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments

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Evaluator: Consensus | Current Overall MRL Rating: 4 | *Capability to produce the technology in a laboratory environment.*

#	Question	Answer	Thread	Sub-thread	MRL	Comments
348	Is an effective production control system in place to support Full Rate Production (FRP)?	No	I -Mfg Mgmt	I.1 - Mfg Plan & Schdl	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. Is an effective production control system in place to support Full Rate Production (FRP)?
349	Have all manufacturing risks been mitigated?	No	I -Mfg Mgmt	I.1 - Mfg Plan & Schdl	10	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
350	Has the technology development article component list been developed with associated lead time estimates?	Yes	I -Mfg Mgmt	I.2 - Mfg Matls Planning	4	[Graham_Sanbo]: Yes. No Comments [Jud_Ready]: Yes. No Comments [Stephan_Turan]: Yes. Default Opinion
351	Is the technology development part list maturing?	No	I -Mfg Mgmt	I.2 - Mfg Matls Planning	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
352	Have make/buy evaluations begun?	No	I -Mfg Mgmt	I.2 - Mfg Matls Planning	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
353	Do the make/buy evaluations include production considerations reflecting the pilot line, Low Rate Initial Production (LRIP), and Full Rate Production (FRP) needs?	No	I -Mfg Mgmt	I.2 - Mfg Matls Planning	5	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
354	Are most material decisions complete (make/buy)?	No	I -Mfg Mgmt	I.2 - Mfg Matls Planning	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
355	Have material risks been identified?	No	I -Mfg Mgmt	I.2 - Mfg Matls Planning	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
356	Have material risk mitigation plans been developed?	No	I -Mfg Mgmt	I.2 - Mfg Matls Planning	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
357	Has the Bill of Materials (BOM) been initiated?	No	I -Mfg Mgmt	I.2 - Mfg Matls Planning	6	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
358	Are the make/Buy decisions and Bill of Materials (BOM) complete for pilot line build?	No	I -Mfg Mgmt	I.2 - Mfg Matls Planning	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
359	Are material planning systems in place for the pilot line build?	No	I -Mfg Mgmt	I.2 - Mfg Matls Planning	7	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
360	Are the Make/Buy decisions and Bill of Materials (BOM) complete to support Low Rate Initial Production (LRIP)?	No	I -Mfg Mgmt	I.2 - Mfg Matls Planning	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
361	Are material planning systems in place for Low Rate Initial Production (LRIP) build?	No	I -Mfg Mgmt	I.2 - Mfg Matls Planning	8	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
362	Are the Make/Buy decisions and Bill of Materials (BOM) complete enough to support Full Rate Production (FRP)?	No	I -Mfg Mgmt	I.2 - Mfg Matls Planning	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments
363	Are material planning systems in place for Full Rate Production (FRP)?	No	I -Mfg Mgmt	I.2 - Mfg Matls Planning	9	[Graham_Sanbo]: No. No Comments [Jud_Ready]: No. No Comments [Stephan_Turan]: No. No Comments

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VITA

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Graham received a TI:GER certificate from Georgia Tech for his completion of the technology commercialization program. From work in this program, he cofounded a medical device startup named ConservoCare. When he is not researching or working on his company, Graham enjoys cycling, beach volleyball, surfing, live music, and culinary experiences.