High-Frequency Measurements of Carbon Nanotube Quantum Dots

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Declaration of Authorship

I, Pavlos Apostolidis, confirm that the work presented in this thesis is my own. Where information has been derived from other sources, I confirm that this has been indicated in the thesis.

"The first principle is that you must not fool yourself - and you are the easiest person to fool."

Richard P. Feynman

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Abstract

The implementation of a quantum computer is expected to revolutionise computation in terms of speed and capabilities. Quantum computing is, therefore, an active area of research. This thesis presents experimental attempts towards advances in the field of quantum computation using carbon nanotube-based quantum dot devices and high-frequency techniques. The motivation behind using carbon nanotubes lies with the fact that they provide a priori confinement in two dimensions, making the quantum dot fabrication procedure simpler. In addition, they allow for control of the carbon isotope ratio before growth. As a consequence, isotropically pure carbon-12 nanotubes can serve as ideal hosts for spin qubits due to the lack of hyperfine interactions, providing a clean spin environment and longer coherence times. On the other hand, nanotubes with a controlled percentage of carbon-13 atoms could be used as quantum memories, upon transferring information to the nuclear spin. For the work presented in this thesis, single-walled carbon nanotubes with natural abundance of carbon isotopes were grown using chemical vapour deposition. Quantum dot devices were fabricated on doped and undoped silicon substrates using electrostatic top-gating techniques and studied at ultra-low temperatures, focusing in particular on quantum state readout with high-frequency electric fields.

The main topic of this thesis revolves around the fabrication and measurements of carbon nanotube single and double quantum dots, with the potential of being used as charge or spin qubit devices. An overview of the relevant theoretical background is given, including the theory of few-electron quantum dots based on the constant interaction model. The carbon nanotube geometry and electronic structure are outlined, along with relevant perturbations to the band structure. A detailed fabrication procedure for devices is presented and experimental methods are discussed, including customisation of a dilution refrigerator, minimisation of the electron temperature and optimisation of the relevant high-frequency setup.

Radio-frequency (RF) reflectometry is exploited as a fast, high-sensitivity, non-invasive technique for quantum dot readout. For readout optimisation, a novel approach for developing voltage-tunable variable capacitors (varactors) that operate reliably at low temperatures is presented. Such varactors are based on strontium titanate and can be used to tune a quantum dot to perfect impedance matching, as well as tune its resonant frequency in situ. It is demonstrated that this approach allows for higher signal-to-noise ratio and results in a charge sensitivity that is among the best reported to date. Furthermore, by investigating iron phthalocyanine molecules, it is demonstrated how RF reflectometry can be used for capacitance spectroscopy of arbitrary molecules or nanoparticles using a simplified device geometry.

Electronic transport and high-frequency measurements of carbon nanotube double quantum dots are presented, including characterisation and attempts for high-frequency gate modulation and interdot transition tuning. A video-mode data acquisition technique is introduced as a fast way to perform RF measurements, with an integration time of about 1 µs per point. This technique allows for the effects of gate electrodes to be observed in situ upon varying the corresponding voltage. Relevant challenges and solutions are given, along with future suggestions and directions.

Impact Statement

The work presented in this thesis aims for advances in the field of quantum computation, with the ultimate objective being the realisation of a universal quantum computer. It has been theoretically demonstrated that a quantum computer will be able to outperform any classical computer in a variety of problems. In fact, some of these problems would be impossible to solve with classical computers in polynomial time.

Some of the aforementioned problems/tasks involve the factorisation of large integers or searching for prime numbers, both of which can be used in encryption and communication systems. Moreover, the travelling salesman problem is in popular demand in industry, and a quantum computer could be able to determine its optimum solutions much faster than a classic counterpart computer. In addition, a universal quantum computer could be used broadly for simulations of other quantum systems that can advance medicine or improve our understanding of the universe. When tackled classically, the time complexity of such tasks scales exponentially with sample size, therefore obtaining a sensible result can be extremely slow.

The experiments and analysis discussed in this thesis could be used for navigation in the field of solid-state quantum computing with high-frequencies. The techniques adapted and/or developed can be utilised for further experiments to advance the relevant field. Those include the optimisation of rapid data acquisition, which is essential for characterising many quantum devices fast. Moreover, a novel technique was developed for improving the charge sensitivity at low temperatures, allowing for more precise measurements and sensitive readout of quantum systems. This is not merely useful for being one of the main readout mechanisms in a quantum computer, but it could also be used in conjunction with other technologies in the industry of quantum sensors and standards.

Finally, all the relevant code developed during experiments is publicly available for other researchers and students to use. The code includes libraries and scripts for various kinds of measurements with a broad range of equipment, but also a number of data analysis tools and techniques.

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For my time at the London Centre for Nanotechnology (LCN), I would like to express my special appreciation and thanks to my supervisor Mark Buitelaar, for his help and guidance during my PhD. Moreover, I would like to thank Byron Villis for his help, ideas and precious knowledge on high-frequency electronics. It was nice to contribute to the development of a new lab (from scratch), piece-by-piece (of equipment) and line-by-line (of code). Other people who made my life easier at the LCN and I am greatful to, include: Cyrus Hirjibehedin, Jeroen Elzerman, Pavlo Zubko, Vijay Krishnan, Lorella Rossi, Rohit Khanna, Richard Thorogate, Alice Sackville-Hamilton, Nick Nicolaou, Jacob Chittock-Wood, Marios Hadjimichael and Elias Peraticos.

I would like to thank Andreas Baumgartner at the University of Basel for teaching me how to grow carbon nanotubes using their chemical vapour deposition system and preparing some for me himself.

A special thanks to Daven Armoogum and Paul Bartlett for the time I spent with them as a postgraduate teaching assistant in the undergraduate physics labs. I had a great time, during which I realised the appreciation of fellow colleagues and students when I became an Associate Fellow of the Higher Education Academy and reveived the Faculty Education Award in 2018.

Outside the world of academia, a special thanks to my father, mother and sister for all the support and guidance. Moreover, I appreciate the support of all my friends during my PhD. Finally, a special thanks to Marianna for all the walks, support and lunches.

Dedicated to my family

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Chapter 1

Introduction

1.1 Quantum Technologies and Motivation

1.1.1 Quantum Computation

The first half of the 20th century established the fundamentals of quantum mechanics, the field that revolutionised the way scientists see the microscopic world. The technological advances that followed quantum theory allowed for its use in electronic devices, including microprocessors, solar cells and medical imaging equipment, among others. Quantum technologies and devices are now an active area of research, aiming for future technological developments. One of the most prominent candidates for such upcoming technologies is the quantum computer. A quantum computer is theorised to be able to take advantage of quantum effects, such as superposition of quantum states, entanglement of particles and quantum tunneling, allowing for exponentially faster calculations, when it comes to specific operations, such as factorising large numbers or simulating other quantum systems [1].

Moore's law states that the number of transistors or the computing capacity of new computer chips doubles about every 18 months [2]. This implies an increase in processing speed and a size reduction of the microchip features. While this law has held true up to now, the semiconductor industry is approaching a fundamental limit. Microdevices are getting too small, reaching the point where quantum effects like quantum tunneling will start to dominate, making transistors unreliable and potentially useless [3]. On the other hand, a quantum computer could utilise these effects to improve on specific computation tasks. While a classical bit can only possess a well-defined state of 0 or 1, a quantum bit (qubit) can exist in a superposition of both. In theory, a qubit can be any two-level quantum system. For such a system, the pure states of a qubit can be

illustrated on the surface of a Bloch sphere as shown in Figure 1.1. The qubit can exist in any superposition of states in the two-dimensional Hilbert space, implying that its wavefunction $|\psi\rangle$ can be written as [4, 5]:

$$|\psi\rangle = \cos(\theta/2)\,|0\rangle + \sin(\theta/2)e^{i\phi}\,|1\rangle \tag{1.1}$$

where θ and ϕ are the polar and azimuthal angles, respectively, and $\langle\psi|\psi\rangle = 1$.

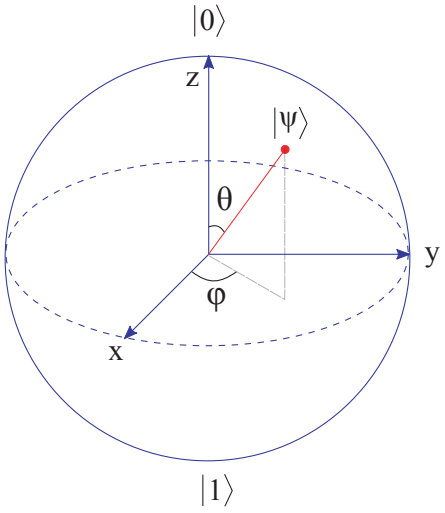

FIGURE 1.1: A geometrical representation of a two-level quantum system on a Bloch sphere. *Adapted from Ref* [6].

Having N qubits allows for 2^N individual states that can exhibit quantum superposition. The general idea of quantum computing is to utilise the fact that any quantum state is governed by a probability amplitude, and choreograph an interference pattern where paths leading to the correct answer interfere constructively, reinforcing each other. Similarly, paths leading to wrong answers would interfere destructively and cancel out. Therefore, taking advantage of quantum superposition might lead to a tremendous increase in computation speed for some optimised algorithms. Such algorithms have been developed by P. Shor [7], D. Deutsch [8], L. Grover [9] and others, and it has been shown that they can fundamentally outperform any classical algorithm that carries out the same task.

The possibilities of a universal quantum computer do not stop here. Classical super computers have trouble simulating the behaviour and evolution of a large quantum system as the system increases in size. In principle, a quantum computer would not have such limitations, and would likely be the best candidate to simulate another quantum system [10]. Moreover, quantum cryptography [11] and quantum internet [12] are also

some potential applications that lie on the table. Quantum technologies and computation are therefore an interesting and promising field of research; if not because of the potential of quantum devices, then because of the interesting physics that governs their microscopic nature. Undoubtedly, the realisation of a universal quantum computer is not an easy task. Although the key points and criteria are well established [4, 13], many challenges remain. Some of these challenges include the need for sufficient isolation of the quantum system from its environment, while maintaining the ability to interact with it on demand for qubit initialisation, manipulation and readout. Moreover, scaling quantum technology to attain sufficient qubits to perform calculations is another major obstacle [14]. Fortunately, progress has been made to individually address many of the requirements for building a quantum computer. That includes demonstrations of long coherence times [15, 16], long quantum information storage times [17, 18], high fidelity readout [19, 20], one- [21] and two-qubit operations [22], but also proposals for large scale integration [23, 24].

1.1.2 Quantum Dots

The fact that any two-level quantum system could be used as a qubit led to different approaches regarding qubit types and device architectures. Some approaches involve photon states [25], cold ion traps [26], superconducting qubits [27], Josephson junctions [28], nitrogen-vacancy centres in diamond [29], quantum dots [5] and others.

The work presented in this thesis focusses on quantum dots. A quantum dot (QD, also known as an artificial atom) is a small semiconducting region that can be used to confine charge carriers [30]. An electron in a quantum dot is confined in all three spatial dimensions, and since the size of the dot is comparable to the Fermi wavelength of the electron, the latter exhibits discrete and quantised energy states. Since electrons are charged spin-$\frac{1}{2}$ particles, they can be utilised as qubits in several ways. The electron can be spatially confined with a tunable probability of tunneling between neighbouring dots, leading to a charge qubit. Another natural two-level quantum system can be made from the electron spin, in which logical qubits can be encoded and manipulated, with quantum dots acting as hosts [5]. In addition, singlet-triplet state qubits have also been demonstrated in quantum dots [31].

A quantum dot is a general term; there are various ways to confine electrons in a variety of materials, leading to different kinds of quantum dots. Some examples include self-assembled quantum dots in materials like InGaAs [31], dots formed from electrostatic confinement of two-dimensional electron gases (2DEG) in GaAs heterostructures [32], dots formed along the length of nanowires [33], or even hybrid dots in silicon [34].

This thesis presents work with quantum dots formed by electrostatic gating of carbon nanotubes [35, 36]. The latter, being one-dimensional nanomaterials, provide a priori confinement in two-dimensions. Restricting the third dimension along the length of a nanotube results in a quantum dot. Such dots can be controlled using gate electrodes and several dots can be coupled in series. In multi-quantum dots, electrons can tunnel from one dot to the other with a tunable rate [37–39].

1.1.3 Carbon Nanotube Devices

For the purposes of the work presented, carbon nanotubes are one of the main ingredients comprising the devices used for measurements. There are several reasons why one would choose nanotubes as hosts for qubits:

1. Carbon nanotubes are relatively simple to grow, compared to other growing mechanisms that may require a molecular beam epitaxy and ultra-high vacuum. They can be grown directly on a variety of substrates using chemical vapour deposition. This is how nanotubes were grown for the discussed experiments. The growth procedure is outlined in Appendix A.

2. Turning nanotubes into quantum dots using electrostatic gating is a straightforward process, since the material is one-dimensional in its nature. Although the fabrication of double dots requires a few stages, several devices can be prepared in a single fabrication step.

3. Carbon nanotubes are a suitable medium for hosting spin qubits since they provide a very clean spin environment. Natural carbon consists of 98.89% ^{12}C, therefore only 1.11% of the host atoms have unpaired nuclear spin. Thus, exceptionally long spin coherence times are expected, arising from the absence of hyperfine interactions [40, 41]. For comparison, natural abundance silicon contains 4.67% of ^{29}Si, which has unpaired nuclear spin [42].

4. The ratio of ^{12}C and ^{13}C atoms can be chosen before growth by using a carbon-containing gas of the desired isotope ratio. This allows for experiments to examine in detail how nuclear spins affect coherence. For the work presented, carbon with natural abundance isotopes was used.

Double quantum dots are widely used to host charge and spin qubits [43]. Such a double quantum dot is defined with a middle gate electrode that has an insulating layer between its conductive region and the nanotube. The application of a voltage depletes charge carriers underneath the gate by creating a potential barrier. Since it is not energetically

favourable for charge carriers to pass through that region, the nanotube is divided into two serially coupled dots with a voltage-tunable coupling. The schematic of such a carbon nanotube double quantum dot device is shown in Figure 1.2.

Finally, one-dimensional materials like nanotubes have some potential disadvantages. These include the fact that there are restricted possibilities for coupling dots (for example, it is only trivial to couple dots in series). Also, the locations and orientations of the nanotubes after growth are random.

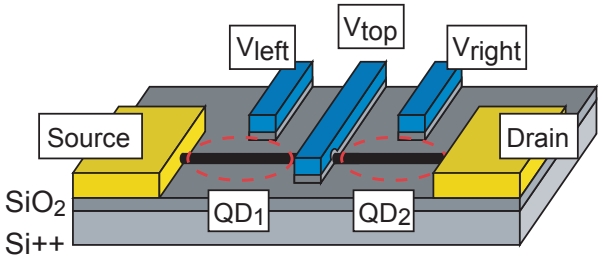

FIGURE 1.2: Schematic diagram of a double quantum dot device on degenerately doped silicon formed by electrostatic gating of a carbon nanotube. The two dots QD_1 and QD_2 are indicated by dashed ellipses. Gate electrodes V_{left} and V_{right} are used to control the corresponding dot, while V_{top} is used to define a tunnel barrier between the two dots. *Adapted from Ref* [43].

1.2 Thesis Outline

This thesis presents experimental attempts and measurements towards advances in the field of quantum computation. The main tools used to explore the field are carbon nanotube quantum dots and high-frequency techniques. An outline for each of the chapters that follow is given below:

- **Chapter 2 - Theoretical Background**
  This chapter presents the relevant theory for carbon nanotubes and quantum dots. This includes an introduction to the geometrical and electronic structure of carbon nanotubes, emphasising on the main band gap-related perturbations of its structure. An introduction to the electrostatics of few-electron single and double quantum dots using the constant interaction model is given, including the spin-physics associated with such systems. The low and high bias regime is discussed for both single and double dots. An introduction to charge and spin qubits in double quantum dots is also given.

- **Chapter 3 - Experimental Methods**
  This chapter briefly outlines the fabrication procedure for nano-devices and presents the relevant experimental methods and setup implemented. The setup includes the customisation of a dry dilution refrigerator to account for aggressive DC filtering and allow for high-frequency techniques. The former involves the steps towards ultra-low (<20 mK) electron temperatures, while the latter explores the evolution of radio-frequency reflectometry and microwave lines. The design of a sample holder and PCB is presented, and a low electronic temperature for quantum dots is demonstrated. A motivation and introduction to radio-frequency reflectometry is also given.

- **Chapter 4 - Impedance Matching and Frequency Tuning using Strontium Titanate Varactors**
  This chapter presents a novel approach for developing voltage-tunable varactors that operate reliably at low temperatures. The varactors are based on strontium titanate and they are used to demonstrate tuning of a quantum dot to perfect impedance matching, as well as tuning of its resonant frequency in situ. Measurements and circuit simulations are presented and discussed in detail. It is demonstrated that tuning to perfect impedance matching allows for higher signal-to-noise ratio and better charge sensitivity.

- **Chapter 5 - Reflectometry on Carbon Nanotube Double Quantum Dots**
  This chapter presents measurements on carbon nanotube double quantum dots. Tuning of the interdot transition and high-frequency modulation are discussed. A video-mode data acquisition technique is presented as a fast way to measure such devices. The challenges related to double quantum dots are outlined.

- **Chapter 6 - Discussion and Overview**
  This chapter summarises and briefly outlines the work presented in this thesis, followed by future work suggestions and directions.

- **Appendix A - Device Fabrication**
  This appendix provides a detailed overview of the fabrication procedure of carbon nanotube quantum dot devices. The overview includes nanotube growth, device designs, clean room work, characterisation, fabrication challenges and tips.

- **Appendix B - RF capacitance spectroscopy of FePc molecules**
  This appendix presents a way of capacitively probing the electronic characteristics of FePc molecules using radio-frequency reflectometry and a simple device geometry. The approach presented can be adapted for arbitrary molecules or nanoparticles.

Chapter 2

Theoretical Background

This chapter presents the relevant theoretical framework underlining the topics presented in this thesis. We start with an introduction to the geometrical and electronic structure of carbon nanotubes, with an emphasis on band gap-related perturbations. An introduction to the electrostatics of few-electron single and double quantum dots using the constant interaction model is given, including the spin-physics associated with such systems. The low and high bias regimes are discussed for both single and double dots. An introduction to charge and spin qubits in double quantum dots is outlined.

2.1 Carbon Nanotubes

Carbon nanotubes (CNTs) are one-dimensional nanostructures made entirely of carbon atoms and they were first reported in 1991 by S. Iijima [44]. CNTs can be thought as folded sheets of graphene, therefore they share many similar characteristics and properties. They can be single-walled or multi-walled (nested nanotubes, equivalent to folded multi-layer graphene), with diameters typically 1-2 nm and 5-15 nm, respectively [45, 46]. The work presented in this thesis focuses on single-walled nanotubes only.

Carbon nanotubes can either be metallic or semiconducting, depending on their chirality (the direction along which the graphene sheet is rolled up). This unique property, in addition to their other extraordinary properties (high mechanical stability, high thermal conductivity, large current carrying capacity) raised a great interest in the semiconductor industry for a vast number of potential applications, including molecular electronics, electron field emitters and fillers in composite materials [45]. Nanotubes can be grown using chemical vapour deposition (CVD), which combines low cost and high control over the growth parameters. With CVD, nanotubes can be grown directly on a variety

of substrates that have been pre-coated with metallic nanoparticles to initiate growth [47–49]. Chemical vapour deposition is discussed in more detail in Appendix A.1.

The following sections outline the physical and electronic structure of carbon nanotubes that relate to the work presented in this thesis. A more complete review on structure and properties of is given by E. Laird et al. [50].

2.1.1 Physical Structure

A single-walled carbon nanotube is equivalent to a rolled-up sheet of graphene. However, different ways of rolling-up such a sheet result in different nanotube structures, sometimes with significantly different properties. Every carbon nanotube structure can be described by a chiral vector $\vec{C}$ or a chiral index (n, m), where n and m are integers. The chiral vector indicates how a graphene sheet is to be folded to form a given nanotube[1]. The chiral vector is shown in Figure 2.1 and is given by:

$$\vec{C} = n\vec{a_1} + m\vec{a_2} \tag{2.1}$$

where $\vec{a_1}$ and $\vec{a_2}$ are the basis unit vectors of graphene.

Since a nanotube is formed by folding a graphene sheet along the chiral vector $\vec{C}$, its circumference is equal to $|\vec{C}|$. The lattice vector $\vec{T}$ is parallel to the direction of the nanotube and perpendicular to $\vec{C}$. The chiral angle θ is the angle between $\vec{C}$ and $\vec{a_1}$, as shown in Figure 2.1. The diameter d and the chiral angle θ are therefore given by:

$$\begin{aligned} d &= \frac{a_0\sqrt{3}}{\pi}\sqrt{n^2 + m^2 + nm} = \frac{|\,\vec{C}\,|}{\pi} \\ \theta &= \arccos\left(\frac{2n+m}{2\sqrt{n^2+m^2+nm}}\right) \end{aligned} \tag{2.2}$$

where a_0 is the carbon-carbon bond length (0.142 nm) [50]. Depending on the chiral index (n, m), different nanotube structures can be formed: armchair (if n=m), zigzag (if m=0), and chiral (otherwise). These structures are illustrated in Figure 2.2. For zigzag and armchair nanotubes, θ=0 and θ=30°, respectively. A chiral nanotube is the most general case and it is non-symmetric under mirroring. Zigzag and armchair nanotubes yield the same structure under mirroring.

[1] By convention, to avoid having different chiral vectors representing the same nanotube structure, we take $-n/2 < m \leq n$ [50].

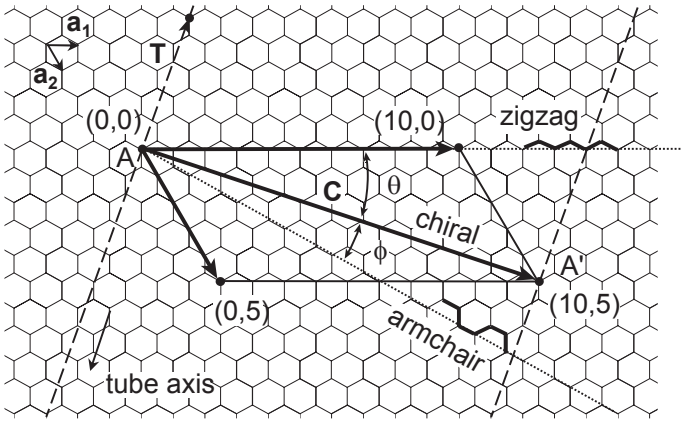

FIGURE 2.1: A chiral vector with index (10,5). The chiral angle θ and the lattice vector $\vec{T}$ are indicated. *Adapted from Ref* [46].

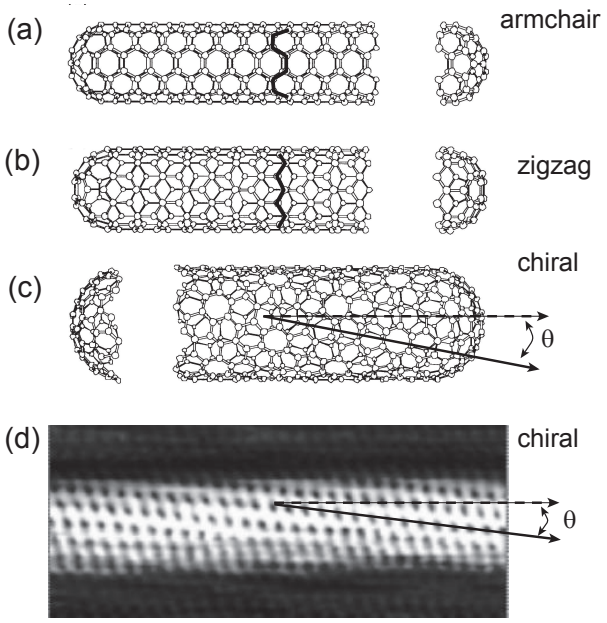

FIGURE 2.2: Schematics of carbon nanotube variations: (a) (5,5) armchair, (b) (9,0) zigzag, (c) (10,5) chiral. All three nanotubes are constructed by rolling up a graphene sheet as indicated in Figure 2.1. (d) Scanning tunneling microscope image of a single-wall chiral carbon nanotube with diameter 1.3 nm and chiral angle 7°. *Adapted from Ref* [46].

2.1.2 Electronic Structure

To understand the electronic properties of carbon nanotubes, the electronic band structure of graphene has to be examined first. In the graphene lattice, every carbon atom has 4 valence electrons, out of which 3 are taken for sp^2 hybridised planar σ-bonds with the 3 neighbouring carbon atoms. The fourth valence electron forms a π-orbital perpendicular to the plane of the graphene sheet. These orbitals result in electrical

conduction in graphene, as each carbon atom has one delocalised electron that allows for electrical conduction. The dispersion relation for p_z electrons in nanotubes (the electrons responsible for conduction) can be obtained by applying the tight-binding model to graphene and then introducing some periodic boundary conditions. The tight-binding model calculates the band structure of electrons using an approximate set of electronic wavefunctions. These wavefunctions are constructed by superposition of localised atomic orbitals, while neglecting interactions between atoms separated by large distances. This approximation greatly simplifies the mathematical analysis without major discrepancies between theory and experiment [45, 50, 51]. The energy dispersion relation for electrons in a sheet of graphene is obtained as a function of the wavevectors k_x and k_y using the tight-binding model, and is given by:

$$E(k_x, k_y) = \pm\gamma_0\sqrt{1 + 4\cos(\sqrt{3}k_y\alpha/2)\cos(\alpha k_x/2) + 4\cos^2(\alpha k_x/2)} \tag{2.3}$$

where α is the lattice constant and γ_0 is the overlap integral between the p_z electrons of two successive carbon atoms (it can also be thought as the C-C bond strength). A detailed derivation of the energy dispersion relation is given by D. Fathi [45], and M. S. Dresselhaus, G. Dresselhaus and P. Avouris [48].

Plotting Equation 2.3 results in the band structure shown in Figure 2.3. Two bands arise: a bonding (bottom) and an anti-bonding (top) band, also called π and π^* bands, respectively. The bonding and anti-bonding bands behave as valence and conduction bands and they correspond to the $\pm$ signs of Equation 2.3, respectively. The two bands touch at six points in reciprocal space, known as K-K′ points or Dirac points, located at $(K, K') = (0, \mp\frac{4\pi}{3\alpha})$, where the density of states is zero. Near the Dirac points the dispersion relation E is approximated as linear [50]. Taking the Fermi energy E_F as the zero-point energy and measuring the distance $\vec{\kappa}$ from a Dirac point, we obtain:

$$E = \pm\hbar v_F|\kappa| \tag{2.4}$$

where $\hbar$ is the reduced Planck constant, $v_F \approx 8 \times 10^5 m/s$ is the Fermi velocity, and $\pm$ applies to electrons and holes, respectively.

Quantisation of the circumferential $\vec{k}$-component

The band structure of carbon nanotubes is obtained starting from the band structure of graphene and applying periodic boundary conditions around the nanotube circumference. This approach is known as the zone-folding approximation [50]. More specifically, the electronic wavefunction must be single-valued around the circumference, suggesting the restriction $\Psi(\vec{r}) = \Psi(\vec{r} + \vec{C})$, where $\vec{r}$ is an arbitrary real space lattice vector. Following this condition, we obtain $e^{i\vec{k}\vec{r}} = e^{i\vec{k}(\vec{r}+\vec{C})}$ which leads to the relation

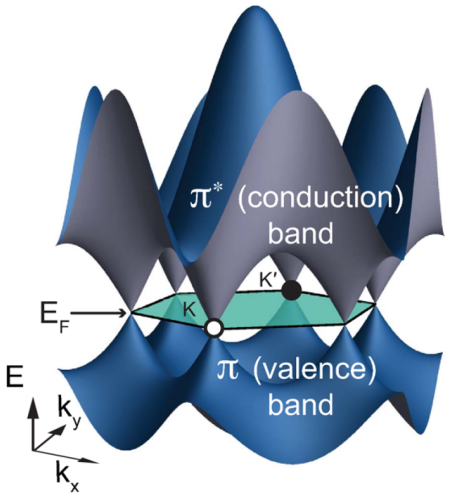

FIGURE 2.3: Schematic of the conduction and valence bands of graphene in $\vec{k}$-space. The bands touch at the six Dirac points. The Fermi level is denoted by E_F and the Brillouin zone is shown in green. *Adapted from Ref* [50].

$\vec{k}.\vec{C} = 2\pi q \Rightarrow k_\perp = 2q/d$, where $k_\perp$ is the component of $\vec{k}$ perpendicular to the nanotube axis, q is an integer and d is the nanotube diameter (in other words, the wave vector along the circumference is quantised). This relation results in allowed values for $k_\perp$, which correspond to a set of lines in $\vec{k}$-space known as quantisation lines. The conducting nature of a nanotube is determined by the quantisation lines closer to the Dirac points, therefore the rest are usually of little interest. Quantisation lines for several nanotube structures are shown in Figure 2.4.

Depending on whether the quantisation lines pass through or miss the Dirac points, the low-energy dispersion relation will be either linear or hyperbolic, respectively [50]. In the hyperbolic case, an energy gap E_g opens up since the conduction and valence bands do not touch at $|k_\parallel| = 0$. For quantised values of $k_\perp$, the dispersion relation E takes the form:

$$E = \pm\sqrt{\hbar^2 v_F^2 k_\parallel^2 + E_g^2/4} \tag{2.5}$$

Following this approach, metallic nanotubes have linear dispersion and they are gapless (the quantisation lines pass through the Dirac points). Semiconducting nanotubes on the other hand, have hyperbolic dispersion relations and their gap is given by:

$$E_g = \frac{4\hbar v_F}{3d} \approx \frac{0.7 \text{ eV}}{d[\text{nm}]} \tag{2.6}$$

For a given nanotube with chiral index (n, m), if $n - m$ is an integer multiple of 3, then the nanotube is metallic (thus all armchair nanotubes are metallic). Otherwise, the nanotube is semiconducting. Although the zone-folding approximation predicts that all metallic nanotubes have zero-band gap, in reality most of them have a small gap of tens of

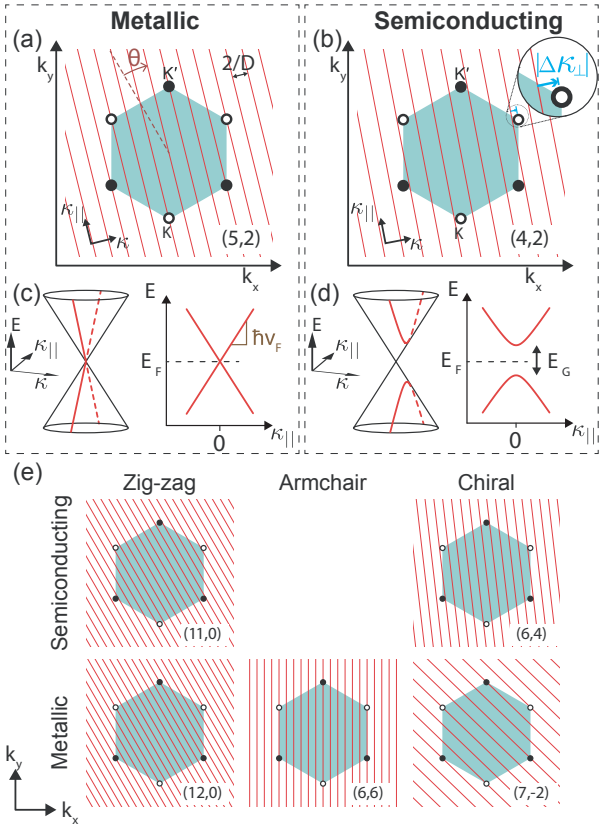

FIGURE 2.4: (a, c) Quantisation lines and dispersion relations for the metallic nanotube with chiral index (5,2). The dispersion relation is linear near the Dirac points and the nanotube is gapless. (b, d) Quantisation lines and dispersion relations for the semiconducting nanotube with chiral index (4,2). The dispersion relation is hyperbolic near the Dirac points and the an energy gap E_g opens up. (e) Examples of quantisation lines for several metallic and semiconducting nanotube structures. *Adapted from Ref* [50].

meV [52–54]. The small gap arises mainly due to perturbations of the band structure by the curvature of the nanotube [50, 55] as well as strain [56, 57] and electron-electron interactions [58]. Curvature perturbations are outlined below; strain and electron-electron interactions are not considered further.

Curvature-induced band gap

The orbitals of the carbon atoms overlap differently in carbon nanotubes compared to graphene due to differences in physical geometry. The overlap difference causes the Dirac cones to shift by a displacement vector $\Delta\vec{k}^c$. In the case of metallic nanotubes, this shift causes the quantisation lines to miss the Dirac points, therefore introducing a small band gap E_g^c:

$$E_g^c = 2\hbar v_F |\Delta k_\perp^c| \sim \frac{50\ \text{meV}}{d[\text{nm}]^2} \cos(3\theta) \tag{2.7}$$

where $|\Delta k_\perp^c|$ is the component of $\Delta\vec{k}^c$ perpendicular to the nanotube axis and θ is

the chiral angle. This curvature-induced gap is much smaller than the gap induced by the quantisation of the circumferential $\vec{k}$-component, thus it has only a minor effect on semiconducting nanotubes. With the exception of armchair nanotubes, for which $\theta = 30$, the curvature-induced gap dominates on all other "metallic" nanotubes. These are known as narrow-gap nanotubes. Therefore, only a small portion of nanotubes have exactly zero band gap. These are known as quasi-metallic nanotubes. The electronic nature of a nanotube can be determined by measuring its conductance with an applied source-drain bias as a function of gate voltage at room temperature. The conductance of a semiconducting, a narrow-gap and a quasi-metallic nanotube is shown in Figure 2.5 as a function of back gate voltage. The electrostatic potential induced by the back

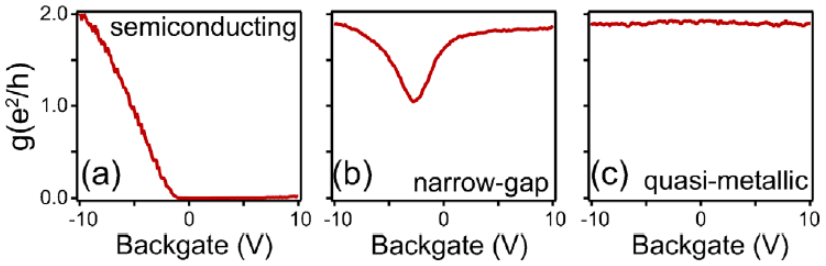

FIGURE 2.5: Room temperature conductance measurements as a function of back gate voltage for (a) semiconducting, (b) narrow-gap and (c) quasi-metallic nanotubes. *Adapted from Ref* [50].

gate V_g shifts the energy levels of the nanotube up or down, tuning in this way the relative position of the Fermi level E_F with respect to the energy band gap. If E_F lies in the band gap, the current through the nanotube is suppressed. For a semiconducting nanotube, the conductance is very small for $V_g > 0$ and favoured for $V_g < 0$, as E_F lies in the band gap and in the valence band, respectively. In this case, no transport can take place via the conduction band since $E_g \gg k_B T$. For a narrow-gap nanotube, partial current suppression takes place since $E_g \sim k_B T$. In this case, the flow of current is not fully suppressed because transport can take place via both conduction and valence bands (since the band gap is small enough), therefore shifting E_F in the band gap does not "turn off" the conduction completely. Lastly, the conductance of a quasi-metallic nanotube shows no significant variation with V_g, since the band gap is zero and E_F will always lie either in the valence or conduction band [50].

Nanotubes in magnetic fields

An electron in a carbon nanotube will experience Zeeman splitting [19, 59] when an external magnetic field is applied. For a magnetic field B, the Zeeman energy E_Z is given by:

$$E_Z = \pm \frac{1}{2} g_s \mu_B B_{\parallel} \tag{2.8}$$

where g_s is the Landé g-factor, μ_B is the Bohr magneton and $B_\parallel$ is the magnetic field component parallel to the nanotube axis. The $\pm$ signs denote parallel and anti-parallel spin to the nanotube axis, respectively. In addition to Zeeman splitting, an external magnetic field couples to the circumferential motion of electrons around the nanotube of diameter d. Therefore, the electron energy increases by an additional E_{orb}, given by [60]:

$$E_{orb} = \mp \tau g_{orb} \mu_B B_\parallel \tag{2.9}$$

where τ determines the circulation direction of the electron and g_{orb} is the orbital g-factor. Therefore, the total energy E_B due to a parallel magnetic field is given by:

$$E_B = (g_s \mp \tau g_{orb}) \mu_B B_\parallel \tag{2.10}$$

A parallel magnetic field splits up the nanotube states according to their combined g-factor $\pm g_s \mp \tau g_{orb}$, thus there are four non-degenerate states. A perpendicular field only splits the spin states (since it is perpendicular to the orbital motion), thus there are two doubly-degenerate states. The nanotube spectrum for perpendicular and parallel magnetic fields is shown in Figure 2.6, where spin-orbit coupling is taken to be zero and no nanotube disorder is considered.

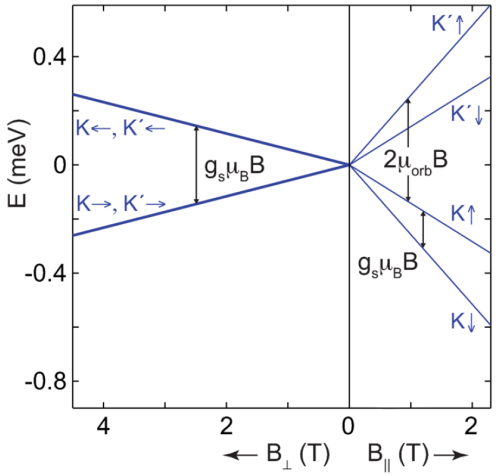

FIGURE 2.6: The nanotube spectrum for perpendicular $B_\perp$ and parallel $B_\parallel$ magnetic fields. The perpendicular field only splits the spin states, thus there are two doubly-degenerate states. The parallel field splits both spin and orbital states, thus there is a total of four states. Spin-orbit coupling is taken to be zero and nanotube disorder is not considered. *Adapted from Ref* [50].

Spin-orbit coupling

Spin-orbit coupling in carbon nanotubes refers to the interaction of the spin of an electron with its circumferential motion around the nanotube, and it was first reported by F.

Kuemmeth et al. [61] in 2008. Theoretical calculations reveal two contributions for spin-orbit coupling: a Zeeman-like [62] and an orbital-like [63]. The Zeeman-like contribution is characterised by a parameter Δ_{SO}^0 and causes the Dirac cones to shift vertically. The shift is equivalent to an effective Zeeman shift $\Delta E^{SO,Z} = \pm\Delta_{SO}^0$, where $\pm$ shows dependence on spin orientation. The orbital-like contribution is characterised by a parameter Δ_{SO}^1 and it is equivalent to a spin-dependent magnetic flux that couples to the orbital motion. It causes the Dirac cones to shift horizontally by $\Delta\kappa_\perp^{SO,orb} = \mp\frac{\Delta_{SO}^1}{\hbar v_F}$, where $\mp$ shows an opposite dependence on spin orientation [50]. The total spin-orbit coupling contribution Δ_{SO} at zero magnetic field is given by:

$$\Delta_{SO} = 2\left(\Delta_{SO}^0 \mp \Delta_{SO}^1 \frac{g_{orb}}{g_{orb}^0}\right) \tag{2.11}$$

where $g_{orb}^0 = \frac{ev_F d}{4\mu_B}$. The nanotube spectrum in magnetic fields is therefore modified to account for spin-orbit coupling. This is apparent when comparing Figures 2.6 and 2.7 where the energy spectrum as a function of perpendicular and parallel magnetic fields is shown for Δ_{SO}=0 and Δ_{SO}=0.2 meV, respectively.

A magnetic field that is misaligned by an angle θ with respect to the nanotube axis introduces further changes to the spectrum. The changes are more profound in a perpendicular field, since the misaligned field also couples to the orbital electronic motion and there are four states instead of two. For the parallel field case, the two highest levels (spin-up and spin-down K′ states) anti-cross due to the spin states being mixed. This leads to a gap $\Delta\theta = |\Delta_{SO}|\tan(\theta)$. An example of a misaligned field is show in the inset of Figure 2.7 for $\theta = 10°$. Again, no nanotube disorder is considered.

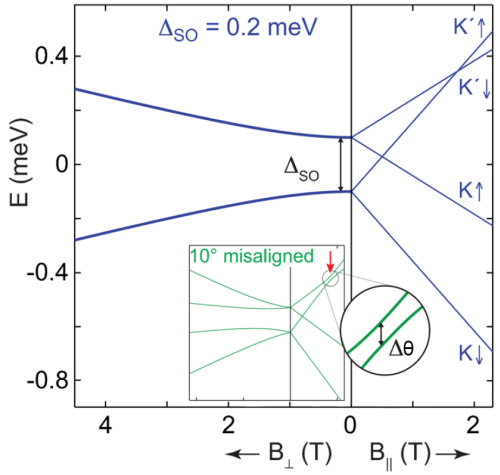

FIGURE 2.7: The nanotube spectrum for perpendicular $B_\perp$ and parallel $B_\parallel$ magnetic fields, including spin-orbit coupling Δ_{SO}=0.2 meV. Similarly to Figure 2.6, there are two doubly-degenerate states for $B_\perp$ and four states for $B_\parallel$. Nanotube disorder is not considered. Inset: a misaligned field introduces anti-crossing between the two highest levels of $B_\parallel$ and lifts the degeneracy in $B_\perp$. *Adapted from Ref* [50].

Nanotube disorder

A more realistic spectrum is one that considers disorder in the nanotube. Such disorder can arise from a number of factors, such as dislocations, impurities, defects and curvature anomalies. Disorder introduces a phenomenological term $\Delta_{KK'}$ in the spectrum that is not derived from first principles. That term mixes the K-K′ states with the same spin, leading to alternations in the spectrum. Such an alternation is the anti-crossing between K↓ and K′ ↑, arising from their mixing. The spectrum of Figure 2.7 now changes to that shown in Figure 2.8, where the spin-orbit coupling is Δ_{SO}=0.2 meV and the mixing term is $\Delta_{KK'}$=0.2 meV.

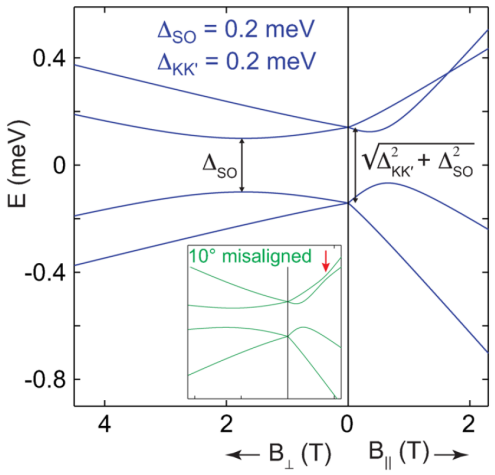

FIGURE 2.8: The nanotube spectrum for perpendicular $B_\perp$ and parallel $B_\parallel$ magnetic fields, including spin-orbit coupling Δ_{SO}=0.2 meV and a mixing term $\Delta_{KK'}$=0.2 meV. Disorder causes an anti-crossing between K↓ and K′ ↑. Inset: a misaligned field with the introduction of a disorder term. *Adapted from Ref* [50].

2.2 Few-Electron Quantum Dots

A quantum dot (QD) is a small semiconducting region in space that can be used to confine charge carriers. The size of the dot is small enough for confined electrons to exhibit discrete and quantised energy states. Therefore quantum dots are often referred to as artificial atoms. The constant interaction model is a convenient description of the physics associated with few-electron quantum dots [30, 59, 64]. In this section, the constant interaction model is outlined for both single and double quantum dots. The model is based on two main assumptions: (i) the Coulomb interactions between electrons on the dots (as well as electrons in the environment) can be parameterised by a single capacitance, (ii) the single-particle energy level spacing (arising from the spatial confinement of the electrons) is independent of the Coulomb interactions and the electron population.

Electron transport through quantum dots is mainly governed by two factors: (i) the charging energy, and (ii) the energy spacing between two discrete energy states. The charging energy E_C concerns the Coulomb repulsion caused by the electrons that are already on the dot. These electrons electrostatically oppose the addition of more electrons, making it energetically unfavourable for electrons to tunnel from the source to the dot. This effect is known as Coulomb blockade. The charging energy is the energy required to overcome this Coulomb repulsion and add one more electron to the dot. The energy spacing between two discrete energy states ΔE concerns the discrete energy spectrum of the electrons arising from spatial confinement on the dot. The value of ΔE is zero if two consecutive electrons are added on the same energy-degenerate level. In general, the total energy required to add a single electron on a quantum dot with N electrons is called the addition energy and it is given by:

$$E_{add}(N) = \mu(N+1) - \mu(N) = E_C + \Delta E \tag{2.12}$$

where $\mu(N)$ is the electrochemical potential of the dot with N electrons. In the following sections, it is assumed that the electron thermal energy is negligible compared to the addition energy; in other words $k_B T \ll E_C, \Delta E$.

2.2.1 Single Quantum Dots

A schematic diagram of a single quantum dot is shown in Figure 2.9. The dot is capacitively coupled to a source s, drain d and gate electrode V_g. Following the two assumptions of the constant interaction model, the sum of capacitances parametrising an electron on such a dot can be expressed as $C = C_s + C_d + C_g$, where C_s, C_d and C_g are the capacitances between the dot and the source, drain and gate, respectively. Applying corresponding voltages V_s, V_d and V_g yields a total energy $U(N)$ for a quantum dot with N electrons, given by:

$$U(N) = \frac{[-|e|(N - N_0) + C_s V_s + C_d V_d + C_g V_g]^2}{2C} + \sum_{n=1}^{N} E_n(B) \tag{2.13}$$

where $|e|$ is the electron charge, $|e|N_0$ is the charge of the dot compensating for any positive background charges and $E_n(B)$ is the single-particle energy levels which dependent on the characteristics of the confinement potential and the applied magnetic field B (if any) [59, 64]. The electrochemical potential $\mu(N)$ is defined as the energy required to

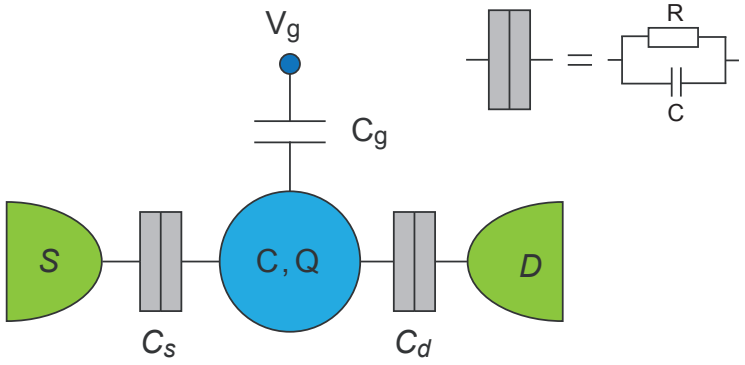

FIGURE 2.9: Schematic diagram of the capacitance model for a quantum dot. The dot is coupled via tunnel barriers to source/drain leads and it is capacitively coupled to a gate electrode V_g. *Adapted from Ref* [65].

add the Nth electron to the dot; therefore it is given by:

$$\begin{aligned}\mu(N) &\equiv U(N) - U(N-1) \\ &= (N - N_0 - \frac{1}{2})E_C - \frac{E_C}{|e|}(C_s V_s + C_d V_d + C_g V_g) + E_N\end{aligned} \tag{2.14}$$

where the charging energy is given by $E_C = e^2/C$. For the case of a carbon nanotube of length L and diameter d, where $L \gg d$, by ignoring C_s and C_d we can approximate the capacitance[2] as $C \approx \epsilon_0 \epsilon_r L$ and the charging energy as:

$$E_C = \frac{e^2}{\epsilon_0 \epsilon_r L} \approx \frac{4.6 \text{ meV}}{L[\mu\text{m}]} \tag{2.15}$$

where we have used $\epsilon_0 = 8.85 \times 10^{-12}$ F/m for the permittivity of free space and $\epsilon_r = 3.9$ for the relative permittivity of SiO_2 [66]. In a similar way, we can approximate the energy level spacing ΔE by taking the $\vec{k}$-component along the length of the nanotube to be $k_{||} = n\pi/L$, just like for a particle-in-a-box. Using Equation 2.4, we obtain:

$$\Delta E = \hbar v_F \Delta k_{||} = \frac{h v_F}{2L} \approx \frac{1.7 \text{ meV}}{L[\mu\text{m}]} \tag{2.16}$$

For electrons to remain localised on the dot, the tunnel barriers between the dot and the source-drain must be sufficiently opaque. This is generally accomplished by weakly coupling the dot to the source-drain leads, such that the contact resistance R_c satisfies $R_c \gg h/e^2$, where $h/e^2 = 25.9$ kΩ is the resistance quantum.

[2] This is a simplification of the classical electrostatic capacitance of a wire to a conductive plane: $C = 2\pi\epsilon_0\epsilon_r L/\ln(4h/d)$, where h= 280 nm is the SiO_2 thickness and d=1 nm.

2.2.1.1 Low-Bias Regime

The ability of electrons to move from source to drain via a quantum dot (vice-versa for holes) depends on the relative alignment of the electrochemical potential of the dot, $\mu(N)$, with respect to the electrochemical potentials of the source and drain, μ_s and μ_d, respectively. The values of μ_s and μ_d relative to each other can be controlled upon applying a bias voltage V_{sd} (conventionally applied to the source). This results in a potential difference between the source and drain and leads to an energy bias window (also known as transport window). The energy levels of the quantum dot can be shifted up or down by applying a gate voltage V_g. Transport only occurs when the energy levels of the dot lie within the bias window, otherwise the dot is in a Coulomb blockade state. This concept is shown in Figure 2.10. If only one energy level lies within the bias window at a time ($\mu_s \geq \mu(N) \geq \mu_d$), then the dot is in the low-bias regime. For a constant addition energy E_{add}, each time an electron tunnels from the source to the dot and then to the drain results in a current peak, as shown in Figure 2.10(c). These peaks are known as Coulomb peaks. In many cases, however, the addition energy E_{add} is not constant for every electron. For example, each energy level on the dot can hold up to two electrons with opposite spins; therefore ΔE is zero when an electron tunnels into a dot with an odd number of electrons. When a higher energy level has to be filled (that is when there is an even number of electrons on the dot), then ΔE is non-zero and E_{add} is larger.

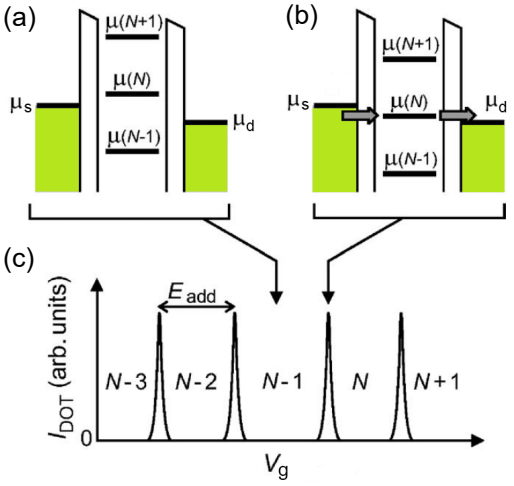

FIGURE 2.10: A low-bias regime schematic: (a) no energy level lies within the bias window: Coulomb blockade, (b) a single energy level lies within the bias window: electron transport is allowed, (c) Coulomb peaks indicating single electron tunneling across the quantum dot for a constant addition energy. *Adapted from Ref* [59].

2.2.1.2 High-Bias Regime

If the source-drain bias V_{sd} is increased, such that at least an excited state of an energy level (ground state) lies within the bias window, then the dot is in the high-bias regime. In this case, an electron can tunnel from the source to the drain via two paths, the ground state or the excited state. If the bias is increased more, the N+1 state can also contribute to tunneling. This concept is shown in Figure 2.11.

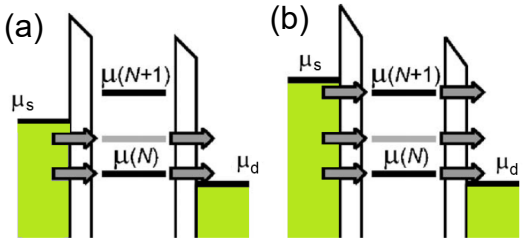

FIGURE 2.11: A high-bias regime schematic: (a) the ground state energy level $\mu(N)$ and its excited state both lie within the bias window, therefore electron tunneling is allowed via two paths, (b) the ground state energy level $\mu(N)$, its excited state and the state $\mu(N+1)$ all lie within the transport window, therefore electron tunneling is allowed via three paths and current through the dot increases. *Adapted from Ref* [59].

The differential conductance $G = dI_{sd}/dV_{sd}$ can be plotted as a function of source-drain bias V_{sd} and gate voltage V_g. Such plots are often referred to as Coulomb diamonds. A Coulomb diamond plot is generally the signature of a quantum dot system. The charging energy E_C and the energy level spacing ΔE can be obtained directly from the diamonds, as shown in Figure 2.12. No current flows inside the diamonds, while transport via excited states can be observed as lines parallel to the edges of the diamonds.

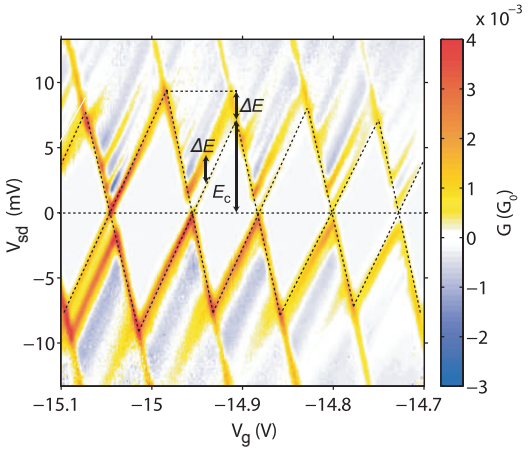

FIGURE 2.12: A Coulomb diamond plot where the differential conductance G is plotted against source-drain bias V_{sd} and gate voltage V_g. No current flows inside the diamonds. The charging energy E_C and the energy level spacing ΔE can be obtained directly from the diamonds as indicated. *Adapted from Ref* [67].

2.2.1.3 Cotunneling

Typical transport through a quantum dot occurs by having an electron tunneling from the source to the dot, and then from the dot to the drain. These are two sequential tunneling events that can only happen when the electrochemical potential of the dot lies within the bias window (otherwise the dot is in a Coulomb blockade state). Cotunneling is a second-order contribution to electron transport that bypasses the Coulomb blockade limitations of regular tunneling and it can occur even if the electrochemical potential of the dot does not lie within the bias window. Cotunneling events can be elastic or inelastic. In elastic cotunneling, an electron tunnels into the dot from the source and the same electron tunnels out to the drain (therefore the initial and final states of the dot have the same energy). In inelastic cotunneling, an electron tunnels into the dot from the source as another electron from a lower energy level tunnels out to the drain (therefore the initial and final states of the dot have different energies). In the latter case, the energy difference is provided by the surroundings (microwave radiation, phonons). Cotunneling events are illustrated in Figure 2.13. Inelastic cotunneling requires that the bias window matches the energy difference between two levels of the dot. In general, cotunneling is expected to be stronger in dots with strong tunnel couplings [60].

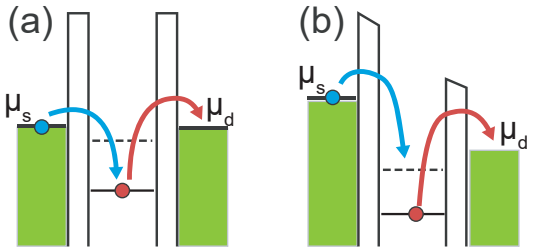

FIGURE 2.13: Schematics of: (a) elastic, and (b) inelastic cotunneling events. *Adapted from Ref* [68].

2.2.1.4 Spins in Single Dots

The simplest spin system is that of a single electron, which can have its spin oriented either up or down. In zero magnetic field, the spin energy states are degenerate; however, the degeneracy is lifted upon applying an external magnetic field. The spin-up and spin-down states are split by the Zeeman energy $\Delta E_Z = g\mu_B B$, where g is the Landé g-factor, μ_B is the Bohr magneton and B is the magnitude of the magnetic field [19, 59]. The lower energy spin state is the one for which the spin is parallel to the magnetic field. The effect of Zeeman splitting can be seen in a Coulomb diamond plot measured in a magnetic field. Such a plot was measured in our lab and it is shown in Figure 2.14, where

the differential conductance is plotted as a function of source-drain bias V_{sd} and gate voltage V_g for (a) B=0, (b) B=3 T, (c) B=6 T, and (d) B=9 T. The device measured is a narrow-gap carbon nanotube quantum dot on degenerately doped silicon, with length 400 nm and room temperature resistance 280 kΩ. The positions of two discrete splittings are indicated with arrows for different magnetic field strengths. At B=9 T, the lower splitting has an energy ΔE_Z=1.2 meV, suggesting a g-factor of 2.3. The latter can include contributions from both the Landé and the orbital g-factors (see Section 2.1.2 for more details).

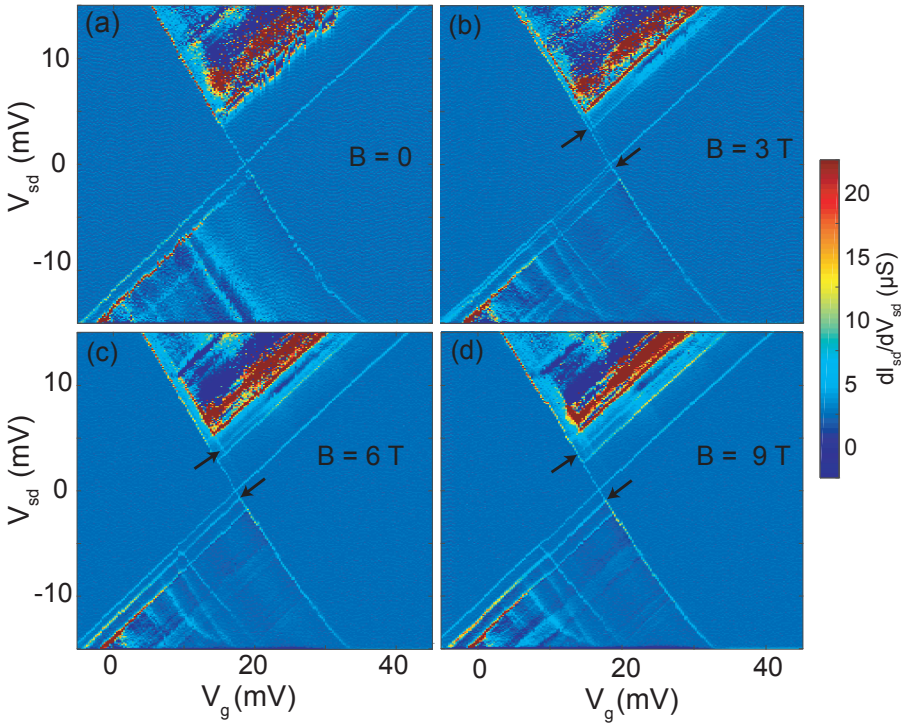

FIGURE 2.14: A Coulomb diamond where the differential conductance is plotted as a function of source-drain bias V_{sd} and gate voltage V_g for different magnetic field strengths: (a) B=0, (b) B=3 T, (c) B=6 T, (d) B=9 T. The positions of two discrete splittings are indicated with arrows for different magnetic field strengths. The device measured is a narrow-gap carbon nanotube quantum dot.

In a system of two electrons, there can exist a total of four spin states, since each electron has two possible spin orientations. There is one singlet spin state which corresponds to the total spin being equal to zero (S=0, S_Z=0), and three triplet states which correspond to the total spin being equal to one (S=1, S_Z=-1,0,+1). All four configurations are listed

below:

$$
\begin{aligned}
|S\rangle &= \frac{|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle}{\sqrt{2}} \\
|T_+\rangle &= |\uparrow\uparrow\rangle \\
|T_0\rangle &= \frac{|\uparrow\downarrow\rangle + |\downarrow\uparrow\rangle}{\sqrt{2}} \\
|T_-\rangle &= |\downarrow\downarrow\rangle
\end{aligned}
\tag{2.17}
$$

The three triplet states are degenerate in energy at zero magnetic field, but the degeneracy is lifted in finite fields since their spin z-components are different: S_Z=+1 for $|T_+\rangle$, S_Z=0 for $|T_0\rangle$ and S_Z=-1 for $|T_-\rangle$. Double quantum dots have richer spin physics to be exploited and used for quantum applications (see Section 2.2.2.4 for more details).

2.2.2 Double Quantum Dots

Serially coupled quantum dots are referred to as "artificial molecules" [30]. Depending on their coupling capacitance, two such dots can form strong or weak "bonds" with strong or weak tunnel couplings, respectively. Since the dots are coupled, the physics behind their behaviour gets more complicated: a change in the energy of one dot affects the energy of the other dot. The coupling strength depends on the tunnel barrier that acts as a separation point between the two dots. The barrier can be introduced by applying a voltage with a gate electrode. The gate voltage depletes the region underneath it and makes it energetically unfavourable for charge carriers to tunnel from one dot to the other.

Following the approach of W. G. van der Wiel et al. [30], a theoretical equivalent of two serially coupled quantum dots is shown in Figure 2.15. The dots are coupled to each other and to the source-drain via tunnel barriers. Each dot is capacitively coupled to a gate electrode that allows tuning of its electrochemical potential. The capacitance between gate 1(2) and dot 2(1) is known as cross capacitance. This is often undesirable, since ideally each dot should only be affected by its corresponding gate electrode. Careful analysis of double dot data can eliminate cross capacitance effects, although the cross capacitance terms are often non-dominant and therefore neglected from some theoretical models. Here, cross capacitance is taken into account. Following the schematic in Figure 2.15, the electrostatic energy $E(n,m)$ of a double quantum dot with n and m electrons on the left and right dot, respectively, is given by [65]:

$$
E_{n,m} = \frac{E_{C_1}}{2n^2} + \frac{E_{C_2}}{2m^2} + E_{C_m} nm + E_1 n + E_2 m \tag{2.18}
$$

where $E_{C_{1(2)}}$, E_{C_m} and $E_{1(2)}$ indicate the charging energy, the electrostatic coupling energy and the single-particle energy of each dot, respectively.

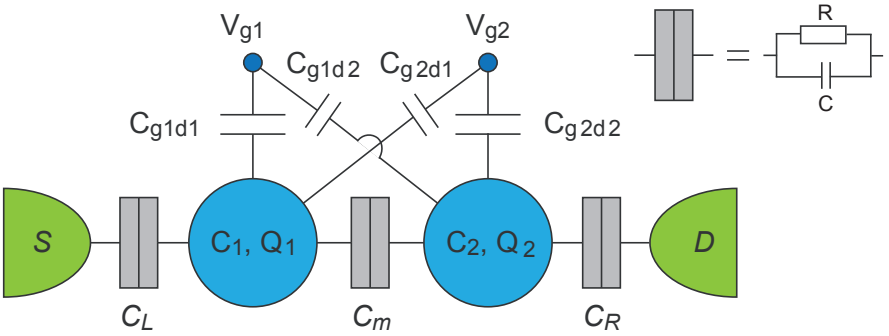

FIGURE 2.15: Schematic diagram of the capacitance model for a double quantum dot. The left (right) dot is coupled to the source (drain) via a tunnel barrier. The two dots are serially coupled to each other by a tunnel barrier and they are capacitively coupled to their corresponding gate electrode. Cross capacitance coupling is included. *Adapted from Ref* [65].

The charging energy $E_{C_{1(2)}}$ and the electrostatic coupling energy E_{C_m} can be expressed in terms of the capacitances $C_{1(2)}$ and C_m. The role of E_{C_m} is to indicate the change of the energy of one dot when an electron is added to the other dot. Expressions for $E_{C_{1(2)}}$ and E_{C_m} are given below:

$$E_{C_{1(2)}} = e^2 \frac{C_{2(1)}}{C_1 C_2 - C_m^2}, \qquad E_{C_m} = e^2 \frac{C_m}{C_1 C_2 - C_m^2} \tag{2.19}$$

where we have defined the capacitances coupled to each dot as:

$$C_{1(2)} = C_{L(R)} + C_{g1(2)d1(2)} + C_{g2(1)d1(2)} + C_m \tag{2.20}$$

The energies $E_{C_{1(2)}}$ correspond to the charging energy e^2/C_Σ for each dot, where C_Σ equals the capacitance of each dot with a correction factor due to the coupling of the dots:

$$C_{\Sigma_{1(2)}} = C_{1(2)} - \frac{C_m^2}{C_{2(1)}} \tag{2.21}$$

The single-particle energies $E_{1(2)}$ are given by:

$$\begin{aligned} E_1 &= AV_{g1} + BV_{g2} = -\frac{1}{|e|}[(C_{g1d1}E_{C1} + C_{g1d2}E_{Cm})V_{g1} + (C_{g2d2}E_{Cm} + C_{g2d1}E_{C1})V_{g2}], \\ E_2 &= CV_{g1} + DV_{g2} = -\frac{1}{|e|}[(C_{g1d1}E_{Cm} + C_{g1d2}E_{C2})V_{g1} + (C_{g2d2}E_{C2} + C_{g2d1}E_{Cm})V_{g2}] \end{aligned} \tag{2.22}$$

where A, B, C, D are lever arms[3] that convert the corresponding gate voltage into energy.

[3]The lever arm is a dimensionless quantity that takes values between 0 and 1 and indicates how much a gate voltage change affects the corresponding quantum dot.

The electrochemical potential $\mu_1(n,m)$ of the first dot is defined as the energy required to add the nth electron to the first dot while having m electrons on the second dot (and vice-versa for $\mu_2(n,m)$). Using Equation 2.18, an expression for μ_1 and μ_2 is obtained:

$$\begin{aligned}\mu_1(n,m) &= E_{n,m} - E_{n-1,m} = (n-1/2)E_{C_1} + mE_{Cm} + E_1 \\ \mu_2(n,m) &= E_{n,m} - E_{n,m-1} = (m-1/2)E_{C_2} + nE_{Cm} + E_2\end{aligned} \tag{2.23}$$

The above equations can be used to calculate the various capacitances associated with a double quantum dot device, as described in the next section.

2.2.2.1 Linear Regime

Electron transport in double quantum dots is often demonstrated with a charge stability diagram, that visualises the equilibrium charge states as a function of plunger gate voltages. In the linear regime, that is $\mu_s - \mu_d = -|e|V_{sd} \approx 0$, only a single energy level of each dot can fit within the bias window. The stability diagram in this regime is illustrated in Figure 2.16(a-c) for small, intermediate and large interdot coupling C_m. The deviation of the stability diagram from a square-like diagram indicates the magnitude C_m. For $C_m \to 0$ the dots are decoupled, while for large C_m ($C_m/C_{1,2} \to 1$), the dots behave as a single large dot. The lines in the diagram indicate the values of the gate voltages for which the number of electrons in the ground state changes [59]. In Figure 2.16(b), a pair of triple points is indicated with a dotted square. Triple points are the result of setting gate voltages such that an electron can tunnel from the source to dot 1, then dot 2 and then to the drain (and vice-versa for holes - see Figure 2.16(d)). Therefore, in the linear regime current only flows through the triple points. This implies that μ_s, μ_1, μ_2 and μ_d are all aligned. In the stability diagram shown, cross capacitance is assumed to be negligible: triple points in Figure 2.16(b) align vertically and horizontally. In reality, the cross capacitance is often non-negligible and stability diagrams appear skewed. The degree of misalignment of the triple points denotes the cross coupling strength [6]. A more detailed explanation of what happens around the triple points is shown in Figure 2.17, where the electrochemical potential lines in the vicinity of the triple points are shown for different tunnel couplings t_c. The solid and dotted lines indicate weak coupling, meaning well-defined electrons on the dots, while dashed lines indicate strong coupling and therefore localised electrons across the dots.

So far, electron spin was not been considered, therefore electrons were treated as spinless particles. Introducing spin into the picture implies doubly degenerate orbitals and deviations to stability diagrams. However, experiments on double dots in the strong coupling regime reproduce the stability diagram of Figure 2.17, even if spin is included.

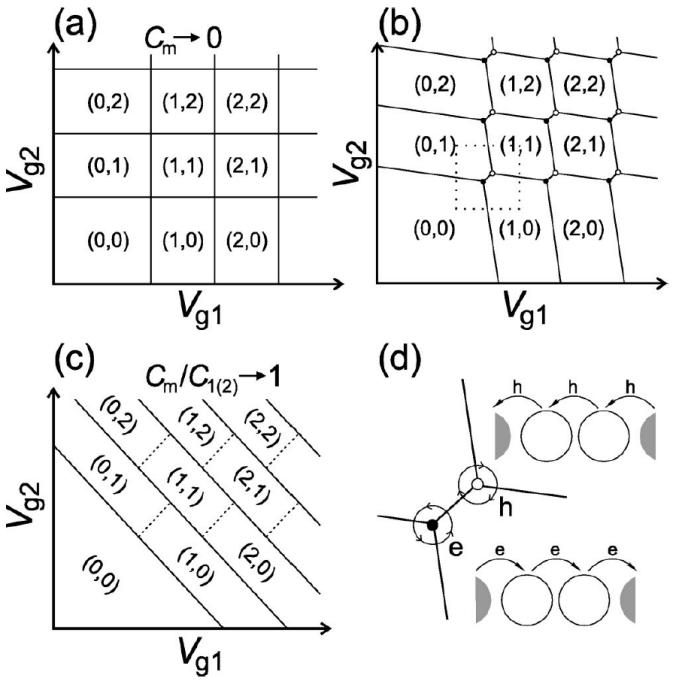

FIGURE 2.16: Stability diagram for a double quantum dot system with various interdot couplings C_m: (a) zero, (b) intermediate, (c) large. The dotted square region of (b) is shown in (d) in more detail. *Adapted from Ref* [30].

A good explanation of this is given by R. Hanson et al. [59]. The Coulomb interactions are usually one or two orders of magnitude larger than the tunnel coupling. Therefore, when the double dot is occupied by two electrons, the electrons are strongly localised. The orbital energy of the two-electron system is equal to the sum of the two single-dot orbitals. When the second electron is added, the tunnel coupling energy that was gained by the first electron has to be recovered, causing the second triple point to appear at higher gate voltages than in the weak-coupling case.

We now discuss how the relevant capacitances can be extracted from a charge stability diagram. The following analysis is based on the approach presented by Z. V. Penfold-Fitch et al. [65]. The dimensions of a well-behaved honeycomb cell of a stability diagram can be used to extract the capacitances of the system. For example, the electron occupancy on the first dot can be changed from n to $n+1$ by changing the voltage on the first gate by ΔV_{g1}, and similarly for the second dot. For the occupancy to change, μ_1 has to be aligned to $\mu_s = 0$, therefore μ_1 does not change during the process. In other words:

$$\begin{aligned} \mu_{1,2}(n, m; V_{g1}, V_{g2}) &= \mu_{1,2}(n+1, m; V_{g1} + \Delta V_{g1}, V_{g2} - \Delta V_{g1}^c) \\ &= \mu_{1,2}(n, m+1; V_{g1} - \Delta V_{g1}^c, V_{g2} + \Delta V_{g1}) \end{aligned} \tag{2.24}$$

Using Equations 2.22 and 2.24 yields expressions for the capacitance between gate 1(2) and dot 1(2), $C_{g1(2)d1(2)}$, and the cross-capacitance between gate 1(2) and dot 2(1),

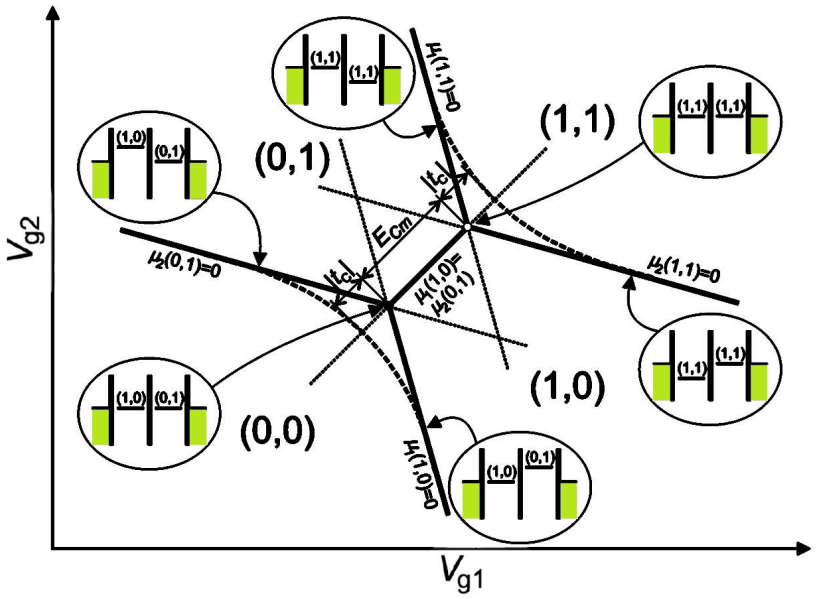

FIGURE 2.17: The electrochemical potential lines in the vicinity of triple points for weak tunnel coupling (solid and dotted lines) and strong tunnel coupling (dashed lines). *Adapted from Ref* [59].

$C_{g1(2)d2(1)}$, are obtained:

$$C_{g1(2)d1(2)} = k\Delta V_{g2(1)}, \qquad C_{g1(2)d2(1)} = k\Delta V^{c}_{g2(1)} \tag{2.25}$$

where $k = |e|/(\Delta V_{g1}\Delta V_{g2} - \Delta V^{c}_{g1}\Delta V^{c}_{g2})$.

Examining the separation between triple points in the horizontal (vertical) axis, namely $\Delta V^{m}_{g1(2)}$, and following a similar approach, the following expressions are obtained:

$$\begin{aligned} \mu_1(n,m;V_{g1},V_{g2}) &= \mu_1(n,m+1;V_{g1}+\Delta V^{m}_{g1},V_{g2}), \\ \mu_2(n,m;V_{g1},V_{g2}) &= \mu_2(n+1,m;V_{g1},V_{g2}+\Delta V^{m}_{g2}) \end{aligned} \tag{2.26}$$

Using Equation 2.26 and measuring the gate-voltage spacing between triple points within a pair $\Delta V^{m}_{g1,2}$, a ratio of the dot capacitance $C_{1(2)}$ and the interdot capacitance C_m can be obtained:

$$\frac{C_{1(2)}}{C_m} = \frac{|e|}{C_{g2(1)d2(1)}\Delta V^{m}_{g2(1)}} - \frac{C_{g2(1)d1(2)}}{C_{g2(1)d2(1)}} \tag{2.27}$$

A schematic of how $\Delta V_{g1(2)}$ and $\Delta V^{m}_{g1(2)}$ lie with respect to the honeycomb cell is shown in Figure 2.18.

A final remark is to note that the approach for obtaining expressions for $\Delta V_{g1(2)}$ and $\Delta V^{m}_{g1(2)}$ does not take into account the quantised energy levels of the system. In other

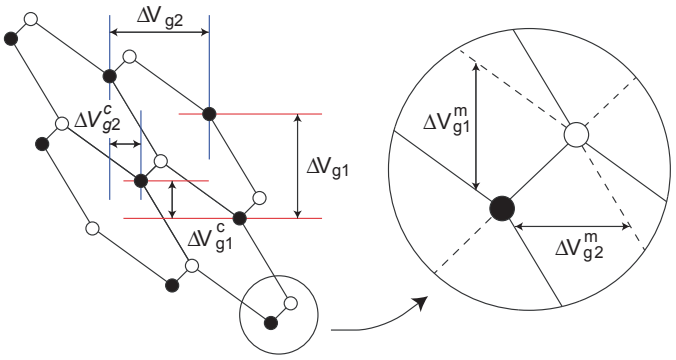

FIGURE 2.18: The dimensions of a honeycomb cell of a stability diagram used to extract the various capacitances of the system. *Adapted from Ref* [65].

words, the energy level spacing ΔE (which can be zero and non-zero in a degenerate system) is also a part of the honeycomb dimensions. The honeycomb cells of the stability diagram thus become larger when ΔE is non-zero. The value of ΔE can roughly be estimated using Equation 2.16. Regardless of the size variation of the stability diagram cells, the charging energies and capacitances can be obtained to a good estimate using a purely electrostatic model.

2.2.2.2 Non-linear Regime

In the non-linear regime, that is $\mu_s - \mu_d = -|e|V_{sd} \neq 0$, more than one states on the dots are available for transport (ground states and excited states). There exists the configuration $\mu_s \geq \mu_1 \geq \mu_2 \geq \mu_d$ which allows for both elastic (between aligned levels) and inelastic tunneling (between misaligned levels). Increasing the source-drain bias V_{sd} for weak tunnel coupling turns the triple points into bias triangles [59]. Current flows through those triangles in the direction the triangles are pointing. An example is shown in Figure 2.19. The total capacitance of each dot, C_1 and C_2, can be obtained by measuring the dimensions δV_{g1} and δV_{g2} of a bias triangle, as shown in the inset of Figure 2.19. The capacitance $C_{1(2)}$ relates to $\delta V_{g1(2)}$ by [65]:

$$|e|\delta V_{g1(2)} = \frac{C_1 C_2 - C_m^2}{C_{g1(2)d1(2)} C_{2(1)} + C_{g1(2)d2(1)} C_m} |e| V_{sd} \tag{2.28}$$

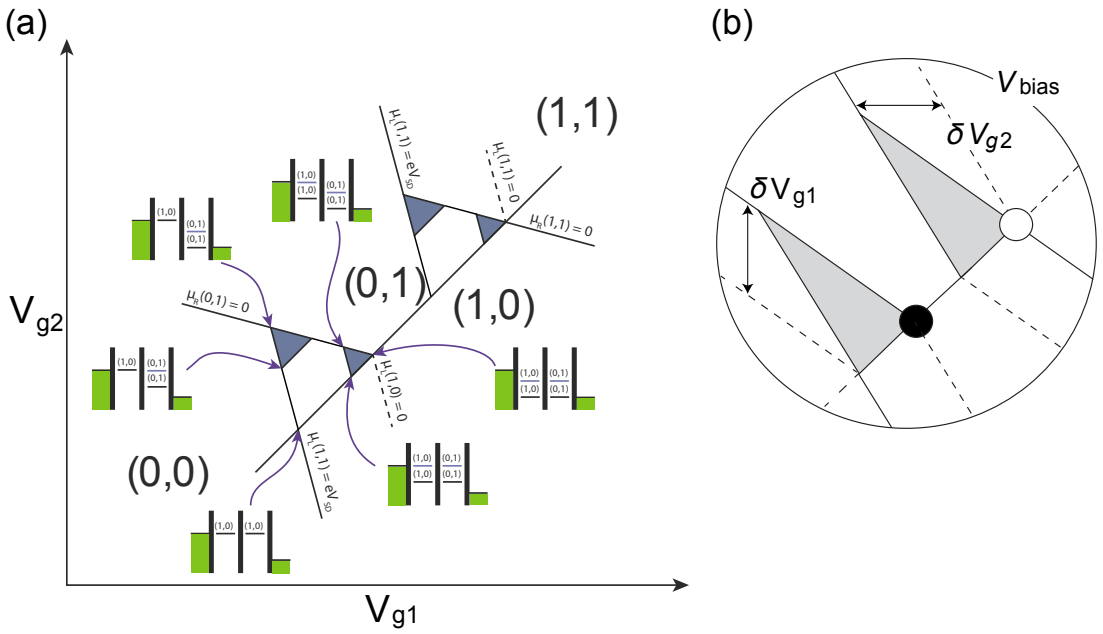

FIGURE 2.19: Non-linear regime stability diagram for a double quantum dot showing bias triangles. The grey lines and regions indicate the gate voltages at which transitions involving excited-state levels are of significance. Inset: triangle dimensions that relate to the capacitances of the system. *Adapted from Ref* [6, 65].

2.2.2.3 Charge Qubits

Two quantum dots with a sufficiently small interdot coupling can be used as a charge qubit by considering the fact that a single electron can either occupy the left or the right dot, and transition between them. The interdot transition behaviour is described by the tunnel coupling t_c and leads to the formation of bonding and anti-bonding states. In a stability diagram, this is apparent by noting that the triple points develop into curved lines. If the tunnel coupling is not taken into account, this two-level quantum system, where spin and lower-level electron interactions are neglected, can be described by a Hamiltonian H_0 with eigenvalues E_{10} & E_{01} and corresponding eigenvectors $|0\rangle \equiv \left(\begin{smallmatrix}1\\0\end{smallmatrix}\right)$ & $|1\rangle \equiv \left(\begin{smallmatrix}0\\1\end{smallmatrix}\right)$, such that $H_0 = E_{10}\,|0\rangle\langle 0| + E_{01}\,|1\rangle\langle 1|$. Given a sufficient tunnel coupling between the two dots, the electron states can mix, resulting in a modified Hamiltonian $H = H_0 + T$, where T is a mixing matrix given by $T = \left(\begin{smallmatrix}0 & t_c\\ t_c & 0\end{smallmatrix}\right)$. Therefore, the Hamiltonian H of a coupled system would be [65]:

$$H = \begin{pmatrix} E_{10} & t_c \\ t_c & E_{01} \end{pmatrix} \tag{2.29}$$

Using Pauli matrices, H can be written as [69]:

$$H = \frac{1}{2}\epsilon\sigma_z + t_c\sigma_x \tag{2.30}$$

where $\epsilon = E_{10} - E_{01}$ is the detuning[4] of the system. The ground and excited state energies for this Hamiltonian (eigenvalues) are shown schematically in Figure 2.20 and they are given by:

$$E_{\pm} = \frac{1}{2}(E_{10} + E_{01}) \mp \frac{1}{2}\sqrt{(E_{10} - E_{01})^2 + 4t_c^2} \tag{2.31}$$

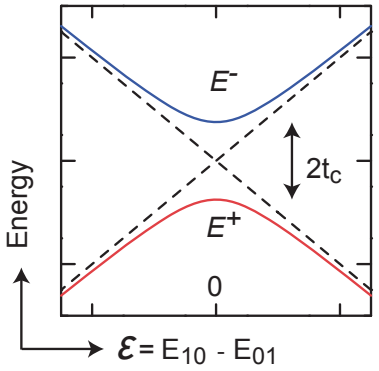

FIGURE 2.20: The bonding (red) and anti-bonding (blue) states as a function of detuning for a charge qubit. At zero detuning, the two states are separated by an energy $2t_c$, where t_c is the tunnel coupling. *Adapted from Ref* [65].

The quantum capacitance of the system is maximised at zero detuning and is given by [6, 34, 65, 69]:

$$C_Q^{\pm} = -e^2\beta^2 \frac{\partial^2 E_{\pm}}{\partial \epsilon^2} \tag{2.32}$$

where β is a level arm that converts between the resonator voltage V_{RF} and detuning ($\Delta\epsilon = -e\beta\Delta V_{RF}$).

The charge qubit band structure and corresponding quantum capacitance are shown in Figure 2.21 as a function of detuning ϵ for (a) one and (b) two electrons. The (n, m) notation denotes the electron occupation of the left and right dot. The singlet and triplet spin configurations are indicated by S and T, respectively.

2.2.2.4 Spin Qubits

In double quantum dots, the transfer of electrons from one dot to the other is easily achieved by changing the voltage on the corresponding plunger gate. Electrons hopping from one dot to the other conserve spin, and their behaviour is governed by spin selection rules [59, 70]. Focusing on the two-electron regime, the dots can be in one of the states $(n, m) = (0, 2)$ or $(n, m) = (1, 1)$. For the former, the possible spin states are the same

[4] The detuning refers to the relative shift between the energy levels of the two dots.

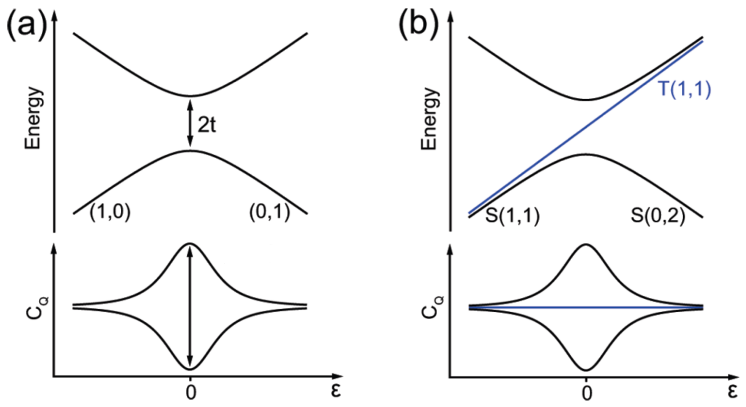

FIGURE 2.21: The energy bands and quantum capacitance of a charge qubit as a function of detuning for a double quantum dot with (a) one and (b) two electrons. The singlet and triplet spin configurations are indicated by S and T, respectively. *Adapted from Ref* [69].

as for a single dot: the two electrons are in a singlet or triplet state, if they occupy the same or different energy level, respectively (see Equation 2.17). A similar situation occurs for the $(n, m) = (1, 1)$ state, but this time each electron sits on a different dot, such that:

$$\begin{aligned} |S(1,1)\rangle &= \frac{|\uparrow_1\downarrow_2\rangle - |\downarrow_1\uparrow_2\rangle}{\sqrt{2}} \\ |T_+(1,1)\rangle &= |\uparrow_1\uparrow_2\rangle \\ |T_0(1,1)\rangle &= \frac{|\uparrow_1\downarrow_2\rangle + |\downarrow_1\uparrow_2\rangle}{\sqrt{2}} \\ |T_-(1,1)\rangle &= |\downarrow_1\downarrow_2\rangle \end{aligned} \tag{2.33}$$

Spin-to-charge conversion

The minuscule magnetic moment associated with an electron spin makes it very challenging to directly measure it. A way around this is to correlate the electron spin states to different charge states, and determine the spin state by measuring the charge on the dot, which is a much easier task. This is known as spin-to-charge conversion [59]. Two methods that allow for spin-to-charge conversion are energy-selective readout and tunnel-rate-selective readout. In energy-selective readout, the spin levels are positioned on either side of the electrochemical potential of the leads, such that an electron can tunnel off the dot from the spin excited state, whereas tunneling from the ground state is energetically forbidden. Therefore, if a charge measurement shows that an electron tunneled off the dot, the spin state was an excited sate, while if there was no electron tunneling, the state was a ground state. Single-shot spin readout using this method was first demonstrated by J. M. Elzerman et al. [71]. Tunnel-rate-selective readout exploits the difference in tunnel rates of the different spin states to the leads. Suppose the tunnel rates from an exited and ground spin state are Γ_{ES} and Γ_{GS}, respectively.

For $\Gamma_{ES} \gg \Gamma_{GS}$, if the two spin states are placed far above the electrochemical potential of the leads, then after time t for which $\Gamma_{ES}^{-1} \ll t \ll \Gamma_{GS}^{-1}$, an electron in the excited state will tunnel off the dot with high probability. On the other hand, tunneling from the ground state is unlikely. Thus, measuring the charge on the dot would reveal the initial spin state. The tunnel-rate-selective readout has been tested experimentally by R. Hanson et al. [72]. The two aforementioned methods are illustrated in Figure 2.22.

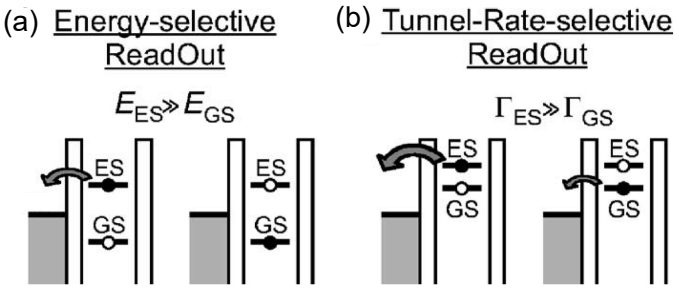

FIGURE 2.22: Energy diagrams illustrating two different methods for spin-to-charge conversion: (a) energy-selective readout, and (b) tunnel-rate-selective readout. The ground and excited spin states are denoted by GS and ES, respectively. *Adapted from Ref* [59].

Spin blockade

The fact that electron tunneling conserves spin can lead to current suppression across a double dot system under the appropriate conditions. This is referred to as spin blockade and originates from the Pauli exclusion principle. Its effects can be observed at finite biases when reversing the source-drain bias while having an electron on each dot in a spin triplet state. In Figure 2.23(a) and (c), a single electron occupies both dots and no current is suppressed upon reversing the bias. In (b) and (d), two electrons occupy the dots and when the bias is reversed, the current is greatly suppressed. In (d), current only flows at the lower and upper edges of the bias triangles, attributed to the exchange of an electron with another of different spin from the source lead. This drives the system to a singlet state, which allows for transport. Spin blockade has been observed in a variety of double quantum dots, including carbon nanotube [41, 73–75], silicon [34] and 2DEG [76] devices.

The energy difference between the lowest-energy singlet and triplet states depends on the tunnel coupling and the single dot charging energies [59]. With an external magnetic field, the two-electron singlet-triplet states hybridise for different detunings. The energies of the singlet-triplet states are shown in Figure 2.24 as a function of detuning ϵ for zero and finite magnetic field B and coupling constant t_c. For $t_c > 0$, the singlet and triplet states hybridise at different detunings and energies. Upon applying an external magnetic field, the triplet state degeneracy is lifted, and this results in some triplet and singlet

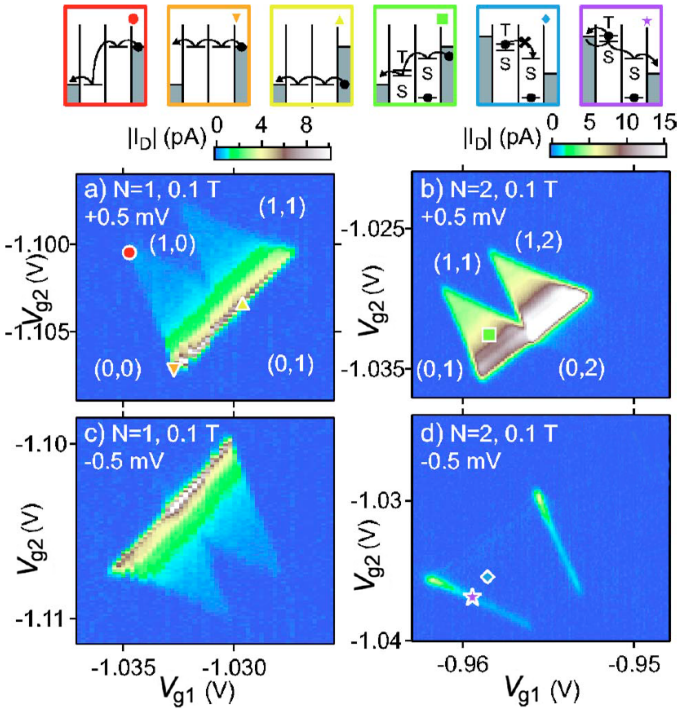

FIGURE 2.23: Bias triangles measured with one and two electrons for $V_{sd} = \pm 0.5$ mV and B=0.1 T. Parts (a) and (c) show that no spin blockade occurs when a single electron occupies the dots and the bias is reversed. Parts (b) and (d) show that if two electrons are present in the dots, spin blockade suppresses the current flow when the bias is reversed. *Adapted from Ref* [76].

states having the same energy for a given ϵ and B, for example $S(0,2)$ and T_+. In the presence of spin-orbit interaction, $S(0,2)$ and T_+ will also hybridise (not shown). A system that shows this behaviour could be used to investigate spin qubits [41].

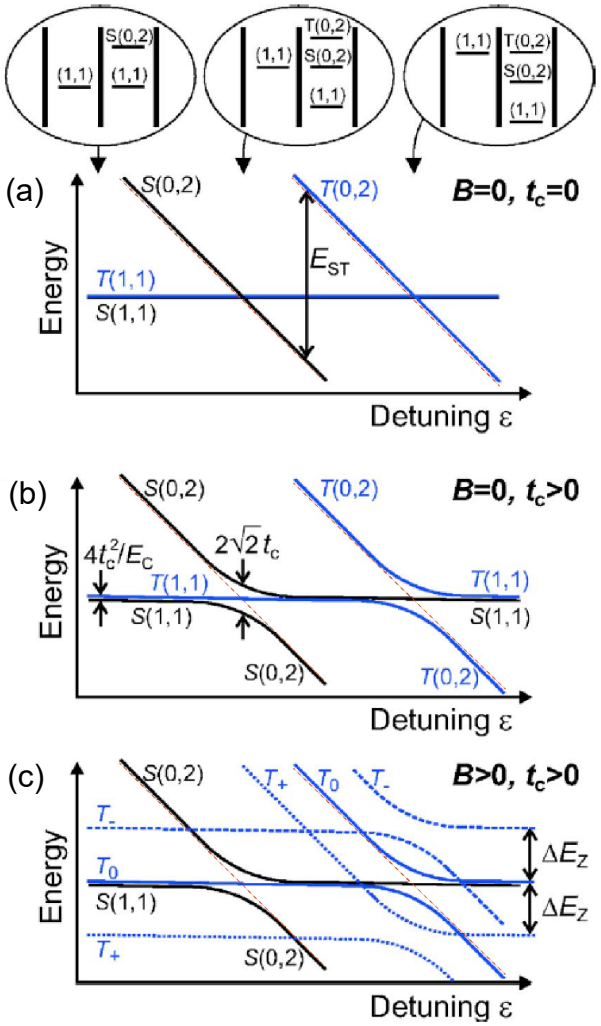

FIGURE 2.24: The energies of singlet-triplet spin states in a double quantum dot as a function of detuning for (a) zero magnetic field and zero tunnel coupling, (b) zero magnetic field and finite tunnel coupling, (c) finite magnetic field and finite tunnel coupling. The singlet states hybridise for a finite tunnel coupling and the triplet state degeneracy is lifted for a finite magnetic field. *Adapted from Ref* [59].

Chapter 3

Experimental Methods

This chapter outlines the experimental methods adapted for the work presented in this thesis. We start by briefly summarising the steps for fabrication of carbon nanotube quantum dot devices, and emphasising on the customisation of a dry dilution refrigerator to allow for ultra-low electron temperatures and high-frequency techniques. The dilution fridge was customised from scratch with the great help of Dr. Byron Villis. The implementation of various electronic filters is discussed, as well as the preparation of high-frequency lines, including active and passive components that accompany them. The design and optimisation of a sample holder and printed-circuit board (PCB) is outlined. A low-electron temperature is demonstrated for quantum dot devices, and an introduction to radio-frequency reflectometry is given.

All measurements presented in this thesis were taken using MathWorks MATLAB, unless otherwise stated. Code scripts were written to allow for fully automated control of all equipment in the lab. Further code was prepared for data acquisition, analysis and presentation. All scripts were developed, tested and optimised by the author, including a total of more than 8600 executable lines of code. The source code is available here: www.ucl.ac.uk/quantum-devices/sites/quantum-devices/files/matlabcode.zip.

3.1 Device Fabrication

Carbon nanotube quantum dot devices were prepared on undoped and degenerately doped silicon. A summary of the fabrication process is outlined below, while the detailed procedure is given in Appendix A.

1. **Carbon nanotube growth** - Single-walled nanotubes were grown directly on silicon substrates using chemical vapour deposition (CVD). The gas used for growth was methane with natural abundance carbon isotopes (98.89% ^{12}C and 1.11% ^{13}C).

2. **Device designs and fabrication** - Bond pads and alignment marks were added on the substrates using electron beam lithography (EBL) and metal evaporation. Atomic force microscopy (AFM) was used to locate nanotubes with respect to the alignment marks, and appropriate device designs were prepared. For double dots, the designs were implemented in two steps (one EBL exposure and one metal evaporation for each step), since the top gates require a separate evaporation due to the insulating oxide layer. Single dot designs require only one EBL and evaporation step.

3. **Room temperature characterisation** - Devices were bonded and tested at room temperature by carrying out basic DC measurements to characterise the nature of the nanotube and the overall quality of the device.

A doped substrate has the advantage that it can be used as a back gate for devices, eliminating the need for an additional gate and bond pad. If the device is on undoped silicon, the substrate cannot be used as a back gate at low temperatures, so a control gate is advised. For experiments where radio-frequency reflectometry is used, devices on undoped silicon are preferred, as the parasitic capacitance of the device is about one order of magnitude lower compared to devices on doped silicon (see Section 3.4 for more details). An SEM image of a carbon nanotube double quantum dot on doped and undoped silicon is shown in Figure 3.1(a) and (b), respectively.

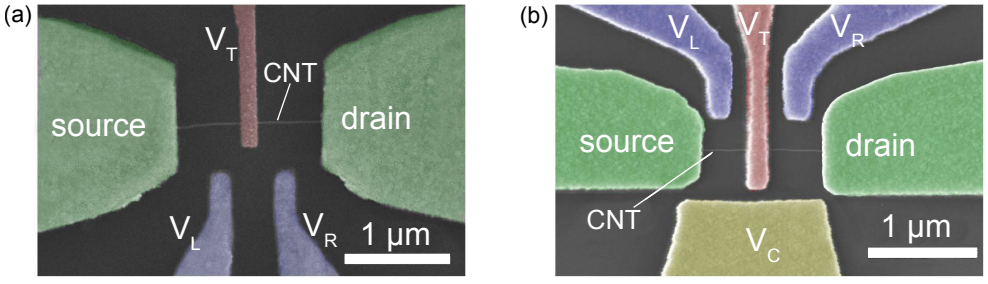

FIGURE 3.1: False colour SEM images of carbon nanotube double quantum dot devices fabricated on (a) doped and (b) undoped silicon. For the latter, an additional control gate V_c is recommended, since the substrate cannot be used as back gate at low temperatures.

3.1.1 Room Temperature Characterisation

Carbon nanotube-based devices can be tested at room temperature and provide a rough estimate regarding the nature of the nanotube and the overall quality of the device. This is a great advantage, given that for other kind of quantum dots (such as 2DEG devices) the device has to be cooled down to a few Kelvin for evaluation. The most typical test for a nanotube quantum dot involves the application of a source-drain bias and a gate sweep. The current as a function of gate voltage reveals the nature of the nanotube (see Figure 2.5) and the overall conductance of the device.

It is generally a good habit to check the PCB and DC lines for shorts before bonding any device. This is easily done by using a source measure unit (SMU) instrument and it can prevent the destruction of devices due to shorts. A voltage of a few 10s of V can be applied to each DC line with the rest grounded, and resistance to ground can be measured. For our setup configuration, every DC line has at least 100 GΩ resistance to ground with 30 V applied (measured with a relative humidity of ∼30%), suggesting negligible current leakage.

After a device is bonded, a source-drain bias V_{sd} of 25 mV is applied and a gate voltage V_g is swept. If the substrate is doped silicon, the gate is a back gate, otherwise it is a side control gate[1]. The typical current response I_{sd} of a semiconducting and a narrow-gap nanotube are shown in Figure 3.2 (a) and (b), respectively. The total DC resistance of the device can be determined by having V_g at a constant voltage for which transport through the Fermi level is allowed (particularly important for semiconducting nanotubes), and stepping V_{sd}. The device resistance is dominated by the contact resistance between the nanotube and the leads. Typically, narrow-gap and semiconducting nanotube devices have a resistance of the order of 100 kΩ and 1 MΩ, respectively [48]. This difference is roughly expected, given that the band gap of a typical semiconducting nanotube is about 10 times larger than that of a narrow-gap. However, semiconducting devices are more susceptible to disorder and their total resistance is typically higher.

For comparison, the same gate sweeps at milliKelvin temperatures with V_{sd}=1 mV are shown in Figure 3.3. Similarly to room temperature, semiconducting nanotubes are only conducting at negative voltages (valence band conduction) as opposed to narrow-gap nanotubes that show conductance both at negative and positive voltages (valence and conduction bands). For semiconducting nanotubes, Coulomb peaks are more sparse, and therefore Coulomb diamonds are larger.

[1] Although an undoped silicon substrate can be used as a back gate at room temperature, it was observed that doing so led to major hysteresis that introduced a lot of drift in the measurements at low temperature, even days later. Using the substrate of an undoped device as a back gate was avoided since then (see Section 5.3 for more details).

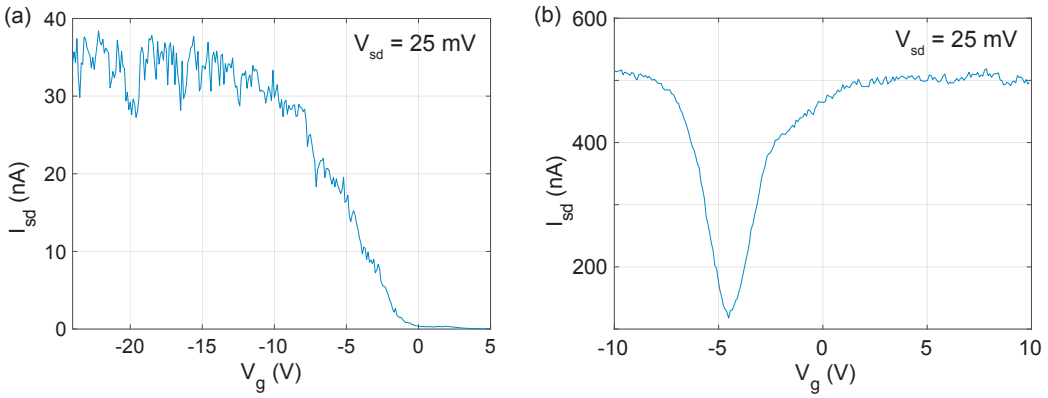

FIGURE 3.2: The current response at room temperature as a function of gate voltage V_g for: (a) semiconducting, (b) narrow-gap nanotube quantum dots. The source-drain bias is 25 mV.

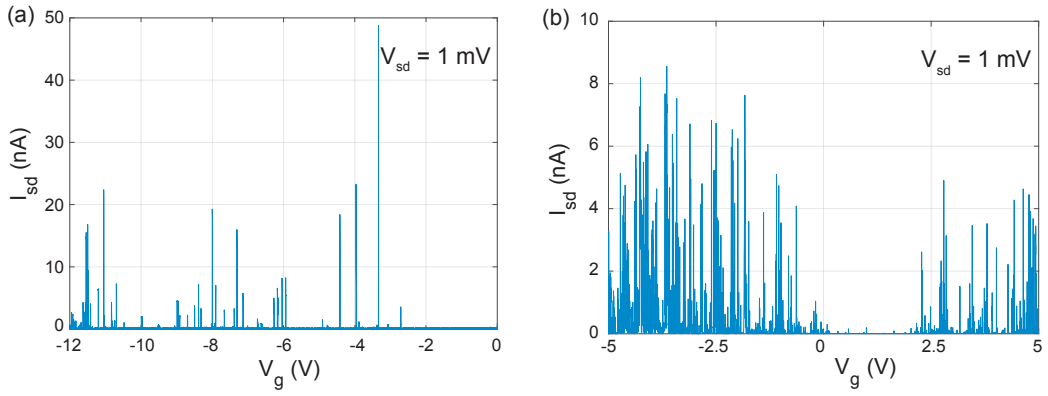

FIGURE 3.3: The current response at 6 mK as a function of gate voltage V_g showing Coulomb peaks for: (a) semiconducting, (b) narrow-gap nanotube quantum dots. The source-drain bias is 1 mV.

The characterisation tests described above are sufficient for single quantum dots, however double quantum dots require further tests due to their more complex geometry. These are discussed in Section 5.1 of Chapter 5, which focuses on double dots.

3.2 Dilution Refrigerator Customisation

Low-temperature measurements were carried out in a BlueFors LD-250 dry dilution refrigerator with a base temperature of 6 mK. The physical size of the fridge allows for a lot of customisation that includes high-frequency components and electronic filters. Coaxial high-frequency lines were installed to allow for radio-frequency (RF) reflectometry and microwave signals, while a series of DC filters were introduced at various stages

to allow for sufficiently low electron temperatures. A schematic of the components installed in the cryostat is shown in Figure 3.4, while a photograph of the cryostat with the components indicated is shown in Figure 3.5. This section outlines the steps taken towards implementing sufficient DC filtering and optimising the high-frequency setup, as well as preparing a sample holder and PCB to accommodate devices.

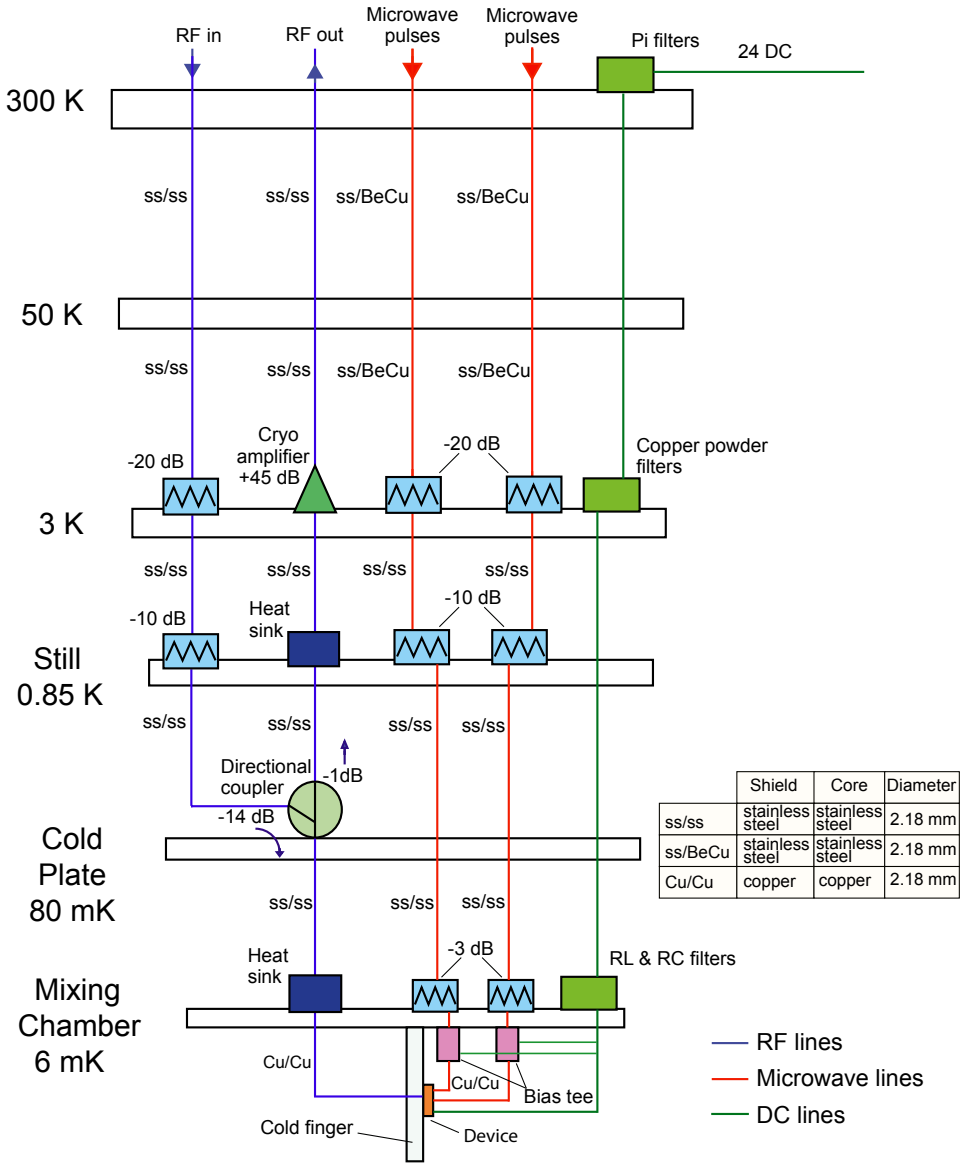

FIGURE 3.4: A schematic diagram showing the customised DC, RF and microwave lines installed in the dilution refrigerator, along with the relevant components.

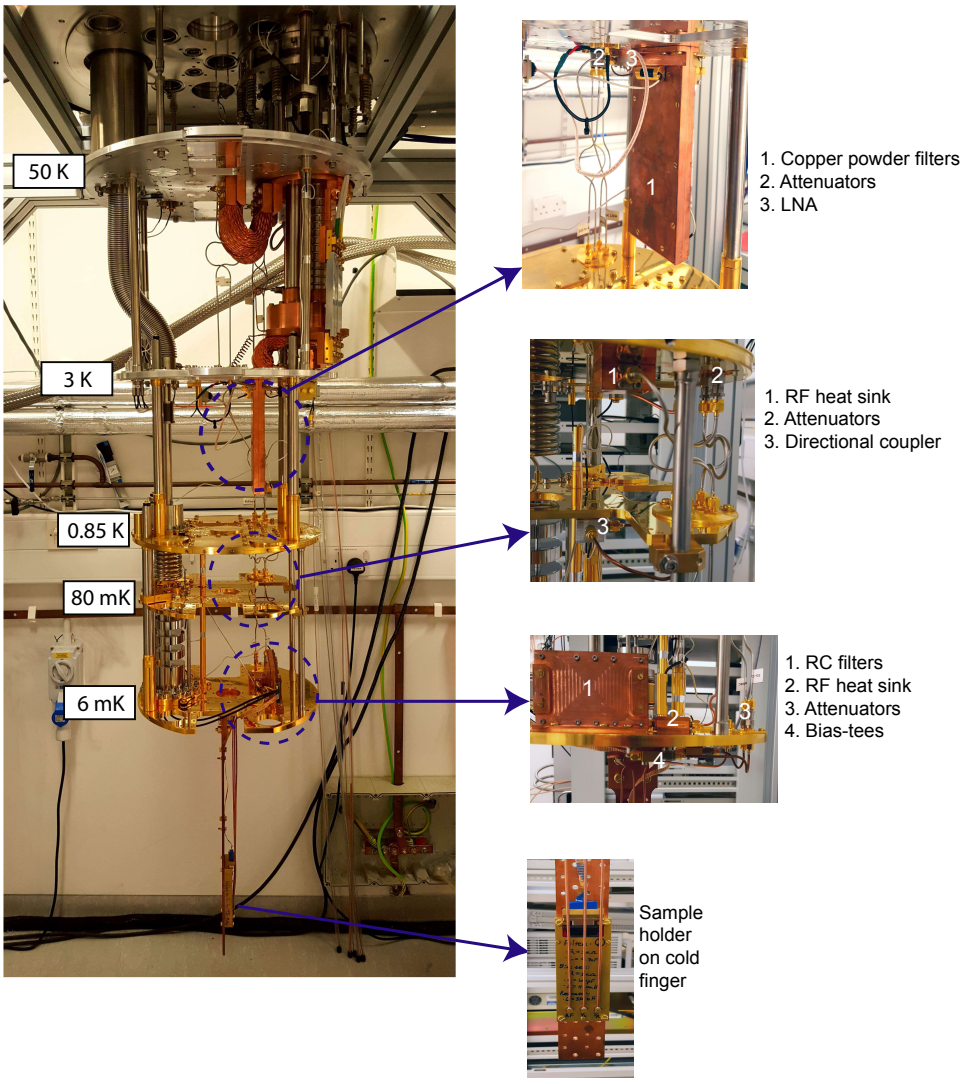

FIGURE 3.5: A photograph of the cryostat indicating the installed components.

3.2.1 DC Filtering

At ultra-low temperatures, the weakening of electron-phonon interactions often results in electron temperatures that are elevated compared to the lattice temperature. At such temperatures, the system cools through conduction electrons, where heat transfer is mediated through electrical contact to the sample [77]. Semiconductor devices have relatively high contact resistance, which makes them vulnerable to heat leaks, such as dissipative heating and high-frequency electromagnetic radiation. The latter is a major source of heating of transport electrons [78]. To overcome this issue, a multi-stage DC filtering setup was implemented to attenuate electronic noise and allow for ultra-low electron temperatures. Given that filtering elements emit thermal noise by themselves, different filtering stages had to be introduced at various temperatures, and especially

at base temperature. Details about how the electronic temperatures were measured are discussed in Section 3.3.

The DC filters introduced are the following: (a) capacitor-input filters (pi-filters) at room temperature, (b) copper powder filters at 3 K, (c) low-pass filters at base temperature (both on mixing chamber and PCB). Commercial capacitor-input filters (TUSONIX 4209-053LF) were used as a first-stage room temperature filter, while all the other filters were fabricated in the lab. It is important to have various kinds of filters, as different types are more effective for attenuating different frequencies. In general, RC filters attenuate the low frequency range (0.01-10 MHz), capacitor-input filters attenuate intermediate frequencies (0.01-1 GHz) and metal powder filters attenuate higher frequencies (0.1-100 GHz) [78].

The copper powder filters were fabricated in a way similar to the approach of F. Mueller et al. [78]. The implementation involves double-sided PCBs with 12 DC lines and one Cinch connector on each side. Each line trace has a length of about 2 m and a width of 150 µm (smaller widths and longer lengths showed current leakage). The PCBs were designed using DipTrace and manufactured by Minnitron Ltd. High-resistivity stycast suitable for low temperature applications[2] was mixed with copper powder (10 µm particle size) and used to coat the front and back sides of the PCB. Oxygen-free copper housing was used to host and mount the filter on the 3 K stage. A 2 mm thick layer of non-magnetic Eccosorb was put in the gaps between the stycast and the box lids as an extra microwave absorbing medium, and conductive copper-tape was used to seal possible gaps around the housing. The copper powder filters are shown in Figure 3.6. For evaluation, the insertion loss S_{21} of the filters was measured at room temperature with and without Eccosorb. The filters seemed to work well, especially for frequencies higher than 1 GHz, while the attenuation becomes about 15 dB more aggressive with the introduction of Eccosorb. A comparison of the insertion loss with and without Eccosorb is shown in Figure 3.7.

The low-pass filters on the mixing chamber consist of RL and RC components on a multi-layer PCB arranged in such a way that they allow for 5 stages of filtering. The first 3 stages include commercial RL filters with cut-off frequencies of 5 GHz, 1.47 GHz and 80 MHz, respectively. The next 2 stages include RC filters with the chosen cut-off frequencies of 160 kHz (R=1 kΩ, C=1 nF) and 48 kHz (R=1 kΩ, C=3.3 nF). The multi-layer filter design used was inspired by the work of F. Kuemmeth and C. M. Marcus [79]. The filters are shown in Figure 3.8. Again, a layer of non-magnetic Eccosorb as put between the filter PCB and its oxygen-free copper housing. Conductive copper-tape was

[2] At first, the stycast used was Loctite 2850FT Black (with catalyst 9), but it was later replaced by 2850FT Blue (with catalyst 11), which is more resistive and better rated for low temperatures.

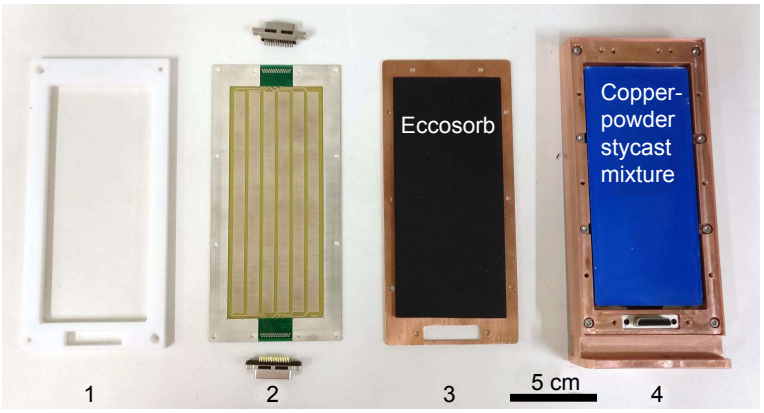

FIGURE 3.6: The components of a copper-powder DC filter. A plastic mould (1) is mounted on top of the PCB (2) after the two Cinch connectors are soldered on it. Stycast is mixed with copper powder and poured on the PCB. The lids are covered with Eccosorb (3) and they shield the filter after it is enclosed in an oxygen-free copper box (4). The box is then mounted on the 3 K stage on the dilution fridge.

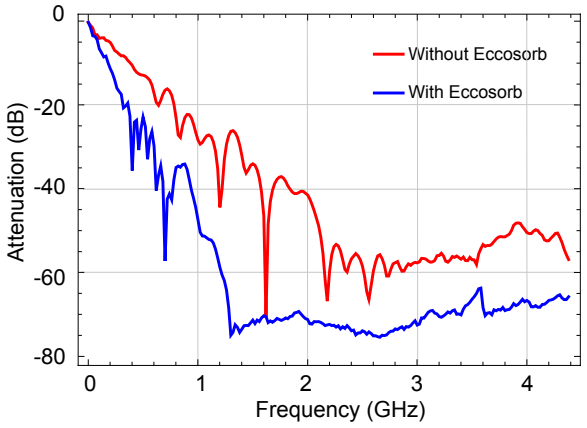

FIGURE 3.7: The insertion loss S_{21} of the copper-powder filters measured at room temperature, without (red) and with Eccosorb (blue).

used to seal possible gaps around the housing. Both copper-powder and mixing chamber filters were thermally cycled several times in liquid nitrogen before testing in the fridge, to ensure normal behaviour and absence of current leakage or physical fracture. In the case of high voltages, the mixing chamber filters had no problems for voltages up to 200 V. On the other hand, for reasons not well understood, the copper powder filters seem to short between twisted pairs for voltages higher than 100 V. This is not an issue, since typical voltages during measurements are much lower.

The final stage of filtering includes *RC* filters on the PCB with a cut-off frequency of 34 kHz (R=1 kΩ, C=4.7 nF). The PCB design is discussed in Section 3.2.3. With several stages of filtering, high-frequencies in the DC lines are heavily attenuated, as desired. On the other hand, it is important for the setup to allow for low-frequency AC

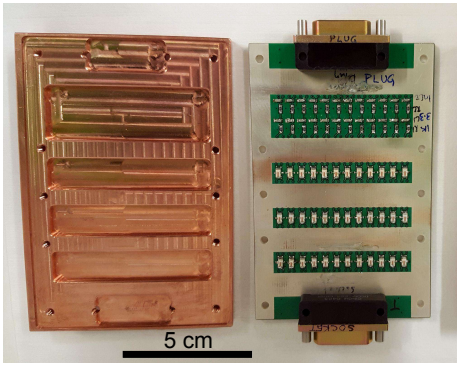

FIGURE 3.8: A multi-layer PCB with low-pass filters soldered in series and its corresponding oxygen-free copper housing. The filter is mounted on the mixing chamber of the dilution fridge.

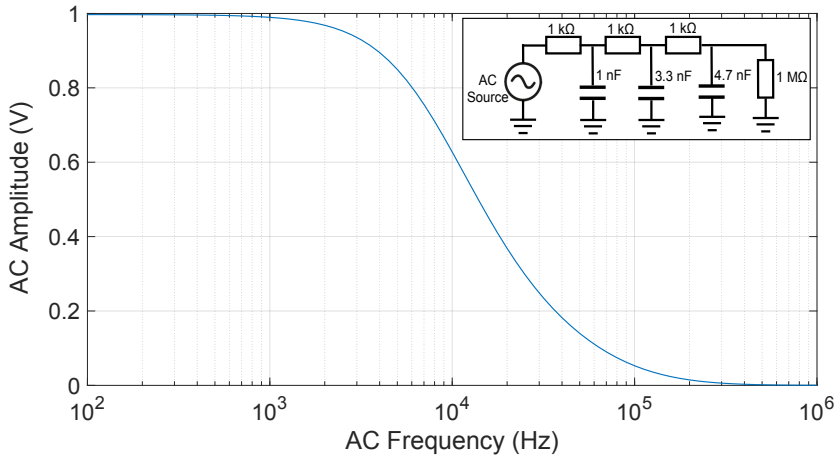

FIGURE 3.9: A simulation of AC voltage input response as a function of AC frequency for the circuit shown in the inset. The circuit refers to the *RC* filters on the mixing chamber and the PCB, with a quantum dot device of typical resistance 1 MΩ. The plot simulates an AC voltage input of 1 V peak-to-peak and indicates the voltage that reaches the device for each driving frequency. The -3 dB point is at ∼8 kHz.

voltages (0.1-10 kHz) for fast gate sweeps and/or gate modulations. A simulation of an AC peak-to-peak voltage response as a function of AC frequency is shown in Figure 3.9 for the circuit combination shown in the inset. That circuit refers to the *RC* filters on the mixing chamber and the PCB, with a quantum dot device of typical resistance 1 MΩ. The plot simulates an AC voltage input of 1 V peak-to-peak and indicates the voltage that reaches the device for each driving frequency. Although the -3 dB point is at ∼8 kHz in the simulation, in practice it was found to be ∼4 kHz when tested with the experimental setup.

3.2.2 High-frequency Setup

High-frequency lines were installed in the dilution refrigerator to allow for radio-frequency (RF) reflectometry measurements and microwave signals. The setup configuration is shown in Figure 3.4. This section discusses the implementation of the relevant setup.

For RF reflectometry, relevant attenuators were installed on different temperature stages of the fridge, to roughly match the temperature change (-20 dB at 3 K and -10 dB at 0.85 K, corresponding to a reduction in temperature by factors 100 and 10, respectively)[3]. A directional coupler (Mini-Circuits ZEDC-15-2B) was installed on the cold plate to distinguish between incident and reflected RF signals. The coupler also acts as a -14 dB and -1 dB attenuator for incident and reflected signals, respectively.

For the RF lines, two impedance-matched microstrip line heat sinks were installed on the still and mixing chamber for thermalisation of the inner core of the lines. Initially, impedance-matched sapphire strip lines were used as heat sinks. Although quartz has a thermal conductivity of nearly one order of magnitude higher than sapphire [80], the latter was used because it is not piezoelectric like quartz. Single-side polished sapphire of thickness 430 µm was cut in 2×0.8 cm pieces and a strip line was fabricated on the polished side. A width of 360 µm was chosen for the strip line, based on the dielectric and thickness of the sapphire [81], such that the total impedance of the heat sink would match the coaxial lines. The strip line had a thickness of 330 nm (30 nm chrome and 300 nm silver, deposited using thermal evaporation). For better thermal conduction, the back of the sapphire pieces was coated with a 10 nm layer of chrome, followed by a 60 nm layer of gold, while the housing was made of oxygen-free copper. The idea for a sapphire microstrip heat sink was adapted from the work of H. Churchill [82]. A picture of such a heat sink is shown in Figure 3.10(a).

On a later stage, the two sapphire stripline heat sinks were replaced by impedance-matched PCB microstrips made of copper and printed on FR4, shown in Figure 3.10(b). The optimum microstrip width with respect to minimum insertion loss below 1 GHz and attenuation at higher frequencies was found to be 0.96 mm. Pieces of Eccosorb were used to cover the copper microstrip and the housing was made of oxygen-free copper. The main reason for these new heat sinks is that the insertion loss for up to 500 MHz was lower in comparison to the sapphire heat sinks (-0.3 dB instead of -1 dB, measured at 77 K). Moreover, with the addition of Eccosorb, the attenuation at high frequencies was quite aggressive, therefore the new heat sinks would also serve as filters. The insertion loss S_{21} and return loss S_{11} of the PCB heat sinks are shown in Figure 3.11(a) and

[3] At first, all attenuators used were from Midwest Microwave Solutions (SF0929-6200-10). However, the attenuators would turn superconducting at temperatures below 1 K, therefore those on the still and mixing chamber were replaced by XMA Cryo attenuators (2082-6418-10-CRYO).

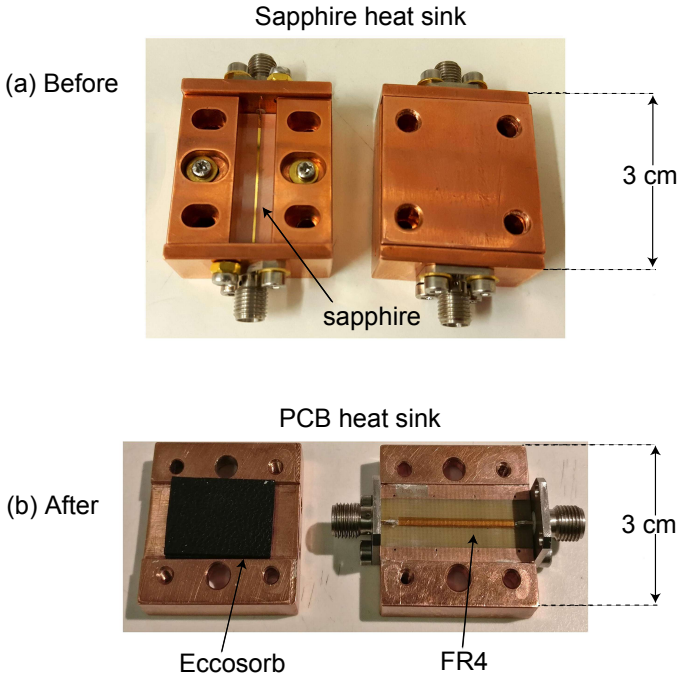

FIGURE 3.10: (a) A sapphire microstrip heat sink initially used for thermalisation of the inner core of the RF lines. (b) A PCB microstrip heat sink that replaced the sapphire heat sink.

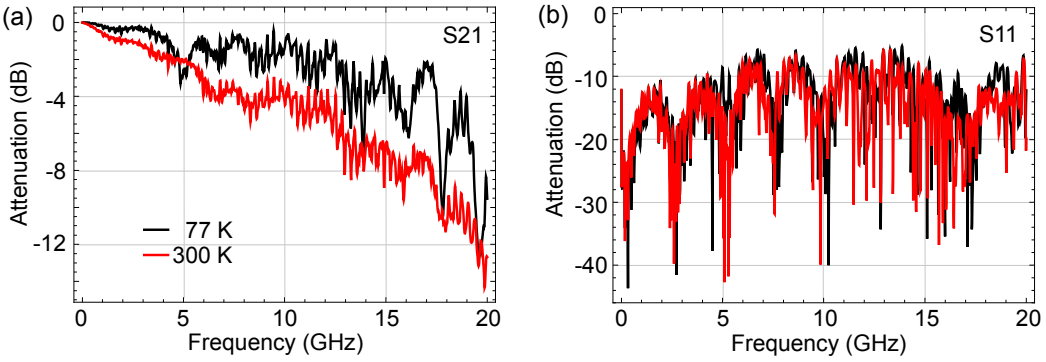

FIGURE 3.11: (a) The insertion loss S_{21} and (b) return loss S_{11} of the PCB microstrip heat sink measured at room temperature (red) and 77 K (black).

(b), respectively, measured at room temperature (red) and 77 K (black). The PCB microstrip heat sinks were generally easier to fabricate compared to sapphire heat sinks.

A low-noise cryogenic SiGe amplifier (CITLF1, 1-1500 MHz, 46 dB gain at 200 MHz, T_N=7 K) obtained from the Weinreb group at Caltech was installed on the 3 K stage to amplify the reflected RF signal coming out of the fridge. This amplifier was found to be exceptionally good at low temperatures compared to commercially available amplifiers, both in terms of gain and heat dissipation. The noise temperature and gain of the

CITLF1 up to 10 GHz measured at 18 K by the Weinreb group are shown in Figure 3.12. Similar home-made low-noise amplifiers (LNAs) were prepared based on the approach of S. Weinreb et al. [83]. The gain of such a home-made LNA is shown in Figure 3.13 at room temperature (red) and 77 K (black). Although the home-made LNAs had a similar performance, the CITLF1 was used as the primary mean of amplification.

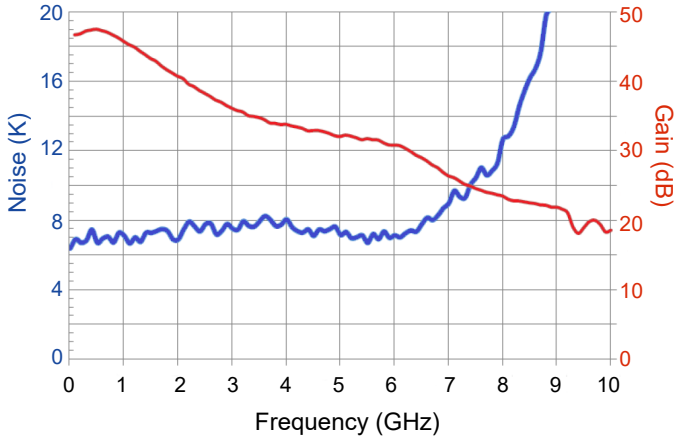

FIGURE 3.12: The noise temperature and gain of the CITLF1 low-noise amplifier measured at 18 K for up to 10 GHz. *Adapted from Ref* [84].

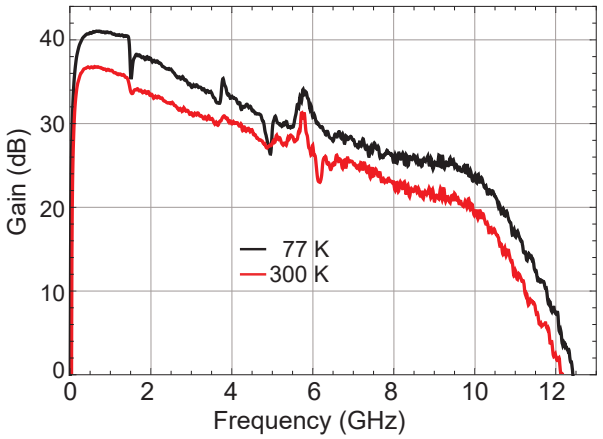

FIGURE 3.13: The gain of a home-made low-noise amplifier measured at room temperature (red) and 77 K (black). The amplifier was made based on the approach of S. Weinreb et al. [83].

Finally, another two high-frequency lines were installed to allow for microwave signals and pulses on either plunger gate of a double quantum dot device. The lines include attenuators of -20, -10 and -3 dB at 3 K, 0.85 K and 6 mK, respectively. Since plunger gates are usually used to apply DC voltages in combination with high-frequency signals, the microwave lines are connected to the sample holder via high-frequency bias-tees (Anritsu K251, 50 kHz - 40 GHz operation range).

3.2.3 PCB and Sample Holder

A custom PCB and sample holder were designed to accommodate devices using DipTrace and SolidWorks, respectively. The PCB allows for a micro-D Cinch connector, three SMP connectors for high-frequency signals, a resonant circuit, a bias-tee and 24 DC lines that are filtered by on-board *RC* filters. The PCB is made of RO4003C, which is suitable for high-frequency applications [85], and it has a thickness of 0.5 mm. All high-frequency lines on the PCB are impedance matched to 50 Ω. The copper electrical pathways of the PCB are 150 µm wide, 35µm thick and have 2.5 µm of silver finish. An image of the PCB mounted into the sample holder is shown in Figure 3.14.

The *RC* filters on the PCB were selected such that they follow the trend of the filters on the previous stages. A cut-off frequency of 34 kHz was chosen (R=1 kΩ, C=4.7 nF). The PCB has a bias-tee (R=1 kΩ, C=100 pF, L=470 nH) that allows for a source-drain bias and an RF signal to be applied on the same lead. For the RF resonant circuit, an inductor of L=330 nH is in series with the source lead, while the parasitic capacitance C_p of the device and the PCB acts as the resonant circuit capacitor. Attempts were made to minimise C_p to improve the quality factor Q. Since $Q \propto \sqrt{L/C_p}$, reducing the parasitic capacitance increases the quality factor of the resonant circuit and thus the signal-to-noise ratio. Inductors with minimum stray capacitance at RF frequencies were chosen and the ground plane underneath and around the resonant circuit was milled away. Further techniques for minimising the parasitic capacitance are outlined in Appendix A.2.2. The PCB shown in Figure 3.14 was later revised to accommodate varactors (see Chapter 4), with the lowest parasitic capacitance achieved being 0.26 pF (without a device).

The sample holder and the lid were made of brass (oxygen-free copper is also a good, but more expensive option). The holder was made such that it allows for pieces of Eccosorb to be added inside the bottom cavities. The sample holder and the lid are shown in Figure 3.15.

The part numbers of the surface mount components used in the setup are listed below:

- resistor 1 kΩ: Susumu RR0816P-102-B-T5
- inductor 330 nH: Coilcraft 0805CS-331
- inductor 470 nH: Coilcraft 0805CS-471
- capacitor 100 pF: Kemet C0805C101JCGAC7800
- capacitor 1 nF: Kemet C0603C102J2GACAUTO
- capacitor 3.3 nF: Murata GCM1885C1H332JA16D
- capacitor 4.7 nF: Kemet C0603C472K1GECAUTO

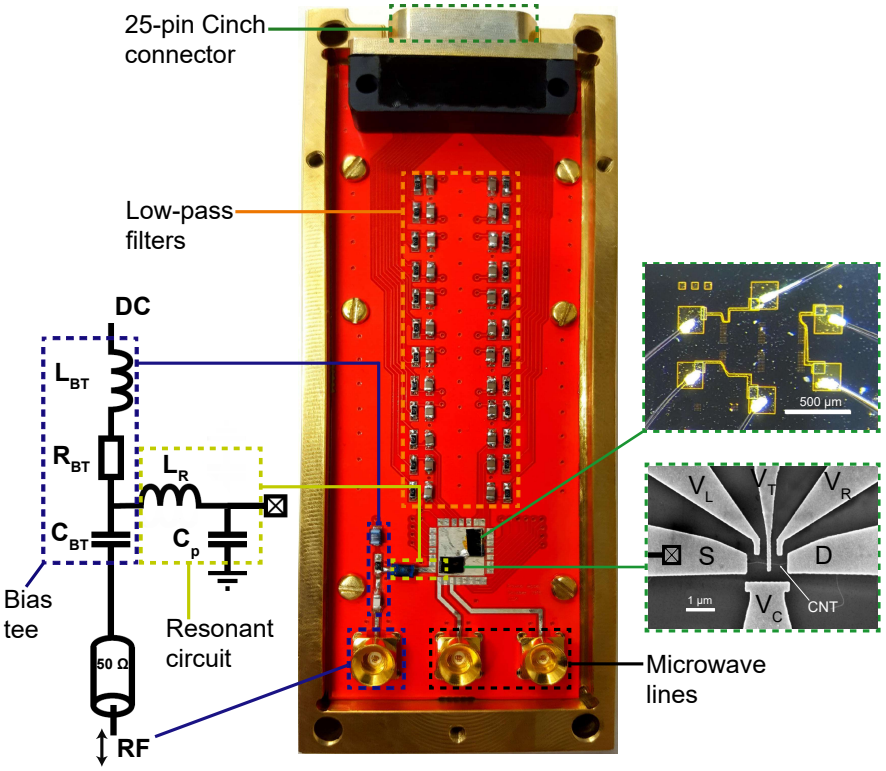

FIGURE 3.14: The PCB and sample holder designed for experiments, with all components attached and some bonded devices.

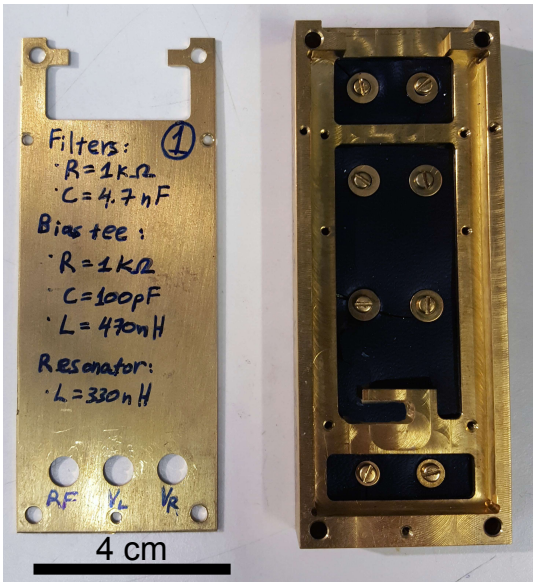

FIGURE 3.15: The sample holder and the lid used to house the PCB. Pieces of Eccosorb were put inside the holder cavities. Both the holder and the lid are made of brass.

3.3 Minimising Electron Temperatures

3.3.1 Introduction

In transport experiments, although the dilution refrigerator is at base temperature, the electronic temperatures are often elevated. This occurs mainly for two reasons: a) at low temperatures the electron-phonon interaction is suppressed, therefore electrons cannot cool further by interactions with the lattice, b) dissipative heating and interactions with the environment, such as high-frequency signals and vibrations, heat up transport electrons [77, 78]. It is generally safe to assume that the electron and phonon temperatures are the same for lattice temperatures of 1 K or higher, but the two begin to deviate at lower temperatures. Actions can be taken to minimise heating of electrons from the electromagnetic noise of the environment. This is achieved with multi-stage DC filtering, ranging from room temperature to base temperature. Details about the filtering configuration related to this thesis are given in Section 3.2.1. The electron temperature can be measured with a quantum dot device, and such measurements are outlined in the next section, each with different filtering setup and device.

3.3.2 Measuring the Electron Temperature

There are several ways to measure the electron temperature of a quantum dot [78]. The way discussed here is about evaluating the width of the Fermi-Dirac function at a lattice temperature T_{bath}. For a source-drain bias $|e|V_{sd} < k_B T_{bath}$ and assuming single energy level tunneling, the width of an isolated Coulomb peak relates to the electron temperature T_e as:

$$\text{FWHM[eV]} = \frac{3.52}{\alpha} k_B T_e \tag{3.1}$$

where FWHM is the full-width at half-maximum of the peak and α is the lever arm. Calculating T_e gives an upper bound to the electron temperature, as the FWHM is determined by the temperature broadening of the Fermi-Dirac function that describes the electron occupation of the leads [78, 86–88]. It was shown by C. Beenakker [89] that such a charge transition is described by:

$$I(\Delta V_g) = I_h \cosh^{-2}\left(\frac{-e\alpha\Delta V_g}{2.5 k_B T_e}\right) + I_0 \tag{3.2}$$

where I_h and I_0 are the step height current and offset current, respectively, and ΔV_g is the gate voltage range across which a peak occurs (centred around zero). The electron temperature can be extracted by fitting a Coulomb peak with Equation 3.2, assuming the tunneling rates are sufficiently small (the dot must be weakly coupled to the leads),

so that the peak is not dominated by lifetime broadening[4]. If the quantum dot is very conductive, such that $h\Gamma \gg k_B T$, where Γ is the tunnel rate, then the charge transition is better described by a Breit-Wigner fit [89].

The electron temperature can be measured with the method described above with relative ease for a quantum dot, since electron tunneling only involves a single energy level. However, when the electron temperature is very low ($\lesssim$50 mK), using the aforementioned method might not be trivial. This is mainly because the thermal broadening of the leads is so small that for $|e|V_{sd} < k_B T_{bath}$ almost no current is observed and the signal-to-noise ratio is too low for a reliable fit. The way around this, is to fit a Fermi-Dirac distribution function at the sides of a peak at larger bias, $|e|V_{sd} \gg k_B T_{bath}$. Such a fit is given below and it is discussed in detail by D. Maradan et al. [77]:

$$I(\Delta V_g) = I_h \left[\exp\left(\frac{\alpha e \Delta V_g}{k_B T_e}\right) + 1\right]^{-1} + I_0 \tag{3.3}$$

where the parameters are the same as described in Equation 3.2.

Prior to introducing any filtering, a narrow-gap carbon nanotube quantum dot was used to measure the electron temperature. The dot was fabricated on degenerately doped silicon, which was used as a back gate. The lever arm was extracted from the corresponding Coulomb diamonds, shown in Figure 3.16. Using Equation 3.2, a curve fit was obtained for the corresponding Coulomb peak with $V_{sd} \approx$1 µV, as shown in Figure 3.17. The electron temperature was found to be relatively high (T_e=370±20 mK) when compared to the lattice temperature $T_{bath} <$ 10 mK. The absence of any kind of DC filtering was assumed to be the main reason.

To reduce the electron temperature, a series of DC filters were introduced at different stages in the dilution refrigerator to attenuate electromagnetic noise (mainly coming from electronic equipment), that could contribute to the heating of transport electrons. At first, capacitor-input filters and low-pass filters were introduced at room temperature and base temperature, respectively, and a narrow-gap carbon nanotube double quantum dot was used to remeasure the electron temperature. The double dot was fabricated on degenerately doped silicon, which was used as the back gate. The geometry of such a double dot device is shown in Figure 3.1(a). The lever arm was extracted by measuring the conductance as a function of source-drain bias and left plunger gate, with the other gates fixed. Similarly, a Coulomb peak was obtained by sweeping the left plunger gate with $V_{sd} \approx$1 µV and the other gates fixed, to ensure single level tunneling. The electron temperature was extracted from the curve fit shown in Figure 3.18. Clearly, the filters contribute to the reduction of the electron temperature, since it was decreased to 90±10

[4]If the dot is strongly coupled to the leads, electrons spend less time on the dot, which results in broadening of the peak width arising from uncertainties in energy, $\Delta E \sim \hbar/\Delta t$.

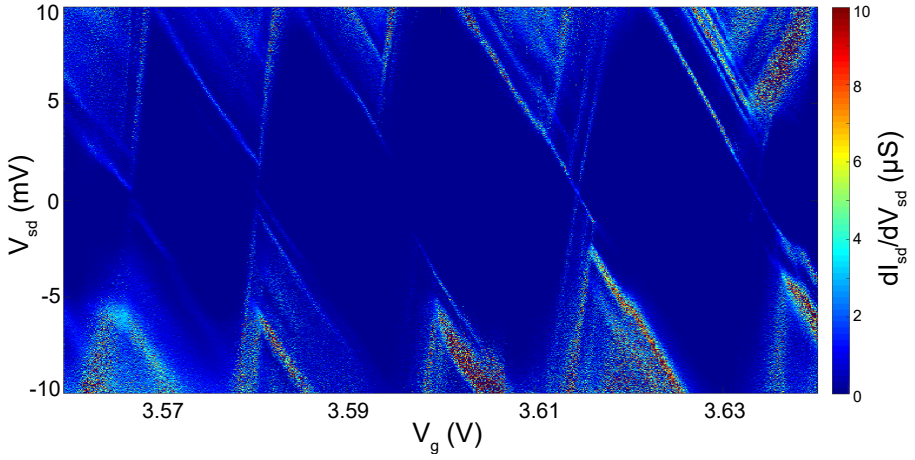

FIGURE 3.16: A Coulomb diamond plot showing the differential conductance of a narrow-gap carbon nanotube quantum dot as a function of source-drain bias V_{sd} and gate voltage V_g. No current flows inside the diamonds.

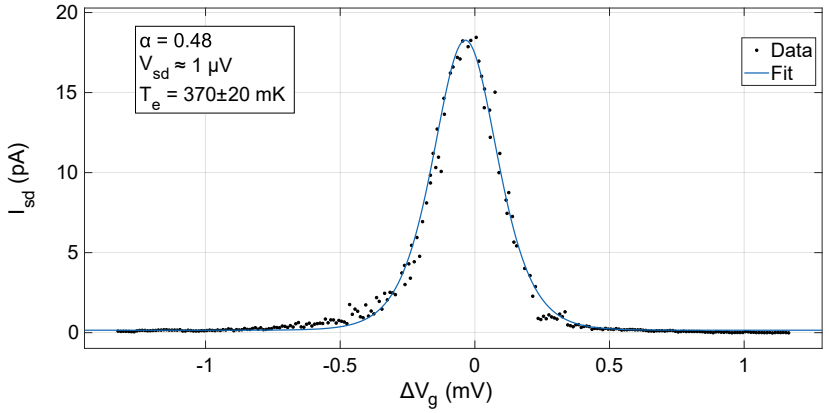

FIGURE 3.17: An isolated Coulomb peak of a narrow-gap carbon nanotube quantum dot measured with V_{sd} ≈1 μV and fitted with Equation 3.2. The fit yields an electron temperature of about 320 mK.

mK (about 4 times lower than before). At this point, it was safe to assume that most of the improvement was due to the filters on the mixing chamber, since they were much closer to the device.

The base temperature of the refrigerator is about 10 times lower than the electron temperature obtained above, and since there was room for improvement, more filters had to be introduced. The final set of filters included copper-powder filters at 3 K and low-pass filters on the PCB close to the device. A semiconducting nanotube quantum dot on degenerately doped silicon was used to remeasure the electron temperature for the final filtering configuration. For $|e|V_{sd} < k_B T_{bath}$, Coulomb peaks were too small and

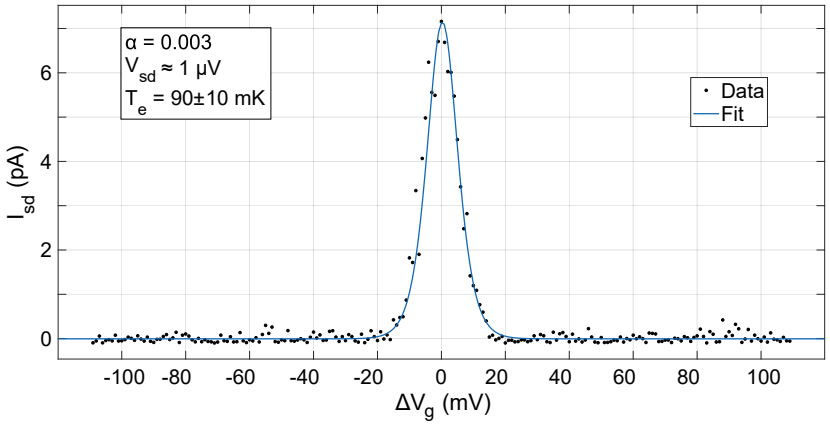

FIGURE 3.18: An isolated Coulomb peak of a narrow-gap carbon nanotube double quantum dot measured with V_{sd} ≈1 μV and fitted with Equation 3.2. The fit yields an electron temperature of about 90 mK.

comparable to the noise level of the measurement[5] for reliable fits, suggesting that the thermal broadening of the leads was very small. For reliable measurements, the electron temperature was extracted from a peak measured with V_{sd}=230 μV, as shown in Figure 3.19. Plateaus on the peak indicate excited state transport, while the edges between plateaus are thermally broadened and described by a Fermi-Dirac function that takes the form of Equation 3.3. The electron temperature was extracted by fitting to the steepest edge of the peak, circled in Figure 3.19. The edge can be broadened by the tunnel coupling to the leads, but the thermal broadening cannot be larger than the steepest edge. Therefore, the steepest edge gives an upper bound for the thermal broadening, and as a consequence, an upper bound for the electron temperature. The value for the lever arm was calculated from the width of the peak (indicated as δV_g in Figure 3.19), but also reproduced independently from its corresponding Coulomb diamond, shown in the inset. Fitting Equation 3.3 to the steepest edge of the peak yields an electron temperature of 13±2 mK, which is a factor of 2 higher than the lattice temperature and about 7 times lower than the previous filtering configuration. The fit is shown in Figure 3.20. A summary of the electron temperatures measured for different filtering stages is concluded in Table 3.1.

To check the reliability of the electron temperature, a series of measurements with V_{sd}=230 μV were performed at elevated lattice temperatures. The deviation of the electron temperature from the lattice temperature begins around 20 mK. The electron temperature plateaus at 6 and 10 mK, suggesting that it saturates below 20 mK. The electron temperature plotted as a function of lattice temperature is shown in Figure 3.21. For the data in the latter figure, a lever arm was extracted as a fitting parameter

[5]The noise level of DC measurements (probably dominated by the noise of the voltage source and data acquisition instruments) was about 0.15 pA.

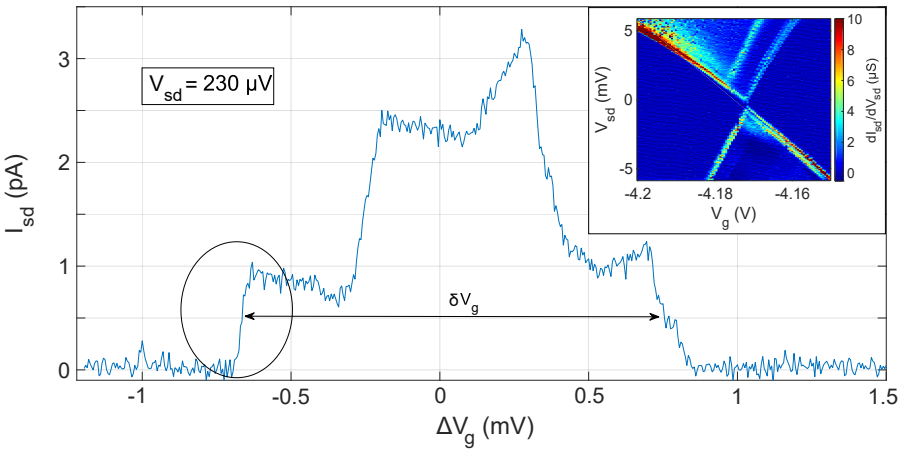

FIGURE 3.19: A Coulomb peak of a semiconducting carbon nanotube quantum dot measured with V_{sd}=230 µV. The steepest edge used to extract the electron temperature is circled and the gate range used to obtain the lever arm is shown as δV_g. Inset: the Coulomb diamond of the corresponding peak, used to verify the value of the lever arm.

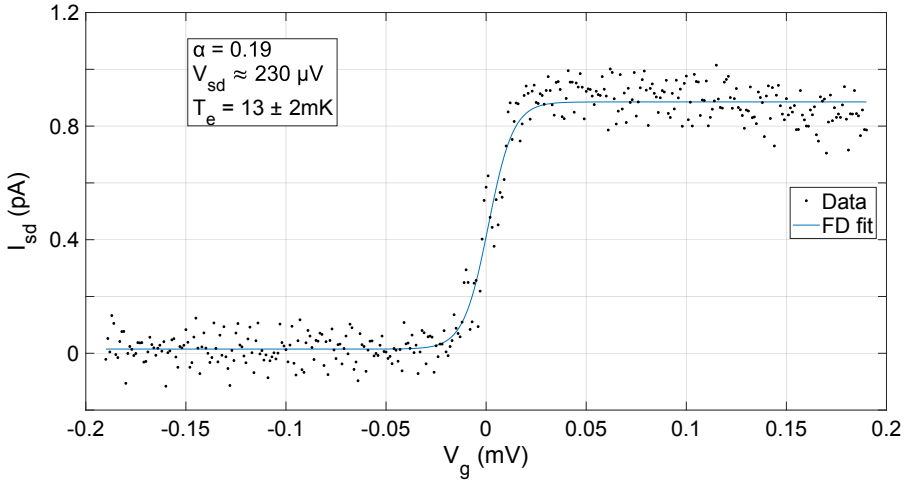

FIGURE 3.20: The circled edge of Figure 3.19 fitted with a Fermi-Dirac distribution function. The fit yields an electron temperature of about 13 mK.

at 160 mK, where it was assumed that $T_e = T_{bath}$. The lever arm was then used to obtain the electron temperatures at lower lattice temperatures.

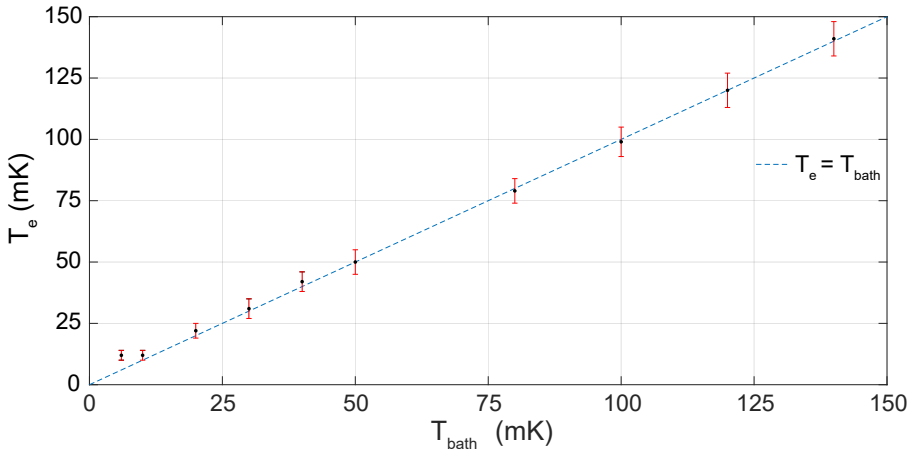

FIGURE 3.21: The electron temperature measured as a function of lattice (mixing chamber) temperature. The former appears to plateau below 20 mK.

Filtering	Electron Temperature (mK)
No filters	370±20
Pi (300 K), RL/RC (MXC - 6 mK)	90±10
Pi (300 K), copper-powder (3 K) RL/RC (MXC - 6mK), RC (PCB - 6mK)	13±2

TABLE 3.1: Electron temperatures obtained for each DC filtering configuration.

3.4 Radio-Frequency Reflectometry

3.4.1 Introduction

For advances in quantum computation, a mechanism for quantum state readout is of high significance. The quantum state of an electronic device needs to be measured fast, with high fidelity and sensitivity. Conventional charge or spin state single-shot readouts for quantum dots require some kind of mesoscopic detector, with the most common probably being the quantum point contact [71, 90, 91]. However, the introduction of such a detector adds to the physical complexity of the device and it is often non-trivial. Radio-frequency (RF) reflectometry is a non-invasive technique that maps the quantum state of interest to an electrical impedance and allows for high sensitivity and high fidelity measurements. It eliminates the need for a separate mesoscopic detector or any additional device components devoted to sensing [43, 69, 92, 93]. The technique has gained lots of interest over the last few years, at first as a hybrid technology of radio-frequency quantum point contact (RF-QPC) [94, 95], and then as a more independent way for charge detection in a variety of quantum dot systems [43, 69, 86, 96–99]. Radio-frequency reflectometry has demonstrated rapid and sensitive readout of charge [34, 65, 94, 95, 100] and spin states [73, 101], while the measurement sensitivity can even

approach the quantum limit under the appropriate conditions [102]. The principles behind RF reflectometry is outlined below.

3.4.2 Basic Principles

For RF reflectometry, we consider the *RLC* circuit shown in Figure 3.22. The circuit consists of a parasitic capacitance C_p, an inductor L and a resistor R, which accounts for the resistances in the wiring and the inductor. A quantum dot device is modelled as an effective capacitor C_{eff} and effective resistor R_{eff} in parallel, as shown. The resonant frequency of the circuit is given by $f_0 = \frac{1}{2\pi\sqrt{LC_\Sigma}}$ [103]. Here, C_Σ is the total capacitance of the system, that consists of parasitic capacitances and the state-dependent capacitance of the device, such that $C_\Sigma = C_p + C_{eff}$ [6, 86]. The parasitic capacitances arise from the parallel-plate capacitor formed by the bond pads and the substrate, as well as parasitics from the PCB. The state-dependent capacitance is affected by the charge carrier distribution across the dots, and a change in that distribution will shift C_Σ, and as a consequence, f_0. Thus, detecting changes in f_0 reveals information about tunneling events. For quantum dot devices, the principle is that C_Σ depends on the ability of charge carriers to tunnel on and off the dots, and that ability depends on the electrochemical potential of the dots, which in turn can be tuned by the gate electrodes. Therefore, a charge stability diagram can be measured not only in DC, but also in terms of reflected amplitude and phase by coupling the source lead of the device to the RF circuit [43]. Reflectometry measurements are presented in Chapters 4 and 5 for single and double quantum dots, respectively. In addition, Appendix B demonstrates how RF reflectometry can be used to perform capacitance spectroscopy of molecules using a simple device geometry.

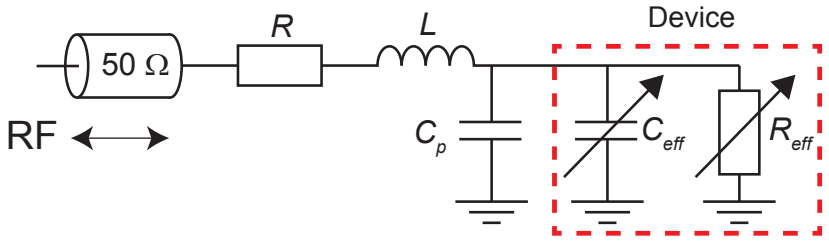

FIGURE 3.22: Schematic model of the *RLC* circuit adapted for RF reflectometry measurements. A quantum dot device is modelled as a capacitor C_{eff} and resistor R_{eff} in parallel, allowing for the entire system to be treated as a simple tank circuit.

One of the main factors that affect the measurement sensitivity is the quality factor Q. The signal-to-noise ratio (SNR) depends on Q, which for a series *RLC* circuit is given by $Q = \frac{1}{Z}\sqrt{L/C_\Sigma}$, where Z is the impedance of the circuit [103]. Therefore, high

Q-factors are preferred in order to maximise the detection sensitivity. Undoped silicon substrates result in higher Q-factors when compared to doped silicon, since the parasitic capacitance is lower. Therefore, to increase the Q-factor of the resonant circuit (for a fixed inductor), the parasitic capacitance should be minimised. Initial experiments carried out with an inductor of 330 nH suggested typical values of C_Σ for devices on doped and undoped silicon to be 2.5 pF ($f_0 \approx 175$ MHz, $Q \approx 8$) and 0.7 pF ($f_0 \approx 320$ MHz, $Q \approx 20$), respectively. The phase response $\phi(f)$, as a function of frequency f, can be fitted with the following equation to extract a value for Q [86]:

$$\phi(f) = 2\arctan\left[2Q(1 - f/f_0)\right] + \phi_0 \tag{3.4}$$

where ϕ_0 is a phase offset. The phase response around resonance for devices on doped and undoped silicon is shown in Figures 3.23(a) and (b), respectively, with corresponding fits. Early measurements suggested that the quality factors were relatively low. The large parasitic capacitance was taken to be the main reason for the poor quality factors and attempts were made to minimise it (see Appendix A.2.2 for more details).

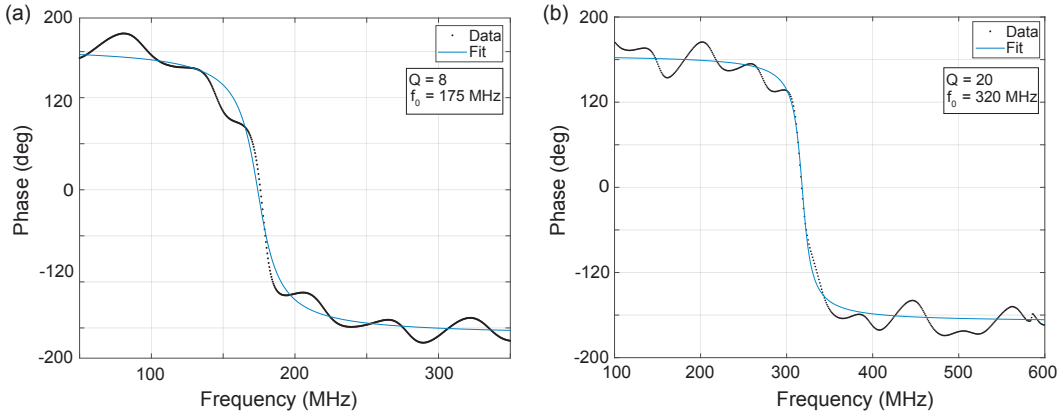

FIGURE 3.23: A 2π phase shift around a resonance of (a) 175 MHz and (b) 320 MHz for a device on doped and undoped silicon, respectively. The value of Q was extracted by fitting Equation 3.4 to the data, as shown.

At room temperature, it is often difficult to observe the resonance of a quantum dot circuit, especially if the quality factor is low. As the system cools down, dopants in the substrate freeze out and the parasitic capacitance decreases. This results in a shift of f_0 to higher frequencies, which is more profound for devices on undoped silicon. The data in Figure 3.24 shows how the resonant frequency of a carbon nanotube double quantum dot on undoped silicon shifts during cool down from 302 to 320 MHz. This change corresponds to about 0.1 pF decrease of the parasitic capacitance from 0.8 to 0.7 pF.

When performing RF reflectometry measurements, it is essential that the RF power delivered to the device is optimum. A high RF power results in a higher SNR, but it can

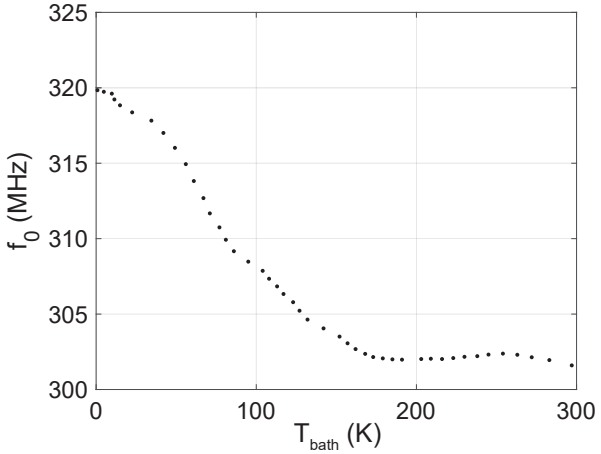

FIGURE 3.24: The resonant frequency of a carbon nanotube double quantum dot on undoped silicon as a function of lattice temperature during cool down. The frequency changes from 302 to 320 MHz, corresponding to a 0.1 pF decrease of the parasitic capacitance from 0.8 to 0.7 pF.

cause thermal broadening of the Coulomb peaks, smearing out sharp charge transitions. A low RF power does not cause thermal broadening, however it compromises the SNR. Therefore, the optimum RF power is one that gives the highest SNR without causing any thermal broadening. Although the exact power differs between different devices and quality factors, for the presented setup the ideal value would typically lie within the range of -105 to -95 dBm. A demonstration is shown in Figure 3.25, where the electron temperature T_e is plotted as a function of RF power at base temperature. It is apparent from the data that T_e is well below 20 mK for RF powers of -95 dBm or lower, while heating occurs for higher powers. The measurements were performed on a narrow-gap carbon nanotube quantum dot on doped silicon.

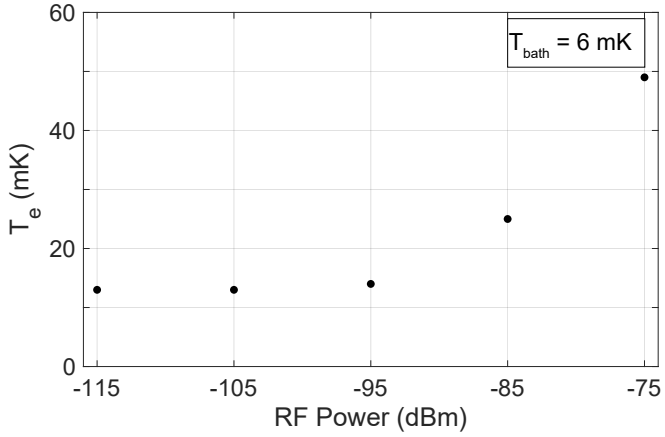

FIGURE 3.25: The electron temperature as a function of RF power measured at base temperature with a narrow-gap carbon nanotube quantum dot. For powers higher than -95 dBm, heating causes the electron temperature to rise.

Chapter 4

Impedance Matching and Frequency Tuning using Strontium Titanate Varactors

Parts of this chapter have been submitted in the journal "Nature Electronics" as:

P. Apostolidis, B. J. Villis, J. Chittock-Wood, A. Baumgartner, and M. R. Buitelaar
"Quantum paraelectric varactors for radio-frequency measurements
at mK temperatures"

Techniques or parts of techniques outlined in this chapter are subjects to patenting.

4.1 Introduction

As discussed in Section 3.4, radio-frequency reflectometry is an important aspect in the field of quantum computation, as it can be used for fast electrical readout of qubits hosted in quantum dots coupled to resonant circuits. However, readout is often hindered by impedance mismatch between the RF line and the quantum system of interest. To maximise sensitivity and power transfer between the external circuitry (RF source) and the quantum system, the two must be impedance matched [104, 105]. This requirement is made more challenging due to the varying resistances and parasitic capacitances among different devices. Therefore, it is difficult to achieve a perfect impedance match by mere selection of tank circuit components, especially over an ensemble of devices. In addition to impedance matching, the ability to tune the resonant frequency of the system is also of importance. For example, resonance tuning is essential for achieving optimum

performance when amplifiers of narrow operation bandwidth [106, 107] are used, or when signal multiplexing of several readout channels is required [108].

The need for impedance matching and frequency tuning has been addressed by using voltage-tunable variable capacitors (varactors). Such varactors allow for in situ tunability of radio-frequency reflectometry measurements [109, 110]. However, free carriers in conventional varactor diodes tend to freeze out at low temperatures, making them unreliable below 1 K or completely unusable at mK temperatures where solid-state quantum devices usually operate [111–113]. This issue puts significant limitations on the operating temperature range of such systems. In this chapter, we present a novel approach that can be used to achieve in situ perfect impedance matching and frequency tuning at temperatures down to 6 mK. Our technique involves custom-made varactors based on the quantum paraelectric material strontium titanate. Such varactors reliably work at low temperatures, are easily tunable, show no leaks or any magnetic field dependence, and operate over a large frequency range. Furthermore, our approach allows for easy design changes to tailor a collection of varactors for various experiments, without the addition of significant complexity to the circuit architecture.

4.2 Strontium Titanate as a Varactor

Strontium titanate ($SrTiO_3$ or STO) is a non-magnetic quantum paraelectric material that belongs to the class of incipient ferroelectrics, in which an electrically ordered state is suppressed by quantum fluctuations. Its most important property that relates to the work presented here, is the fact that its relative permittivity (or dielectric constant) changes when an electric field is applied to the material. This change is more apparent at temperatures below 25 K. The relative permittivity as a function of temperature for various electric fields is shown in Figure 4.1. Typically, strontium titanate has a permittivity of $\sim$30 at room temperature, which increases to $\sim 10^4$ below 4 K [114–120].

In addition to the tunability of its relative permittivity, strontium titanate performs relatively well in terms of low dielectric losses, thermal stability and low leakage current [121]. This material was used to make varactors, which are the basis of the work presented in this chapter.

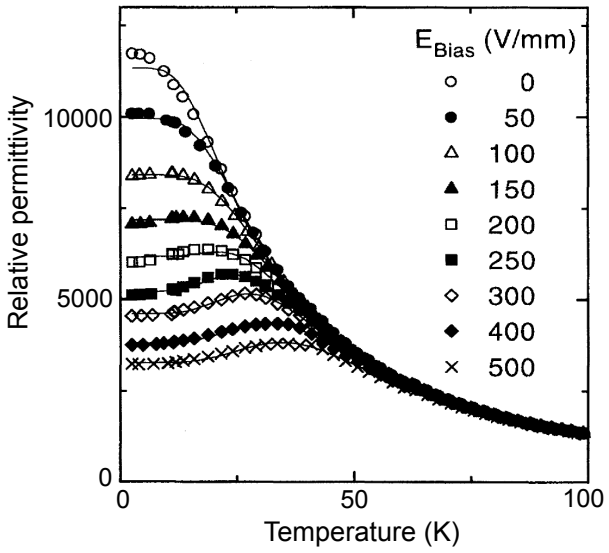

FIGURE 4.1: The relative permittivity of strontium titanate as a function of temperature for various electric fields. *Adapted from Ref* [120].

4.2.1 Varactor Fabrication

A strontium titanate substrate (TiO_2-terminated, single-crystal (001), single-side polished, purchased from SurfaceNet) of thickness d=0.5 mm was used to form two parallel plate capacitors by fully metallising the bottom and implementing metallic square pads on the top. The fabrication steps are outlined below[1]:

1. **Preparation** - The substrate was cut using a diamond wire saw into approximately 3×3 mm pieces. For cleaning, the pieces were sonicated 5 minutes in acetone followed by 5 minutes in IPA.

2. **Metal Evaporation (back side)** - The substrate was loaded in an electron beam evaporator with the unpolished side facing down. A thin layer of titanium (5 nm) was evaporated for adhesion, followed by a layer of gold (60 nm).

3. **Photolithography** - The polished side of the STO substrate was coated with a double layer of photoresist. The first layer was MicroChem LOR10B photoresist (required for successful lift-off after metal evaporation), spun at 4000 rpm (thickness of about 1 µm) and baked at 190 °C for 10 minutes. The second layer was Microposit S1805 photoresist, spun at 4000 rpm (thickness of about 0.5 µm) and baked at 115 °C for 1 minute. A quartz-chrome photomask was used to expose square pads of area 120 μm^2 on the photoresist (exposure time 1.4 s, UV light

[1]We thank Dr. Pavlo Zubko for providing the STO substrates and Marios Hadjimichael for his help with photolithography.

intensity 15 mW/cm^2 at 365 nm). The substrate was developed in Megaposit MF-26A for 45 seconds.

4. **Metal Evaporation (top side)** - The substrate was again loaded in an electron beam evaporator with the photoresist coated side facing down. A thin layer of titanium (5 nm) was evaporated for adhesion, followed by a layer of gold (60 nm). The substrate was sonicated in Microposit Remover 1165 in a heat bath at 80 °C for lift off.

The bottom side of the STO is adhered on the RF line of the PCB using silver paste and annealed at 120 °C for 5 minutes for better conductance. The square pads are bonded on the PCB with gold wire. A schematic of the STO substrate with the two varactors is shown in Figure 4.2. Here, C_m and C_f denote the capacitances of each capacitor, and V_m and V_f are their corresponding bias voltages. The letters m and f stand for "matching" and "frequency", respectively. The voltages are applied via bias tees (R=1 kΩ, C=100 pF, L=470 nH) through filtered wires with a bandwidth of about 4 kHz (see Section 3.2.1 for details on DC filtering).

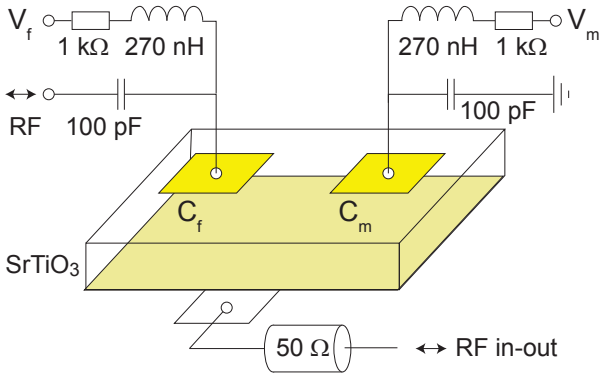

FIGURE 4.2: A schematic of a strontium titanate substrate used to define two parallel plate varactors C_m and C_f. The varactors are biased with voltages V_m and V_f via the bias-tees shown. RF signals are applied to the bottom of the substrate.

To minimise cross-capacitance between the two varactors, the pads used to define them were about 1.5 mm far from each other, but not too close to the edge of the substrate[2]. The capacitance C of each pad was measured using a capacitance bridge at room temperature and found to be about 1 pF. This is generally much larger than one would expect from the typical parallel-plate capacitor model: $C = \epsilon_r \epsilon_0 A/d \approx 8$ fF, where ϵ_0=8.85×10^{-12} F/m is the permittivity of free space [122], $\epsilon_r \approx 30$ is the STO dielectric constant at room temperature [114, 115], A is the surface area of the pad and d is the

[2]To reduce any possible cross-capacitance effects even more, two different STO substrates can be used, one accommodating each varactor (this increases the PCB complexity though).

substrate thickness. This discrepancy mainly arises from fringing effects, which increase the capacitance when $d > \sqrt{A}$ [123].

The PCB design of Figure 3.14 was modified accordingly to accommodate an STO substrate and allow for varactor usage. The new design adapted the same material and thickness, with adjustments made to minimise parasitic capacitances (see Appendix A.2.2 for more details). Two of the DC lines on the PCB were used to bias the two varactors, and a bias-tee was introduced on each line, as shown in Figure 4.2. The revised PCB is shown in Figure 4.3, where an STO substrate and quantum dot device on silicon are mounted. A schematic of the corresponding RF circuit is shown in Figure 4.4. From the schematic, C_m and C_f are the capacitances of the two STO varactors responsible for impedance matching and frequency tuning, respectively. The effective resistances R_m and R_f are used to parametrise the parasitic losses associated with each varactor. The component L is an on-chip inductor. To carry out reflectometry measurements, a radio-frequency signal with frequency f_c is injected in the high-frequency setup and directed towards the quantum dot via a directional coupler. The reflected signal S_{21} is amplified by a low-noise cryogenic amplifier and measured using a network analyser. The high-frequency components of the setup are discussed in Section 3.2.2 in more detail.

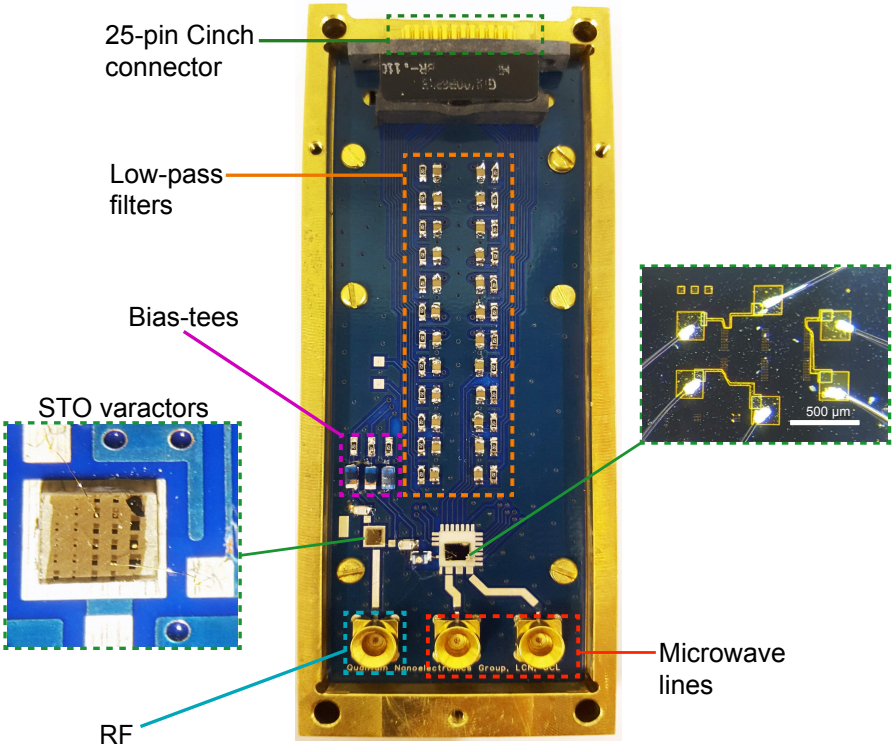

FIGURE 4.3: The revised PCB that allows usage of STO varactors for impedance matching and frequency tuning. The new design was based on the original design of Figure 3.14.

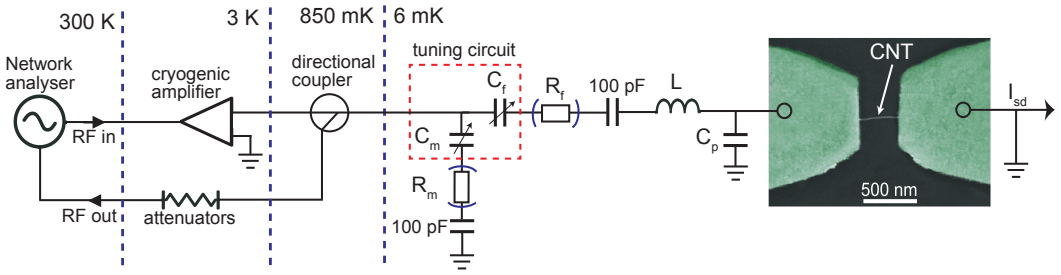

FIGURE 4.4: A schematic of the RF circuit with the introduction of voltage-tunable STO varactors C_m and C_f. Parasitic losses in the circuit are parametrised by the effective resistances R_m and R_f. The device attached on the circuit is a narrow-gap carbon nanotube quantum dot on doped silicon.

4.3 Impedance Matching and Frequency Tuning

This section demonstrates perfect impedance matching and resonant frequency tuning of a quantum dot device at a lattice temperature of 6 mK. The device under investigation is a narrow-gap carbon nanotube quantum dot on degenerately doped silicon terminated by 280 nm of SiO_2. The dot has a room temperature resistance of R_d=280 kΩ and length 400 nm. The charging energy E_C and energy level spacing ΔE are about 11 meV and 4 meV, respectively. For the measurements presented below, the gate voltages are set such that the dot is pinched-off completely (R_d >1 GΩ).

The reflected amplitude $|\Gamma|$ and phase response Φ were examined as a function of carrier frequency and varactor biases V_m and V_f. The system was also simulated (see Section 4.3.1 for simulation details) to compare with experimental data. Experimental data and simulations for the varactors C_m and C_f are shown in Figures 4.5 and 4.6, respectively. The reflected amplitude and phase measured are shown in (a) and (c), while the corresponding simulated data are shown in (b) and (d) for each Figure. The simulations for C_f are taken to be more reliable compared to those of C_m. This is mainly because of the extra degree of freedom that accompanies the C_f varactor: a change in both the resonant frequency and matching as opposed to a change in matching only for C_m.

In Figure 4.5, the varactor C_m is biased from V_m=-24 to 24 V with V_f=0. The system is perfectly matched at V_m=7.5 V, and that is easy to see in the phase, which switches from under coupled ($Z > Z_0$, $0 \leq \Delta\Phi \leq \pi$) to over coupled ($Z < Z_0$, $\Delta\Phi = 2\pi$) [86]. The fact that the resonance is maintained at 173 MHz throughout the measurement indicates minimum cross-talk between C_m and C_f. This measurement demonstrates that the system can be driven into perfect impedance match by approaching from either under or over coupled regimes, sorely by biasing C_m accordingly.

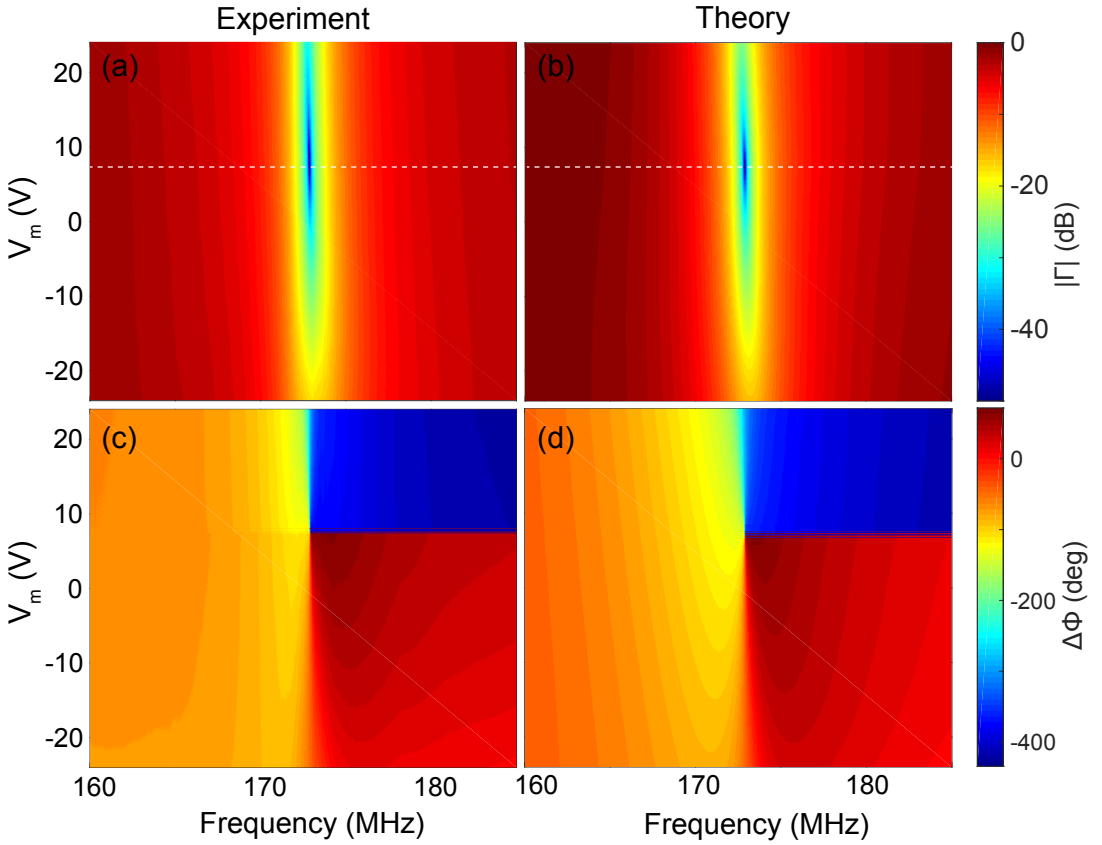

FIGURE 4.5: (a, b) The reflected amplitude $|\Gamma|$ measured and simulated as a function of carrier frequency and varactor bias V_m. (c, d) Similarly, the corresponding phase response Φ as measured and simulated. The system switches from under to over coupled at V_m=7.5 V (the phase response undergoes a 2π phase shift), indicating perfect impedance matching at that voltage. For this data, V_f=0.

Similarly, in Figure 4.6, the varactor C_f is biased from V_f=-24 to 24 V with V_m=0. The resonant frequency shifts with respect to V_f, as indicated. The resonance shifts to lower (higher) frequencies for negative (positive) V_f biases. The plot demonstrates the coherent shifting of the resonant frequency and how impedance matching changes along the way. Here, the system is well-matched around V_f=-10 V and the resonant frequency at V_f=0 is 175 MHz. Deviations from the corresponding data of Figure 4.5 arise mainly because of charge redistribution in the STO substrate which happens when large voltages are applied across it. This changes the "default" values of C_f and C_m at a given V_f and V_m; however, it is not an issue, since the original capacitances can be re-obtained by biasing the varactors accordingly. This behaviour suggests some kind of hysteresis, which is discussed in more detail in Section 4.3.2.

Individual fits at several voltages V_m and V_f are shown in Figure 4.7(a) and (b), respectively. The data and fits are line traces taken from Figures 4.5 and 4.6, as indicated.

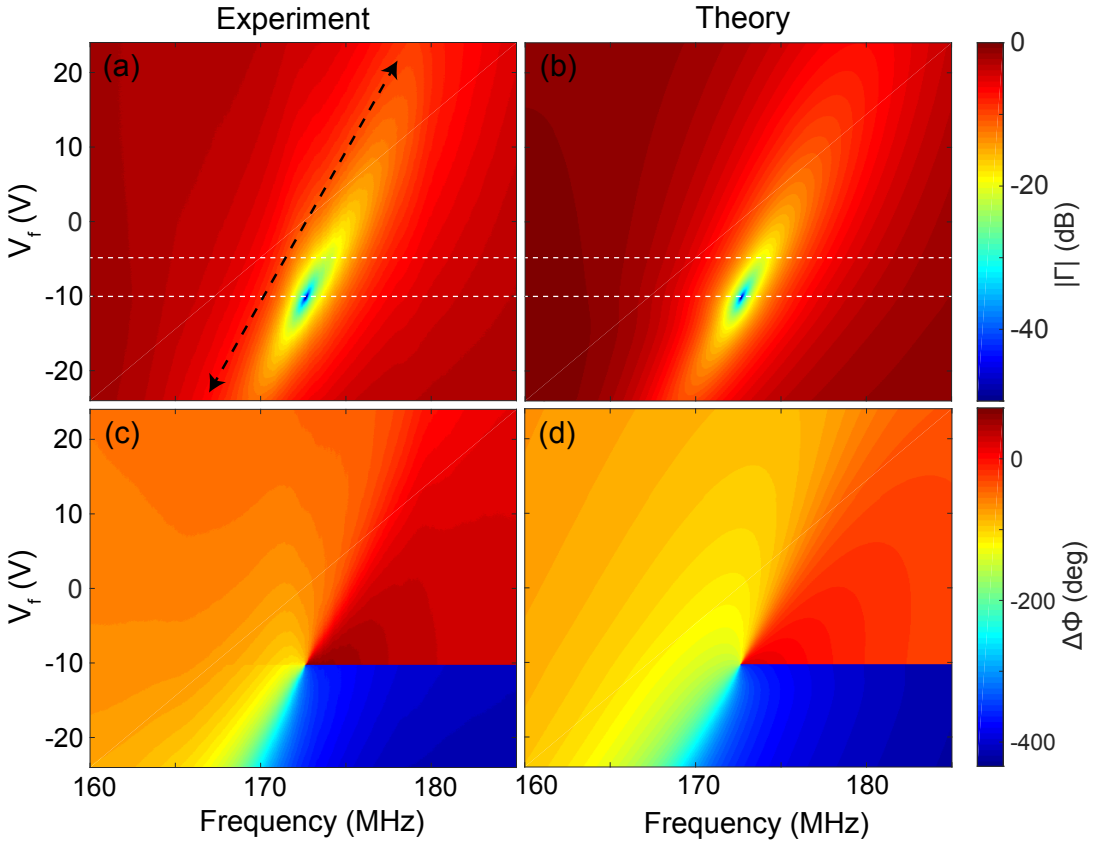

FIGURE 4.6: (a, b) The reflected amplitude |Γ| measured and simulated as a function of carrier frequency and varactor bias V_f. (c, d) Similarly, the corresponding phase response Φ as measured and simulated. The resonance shifts to higher frequencies with respect to V_f, as indicated by the black dashed arrow. The overall frequency shift is about 10 MHz. For this data, V_m=0.

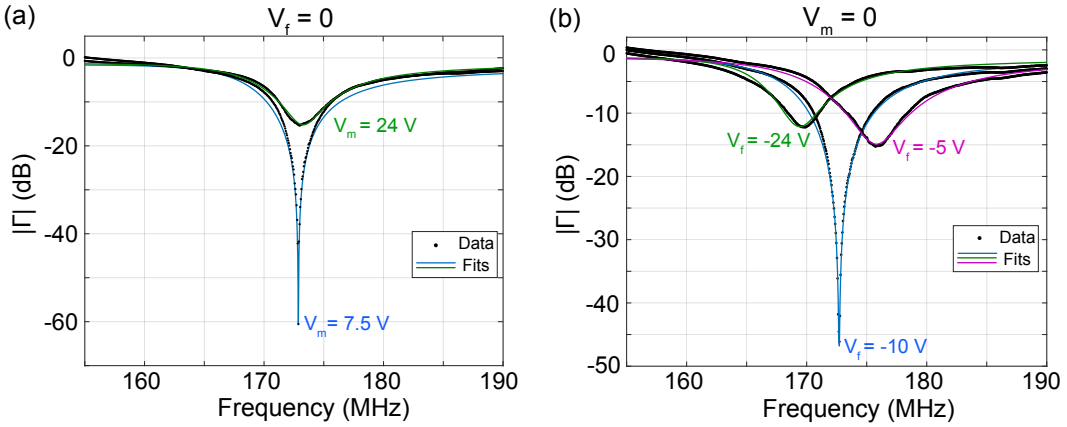

FIGURE 4.7: The reflected amplitude |Γ| and corresponding fits for: (a) V_m=-24 V (green, far from impedance matching) and V_m=7.5 V (blue, perfect impedance matching), (b) V_f=-24 V (green), V_f=-10 V (blue, perfect impedance matching) and V_f=-5 V (purple).

The resonant frequency shift across a larger range is shown in Figure 4.8 for -60< V_f <60 V. The resonance is mostly tunable in the range -30 to 20 V, while its tunability is compromised for more negative voltages. The maximum frequency tunability is calculated from the steepest gradient and yields 0.21 MHz/V.

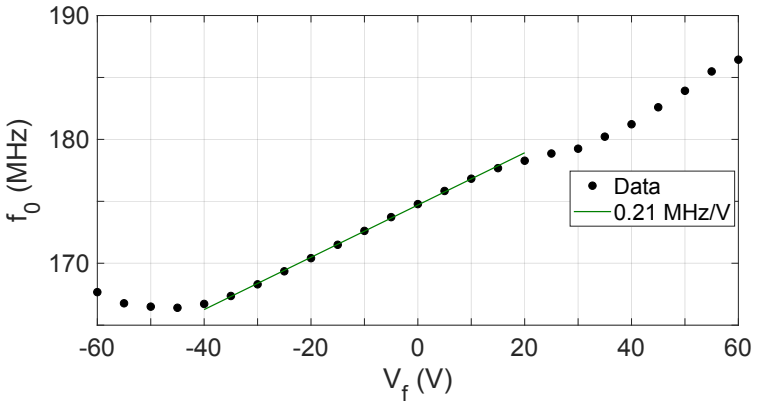

FIGURE 4.8: The resonant frequency f_0 as a function of V_f for a carbon nanotube quantum dot device. The maximum frequency tunability is 0.21 MHz/V. The resonance shifts by about 20 MHz in a range of 100 V.

From the data in Figures 4.5 and 4.6, we extract the response of C_m, C_f, R_m and R_f as a function of the corresponding bias voltage. The response of each varactor is shown in Figure 4.9. The values of C_m and C_f decrease for more positive voltages, while their corresponding effective resistance increases, as expected [117]. For C_m and C_f, a monotonically decreasing capacitance from 59 to 42 pF and 40 to 14 pF is observed, respectively. At the same time, a monotonically increasing effective resistance R_m and R_f, from 0.5 to 4.5 Ω and 3 to 16 Ω is observed, respectively. These effective resistances also include contributions from the chip inductor and circuit board, so they should be considered an upper bound for the varactor losses. A summary of the parameters for each varactor is given in Table 4.1 for V_m=V_f=0, including the quality factor calculated using $Q = \frac{1}{2\pi f C R}$ [103] with f=173 MHz.

These measurements are consistent with the behaviour of strontium titanate at higher temperatures and show that the material retains its characteristic tunability down to mK temperatures. The voltages for which the maximum capacitances are observed are outside the range of the measurements of Figures 4.5 and 4.6. Focusing on the data and simulations for C_f, by increasing the bias voltage to more negative values, a maximum capacitance resulting in the lowest observed resonant frequency f_0 ≈166 MHz is seen at V_f=-45 V (see also Figure 4.8). The maximum capacitance at this point is approximately 52 pF, and using finite-element simulations of the device geometry yields a dielectric constant ϵ_r^{max} = 23 000, which is in good agreement with expectations for strontium titanate [117].

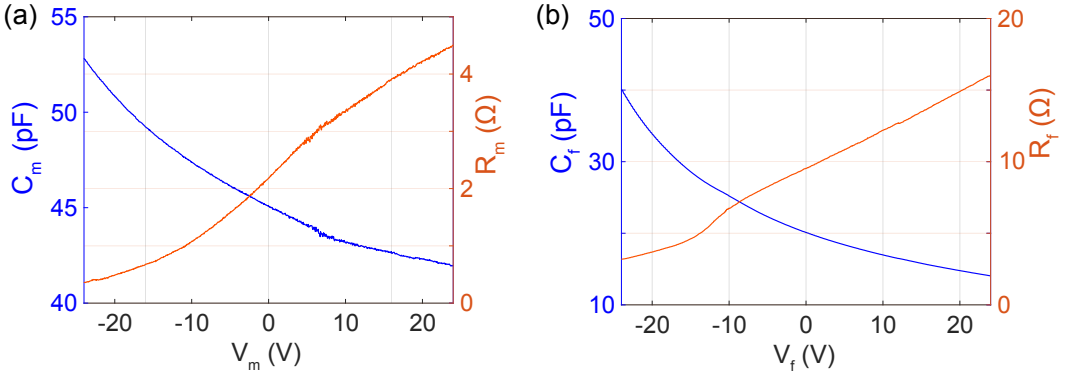

FIGURE 4.9: The response of (a) C_m & R_m, and (b) C_f & R_f as a function of bias voltages V_m and V_f, respectively. The data was extracted from the simulations of Figures 4.5 and 4.6.

Varactor	Intrinsic Capacitance (pF)	Series Effective Resistance (Ω)	Quality Factor	Maximum Tunability (pF/V)
C_m	45.1	2.2	9.3	0.32
C_f	20.1	9.5	4.8	0.15

TABLE 4.1: A summary of the parameters related to the STO varactors C_m and C_f at zero electric field.

The extracted values for the capacitance and effective series resistance also allow for estimation of the dielectric loss tangent of the varactors. The loss tangent is defined as $\tan(\delta)=\epsilon^{''}/\epsilon^{'}$, where $\epsilon^{''}$ and $\epsilon^{'}$ are the imaginary and real part of the relative permittivity [103]. The loss tangent relates to the effective series resistance as $\tan(\delta)=2\pi f R_f C_f$. Since in our experiments we can not distinguish between loss contributions from the STO varactors, the chip inductor and circuit board, it is difficult to provide an exact value for the varactor loss tangent. Nevertheless, using the values of R_f and C_f from Figure 4.9(b), we estimate $\tan(\delta)$ to be in the range of 10^{-1} to 10^{-2} for large negative voltages, where C_f has a maximum. Dissipation in STO has been attributed to the interaction between the oscillating RF electric field and acoustic phonons, where the presence of a large DC electric field breaks the crystal lattice symmetry and introduces a field-dependent dipole moment in the unit cell, making the system more susceptible to RF losses [124]. In single crystals, this results in an increase of the observed loss tangent for larger DC electric fields, which is consistent with our data.

The shift of the maximum capacitance to negative voltages as seen in Figure 4.8 has previously been reported and attributed to trapped charges in the crystal, such as oxygen vacancies [125]. This also gives rise to hysteretic behaviour and a dependence of the capacitance on the voltage sweep history, but it does not affect the device stability. Importantly for device operation, the relaxation processes were of the order of seconds

when the electric field was changed, after which the observed RF response was completely stable. For more details on stability, see Section 4.3.2.

The ability to match the impedance of a quantum dot to the impedance of the RF network has been demonstrated. It was also shown that the resonance of the system can be shifted to lower or higher frequencies. Now, the ability to achieve impedance matching at shifted frequencies is also investigated. Following the data of Figure 4.5, where impedance matching is demonstrated f_0=173 MHz, matching is also achieved for lower and higher frequencies. This is demonstrated in Figure 4.10, where resonances of 167 and 182 MHz are shown without (blue) and with (green) adjustment of C_m. Although the resonance can be tuned further (see Figure 4.8), there exist frequency ranges for which matching can be improved, but no perfect matching can be achieved. This is further discussed in Section 4.3.2.

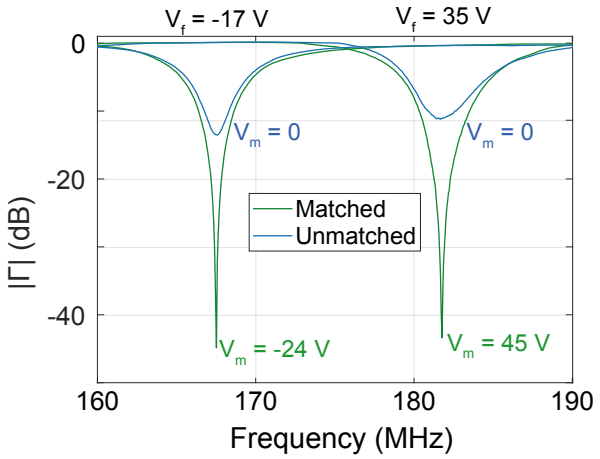

FIGURE 4.10: The reflected amplitude around 167 and 182 MHz, without (blue) and with (green) adjustments for good impedance matching. The corresponding voltages V_m and V_f are indicated.

4.3.1 Simulations

For the simulations of Figures 4.5(b,d) and 4.6(b,d), the circuit model shown in Figure 4.11 was adapted. From the circuit, the varactors C_m and C_f are taken as lumped elements. The inductors of the circuit are modelled as a network of elements (L, R_L, R_c, C_L), which simulate self-resonances and parasitic losses. Other losses are modelled by the effective resistors R_m and R_f. The quantum dot device is parametrised by a parallel RC circuit with resistance R_d and capacitance C_p.

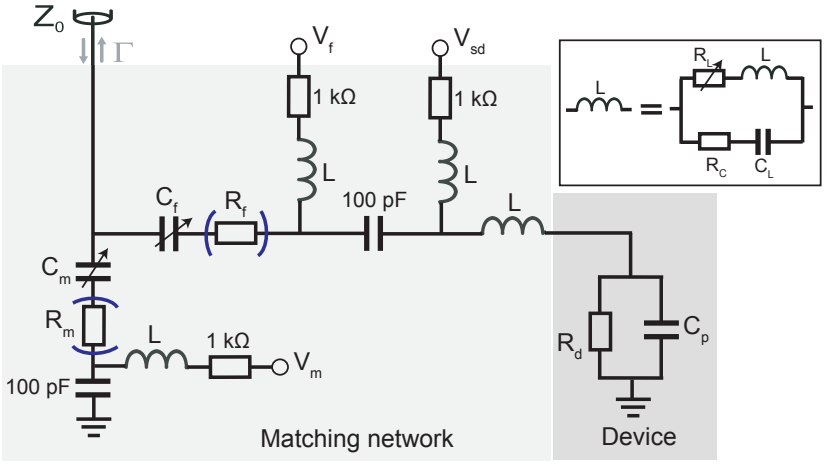

FIGURE 4.11: The circuit model used to simulate the matching network and device. The varactors C_m and C_f are taken as lumped elements, including any parasitic capacitances in parallel. The effective resistors R_m and R_f model other parasitic losses in the circuit. The quantum dot is parametrised by a resistance R_d and capacitance C_p. Inset: Elements R_L, R_c and C_L model parasitic contributions to the impedance of the inductors L.

To simulate the reflected amplitude and phase response of the system, we calculate the reflection coefficient Γ, which is given by:

$$\Gamma = \frac{Z(f_c) - Z_0}{Z(f_c) + Z_0} \tag{4.1}$$

where $Z(f_c)$ is the total impedance from the RF input port for a given carrier frequency f_c and Z_0=50 Ω is the line impedance. The reflected signal S_{21} is measured by a vector network analyser and relates to Γ by an overall insertion loss A. The latter incorporates losses in the measurement setup and assumed to be constant. Therefore, for simulations we use:

$$|S_{21}(f_c)| = A|\Gamma(f_c)| \tag{4.2}$$

The data fits were obtained using the SciPy library (open-source scientific software environment for Python[3]). The library uses the Levenberg-Marquardt algorithm (also known as the damped least-squares method), that analyses a set of m observations with n unknown parameters, where $m > n$ [126]. The model is approximated linearly and with each successive iteration, the unknown parameters are refined to give an ideal fit. Relevant fitting constraints were introduced to ensure the fitting parameters made physical sense. For the data fits of C_m, a small linear cross-talk was assumed between the two varactors: 0.13 pF/V increase in C_f and 0.07 Ω/V decrease in R_f for V_m=-24 to 24 V.

[3]The Python code was developed by Jacob Chittock-Wood and it is available here: www.ucl.ac.uk/quantum-devices/sites/quantum-devices/files/pythoncode.zip.

For the tank circuit inductor, we take from the datasheet (model: Coilcraft 0805CS-331): L=320 nH, R_L=4.74×10$^{-4}\sqrt{f}$ Ω, R_c=31 Ω and C_L=0.096 pF. For the bias-tee inductors (model: Coilcraft 0805CS-471) we take: L=470 nH, R_L=6.14×10$^{-4}\sqrt{f}$ Ω, R_c=66 Ω and C_L=0.132 pF. However, for all inductors R_L was set to zero for the simulations. For a pinched-off device, we assume R_d= 1 GΩ. The parasitic capacitance was measured at 6 mK using the same setup and by-passing the varactors, yielding C_p=3.2 pF.

Varactor geometry simulations

Furthermore, the schematic of Figure 4.2 was simulated using COMSOL Multiphysics simulation software[4]. Taking ϵ_r=18 700 as an approximate dielectric constant value at zero electric field [117], the simulation yields a capacitance of 53.6 pF for each varactor. This is roughly in agreement with the values listed in Table 4.1. The electric field simulation is shown in Figure 4.12.

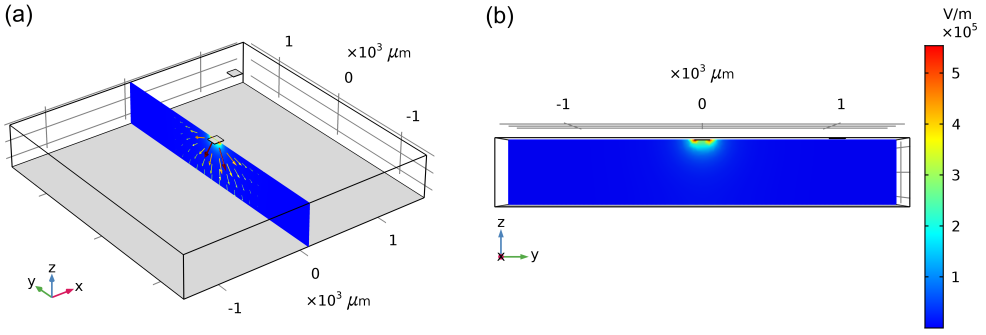

FIGURE 4.12: COMSOL Multiphysics simulations of the varactor geometry electric field for ϵ_r=18 700. (a) Side view, (b) side cross-section.

4.3.2 Resonance Stability

STO hysteresis

Strontium titanate is subject to hysteresis when biased across a large voltage range [117]. For the matching network, the hysteresis is quantified by plotting the reflected amplitude at resonance as a function of both V_m and V_f. This is done by measuring the amplitude in the frequency range from 150 to 200 MHz for each V_m & V_f pair and extracting the minimum value. Such measurements are shown in Figure 4.13. The system is in perfect impedance match along the blue curves. In Figure 4.13(a), the measurement is taken from the bottom left to the top right corner (V_m=-30 V, V_f=-24 V to V_m=30 V, V_f=24 V) and vice-versa for (b). The displacement of the blue curve indicates hysteretic behaviour by the STO substrate, possibly arising from charge redistribution and remnant polarisation that alter the capacitances C_m and C_f at a given bias voltage. This is not

[4]COMSOL simulations were developed by Alex Owens and Dr. Byron Villis.

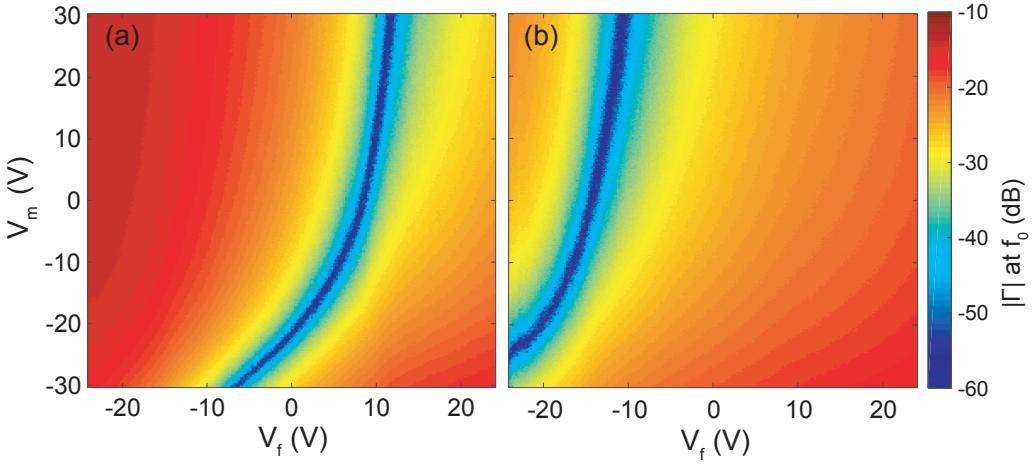

FIGURE 4.13: The reflected amplitude at resonance as a function of V_m and V_f measured to demonstrate the hysteresis of the STO substrate. (a) Measurement is taken from bottom left to top right corner, and (b) measurement is taken from top right to bottom left corner. The system is in perfect impedance match along the blue curves.

a practical problem for the varactors, since matching and tuning can still be achieved by adjusting to the right voltage. The data of Figure 4.13 can be used not only to quantify the hysteresis of the substrate, but also as a guidance for achieving the best impedance match possible by applying the corresponding V_m bias after shifting to the desired resonance along V_f.

Stability in time

The resonance stability was investigated as a function of time for fixed varactor settings. Long-term stability is important if specific varactor settings are to be kept constant for long periods of times. The deviations at resonance in relative reflected amplitude $\Delta|\Gamma|$ and phase $\Delta\Phi$ measured every minute for 60 minutes are shown in Figure 4.14 for three different varactor settings. The measurement is carried out for V_m=3 V (top), 5 V (middle) and 7 V (bottom), with perfect impedance matching achieved at 7.5 V. As expected, the resonance fluctuates more when closer to perfect matching, since the system is more susceptible to noise. The latter can be attributed to noise in the experimental setup, or charge noise in the substrate that causes the parasitic capacitance to fluctuate. Overall, the resonance is very stable with respect to the typical duration of measurements, and the exact resonant frequency can be sustained for days throughout experiments.

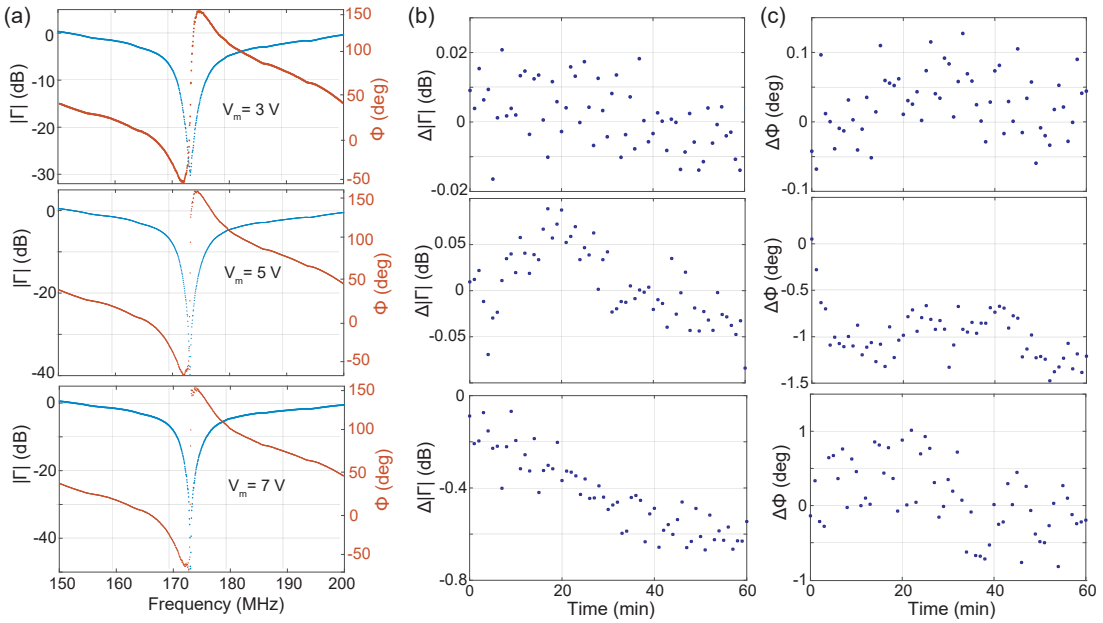

FIGURE 4.14: (a) Reflected amplitude and phase for given varactor settings, along with relative fluctuations in (b) amplitude and (c) phase as a function of time.

Stability in magnetic fields

There are various experiments and applications were magnetic fields are often required to tune device characteristics, such as spin-based quantum information processing. Therefore, it is important for the circuit to retain its impedance match and resonant frequency in a magnetic field. The fact that strontium titanate is a non-magnetic material has proven ideal for such a requirement. This is demonstrated with a magnetic field B (parallel to the STO varactors) that was set to 9 T, with C_m and C_f biased accordingly for perfect impedance matching at 172 MHz. The field was then ramped to zero, and the reflected amplitude and phase around resonance were measured as a function of B and carrier frequency. The data is shown in Figure 4.15. The resonance does not shift at all with respect to B, and the impedance matching is retained throughout the measurement[5]. This suggests that STO-based varactors can be used for RF measurements even in strong magnetic fields, and any variation in the measured amplitude or phase can confidently be attributed to the devices under investigation, rather than changes in the matching or detection circuit.

4.3.3 RF Coulomb Diamonds

Matching the impedance of a quantum dot to the RF network improves the signal-to-noise ratio (SNR). This is evident by looking at the reflected amplitude and phase

[5]The reflected amplitude at resonance is slightly changing at lower magnetic fields due to heating.

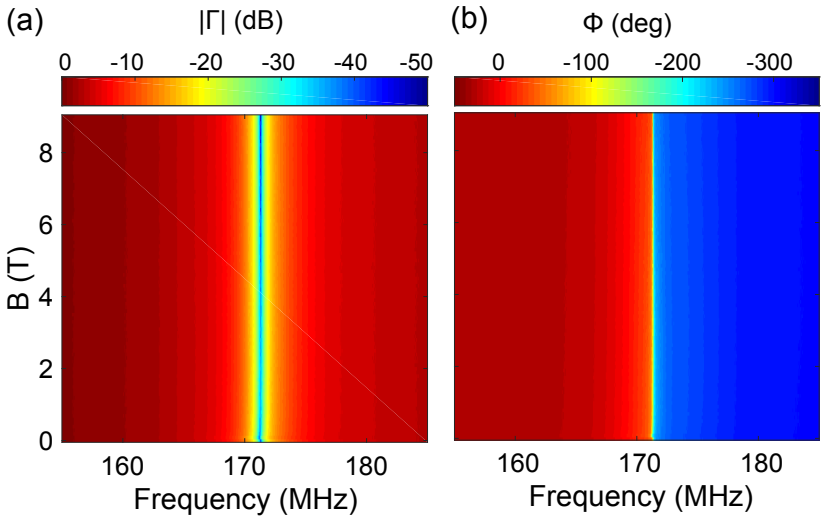

FIGURE 4.15: (a) The reflected amplitude and (b) phase as a function of magnetic field B and carrier frequency. The circuit is set to perfect impedance match at 172 MHz at 9 T and retains its resonance and good matching down to 0 T.

response; the steeper they are around resonance, the higher the sensitivity. The advantage of having a good impedance match is demonstrated in Figure 4.16, which focuses on a Coulomb diamond measured as a function of source-drain bias V_{sd} and back gate voltage V_g. In Figure 4.16(a), the differential conductance dI_{sd}/dV_{sd} of the diamond is shown as measured in DC transport, while in (b) and (c) the same diamond is measured in relative reflected amplitude $\Delta|\Gamma|$ far from (V_m=20 V) and close to (V_m=8 V) perfect impedance matching, respectively. The colour scale is the same for both amplitude measurements for direct comparison. In Figure 4.16(c), where the system is closer to matching, the SNR is about 10 times higher than that of 4.16(b), and more details can be probed. The phase response is not presented here, since due to the nature of the device (single dot), shifts in phase are very weak and not much information can be obtained from Coulomb diamond phase measurements. This is due to the very small capacitive changes that take place when transport of charge carriers occurs between the source and drain through the dot. On the other hand, dissipative changes that occur during transport are easier to see in the reflected amplitude. This differs from double quantum dot devices where interdot transitions cause a dispersive change, which is easier to see in the phase than the corresponding amplitude. For comparison, Figure 4.17 shows a Coulomb diamond plot as seen in DC transport, relative reflected amplitude and relative phase. The measurement is taken with V_m=8 V (close to perfect impedance matching). Dashed lines are used to indicate how the diamonds seen in DC transport compare to those seen in amplitude and phase. The alternation between large and small diamonds suggests spin degeneracy.

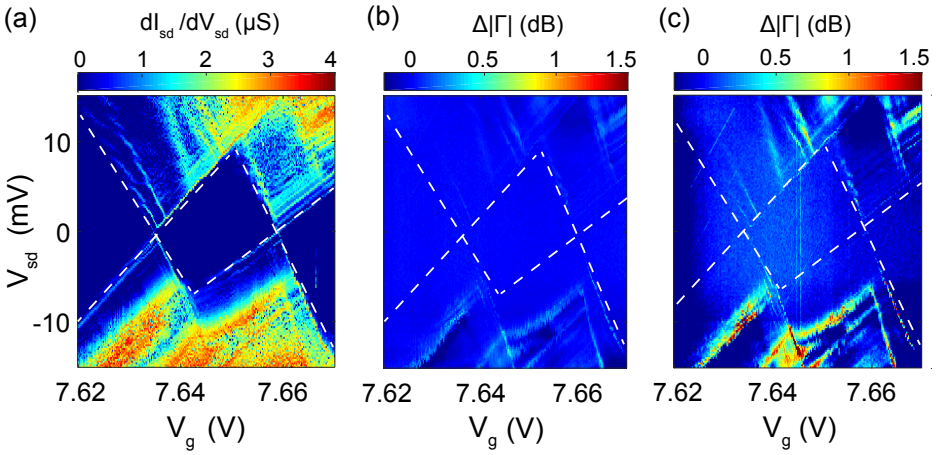

FIGURE 4.16: A Coulomb diamond as a function of source-drain bias V_{sd} and back gate voltage V_g as seen in: (a) DC transport (differential conductance), (b) reflected amplitude far from matching, and (c) reflected amplitude close to matching. The SNR is about 10 times higher when the system is closer to matching.

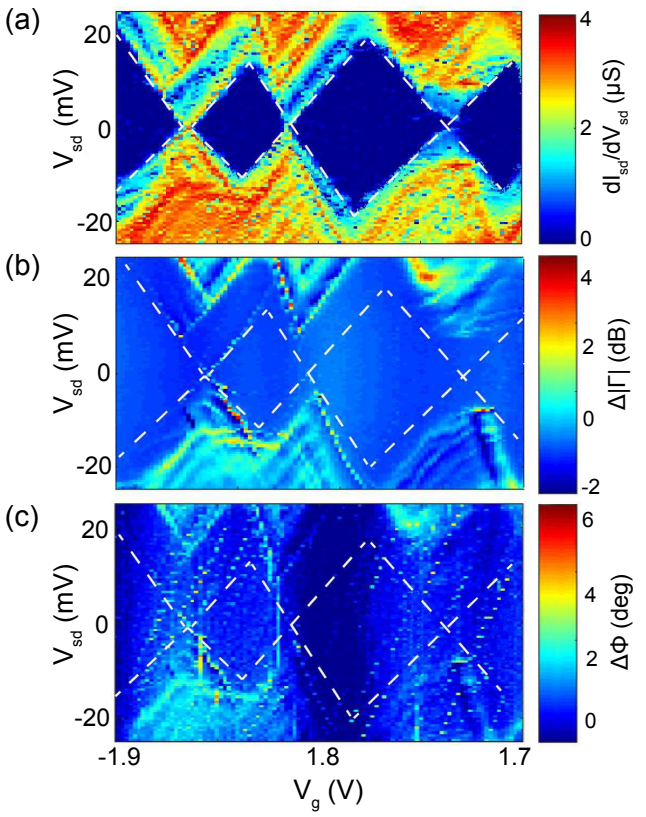

FIGURE 4.17: A Coulomb diamond plot as a function of source-drain bias V_{sd} and back gate voltage V_g as seen in: (a) DC transport, (b) relative reflected amplitude, and (c) relative phase. The measurements are taken with the system close to perfect impedance matching. The alternation between large and small diamonds suggests spin degeneracy.

4.4 Charge Sensitivity

The ability to tune the RF circuit to perfect impedance matching allows for high charge sensitivity measurements. This section demonstrates such measurements and examines how the SNR varies with the impedance matching of the circuit. To measure the charge sensitivity of the system, the technique outlined by R. Schoelkopf et al. [92] was adapted. A small sinusoidal voltage V_{rms} is used to modulate the gate of the device. The voltage has a root mean square charge equivalent amplitude Δq_{rms} and frequency f_m. This gate modulation causes an amplitude modulation of the carrier frequency that leads to sidebands in the reflected power spectrum P_r, as shown in Figure 4.18. The sidebands appear at $f_c \pm f_m$, where f_c is the carrier frequency. The SNR is determined in dB by the height of the sidebands with respect to the noise floor. The charge sensitivity δq is given by [14, 127]:

$$\delta q = \frac{\Delta q_{rms}}{10^{\frac{\mathrm{SNR}}{20}}\sqrt{2\Delta f}} \tag{4.3}$$

where Δf is the resolution bandwidth of the spectrum analyser in Hz.

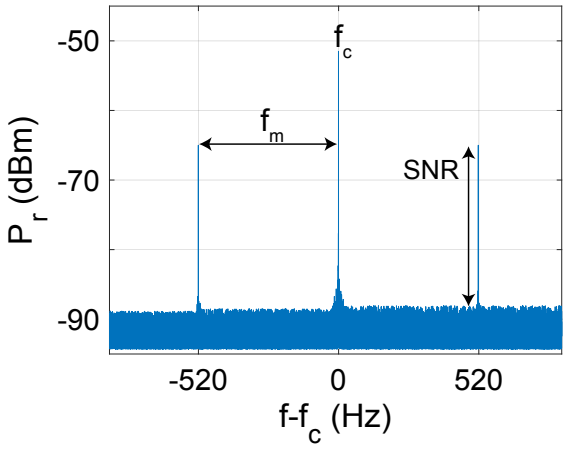

FIGURE 4.18: The reflected power spectrum P_r revealing sidebands at $f_c \pm f_m$ due to a sinusoidal gate modulation. The carrier frequency is 173 MHz and the SNR is 25.6 dB (obtained at the optimal working point).

For the measurements discussed in the rest of this section, the STO varactors were biased such that the system was at perfect matching at a resonance of 173 MHz, unless otherwise stated.

4.4.1 Optimal Working Point

To obtain the best charge sensitivity, it is essential that the device is operated at the optimal working point. Following the approach of T. Müller et al. [128], a relative

reflected amplitude $\Delta|\Gamma|$ across a gate modulation V_{rms} gives an upper bound for the SNR as:

$$\text{SNR} = \Delta|\Gamma|^2 \times \frac{P_0}{P_N} \tag{4.4}$$

where P_0 is the carrier power and $P_N{=}k_B T_N \Delta f$ is the noise in the measurement (dominated by the cryogenic amplifier noise temperature of T_N=7 K). Therefore, for the highest SNR, the relative reflected amplitude has to be maximised across a gate modulation and the carrier power must be optimum.

Charge transition

Maximising $\Delta|\Gamma|$ is achieved by modulating the gate across the steepest region of a charge transition. For this aspect, a Coulomb peak of resistance R=860 kΩ was chosen. The peak is shown on the left hand side of Figure 4.19(a) as a function of gate voltage V_g for a source-drain bias V_{sd}=50 µV. The corresponding Coulomb diamond is shown in Figure 4.19(b), from which we obtain ΔV_g=41 mV, as shown. The value of ΔV_g indicates the gate change that corresponds to the addition of one electron on the dot.

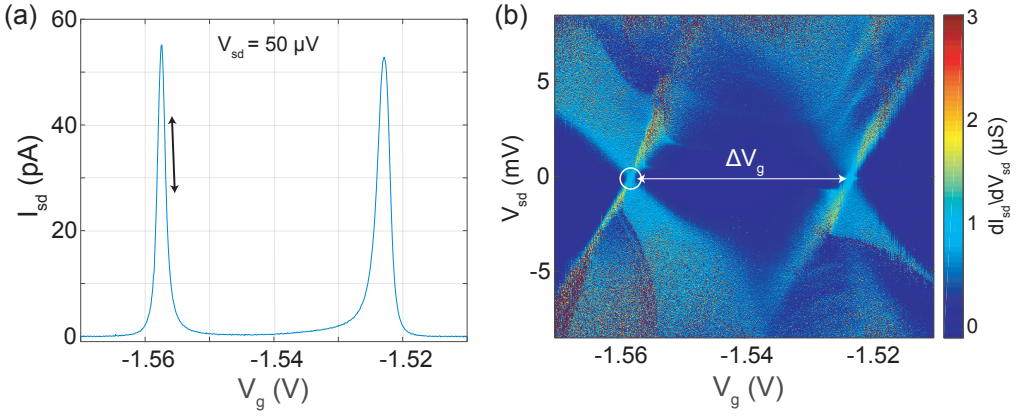

FIGURE 4.19: (a) The source-drain current I_{sd} as a function of gate voltage V_g for a source-drain bias V_{sd}=50 µV revealing two Coulomb peaks. The peak on the left has a resistance of 860 kΩ and was chosen for high charge sensitivity measurements. The black arrow denotes the steepest edge of the peak. (b) A Coulomb diamond plot showing the differential conductance around the region of interest as a function of V_{sd} and V_g. The white circle indicates the Coulomb peak of (a) that was used to characterise the charge sensitivity of the system. Here, ΔV_g=41 mV indicates the gate change that corresponds to the addition of one electron on the dot.

Modulation frequency and amplitude

The modulation frequency of f_m=520 Hz was chosen based on the cut-off frequency of the DC filtering setup. The cut-off is ∼5 kHz, and a modulation frequency of about 10 times lower was adapted to ensure lack of attenuation. The modulation amplitude V_{rms}=10 µV was chosen as the minimum amplitude that retains a high SNR, since

$\delta q \propto V_{rms}$. Values of V_{rms} lower than 10 µV would decrease the SNR, while higher values would show no significant improvement of the charge sensitivity.

Carrier power

To decide on the ideal carrier power, a series of SNR measurements were taken with various P_c powers. The SNR was plotted as a function of P_c and V_g, as shown in Figure 4.20. For a given value of P_c, the SNR has two maxima that are separated by a voltage of a few tens of µV. The maxima correspond to the maximum slope of either side of the Coulomb peak. As expected, the separation between the SNR maxima increases with P_c, since the peak is broadened by the RF power. For powers lower than -105 dBm, the SNR decreases. This is attributed to the fact that the incident RF power is too low for sidebands to be properly resolved. In addition, the SNR was plotted as a function of gate voltage V_g for different values of P_c. Such measurements are shown in Figure 4.21. For higher powers, the Coulomb peak under examination is thermally broadened; however, at low powers the SNR decreases. Therefore, the ideal value for P_c is one that maximises the SNR but does not broaden charge transitions. Plotting the SNR as a function of carrier power (see Figure 4.22) suggested the optimum power P_c=-99 dBm, which is also in agreement with the data from Figures 4.20 and 4.21.

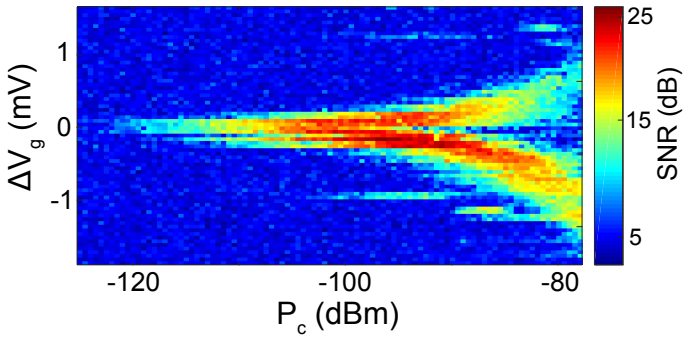

FIGURE 4.20: The SNR extracted from sidebands as a function of P_c and V_g. The measurement was taken with f_m=520 Hz and V_{rms}=10 µV along the peak indicated in Figure 4.19(a). The SNR maxima for a given P_c correspond to the maximum slope of either side of the Coulomb peak. The separation between maxima increases with P_c due to thermal broadening of the peak by the RF power.

In summary, the optimum working parameters were obtained as follows: P_c=-99 dBm, f_m=520 Hz and V_{rms}=10 µV. These parameters lead to a maximum SNR of 25.6 dB and correspond to a resistance change δR=80 kΩ across a gate modulation. Using ΔV_g=41 mV, we obtain Δq_{rms}=2.4×10^{-4}e. With a spectrum analyser resolution bandwidth of B=3.35 Hz (chosen as the highest bandwidth for which the SNR retains its maximum value), the best charge sensitivity was obtained as δq=4.8 µe/Hz$^{1/2}$. This result indicates a charge sensitivity of the same order of magnitude as sensitivities obtained with setups

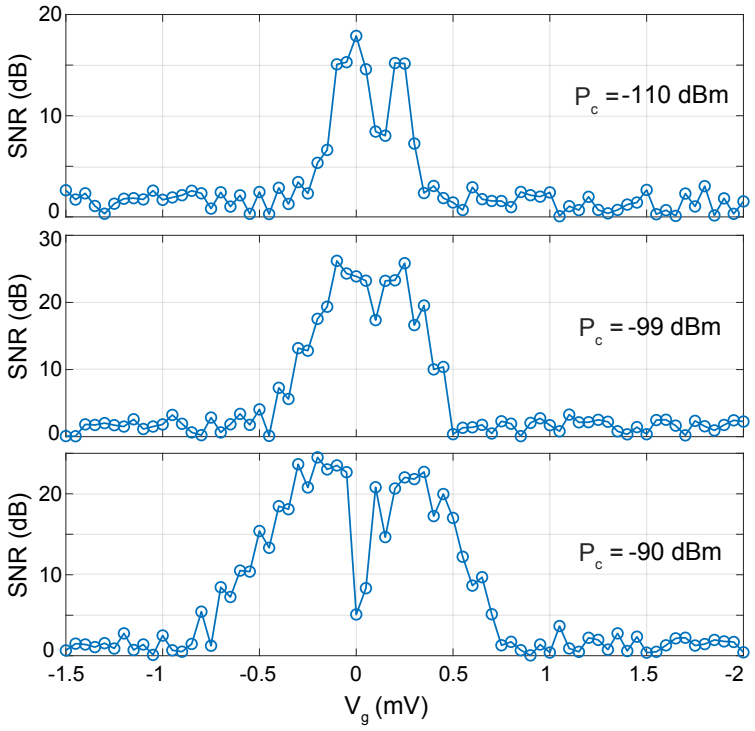

FIGURE 4.21: The SNR as a function of gate voltage V_g measured with three different carrier powers P_c. The SNR is extracted from sidebands and measured along the peak indicated in Figure 4.19(a) with a gate modulation of V_{rms}=10 µV.

that use superconducting spiral inductors [14], which are among the best reported to date.

4.4.2 Dependence on Impedance Matching

To characterise the sensitivity as a function of impedance matching, measurements were taken with various V_m biases. The SNR was measured as a function of carrier power P_c for several voltages V_m, distinguishing between the under and over coupled regimes. Such measurements are shown in Figure 4.22. As expected, the SNR decreases when far from matching and it is maximised when the system is perfectly matched at V_m=14 V. This is also observed when focusing on lower powers for various varactor settings. Looking at the SNR as a function of V_m for -125< P_c <-110 dBm, the former peaks at matching (V_m=14 V) and decreases away from matching, as shown in Figure 4.23. The charge sensitivities obtained are shown in Figure 4.24 as a function of V_m for P_c=-99 dBm.

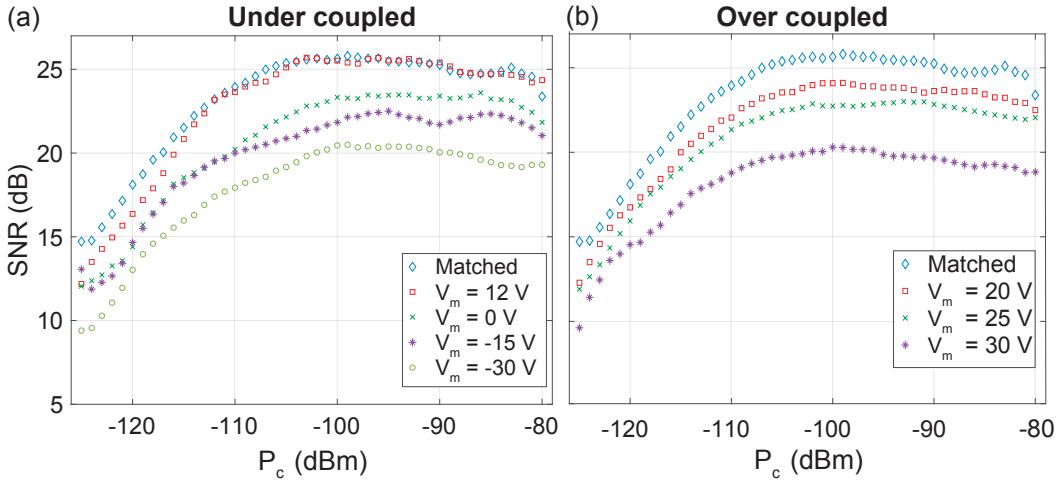

FIGURE 4.22: The SNR as a function of carrier power P_c for various V_m voltages, corresponding to different impedance matchings. (a) Measurements in the under coupled regime, (b) measurements in the over coupled regime. The maximum SNR is 25.6 dB and is obtained at matching, for which V_m=14 V.

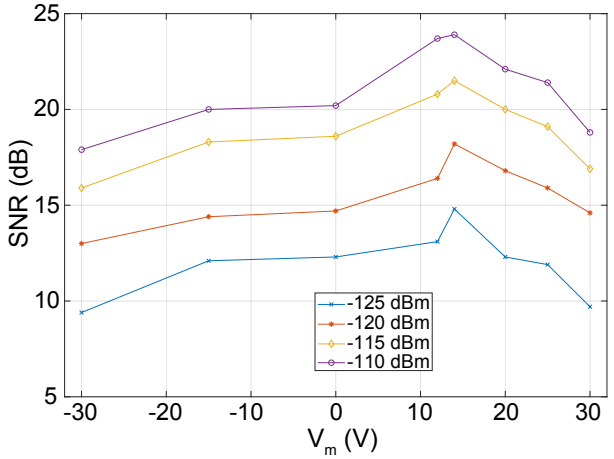

FIGURE 4.23: The SNR as a function of V_m for lower carrier powers. The SNR peaks at matching (V_m=14 V) and decreases otherwise.

4.5 Operation at Higher Frequencies

This section demonstrates perfect impedance matching and frequency tuning of the resonant circuit with the absence of a quantum dot device. By removing the quantum dot from the circuit, the parasitic capacitance C_p is reduced by about an order of magnitude, and as a consequence, the resonance shifts to higher frequencies. The rest of the experimental setup remains the same. The purpose of this experiment is to demonstrate that the STO varactors can be operated over a large frequency range.

With the absence of a quantum dot, we take $R_d \to \infty$ and C_p=0.26 pF. The parasitic

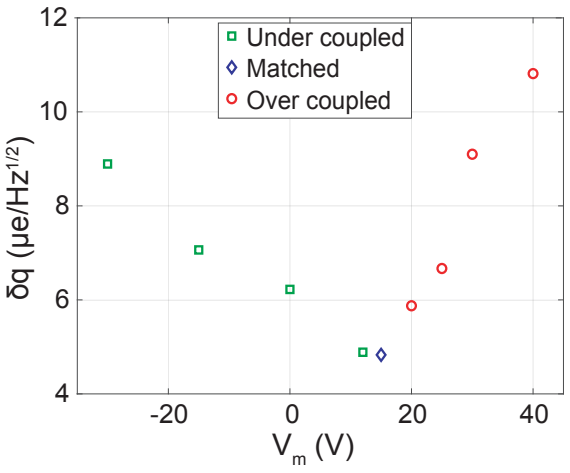

FIGURE 4.24: The charge sensitivity as a function of V_m bias for under and over coupled regimes measured with P_c=-99 dBm. The best sensitivity of 4.8 μe/Hz$^{1/2}$ is obtained at perfect matching.

capacitance is now dominated by the stray capacitances of the PCB, circuit inductor, sample wiring and metallic leads [108]. The resonance is now f_0=552.5 MHz. Similar to Section 4.3, the reflected signal S_{21} was measured with a network analyser for -40≤ V_m ≤40 V with V_f=0. The reflected amplitude |Γ| and phase response Φ are shown in Figure 4.25 as a function of carrier frequency. From the phase, it is clear that the system switches from over coupled to under coupled between 20< V_m <30 V. It is also of interest that for more negative voltages, V_m <-20 V, the resonance disappears completely. Examining the matching voltage in more detail yields perfect impedance match at V_m=22.5 V. The measurements at perfect matching are shown in Figure 4.26.

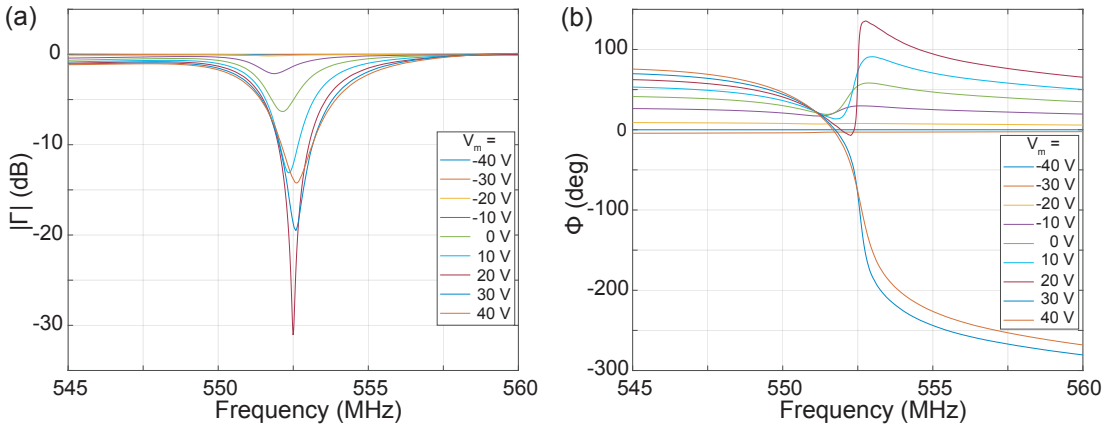

FIGURE 4.25: The (a) reflected amplitude, and (b) phase response of the resonant circuit for -40 ≤ V_m ≤ 40 V and V_f=0. The resonant frequency is 552.5 MHz. The system switches from over coupled to under coupled between 20< V_m <30 V.

Similarly, we tune the resonant frequency by changing the capacitance C_f with a bias voltage V_f. The reflected signal was measured for -30≤ V_f ≤60 V with V_m=0. The reflected amplitude |Γ| and phase response Φ are shown in Figure 4.27 as a function of carrier frequency. Over a range of 90 V, the resonance shifts only by about 2 MHz, roughly 10 times less than the resonance of Figure 4.8. This is attributed to the parasitic capacitance being about 10 times smaller, and therefore reducing the tunability of f_0 (see Section 4.6 for more details).

The resonant frequency shift as a function of V_f is shown in Figure 4.28 for a larger voltage range, where three distinct gradients can be resolved. The maximum frequency tunability occurs in the range -20< V_f <20 V, corresponding to 28 kHz/V. A small decrease in tunability is observed for V_f >20 V (23 kHz/V), while a large decrease

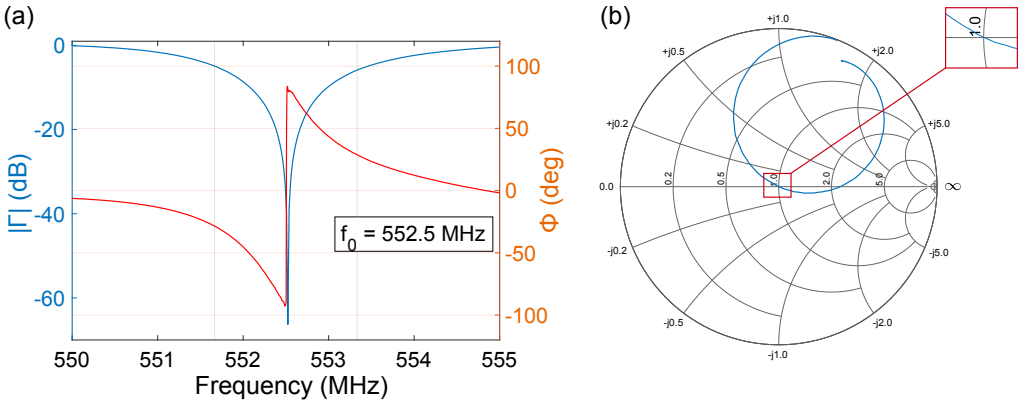

FIGURE 4.26: Perfect impedance match between RF line and resonant circuit achieved by biasing the STO varactor C_m with V_m=22.5 V and V_f=0. (a) The reflected amplitude and phase, (b) the corresponding Smith chart.

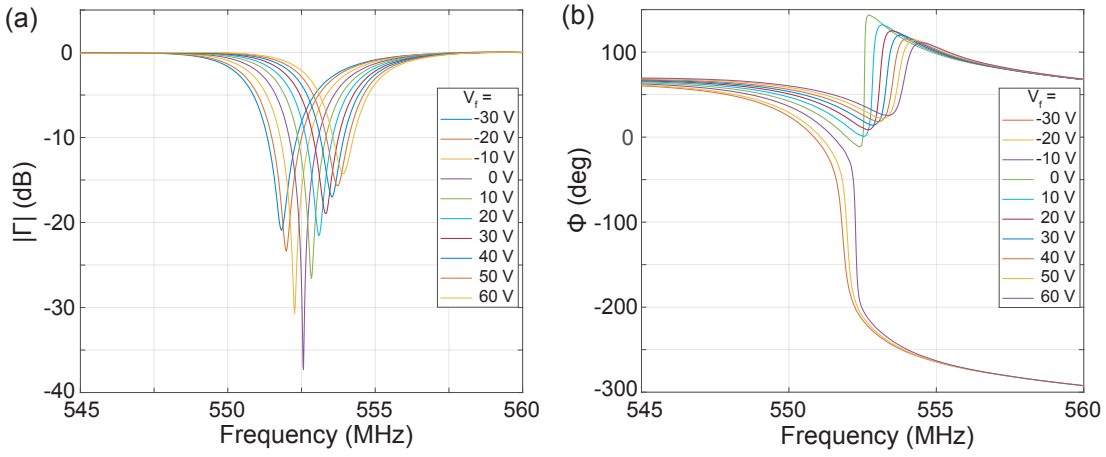

FIGURE 4.27: The (a) reflected amplitude, and (b) phase response of the resonant circuit for -30≤ V_f ≤60 V with V_m=0. The resonant frequency shifts from 551.8 MHz (V_f=-30 V) to 553.9 MHz (V_f=60 V), suggesting a tunability of about 25 kHz/V.

and polarity change is observed for V_f <-30 V (11 kHz/V). This is attributed to the capacitance response as a function of voltage, which follows again a similar behaviour as the one shown in Figure 4.9.

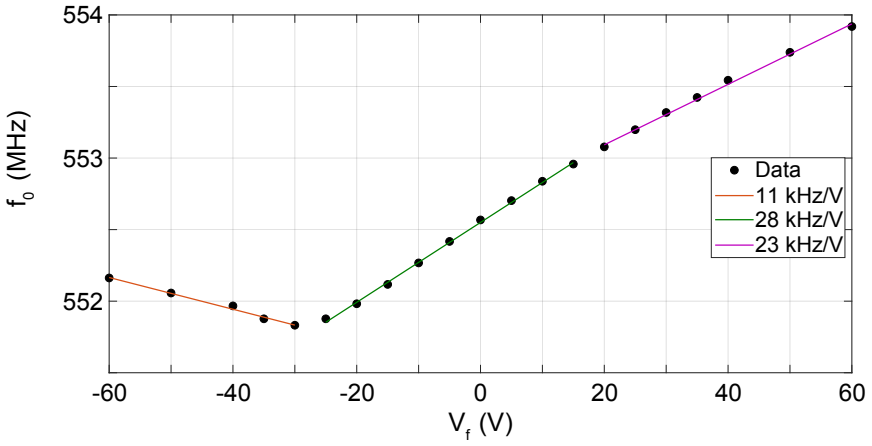

FIGURE 4.28: The resonant frequency f_0 as a function of V_f bias. The maximum tunability occurs at lower voltages -20< V_f <20 V, corresponding to 28 kHz/V.

Finally, although all experiments were performed at frequencies around 170 and 550 MHz, the varactors are expected to be operational at much higher GHz frequencies as well; ultimately limited by the soft optical mode phonon frequency [129].

4.6 Discussion

Conventional varactor diodes were proven to be unreliable when used at milliKelvin temperatures. In this chapter, we have demonstrated that custom-made voltage-tunable varactors based on strontium titanate can be used at temperatures as low as 6 mK to drive a resonator into perfect impedance match and tune its resonant frequency. Our STO varactors reliably work with long-run measurements, are easy to tune, simple to fabricate and they operate over a large frequency range. In addition, they are magnetic field insensitive, they take up little space in an experimental set-up, and they add no significant complexity to the circuit architecture. A variety of varactors can be prepared a priori, such that each pair meets the criteria of the device under investigation. An example is the implementation of interdigital capacitors on the surface of the STO to replace the parallel plate design. Interdigital capacitors adapt a "finger" geometry and they can have an intrinsic capacitance of a few pF or less [130], achieving the ideal condition of $C_m \sim C_f \sim C_p$ (depending on the device) and improving tunability by requiring smaller voltage biases. Since the STO substrate that accommodates the

varactors is separate from quantum devices, it can be changed on demand without damaging the device of interest.

Our measurements show that STO varactors can be used to obtain higher signal-to-noise ratios and better measurement sensitivities. The latter is maximised at impedance matching as expected [128]. Our method allows for improvement of the radio-frequency readout in a variety of device configurations, and flexibility in cases where the resonance range allowance is limited. By measuring the charge sensitivity using a carbon nanotube quantum dot, we show that state of the art sensitivities can be obtained without superconducting inductors or precise selection of electrical components. We demonstrate a charge sensitivity of δq=4.8 µe/Hz$^{1/2}$, which is of the same order of magnitude as the best sensitivities reported to date. The charge sensitivity can be further improved by reducing the parasitic losses in the detection circuit. To a certain extend, the latter depends on the quality of the STO crystal, which could be improved in future work.

Finally, while strontium titanate was chosen in this work for the large tunability of its relative permittivity, it is by no means the only quantum paraelectric material suitable for low temperature operation, and other materials can also be considered [131, 132]. One example is potassium tantalate (KTaO3 or KTO), which has a predicted loss tangent two orders of magnitude smaller compared to STO at temperatures below 1 K [133, 134]. The expense for the lower loss is a somewhat lower tunability. The choice of material thus depends on the relative importance (large tunability or low loss tangent) for the specific application.

Chapter 5

Reflectometry on Carbon Nanotube Double Quantum Dots

This chapter presents characterisation and measurements on carbon nanotube double quantum dot devices at room and low temperatures. Attempts for tuning the interdot transition coupling are discussed, along with high-frequency gate modulation and challenges. A video-mode data acquisition technique is presented as a fast and easy-to-use way for characterising and measuring double dot devices at low temperatures.

5.1 Room Temperature Characterisation

Carbon nanotube double quantum dot devices can be tested at room temperature similarly to single dots (see Section 3.1.1 for more details). However, double dots require further tests due to their more complex geometry. That includes examination of the functionality of the plunger and top gates. The two plunger gates can be tested the same way as the back/control gate - a similar behaviour to Figure 3.2 should be attained, although the voltage range might be larger since the lever arm is smaller. A crucial test for double quantum dots involves the top gate. It is important that there is no current leakage between the top gate and the nanotube. This depends on the quality of the Al_xO_x oxide. The effect of the top gate on electron transport can be examined at room temperature by applying a source-drain bias and sweeping the top gate voltage V_T. Typical values for V_T are usually no more than ± 1 V[1]. By sweeping V_T, the transport of electrons from source to drain is impeded and there is a reduction in the current. With semiconducting nanotube double quantum dots, it is common to observe zero current

[1]The actual voltage depends on the oxide thickness and quality.

above a critical V_T voltage. For narrow-gap nanotube double quantum dots, there is usually a small V_T range (typically 10s of mV) for which the current is relatively lower.

The current response with an applied bias V_{sd}=150 mV as a function of V_T at room temperature for a semiconducting nanotube is shown in Figure 5.1(a). The current is "pinched-off" around V_T=0.1 V. The current response of another semiconducting nanotube as a function of gate voltage V_g with V_{sd}=25 mV is shown in Figure 5.1(b) for V_T=-1 V (blue), V_T = 0 (red) and V_T = +1 V (green). The device is more conductive for V_T=-1 V, since the Fermi level is lowered into the valence band and holes contribute to transport. At zero top gate voltage, conductance is observed at more negative, but also more positive V_g voltages, due to the contribution of holes and electrons, respectively. At V_T=+1 V, transport is favoured in the conduction band (electrons), while transport via holes is totally suppressed. The equivalent measurement is shown in Figure 5.2 for a narrow-gap nanotube. The current is suppressed around V_T=-35mV, while no significant difference is observed for other top gate voltages.

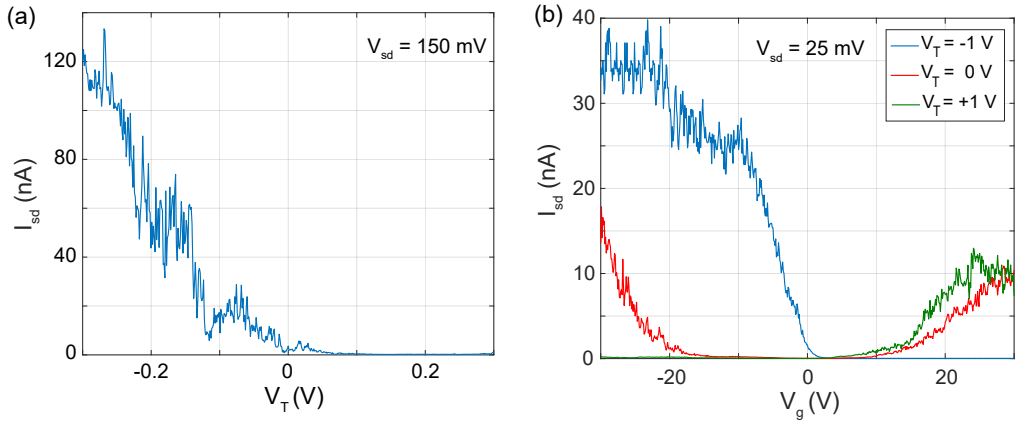

FIGURE 5.1: The source-drain current for semiconducting nanotube double quantum dots at room temperature: (a) as a function of top gate voltage (the current is "pinched-off" around V_T=0.1 V), (b) as a function of gate voltage V_g for V_T=-1 V (blue), V_T = 0 (red) and V_T = +1 V (green).

5.2 RF Reflectometry on Double Quantum Dots

For a quantum dot to favour RF reflectometry, the device must be conductive enough. The readout sensitivity is greatly compromised for devices with room temperature resistance higher than ∼1 MΩ, therefore readout on semiconducting nanotubes is non-trivial. Narrow-gap nanotubes are usually much easier to work with, since the tunnel rates are typically faster than the drive frequency. The characteristic stability diagram for a narrow-gap carbon nanotube double quantum dot (room temperature resistance of 320

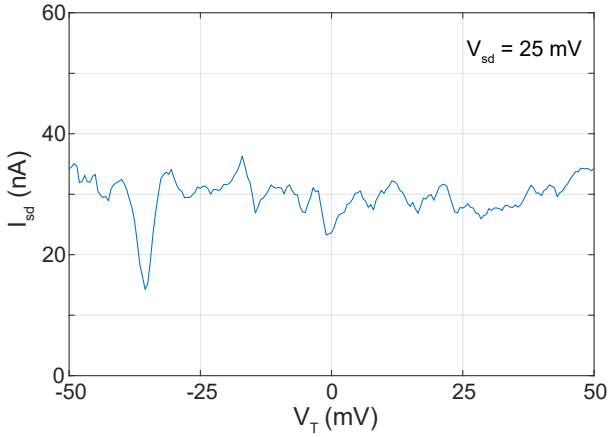

FIGURE 5.2: The source-drain current for a narrow-gap nanotube double quantum dot at room temperature as a function of top gate voltage. The current is suppressed around V_T=-35 mV.

kΩ) on doped silicon near the band gap for zero source-drain bias measured with RF reflectometry is shown in Figure 5.3(a). The black dashed lines are added for guidance and they indicate cotunneling to the drain. The same data after the removal of cross-capacitance effects is shown in Figure 5.3(b). Visible interdot transitions between triple points are circled in blue. The honeycomb size periodicity indicates the two-fold spin degeneracy of the energy levels. The RF power delivered to the device is about -100 dBm.

5.2.1 Tunnel Coupling Tuning

In well-behaved double quantum dots, the top gate allows for tuning of the potential landscape in such a way that the tunnel coupling between the two dots can be adjusted as desired. Broadly speaking, a smaller tunnel coupling indicates a sharper and more profound interdot transition in stability diagrams, while a larger coupling results in more curved triple points and a weaker interdot transition. The tunnel coupling can be determined by several ways [65, 88, 135]: (a) by analysing sidebands caused by high-frequency plunger gate modulation, (b) by measuring the curvature of the triple point wings, and (c) by measuring the width of the interdot transition at zero detuning. All three methods require parameters extracted from bias triangles, while (c) also requires knowledge of the electron temperature.

The device investigated in the rest of this section is a narrow-gap carbon nanotube double quantum dot on degenerately doped silicon. A detailed measurement of two consecutive triple point pairs is shown in Figure 5.4. The two interdot transitions clearly have different tunnel couplings. The triple point on the right is shown in more detail in

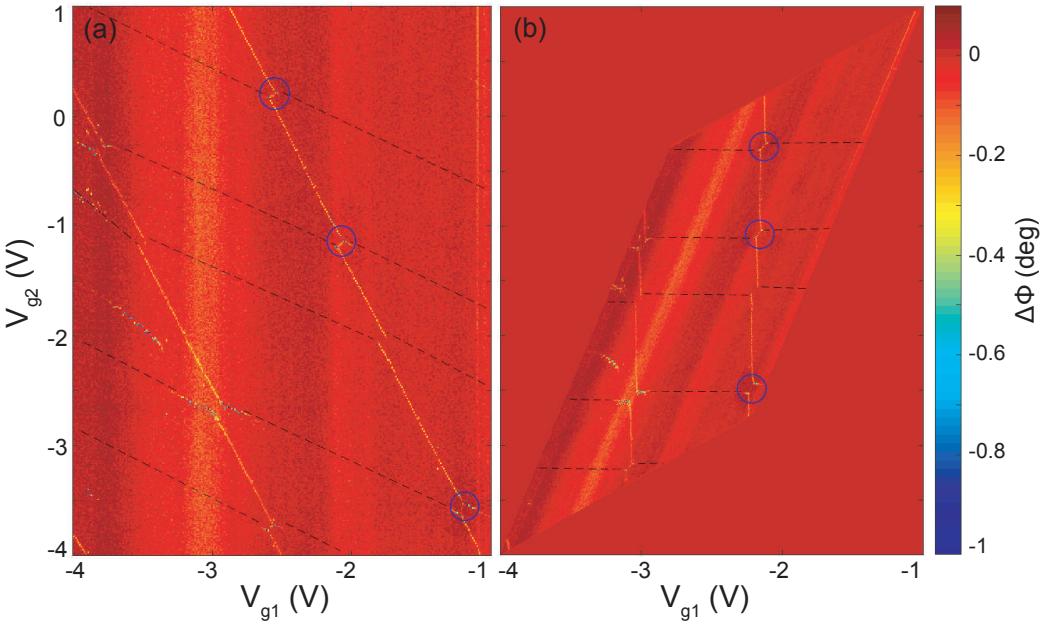

FIGURE 5.3: A charge stability diagram for a narrow-gap carbon nanotube double quantum dot on doped silicon near the band gap for zero source-drain bias, as seen in relative phase. (a) Original data, (b) data after the removal of cross-capacitance effects. Visible interdot transitions between triple points are circled in blue. Cotunneling to the drain is shown as dashed black lines for guidance. The honeycomb size periodicity indicates spin degeneracy. The RF power delivered to the device is about -100 dBm.

Figure 5.5, both in relative phase and amplitude. The notation (n, m) indicates n and m electrons on the right and left dots, respectively. The relative amplitude changes sign from positive to negative at the cotunneling transitions, suggesting the contribution of some dissipative changes to the system.

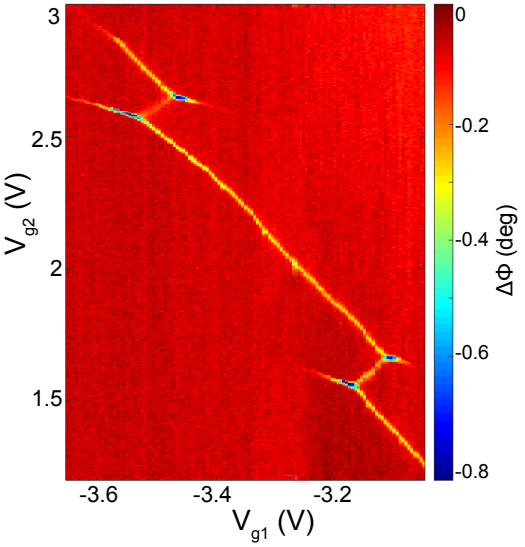

FIGURE 5.4: Two triple point pairs on an RF stability diagram. Interdot transitions of different tunnel couplings are visible.

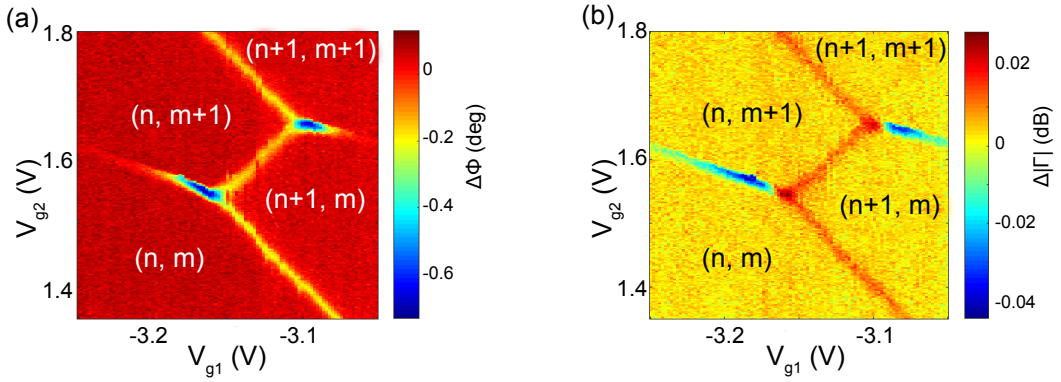

FIGURE 5.5: The interdot transition between a pair of triple as seen in: (a) relative phase, (b) relative reflected amplitude. The notation (n, m) indicates n and m electrons on the right and left dots, respectively.

The effect of V_T on a pair of triple points is shown in Figure 5.6. For V_T=0, the triple points are curved and the interdot transition is not visible - the tunnel coupling is large. For V_T=20 mV and V_T=40 mV, the triple points come closer and the interdot transition appears - the tunnel coupling is getting smaller. For V_T=60 mV, the triple points begin to curve again and the interdot transition becomes less profound - the tunnel coupling is getting larger.

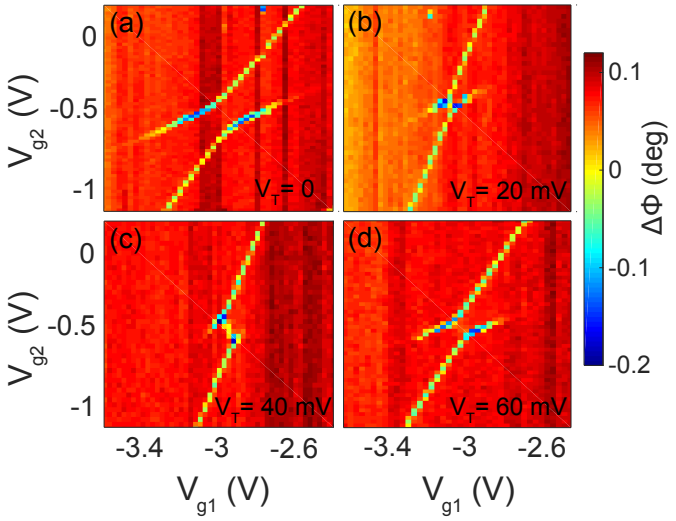

FIGURE 5.6: (a-d) A triple point pair as seen in relative phase for four different top gate voltages. The tunnel coupling changes with each voltage.

5.2.2 High-Frequency Modulation

Modulating the plunger gates perpendicularly to the interdot transition leads to sidebands, if the modulation frequency exceeds the tunnel coupling energy. This occurs for finite detunings when charge carriers on either dot absorb a microwave photon and tunnel to the other dot whose electrochemical potential is higher in energy and otherwise suppressed by Coulomb blockade. This is known as photon-assisted tunneling and can be used to probe charge qubit characteristics, such as the charge-dephasing time T_2^* [30, 59, 65, 136–139].

Sinusoidal modulation of plunger gates was attempted on double quantum dot devices on doped silicon. The modulation was generated using a fast arbitrary wave form generator (AWG) with sampling rate 65 GSa/s and bandwidth 25 GHz. The modulation was applied to the microwave lines installed in the cryostat and delivered to the device via the Anritsu K251 bias-tees on the mixing chamber (see Section 3.2.2 for more details). The effects of a 15 GHz modulation on V_{g1} for different modulation powers P_m are shown in Figure 5.7. The device under examination was tuned to allow for the sharpest interdot transition (smaller tunnel coupling). Despite the effects of the modulation, no sidebands were observed. As seen in Figure 5.7(c) and (d), the interdot transition is smeared and washed out for higher powers. A similar behaviour was observed for higher modulation frequencies. A possible explanation is that the tunnel coupling was large compared to the modulation frequency, therefore no sidebands could be resolved. Moreover, the dopants in the silicon substrate might partially screen the modulation effect.

5.2.3 Video-mode Data Acquisition

Most radio-frequency reflectometry measurements presented in this thesis were carried out using a vector network analyser operated via MATLAB. Although this has proven to be an effective way of acquiring data, it was very slow when it came to large data sets such as colour map plots. The bottleneck lies with the fact that there had to be a communication step between the network analyser and the computer at each point on the map, which slowed down the measurement dramatically. This happens because the network analyser supports no internal data buffers, so the data could not be stored locally for later retrieval. Fortunately, after the purchase of an FPGA-based lock-in amplifier[2], a video-mode approach [106, 135] was implemented that allowed for much faster RF data acquisition. Specifically, when measuring a stability diagram, one plunger gate is now swept back and forth with a typical frequency of 1 kHz, while the other is stepped

[2]Zurich Instruments UHFLI (600 MHz, 1.5 GSa/s).

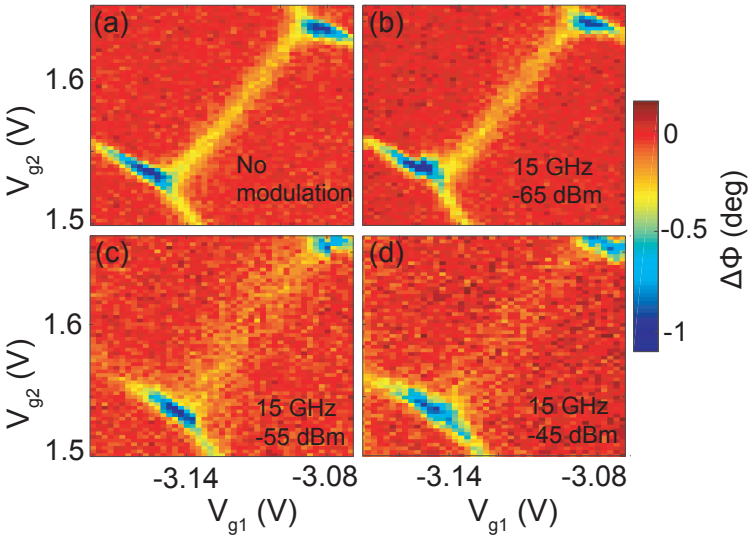

FIGURE 5.7: The effect of a 15 GHz sinusoidal modulation of V_{g1} on the interdot transition for various powers: (a) no modulation, (b) P_m=-65 dBm, (c) P_m=-55 dBm, and (d) P_m=-45 dBm. No sidebands are observed and the interdot transition is washed out at higher powers. The device under investigation is a narrow-gap carbon nanotube double quantum dot on degenerately doped silicon.

after each sweep. This results in a reflected amplitude and phase stability diagram measurement of the order of 1 second, or a few seconds including averaging. This is an improvement of about three orders of magnitude in measurement speed when compared to the conventional method of using a network analyser. The dramatic increase in speed is the result of several aspects of the new instrument: (a) much faster acquisition rate, (b) no need for continuous communication between the instrument and the computer, as the FPGA is programmed in advance to follow a voltage source and acquisition sequence, and (c) the instrument supports local storage of data in buffers for batch transmission.

This new video-mode technique allows not only for a much faster low-temperature characterisation of double dot devices, but also for "live" probing. By acquiring a new stability diagram every ∼1 s, the effect of each gate can be directly observed by tuning the corresponding voltage. Since the interface of the instrument allows for refreshing newly acquired data, the illusion of a live video measurement emerges. A demonstration is shown in Figure 5.8, which shows a stability diagram measurement as seen on the user interface of the instrument. The relevant control functions of the measurement are indicated and they can be altered at any instant with the measurement automatically adjusting accordingly. The left plunger gate V_{g1} is swept at a frequency of 1 kHz with a saw-tooth waveform, during which the instrument measures 1000 points. This yields an integration time of ∼1 µs per data point. The right plunger gate V_{g2} is stepped every time V_{g1} completes a period, typically for 500 steps (points). This results in a measurement of 1000×500 points that takes ∼0.5 s and scales linearly with averaging.

The number of points is subject to FPGA memory limitations. A key point is that the measurement time does not depend on the number of points along V_{g1}, but only on the sweeping frequency and averaging. The sweeping and stepping sequence of the plunger gates is programmed via the AWG control panel on the interface of the instrument. The relevant code prepares the appropriate waveforms based on given parameters, which are then loaded to the instrument along with triggering instructions for data acquisition[3].

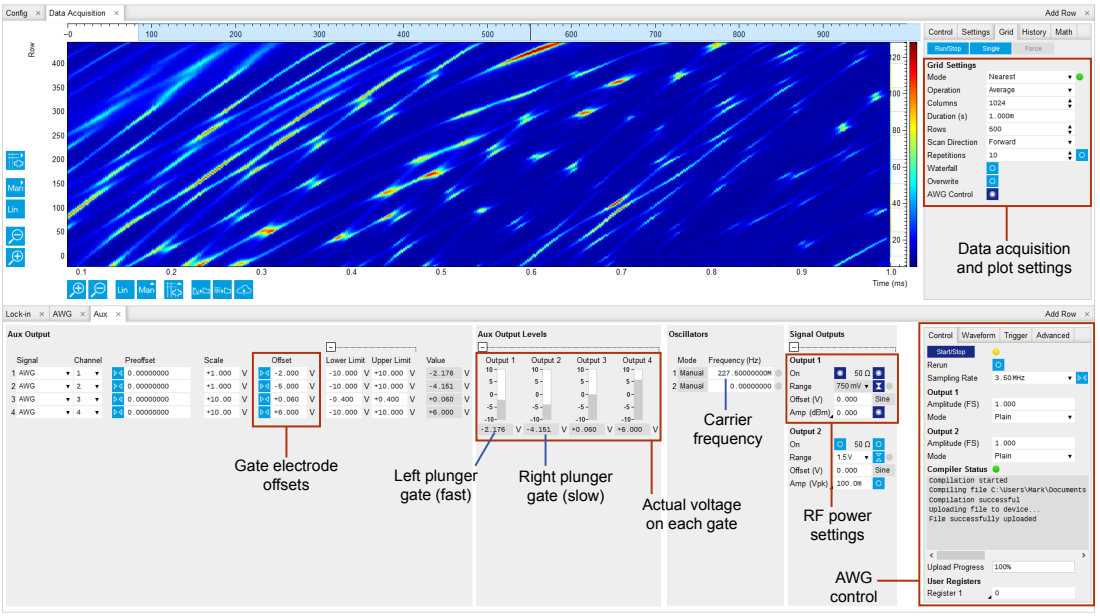

FIGURE 5.8: The lock-in amplifier user interface during a video-mode measurement. A stability diagram measurement can be seen the top panel, while gate voltage control and other parameters can be adjusted in the bottom panel during measurements.

As discussed in detail in Chapter 4, it has been demonstrated that custom-made strontium titanate varactors can dramatically improve the measurement sensitivity by matching the impedance of the resonant circuit to the impedance of the RF line. Combining impedance matching with video-mode data acquisition was proven a very useful tool for fast and reliable characterisation of double quantum dots at base temperature. The varactors ensure the signal-to-noise ratio is high enough for no or little averaging to be required during characterisation. On the other hand, video-mode data acquisition ensures fast evaluation and navigation along the parameter space of a device, which allows for a full device characterisation in only a few hours, as opposed to days or weeks with the previous measuring setup. An example of varactor and fast acquisition combination is shown in Figure 5.9 for a carbon nanotube double quantum dot on doped silicon. A stability diagram was measured with the lock-in amplifier and averaged 20 times. The

[3]The code is based on the C language syntax and it is available here, along with the relevant instrument settings: www.ucl.ac.uk/quantum-devices/sites/quantum-devices/files/videomode.zip.

measurement took about 10 seconds. In addition to the original data, the stability diagram with cross-capacitance correction is shown. The signature honeycomb structure and triple points are easily visible. When compared to stability diagrams acquired in earlier stages, there is an immediate sensitivity improvement of more than two orders of magnitude. The corresponding resonance is shown in Figure 5.10, after matching was improved with the STO varactors. The corresponding phase fit shown suggests a quality factor of 140. This is a significant improvement when compared to the phase fits of Figure 3.23, where the quality factor was 8 and 21 for doped and undoped silicon, respectively.

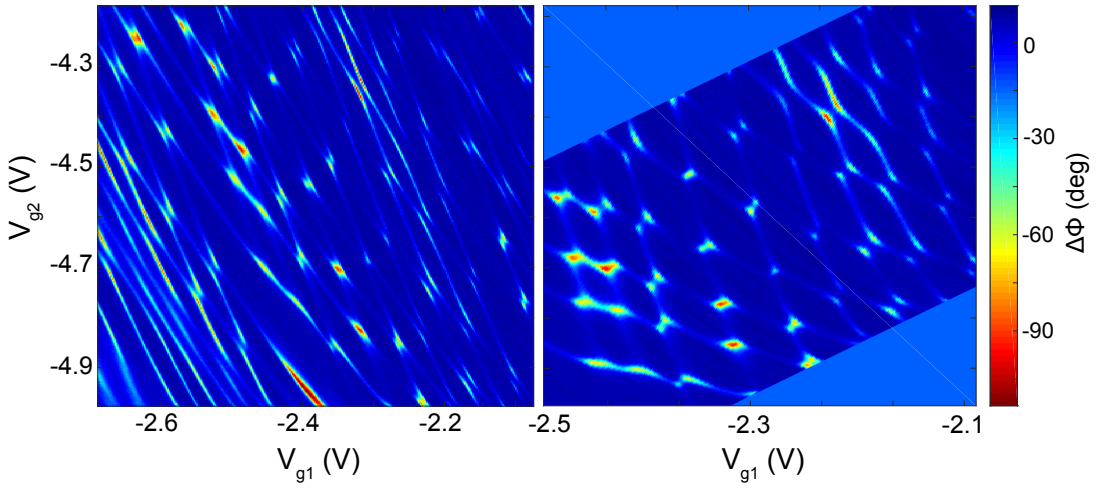

FIGURE 5.9: A charge stability diagram measured with video-mode data acquisition without (left) and with (right) cross-capacitance correction. The signal-to-noise ratio is significantly improved by adjusting the STO varactors.

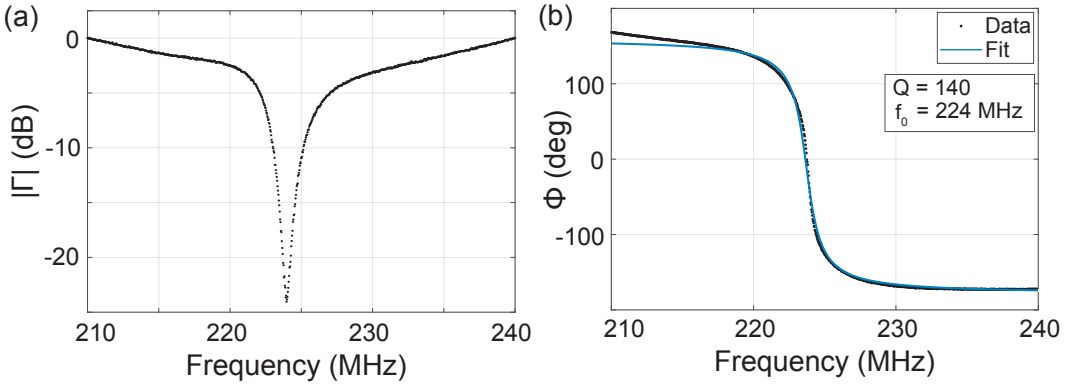

FIGURE 5.10: (a) The reflected amplitude and (b) phase around resonance after improving impedance matching with the STO varactors for a carbon nanotube double quantum dot on doped silicon. The phase fit suggests a quality factor of 140.

5.3 Challenges

This section outlines some of the main challenges faced when working with double quantum dots. In terms of fabrication, carbon nanotubes contacted undesirably were the main source of shorts, especially for substrates with nanotube density higher than ideal. Shorting nanotubes and electrostatic sparks were probably the most common means of rendering a device useless (whether single or double dot - see Appendix A.2.2 for more details). We now focus on challenges more specific to double dot devices.

Top gate shorts

A major issue that reduced the yield of double dot devices dramatically was shorts between top gates and nanotubes. As discussed in Appendix A.2, the oxide layer between the nanotube and the conductive part of the top gate is introduced by three successive thermal evaporations of thin layers of aluminium, each followed by exposure in atmosphere for oxidation. Unfortunately, this is a rather unreliable way of introducing a good quality oxide, as there is no proper control over the procedure and moisture from the atmosphere comes in contact with the aluminium metal at every stage. Many times this results in a bad quality oxide, which leads to current leakage between the nanotube and the top gate. Good oxides where found to be quite resistive ($\sim$ 1 GΩ), while bad ones much more conductive ($\sim$ 1 MΩ). Whether the oxide is good or not appeared to be a random occurrence among devices, with about 30% of devices showing leakage. In such cases, the device is unusable. A way around this issue is to perform the aluminium evaporations in an evaporator that allows for controlled oxygen flow, thus eliminating the need to vent the system after each aluminium layer. Such evaporators provide much more flexibility and control, as well as monitoring of the oxide thickness. On the other hand, switching to bottom gated device geometries (suspended nanotubes) [50] could help avoid the problem of leaky oxides all together (see Section 6.2 for more details).

Substrate hysteresis

Initially, devices on undoped silicon would show some kind of hysteresis at low temperatures when performing any kind of measurements. The hysteresis would dominate over the measurements even days after cool down, making experiments impossible to perform. A DC transport and an RF measurement of a narrow-gap carbon nanotube double quantum dot on undoped silicon revealing such a hysteresis are shown in Figure 5.11(a) and (b), respectively. Although it is not clear what causes this major hysteresis, it was speculated that applying a back gate voltage on an undoped silicon substrate at room temperature could be the cause. Typically, this is avoided at low temperatures, but it was taken as a common practice at room temperature when evaluating the nature and quality of a device. Applying a back gate voltage on undoped silicon substrates

was avoided since then, and the corresponding substrates were considered to be of bad quality and replaced (see Appendix A.1 for more details).

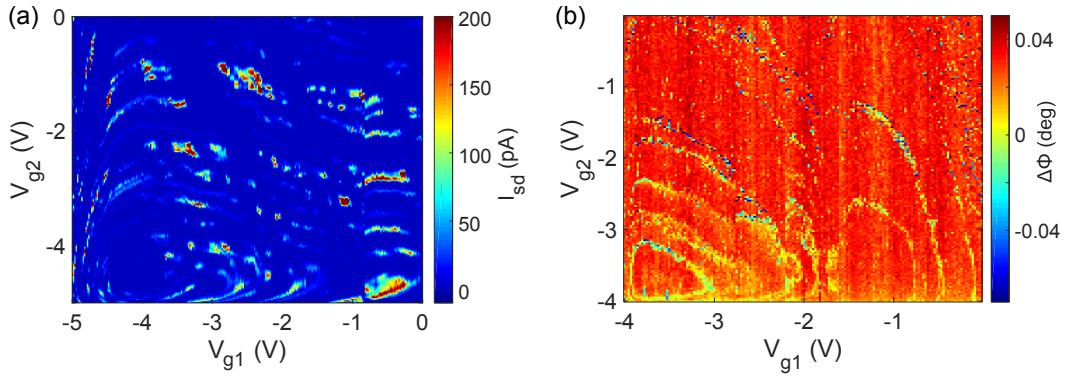

FIGURE 5.11: Measurements of a narrow-gap carbon nanotube double quantum dot on undoped silicon revealing major hysteresis as seen in: (a) DC transport, (b) relative phase. The dramatic effect of the hysteresis dominates over measurements.

Pulse tube noise

Another issue that arose during RF measurements of double quantum dots was noise in the frequency spectrum of measurements, coming from the pulse tube of the dilution refrigerator. The noise was dominant at the fundamental frequency of the pulse tube, 1.4 Hz [140–142]. This issue was observed after introducing STO varactors on the PCB, since measurements from that point onwards were much more sensitive. The noise can be seen in the measurements of relative reflected amplitude and phase shown in Figure 5.12(a) and (b), respectively. The noise appears as periodic lines in the background, whose number depends on how long the measurement takes. Upon turning the pulse tube off, the noise would disappear, suggesting its source was mechanical vibrations. This issue was resolved by taping down firmly all DC wires in the cryostat with low-temperature rated tape and avoiding free hanging cabling subject to physical vibrations.

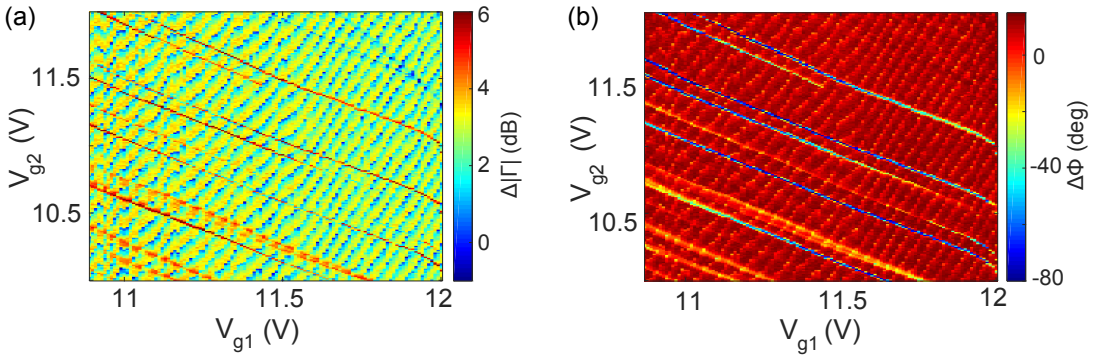

FIGURE 5.12: Pulse tube 1.4 Hz background noise in RF measurements as seen in: (a) relative reflected amplitude, (b) relative phase.

Chapter 6

Conclusion and Outlook

6.1 Overview of Work

This thesis presents experimental results aiming towards the implementation of a solid-state quantum computer, focusing on fabrication and measurements of carbon nanotube quantum dots. Carbon nanotubes are presented as an attractive candidate material for hosting qubits. The physics of few-electron quantum dots is discussed, and a detailed fabrication procedure for top-gated carbon nanotube quantum dots is given, along with relevant tips and challenges.

The steps towards the customisation of a dry dilution refrigerator to allow for (a) low electron temperatures and (b) high-frequency techniques are discussed. The former involves multi-stage custom-made filters that attenuate electromagnetic noise in the cryostat, resulting in demonstrated electron temperatures of 13 mK. The latter includes a setup for radio-frequency reflectometry and high-frequency arbitrary waveforms. Radio-frequency reflectometry is presented as a fast and non-invasive way to measure the charge state of quantum dots by coupling the resonant circuit to the source lead of the device. The steps towards readout optimisation are outlined. Radio-frequency reflectometry is also investigated as a way to perform capacitance spectroscopy on molecules (or nanoparticles) with a simplified device geometry.

The fabrication and usage of quantum paraelectric-based voltage-tunable varactors are presented as a novel technique for achieving reliable in situ perfect impedance matching and frequency tuning of a resonant circuit at temperatures down to 6 mK. This technique uses a strontium titanate substrate and works reliably in strong magnetic fields, is easy to implement, and does not add significant complexity to the circuit architecture. The varactor fabrication procedure is outlined, along with PCB alterations to host such

varactors. The ability to perfectly match the resonant circuit to the impedance of the line and tune its resonant frequency is demonstrated for a system with and without a quantum dot device. Using a carbon nanotube quantum dot, it is shown that the signal-to-noise ratio and charge sensitivity are improved significantly by driving the system closer to impedance matching. A charge sensitivity of 4.8 $\mu e/Hz^{1/2}$ was obtained, which is comparable with measurement techniques that use superconducting spiral inductors, and it is among the best reported to date.

In addition, characterisation and measurements on carbon nanotube double quantum dots are presented, with attempts for high-frequency gate modulation and tunnel coupling tuning. A video-mode data acquisition technique is introduced as a fast way to perform RF measurements on such devices. This technique demonstrates an integration time of $\sim$1 µs per point, and allows for the effects of gate electrodes to be observed in situ upon varying the corresponding voltage.

6.2 Future Work

This section outlines a few perspectives emerging from the presented work, and some directions in which further experiments could be taken.

Suspended nanotubes

The fabrication procedure of top-gated carbon nanotube quantum dot devices has been exploited with success. One disadvantage of such devices is that nanotubes are exposed to various stages of processing (for example, several PMMA coatings), which can lead to possible contamination and introduction of defects [37]. In addition, nanotubes are in contact with the substrate, and subject to any electrical potential fluctuations induced by the substrate [67]. A way around these two drawbacks is to adapt bottom gated devices using the experimental technique of nanotube stamping [143–146]. This technique can be used to obtain ultra-clean devices, reducing both contamination and the effect of charge traps. Nanotubes in such devices are suspended, less susceptible to disorder, and exposed to a much cleaner environment, allowing for higher quality quantum dots.

Josephson parametric amplifier

A way to improve the signal-to-noise ratio of quantum state readout is to use a Josephson parametric amplifier (JPA) to amplify the reflected RF signal at the mixing chamber of the cryostat [106]. A JPA has a much lower noise temperature compared to the CITLF1 low-noise amplifier adapted for this thesis ($\lesssim$0.1 K as opposed to $\sim$ 7 K), therefore its noise contribution in the measurements is almost negligible [147]. From Equation 4.4, the noise power P_N of a JPA is at least 20 dB lower compared to the

noise of CITLF1. JPAs are usually used in conjunction with circulators, which have a relatively narrow frequency range of operation. For optimum performance, the resonant frequency should lie within the ideal operation range. This can be achieved by choosing a suitable inductor and tuning the resonance using the STO varactors, as discussed in Chapter 4. Incorporating a JPA in the RF reflectometry setup could greatly improve the signal-to-noise ratio and readout sensitivity.

Spin blockade

Spin blockade is usually identified by current suppression for reversed source-drain bias and it has been demonstrated in carbon nanotube double quantum dot devices [41, 73–75]. Such devices can be used to extract information on spin coherence (see Section 2.2.2.4 for more details). It is therefore of interest to investigate the relaxation and coherence times of spin qubits hosted in carbon nanotube quantum dots, while examining the limiting factors.

Isotropic purification

The carbon nanotubes grown for the work presented in this thesis had a natural abundance of carbon isotopes. The isotope ratio can be controlled before growth by using a carbon-containing gas (for example, methane) that has the desired isotope ratio. An interesting experiment would be to measure spin coherence times in carbon nanotube double quantum dots of different isotope ratios. Isotropically pure nanotubes ($\sim 100\%$ ^{12}C) should have the longest coherence times, while nanotubes of known isotope ratios (besides the natural ratio) can be useful for understanding how hyperfine interactions affect spin coherence.

Appendix A

Device Fabrication

This section outlines the fabrication procedure details for carbon nanotube quantum dot devices. The parameters presented were obtained after optimisation and they can be used as a good starting point for fabrication on similar equipment. Several fabrication tips and challenges are given.

A.1 Chemical Vapour Deposition

Single-walled carbon nanotubes were grown using chemical vapour deposition at the University of Basel (Nanoelectronics group of Prof. Christian Schönenberger). The author grew nanotubes with help from Dr. Andreas Baumgartner, who carried out more growths himself at a later stage. The growth procedure involves coating clean substrates with a solution that contains metallic catalyst nanoparticles, usually based on Fe, Co or Ni. The carbon nanotube formation starts at the nanoparticles when the right conditions are met. The size of the catalyst particle correlates to the diameter of the resulting nanotube. Broadly speaking, particles of a few nm in size favour the formation of single-walled nanotubes, while particles of tens of nm in size favour the formation of multi-walled nanotubes [148, 149]. The concentration of the particles determines the growth density. Methane of natural abundance (98.89% ^{12}C and 1.11% ^{13}C) was used as the carbon-containing gas required to initiate growth. Initially, two different catalyst recipes were used, and the second recipe was retained for later growths. The recipes include the following main ingredients:

Recipe 1:

- $Fe(NO_3)_3$-$9H_2O$
- $RuCl_3xH_2O$

- Al_2O_3
- Solvents: water, methanol, ethanol, IPA
- Growth temperature: 850 °C

Recipe 2:

- $Fe(NO_3)_3$-$9H_2O$
- MoO_2Cl_2
- Al_2O_3
- Solvents: water, methanol, ethanol, IPA
- Growth temperature: 950 °C

Each recipe had a catalyst-to-solvent concentration of 1:25 and the aim was to achieve a density of about one nanotube per 25 μm^2. More details about the preparation and optimisation of the recipes are given by M. Graber [150]. A schematic of the CVD system used is shown in Figure A.1. The growth uses hydrogen, methane and argon. The relative flow of each gas is 0.07, 0.4 and 1, respectively. The growth steps are given below:

1. **Substrate and catalyst preparation**
   The substrates are cut using a diamond pen or dicing saw (1×1 cm size). They are sonicated in acetone for 10 minutes, followed by another 10 minutes in IPA, and dried with nitrogen gas. The catalyst nanoparticle solution is sonicated for at least 2 hours, since the nanoparticles tend to cluster together when in a solution; therefore if not agitated, the growth could be problematic.

2. **Substrate coating**
   One drop of catalyst nanoparticle solution is added on each substrate and the substrates are spun to disperse the nanoparticles on the surface. Coated substrates are loaded into the centre of the CVD system. Since the growth quality highly

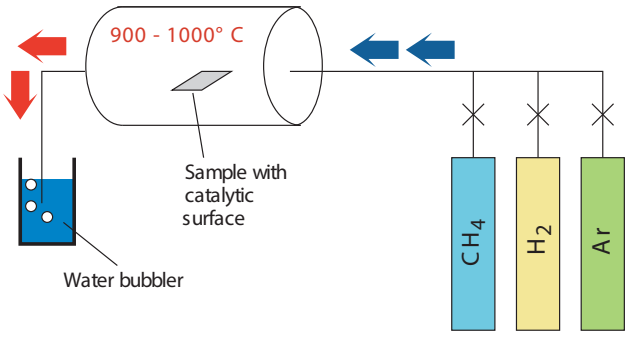

FIGURE A.1: Schematic diagram of the chemical vapour deposition system used for carbon nanotube growth. *Adapted from Ref* [150].

depends on temperature, no more that 4 substrates[1] should be loaded to prevent temperature variations between different substrates.

3. **Growth procedure**
   The process starts by letting argon flow through the tube for a minute, followed by a minute of hydrogen and methane. It is essential that all oxygen and other impurities are flashed out. Methane is turned off and the temperature is now set at the required growth temperature, depending on the catalyst solution used. At this stage, argon and hydrogen are flowing (heating up with hydrogen flowing is good for cleaning). When the desired temperature is reached, argon is turned off (otherwise the other gases will be diluted and growth might not occur) and methane is turned on and left to flow with hydrogen for about 10 minutes. Then, the methane and the heater are turned off, while argon is turned back on. The system is left to cool down with argon and hydrogen flowing. At about 200 °C, all gases can be turned off and the substrates can be unloaded. If unloading happens at higher temperatures, oxygen from the atmosphere could contaminate the growth.

Carbon nanotubes were grown on doped and undoped silicon substrates with the specifications outlined below. For undoped silicon devices, it was speculated that using the substrate as a back gate at room temperature introduces a major hysteresis problem in measurements at low temperature, even days later (see Section 5.3 for more details). That being a sign of bad wafers, undoped silicon of different specifications was used for later fabrication procedures. Nevertheless, undoped substrates were not used as a back gate again.

- **Degenerately doped silicon** - Boron dopants, 350 µm thickness, terminated by 280 nm of SiO_2 (wet process), single-side polished, resistivity of <1.5 mΩcm.
- **Undoped silicon (initially)** - 350 µm thickness, terminated by 280 nm of SiO_2 (wet process), single-side polished, resistivity of >10 kΩcm.
- **Undoped silicon (later)** - 525 µm thickness, terminated by 290 nm of SiO_2 (dry process), single-side polished, resistivity of >7 kΩcm.

All wafers were provided by PI-KEM Ltd.

[1] The number depends on the temperature profile of the CVD system being used and the size of the substrates.

A.2 Quantum Dot Device Fabrication

The fabrication steps for nanodevices were optimised by the author and they are outlined below. At this stage, it is assumed that nanotube growth has already been done. The fabrication was carried out at the clean room facilities at the London Centre for Nanotechnology.

1. **Bond pads and alignment marks**
   The substrates are briefly cleaned with IPA after growth, to remove possible residues from the catalyst nanoparticle solution, and dried with nitrogen gas. The substrates are then coated with MicroChem PMMA 950A4 electron resist and spun at 4000 rpm, resulting in a resist thickness of 200 nm. The substrate is baked at 150 °C for no more than 1 minute. Alignment marks and bond pads designs are exposed on the substrate using electron beam lithography (EBL) and developed in MIBK-IPA (1:3) for 60 seconds. The next step is electron beam metal evaporation of titanium (6 nm) and gold (60 nm). After evaporation, the substrate is left overnight in acetone for lift-off. It is then rinsed in IPA and dried with nitrogen gas.

   - **Alignment designs** - All EBL designs were prepared using KLayout. A typical design includes 6 to 9 blocks, and each block has 12 bond pads. The bond pads for doped and undoped silicon have an area of 100×100 µm and 150×150 µm, respectively. The bond pads on doped silicon are smaller to reduce the stray capacitance of the device and possible screening effects the dopants might cause to microwave signals. Inside each block there are 10 arrays of crosses, which are used to identify local nanotubes. Each cross is 1×1 µm in size and there is a 10 µm distance between adjacent crosses. Bond pad and alignment mark designs for undoped devices are shown in Figures A.2(a) and (b), respectively. Note that the crosses in Figure A.2(b) are shown next to each other only to indicate their pattern.

2. **AFM and device designs**
   Atomic force microscopy (AFM) is used to locate nanotubes with respect to their local alignment marks. Therefore, it is important for the substrates to be as clean as possible, otherwise locating nanotubes might not be trivial. Tapping mode AFM is used to minimise interaction with the surface. After suitable nanotubes are located in the vicinity of the alignment marks, device designs are prepared. To ensure design precision, the designs are overlapped with the AFM images, as shown in Figure A.3.

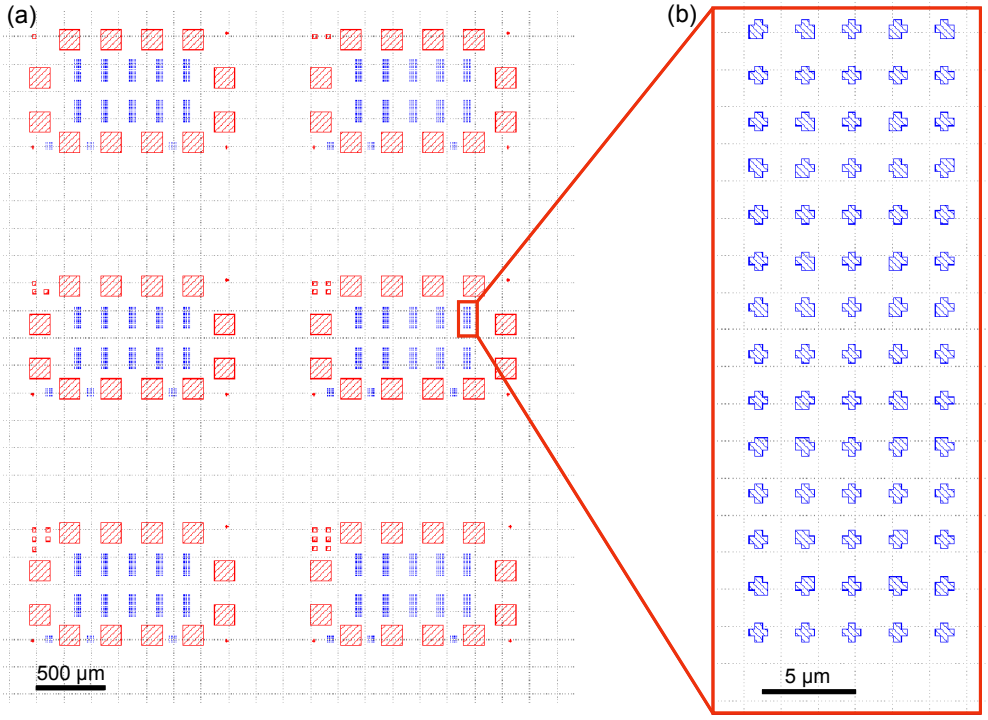

FIGURE A.2: Bond pad and alignment mark designs for undoped silicon devices implemented with EBL: (a) the whole design map, (b) a closer look to the arrays of crosses. The actual distance between each cross and its neighbours is 10 µm. Nanotubes are located with an AFM in reference to their nearby crosses.

3. **Device implementation**

   The substrate is coated, exposed and developed in the same way as in step 1. At this stage, everything is exposed except the top gates. Metallisation follows with 2 nm of titanium and 60 nm of gold. The substrate is left overnight in acetone for lift-off, followed by rinsing in IPA and drying with nitrogen. A similar procedure is carried out for the exposure of top gates. This time, the evaporation consists of a multi-stage thermal evaporation of aluminium to form the oxide layer between the top gate and the nanotube. The process involves deposition of 1-2 nm of aluminium followed by 5 minute exposure in atmosphere for oxidation. The aluminium evaporation and oxidation are carried out three times. Finally, 60 nm of gold are evaporated on top of the aluminium oxide and the substrate is left overnight in acetone for lift-off. It is then rinsed in IPA and dried with nitrogen gas. Optical images of a substrate holding 36 single quantum dots on undoped silicon and two double quantum dots on doped silicon are shown in Figure A.4(a) and (b), respectively.

4. **Room temperature characterisation**

   After the fabrication process is completed, each substrate is cut to pieces such that each piece contains one or two bond pad blocks. Each piece is glued on the PCB

using GE varnish and a device is bonded with gold wire of 25 µm diameter. Room temperature DC measurements are performed to characterise the overall quality of device and the nature of the nanotube (see Section 3.1.1 for more details). Devices that pass all the tests are cooled down for low temperature characterisation.

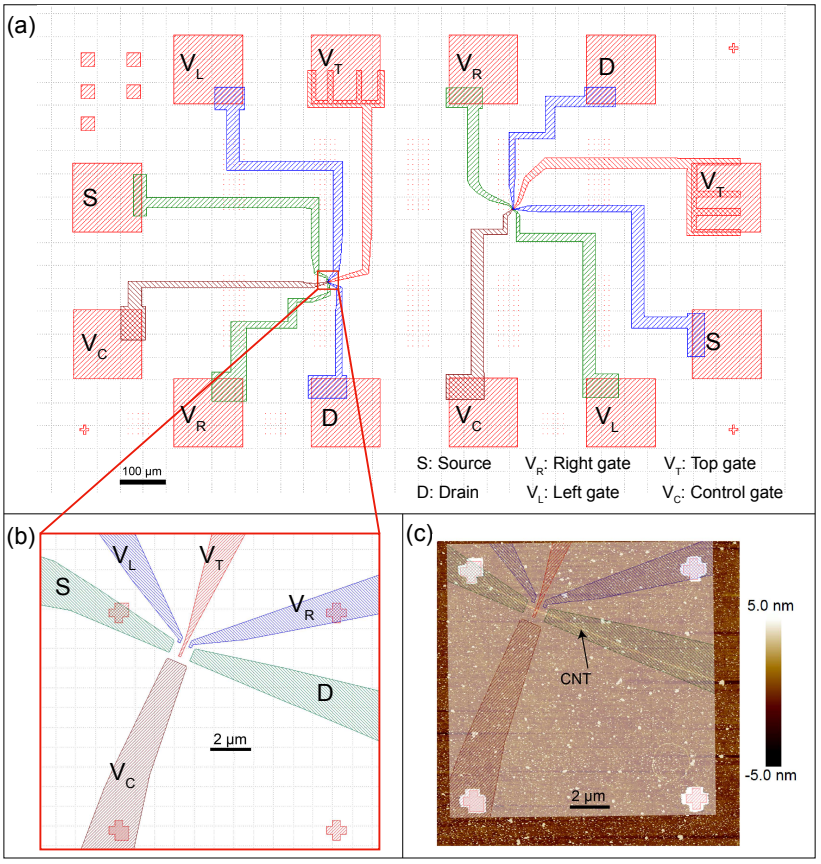

FIGURE A.3: (a) Designs for two carbon nanotube double quantum dot devices on undoped silicon. (b) A closer look to the double dot region of the device on the left. (c) An overlap of the double dot region with an AFM height image of the nanotube to be contacted.

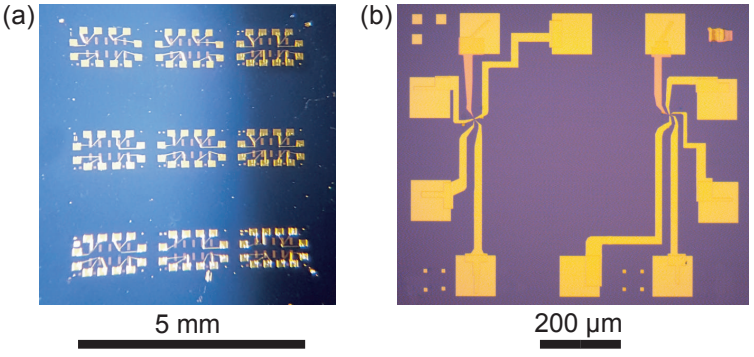

FIGURE A.4: Optical images of devices after fabrication. (a) Undoped silicon with 36 single quantum dots, (b) two double quantum dots on doped silicon.

The EBL system used for device fabrication was Raith-150 TWO 30 kV. The parameters used during fabrication are summarised in Table A.1. All the parameters are set, except for the beam current which is measured. To reduce the exposure time, coarse and fine structures were exposed with different parameters. Here, coarse and fine are the structures larger and smaller than 1 µm, respectively.

Parameters	Coarse Structures	Fine Structures
Aperture (µm)	60	30
EHT (kV)	10	30
Dose (µC/cm^2)	110	380
Step size (nm)	45	8
Write field (µm)	100	100
Beam current (pA)	950	320

TABLE A.1: The parameters used for coarse and fine structures during electron beam lithography fabrication steps. Coarse and fine refer to structures larger and smaller than 1 µm, respectively.

A.2.1 Fabrication Tips

This section summarises a few tips that can be used during fabrication and could increase the yield and/or quality of devices.

1. **Inspection** - An optical microscope with dark field imaging is probably one of the best ways to inspect a substrate throughout the fabrication steps. Such inspection is advised after every step.

2. **Sonication** - It is advised not to sonicate a substrate with nanotubes (for example after growth). It was observed that doing so reduces the nanotube density. Sonication after growth should only be an option if the nanotube density is too high for the substrate to be used for fabrication.

3. **Locating nanotubes** - Using an AFM to locate nanotubes gives a very good idea of the topography in the nanotube vicinity, but it usually takes a long time to complete, especially for dozens of devices. An alternative way would be to use a scanning electron microscope (SEM). When imaged properly, nanotubes on insulating surfaces (like SiO_2) have apparent diameters that are about 50 times larger than their corresponding AFM height profile. Steps on how to optimise SEM imaging for nanotubes are given by A. Baumgartner et al. [67] and T. Brintlingeret al. [151]. The disadvantage of using an SEM is that amorphous carbon could be disposed on the substrate and contaminate the nanotubes that are being imaged; however, an SEM could speed up the process significantly.

4. **PMMA baking** - The baking times should not exceed 1 minute, otherwise the PMMA becomes hard to sufficiently remove. This is particularly important after implementation of bond pads and alignment marks, since locating nanotubes with an AFM becomes much harder with major PMMA residues on the substrate surface.

5. **EBL alignment** - For EBL steps that involve alignment to a pre-existing structure, it is advised that any alignment marks used are made in such a way that the location of their centre point is not ambiguous. This can be done by making alignment marks smaller or having them grow smaller at their centre. This could minimise the alignment errors during exposure.

6. **Titanium evaporation** - Titanium is a metal that oxidises very easily, therefore getting rid of oxygen in the evaporation chamber is essential. Pumping overnight might not be enough, therefore filling the evaporation chamber with titanium vapour (with the substrate shutter closed) can be beneficial. Typically, the chamber pressure reduces rapidly as the gaseous titanium is oxidised by the oxygen left in the chamber. A good pressure for evaporating titanium is 5×10^{-7} mbar or lower.

7. **Aluminium evaporation** - Aluminium evaporates rapidly and controlling its evaporation might not be trivial. To create the oxide layer of top gates, the substrate should be mounted directly above the aluminium source and the current through the source should be increased slowly to allow for uniform thermalisation. Increasing the current fast could result in a rapid evaporation of aluminium that well exceeds the 2 nm required.

8. **Problematic lift-off** - Some times after lift-off, bits of PMMA that were meant to be removed remain on the substrate and could cause shorts or other problems to the device. A way around this is to bombard the substrate with acetone blows using a pipette or an acetone bottle. If the problem persists, sonicating the substrate for bursts of no more than a second might help (sonicating for longer might damage neighbouring devices).

9. **Probe station** - After nanotubes are contacted, a probe station can be used to obtain an I-V curve for each device. The I-V curve can give a good indication whether the nanotube is semiconducting or narrow-gap. A narrow-gap nanotube would measure 10s of nA with a bias of 10 mV, while a semiconducting nanotube would measure about 1 nA or less. This is a quick way to identify which devices are likely to have a narrow-gap nanotube. For this task, the user must be well grounded with respect to the devices to prevent electrostatic sparks that could render the devices useless.

10. **Cleaving devices** - At the end of the fabrication procedure, the substrates must be cleaved so that they can fit on the PCB. A neat trick for cleaving substrates involves the use of a diamond pen and a thin wire (about 0.3 mm in diameter). The pen is used to scratch the substrate near the edge of the cleaving line, and the wire is put underneath the scratch, aligned with the cleaving line. Holding the substrate down on one side and pushing down the other side with tweezers causes the substrate to break along the wire. It is recommended to clean the cleaved substrates in IPA, since cleaving can introduce lots of small silicon pieces on the surface.

A.2.2 Fabrication Challenges

There are many challenges that arise during fabrication of nanodevices. Some of them are tied to a particular piece of equipment; for example achieving a perfect alignment of a top gate between two plunger gates with an EBL system. Equipment-specific challenges are not discussed here, as they may not apply to newer, state of the art machines. Some more general challenges are outlined below, along with potential solutions.

Nanotube shorts

If the nanotube density on the substrate is high, sometimes nanotubes are unintentionally contacted in addition to the targeted nanotube. This introduces shorts between different parts of the device (for example a nearby nanotube can short the source lead to the left plunger gate). Such nanotube shorts can easily be identified (might be a bit difficult with high-resistivity nanotubes) before cool down. This is done by applying a few volts on each plunger gate individually while the rest of the device is grounded, and measuring current leakage to ground. The undesired nanotube can be burned off by stepping the applied voltage to a sufficient value. This is much easier to do at room temperature and air, since the nanotube is destroyed by heating up and burning in oxygen. This process typically requires a voltage that drives a current of 10s of µA through the shorting nanotube. A plot of the current response in such a case is shown in Figure A.5(a). When the nanotube is destroyed, the current immediately drops to zero. If several nanotubes are shorting, the current might reach zero in steps, as shown in Figure A.5(b). Alternatively, shorting nanotubes can be cut using an AFM tapping mode tip in contact mode. A tapping mode tip is generally stiffer than a contact mode tip (usually made of silicon and silicon nitride, respectively). Therefore, a tapping mode tip in contact mode with a large force can be used to run over and cut a shorting nanotube, as shown in Figure A.6. Utilising tips in such a way makes them blunt, however.

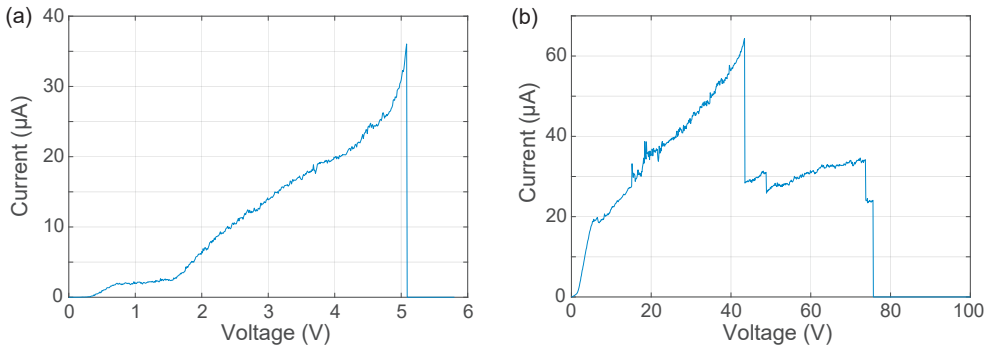

FIGURE A.5: The current as a function of applied voltage, through: (a) a single shorting nanotube, (b) multiple shorting nanotubes. Each time a nanotube is burned off, there is a sudden current drop.

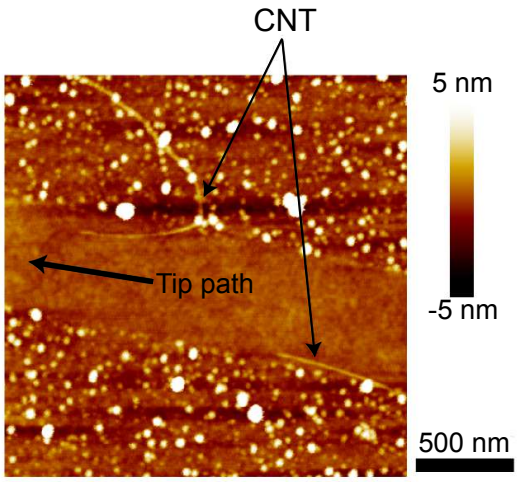

FIGURE A.6: An AFM height image of a shorting nanotube after it has been cut with a tapping mode tip used in contact mode.

Electrostatic sparks

After a nanotube is contacted with source and drain leads, the device is very sensitive to electrostatic discharge. Such a discharge mainly arises from human interaction with devices, for example during transportation, bonding, or mounting on a sample holder, and it is probably the most common way to destroy devices. The more resistive the substrate is, the easier it is for a device to be destroyed by electrostatic discharge. Therefore, devices on doped silicon are typically less likely to be blown up in such a way, but care must be taken in all cases. An SEM image of a destroyed device on undoped silicon is shown in Figure A.7(a). Here, a small static spark has destroyed a small part of the nanotube before the implementation of a top gate. In worse cases, a large spark can cause complete meltdown of the metallic leads of the device. Such a case is shown in Figure A.7(b), where a device on undoped silicon was obliterated. Therefore, it is recommended to be grounded at all times when handling devices, especially when

bonding or cleaning. For storage and transportation, only gel anti-static boxes should be used (boxes from Gel-Pak are a good choice). It is also a good practice to coat substrates with PMMA if they are to be transported far away. For cleaning, plastic beakers are usually a better option than glass counterparts. Polytetrafluoroethylene (PTFE) beakers are a good option for such a task.

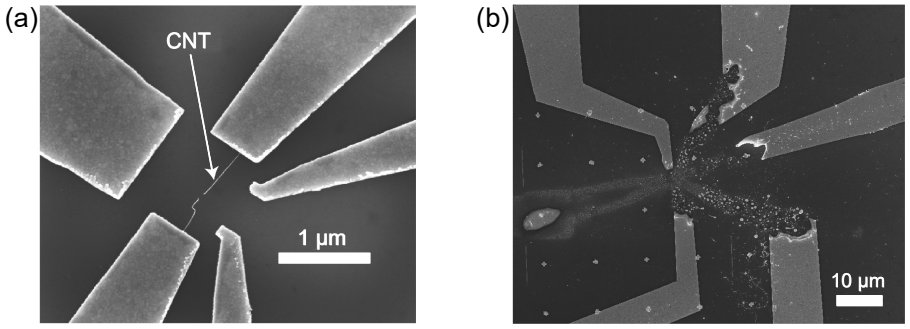

FIGURE A.7: SEM images of destroyed devices on undoped silicon. (a) A small static spark has destroyed a part of the nanotube before the implementation of a top gate. (b) A large electrostatic spark has completely destroyed the metallic leads of the device.

Minimising parasitic capacitances

Having a small parasitic capacitance is essential for RF reflectometry experiments. Since $Q \propto \sqrt{L/C}$, where L is a chosen inductance and C includes the stray capacitances of the PCB and the device, small parasitic capacitance results in a higher quality factor Q and a higher signal-to-noise ratio. To minimise parasitic capacitance on the PCB, there should be no ground plane around or underneath the resonant circuit (that includes the inductor, the substrate and anything between them). The lead onto which the source of the device is bonded, should be as small as possible, since itself acts as a parallel plate capacitor. Moreover, there should be no metallic part of the sample holder directly underneath the resonant circuit. Finally, inductors of high quality factors rated around the frequencies of interest should be used. For the work presented in this thesis, the parasitic capacitance of a prototype PCB was as high as 0.62 pF, and following the suggestions outlined here, it was reduced to 0.26 pF. To minimise the stray capacitance of the devices, the bond pad which is used for RF reflectometry should be made as small as possible. This is especially important for devices on conductive substrates and becomes less important for more resistive substrates.

Appendix B

RF Capacitance Spectroscopy of FePc Molecules

This appendix demonstrates how RF reflectometry can be used as an alternative way to perform spectroscopy on arbitrary molecules or nanoparticles. A simple device geometry is introduced that can be used with a variety of molecules to readout discrete quantum states without the need of high accuracy positioning or precision. The technique is demonstrated with measurements on iron phthalocyanine (FePc) molecules.

B.0.1 Introduction

For DC electrical characterisation of molecules, it is common to have source and drain leads capacitively coupled to the molecule of interest, so that electrons can tunnel on or off upon varying the electrochemical potential of the molecule with a gate electrode [86]. A schematic of a device that allows for such measurements is shown in Figure B.1(a). This approach usually involves a non-trivial fabrication procedure with the yield of devices being highly variable. Radio-frequency capacitance spectroscopy is a technique that requires only a single tunnel contact to study an arbitrary molecule or nanoparticle. This simplifies the fabrication procedure, along with the fact that there is no need for precise positioning. The molecule of interest if randomly deposited on an RF electrode and it is capacitively coupled to a gate electrode used to tune its electrochemical potential. A schematic of a device that allows for RF capacitive spectroscopy is shown in Figure B.1(b).

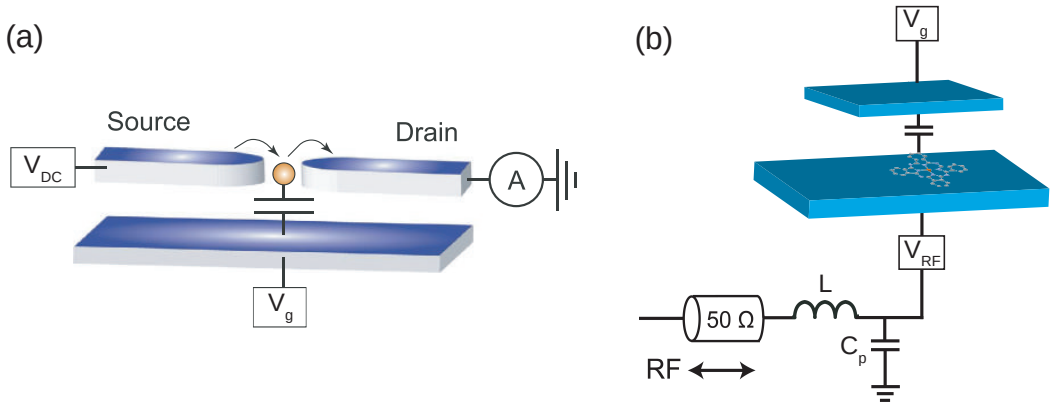

FIGURE B.1: Schematics of: (a) a conventional DC measurement device, and (b) a device that uses radio-frequency reflectometry for capacitive spectroscopy. The molecule on the RF electrode is iron phthalocyanine. *Adapted from Ref* [86].

A system such as the one shown in Figure B.1(b) can be parametrised by an effective resistor ΔR and an effective capacitor ΔC in parallel. The two satisfy the following expressions [86, 87]:

$$\Delta R = \frac{4k_B T_e}{e^2\alpha^2\gamma}\left(\frac{\gamma^2}{\omega^2}+1\right)\cosh^2\left(\frac{-e\alpha\Delta V_g}{2k_B T_e}\right) \tag{B.1}$$

$$\Delta C = \frac{e^2\alpha^2}{4k_B T_e}\left(\frac{\omega^2}{\gamma^2}+1\right)^{-1}\cosh^{-2}\left(\frac{-e\alpha\Delta V_g}{2k_B T_e}\right) \tag{B.2}$$

where e is the electron charge, k_B is the Boltzmann constant, T_e is the electron temperature, α is the corresponding lever arm, γ is the tunnel rate, ω is the drive frequency and ΔV_g is the corresponding change in gate voltage. If the tunnel rate and the drive frequency are comparable ($\gamma \sim \omega$), dissipation in the system can be significant [152, 153]. However, if the tunnel rate is considerably faster than the drive frequency ($\gamma \gg \omega$), the effective resistance ΔR diverges and the junction is capacitive only. Here, only this limit is considered.

The phase response $\phi(f)$ as a function of frequency f is given by Equation 3.4. The latter can be used to fit the phase around resonance and extract the quality factor Q, that relates to the relative phase $\Delta\Phi$ by:

$$\Delta\Phi = -2Q\Delta C/C_\Sigma \tag{B.3}$$

where C_Σ is the total capacitance of the device.

B.0.2 Implementation and Measurements

The experiment was conducted with FePc molecules, deposited on undoped silicon. The fabrication procedure involves the following steps:

1. **RF electrode fabrication**
   RF electrodes were fabricated using electron beam lithography and metal evaporation (10 nm Ti followed by 60 nm of Au).

2. **FePc deposition**
   The substrate was loaded in an scanning tunneling microscope preparation chamber and degassed overnight at 120 °C. A source of iron phthalocyanine molecules was heated to 350 °C and the deposition lasted about 5 seconds. These deposition times give a rough molecule coverage of approximately 1 molecule per 50×50 nm. The molecule evaporation was done by Dr. Toby Gill (Hirjibehedin group) at the London Centre for Nanotechnology.

3. **Atomic layer deposition**
   A thin layer of Al_2O_3 (about 5 nm) was deposited on top of the substrate. This step was done by Dr. Mark Buitelaar and Dr. Chiara Ciccarelli at the Cavendish Laboratory, University of Cambridge.

4. **Gate electrode fabrication**
   Gate electrodes that overlap the RF electrode by different area sizes were fabricated using electron beam lithography and metal evaporation (10 nm Ti followed by 60 nm of Au). An SEM image of the device is shown in Figure B.2. The device was bonded on a PCB and tested for current leakage before cool down.

Scanning electron microscope images of a Ti/Au RF electrode with and without FePc molecules are shown in Figure B.3(a) and (b), respectively. The molecules appear as bright spots on top of the metallic grains. Three individual molecules are circled for clarity. The apparent density is about 3 molecules per 50×50 nm. Having various gate electrodes that overlap the RF electrode differently allows for switching between different numbers of molecules during experiments.

For the resonant circuit, a surface mount inductor L=180 nH was used and the resonant frequency was f_0=583 MHz, corresponding to a parasitic capacitance of 0.41 pF. By stepping the voltage on the gate electrode and measuring the relative phase, phase dips begin to appear, indicating electrons tunneling on or off a molecule. Phase dips were only observed for the gate electrodes with the smallest area overlap, possibly because the large number of molecules probed by the larger area electrodes was causing the dips

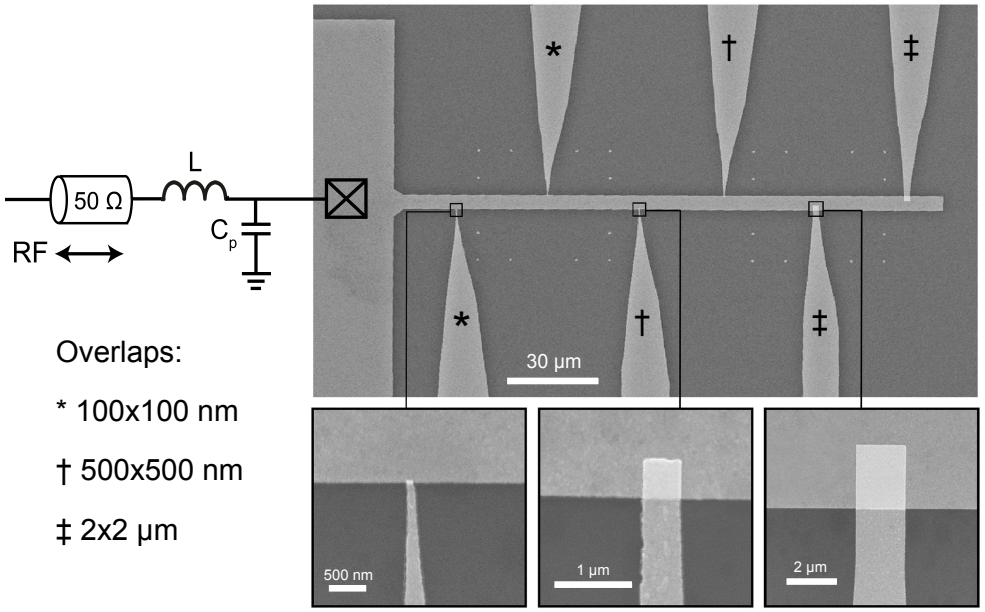

FIGURE B.2: An SEM image of the device used for RF capacitance spectroscopy measurements on iron phthalocyanine molecules. The central lead is used as an RF electrode and the overlap of each gate with the lead is indicated.

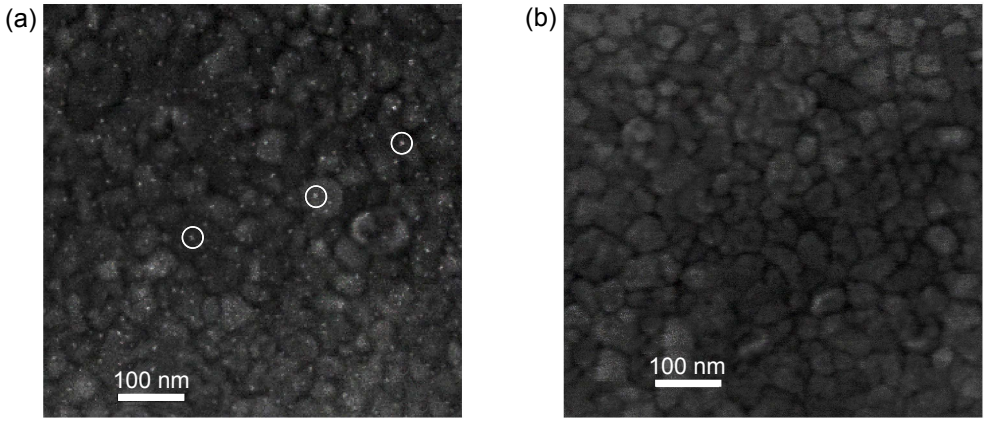

FIGURE B.3: SEM images of a Ti/Au RF electrodes (a) with and (b) without evaporation of FePc molecules. The molecules appear as bright spots on top of the metallic grains. Three individual molecules are circled for clarity. The apparent density is about 3 molecules per 50×50 nm.

to overlap considerably. Such phase dips can be fitted with Equation B.2, using the lever arm α and electron temperature T_e as fitting parameters. Such a fit is shown in Figure B.4, where α=0.083 and T_e=130 mK. The width of the dip is proportional to T_e/α and the amplitude is proportional to α^2/T_e [86]. These two relations (for width and amplitude) can be used to determine T_e and α independently. Phase dips can be broadened by the RF power, which can elevate the electron temperature (see Section 5.2 for more details). The experiment was performed with room temperature pi-filters

and RL/RC filters on the mixing chamber as the only DC filters (see Section 3.3.2 for more details). For an optimal signal-to-noise ratio and no dip broadening, an RF power of -100 dBm was delivered to the device. As expected, the phase dips become less deep with increasing lattice temperature, nearby vanishing above 300 mK. This is shown in Figure B.6, where a phase dip is plotted for various lattice temperatures. Such a device could be used as a primary thermometer [86, 87].

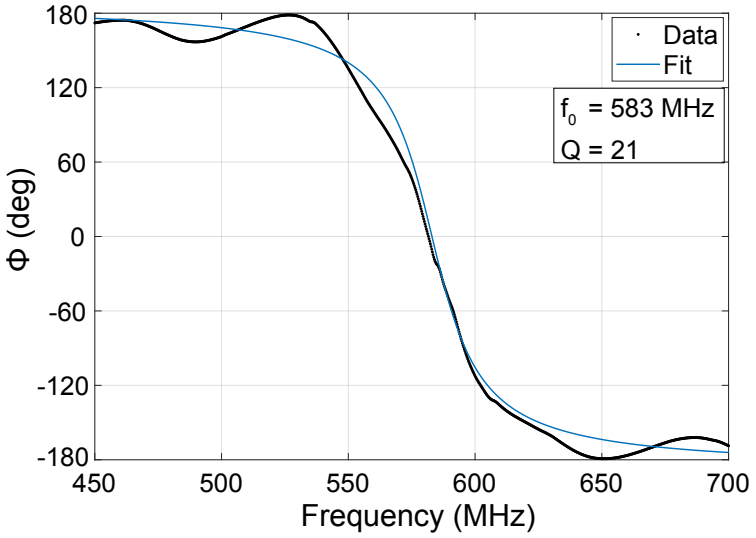

FIGURE B.4: The phase as a function of carrier frequency for the resonant circuit of the device. A curve fit (blue line) as used to extract the quality factor Q=21. The resonant frequency is 583 MHz.

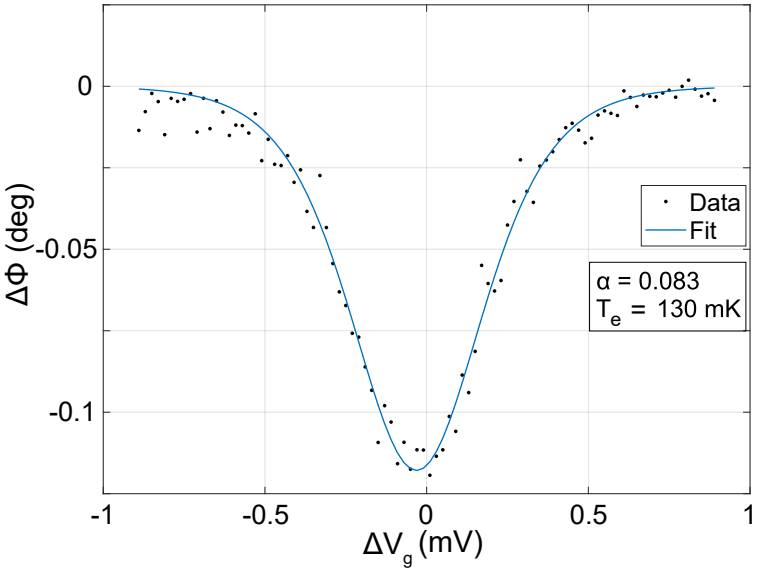

FIGURE B.5: The relative phase as a function of gate voltage. A phase dip is shown with its corresponding curve fit, along with extracted lever arm α and electron temperature T_e. The RF power used is -100 dBm.

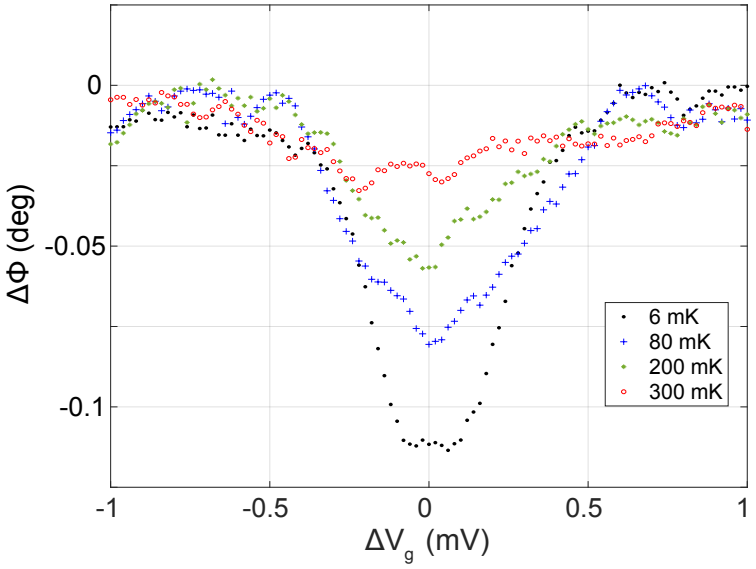

FIGURE B.6: A phase dip as a function of gate voltage measured at various lattice temperatures. The RF power used is -100 dBm.

By measuring the relative phase as a function of gate voltage and magnetic field, the phase dips are expected to shift with respect to the field. A theoretical model of this behaviour for copper phthalocyanine is outlined by B. Siegert et al. [154], while a similar behaviour is expected for iron phthalocyanine. Such a measurement was taken from zero to 9 T. The data is shown in Figure B.7, where the background was subtracted. Three indicated phase dips appear to move (each on its own way) with respect to the magnetic field.

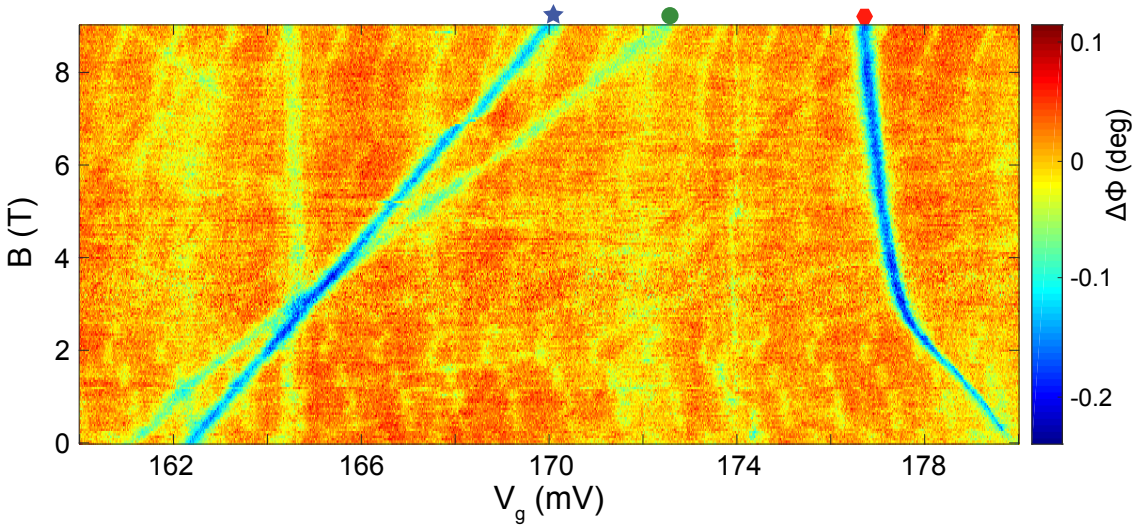

FIGURE B.7: The relative phase as a function of magnetic field B and gate voltage V_g measured with an RF power of -100 dBm. The shifting of three independent phase dips with respect to the field is apparent.

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