Electron Transport in Two-Dimensional Molybdenum Disulphide

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I, Alice Charlotte Sackville Hamilton, confirm that the work presented in this thesis is my own. Where information has been derived from other sources, I confirm that this has been indicated in the work.

Abstract

This thesis will describe the experimental details used to make two-dimensional field-effect transistors using monolayer and bilayer transition metal dichalcogenides, including the fabrication of new sample holders required to cross between multiple experimental set-ups. Electron transport in these devices is measured at room temperature and at low temperature in a dilution refrigerator with a base temperature below 10 mK.

Atomic force microscope lithography is explored as a technique for locally functionalising the surface of the device to create nano-features, with particular interest paid to the formation of quantum dots. Transport curves before and after lithography demonstrate the change in transport characteristics.

A comprehensive study of device behaviour at room temperature is carried out. The effects of pumping and heating on the device are measured and discussed. Improvements in the transport occur from the removal of charge traps and the improved contact between the Ti/Au contact and the crystal.

Low temperature ($\leq$10 mK) measurements of bilayer MoS_2 devices show evidence of Coulomb blockade and the presence of small, unstable, naturally formed quantum dots. We suspect that interface states due to naturally occurring atomic defects in MoS_2 which result in Fermi level pinning at room temperature are being probed here. The evolution of these states with magnetic field is measured, for devices positioned parallel and perpendicular to the magnetic field.

Impact Statement

The work in this thesis will directly affect future students in the research areas of molybdenum disulphide, MoS_2, and low temperature physics, as well as making significant contributions to the current public understanding. Two-dimensional MoS_2, now known for its exciting electronic and optical properties, requires more research to fully understand the possible commercial applications, and to reliably reproduce data with a thorough understanding of the influential parameters.

The current understanding of MoS_2 transport behaviour will be enhanced by the work presented in this thesis. In particular the study of charge traps and mid-gap interface states which both alter the transport properties unpredictably are studied in depth. This thesis will help the realisation of exciting potential applications which may be limited by charge noise and defect states.

A theoretical model developed to explain modification of transport behaviour due to charge traps may prove to be beneficial to a wide range of academics. The model is not specific to MoS_2 and could be used to analyse any device affected by changing charge trap occupation with time.

In addition to scientific endeavours, the expertise gained from practical aspects such as fabrication of a new sample holder, set-up of an atomic force microscope lithography station, and set-up of a new dilution refrigerator, is described here in detail. This work can be used as a reference for future students, providing enough background and specific experimental details for them to tackle a whole range of problems in the lab.

Acknowledgements

I would first like to thank my supervisor Dr. Mark Buitelaar, a fountain of knowledge. Thank you for the hard work and dedication you gave this work, and for the support you gave me. Jointly setting up a new laboratory equipped for exciting new physics has been a pleasure. Thank you to Dr. Byron Villis, who made many of the measurements possible and was a constant source of practical information.

An experimental PhD is not possible without plenty of technical help, and I would like to thank John Langdon, and Tom Hamer, for teaching me about design software and for realising my (tiny, intricate) sample holders. Thank you to Dr. Guy Matmon for having such a well-equipped lab. Thank you to Dr. Nicolas Constantino, Vijay Krishnan, Dr. Chris Graham and Dr. Wing Ng, who helped out countless times in the cleanroom.

My family, adopted family, and friends have been so supportive throughout. Thank you to Jon, who went through all of the ups and downs with me and helped me get to the finish line. Thank you to my mother, father, and brother for endless support and proofreading. Thank you to Liz, Rachel, Kerri, Helen, James, Emily and Henry for always being there.

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Chapter 1

Introduction

Two-dimensional materials such as graphene, transition metal dichalcogenides (TMDs), silicene, and phosphorene, contribute to an active area of research. Their naturally reduced dimensionality provides a platform for device fabrication on a very small scale. Potential applications include electronics [14, 15], opto-electronics [16], spin-valley tronics [17, 18], photonics [16, 19], and quantum information processing [19], with the reduced dimensionality making the devices transparent and flexible. This work focusses on molybdenum disulphide, MoS_2, a member of the semiconducting TMDs.

MoS_2 is very widely studied due in part to its natural abundance. Few-layer crystals of MoS_2 ($<$100 $\mathring{A}$ thickness) were isolated as early as 1966 by mechanical exfoliation [20], and monolayer MoS_2 was isolated in 1986 using lithium intercalation [21]. However, the excitement surrounding research into two-dimensional materials only really took off in 2004, after the study of novel electronic properties of single-layer graphene [22]. The stability of an isolated two-dimensional material had potential for new, smaller, devices, but the lack of bandgap in graphene rendered it unsuitable for some applications such as switching in electronics. Other two-dimensional materials such as the family of TMDs show a range of electronic behaviours from metallic to semiconducting to superconducting. Semiconducting TMDs can be used in a number of electronic applications including field-effect transistors [23, 36, 37], quantum emitters [38], photodetectors [39], memory storage [40], and photovoltaics [41].

The bandgap in semiconducting TMDs is thickness dependent. Reducing the number of layers has been found to dramatically alter the electronic band-structure, particularly in the monolayer limit, at which the bandgap shifts from indirect to direct. Strong quantum confinement leads to high exciton binding energies; spin-orbit coupling lifts the spin degeneracy in the monolayer; strong spin-valley coupling could be exploited for valleytronics.

Few-layer MoS_2 crystals have been fabricated into field-effect transistors (FETs) with mobilities over 200 $cm^2V^{-1}s^{-1}$ [23], but the transport behaviour is still not well understood. Hysteresis is seen in measurements of current as a function of gate voltage; it has been attributed to common adsorbants such as water and oxygen behaving as charge traps [24, 25, 26]. These can be removed by pumping and annealing on the device [27]. Defects in the MoS_2 were found to dominate transport in a number of studies [28, 29, 30, 31], and have been explored using a variety of techniques including scanning tunnelling microscopy [29], transmission electron microscopy [28], and conductive atomic force microscopy [31].

This work aims to enhance the understanding of MoS_2 transport properties, specifically single-electron transport resulting from nano-lithographic electronic confinement structures. This requires a more in-depth understanding of hysteresis, contact resistance, and defects. MoS_2 field-effect devices are fabricated and the changes in hysteresis are analysed at room temperature in different measurement environments. Charging and discharging of charge traps in the MoS_2 FET are suspected to be the dominant source of hysteresis, and a model is developed in this work which qualitatively explains the data.

Measurements at low temperature reveal single-electron transitions which we suspect to be defect states. An analysis of these zero-dimensional features in a magnetic field adds to the current understanding of the defect states. A nano-lithography technique undergoing development is presented in this thesis; it could be used to define MoS_2 quantum dots for analysis at low temperature, but would first require the fabrication of defect-free devices.

This thesis is structured as follows. Chapter 2 is a theoretical exploration of TMD physical and electronic properties and FET behaviour at room temperature. The chapter concludes with a discussion of how to interpret measurements of a quantum dot at very low temperature.

Chapter 3 describes the methods used for different experimental techniques. This includes an in-depth discussion of the development of a nano-lithography technique used to define quantum dots in MoS_2. Chapter 4 provides preparation details for experimental set-ups and device fabrication. Appendix A describes the development of a working shadow-masking method that had to be abandoned during this work due to technical issues.

Chapter 5 follows room temperature measurements of three bilayer MoS_2 devices in different environments to explore the effects on hysteresis in transfer curves. Hysteresis is likely to arise from the charging and discharging of charge traps during the course of the measurement. A model presented in the chapter was developed using this assumption, and qualitatively explains the changes in hysteresis. Appendix B presents rudimentary room temperature measurements of four tungsten diselenide, WSe_2, devices, which were too resistive to study further.

Chapter 6 briefly explores the effect of temperature on field-effect mobility, and continues to analyse three single-electron transitions seen in a bilayer MoS_2 device, measured at the dilution refrigerator base temperature T $\leq$10 mK. Appendix C shows data collected from a monolayer MoS_2 device at base temperature; it was too resistive to study further.

The work is concluded in chapter 7, with suggestions for further study.

Chapter 2

Theoretical Background

This chapter covers the theory required for the study of molybdenum disulphide field-effect transistors (MoS_2 FETs). The physical and electrical properties of MoS_2 are explored, along with basic FET transport behaviour.

Deviations from basic transport behaviour have been ascribed to MoS_2 defects, the possible origins of which are discussed. Quantum dots which are likely to be defects are observed at low temperature; quantum dot theory and an understanding of analysis of differential conductance measurements is covered here.

2.1 Transition Metal Dichalcogenides

Few-layer transition metal dichalcogenides have existed for a long time. MoS_2 crystals less than 100 $\AA$ thick were isolated using mechanical exfoliation in 1966 [20]; monolayer MoS_2 crystals were isolated using lithium intercalation in 1986 [21]. However, the excitement surrounding two-dimensional material research only really began in 2004, when graphene, a single layer of carbon atoms arranged in a honeycomb, was first isolated experimentally also using mechanical exfoliation [22]. Since then, single layers of silicene, hexagonal boron nitride, phosphorene, transition metal dichalcogenides, and others have also been studied. Graphene has excellent properties such as high electrical and thermal conductivities, flexibility, strength, and elasticity, making it useful for a wide range of applications in biomedicine [32], protective coatings [33], filtering membranes [34] and energy storage [35] amongst others. However, graphene is a semi-metal, with zero

bandgap, which is often undesired in electronics. Atomically thin semiconducting transition metal dichalcogenides (TMDs) such as molybdenum disulphide have a thickness dependent bandgap, leading to applications in electronics, including field-effect transistors [23, 36, 37], quantum emitters [38], photodetectors [39], memory storage [40], and photovoltaics [41].

2.1.1 Physical Structure

Bulk TMDs have a structure analogous to that of graphite: layers of covalently bonded atoms are stacked, with weak interlayer van-der-Waals interactions. In TMDs, each layer is made up of a plane of transition metal atoms (e.g. molybdenum (Mo), tungsten (W), niobium (Nb)) sandwiched between two planes of chalcogens, or group VI elements (e.g. sulphur (S), selenium (Se)), to form a trigonal prismatic geometry. Few-layer TMDs can be isolated in the same way as graphene, using mechanical exfoliation.

Figure 2.1(a) shows the TMD structure. Transition metal (chalcogen) atoms are shown in black (yellow). The lattice constant a is material dependent, taking values from 3.1 to 3.7 $\AA$ ($a = 3.15$ $\AA$ for MoS_2). Layers can be stacked in a number of ways, as shown in figure 2.1. Hexagonal stacking (2H) is the most common, with a stacking index $c = 2$. Distance between layers is ~ 6.5 $\AA$.

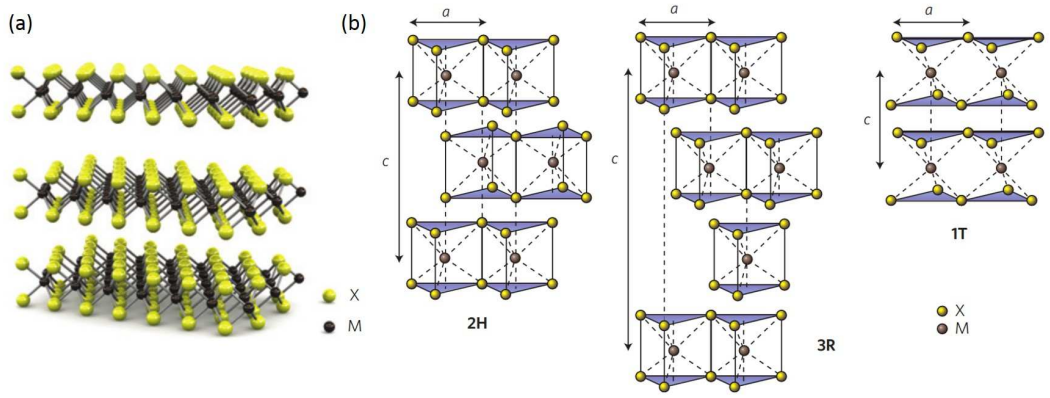


Figure 2.1: (a) Schematic representation of the TMD structure. Transition metal, M (chalcogen, X) atoms shown in black (yellow). (b) Schematic showing variation in interlayer stacking. c is a stacking index, a is the lattice constant. *Adapted from ref* [1].

The properties of some of the most studied TMDs are tabulated below.

Metallic, CDW, superconducting TMDs

Material	Superconducting transition temperature /K
$NbSe_2$	7.2 (ref. [42])
NbS_2	6.3 (ref. [43])

Semiconducting TMDs (ref. [44])

Material	1L bandgap /eV	bulk bandgap /eV
MoS_2	1.88	1.23
$MoSe_2$	1.57	1.09
WS_2	2.03	1.32
WSe_2	1.67	1.21

2.1.2 Band Structure

The majority of the work carried out for this thesis has been done on bilayer molybdenum disulphide, MoS_2. MoS_2 is a semiconductor, with an indirect bandgap in bulk form ($E_{bulk} = 1.23$ eV) that switches to a direct bandgap for monolayer MoS_2 ($E_{1L} = 1.88$ eV). As the number of layers decreases from bulk to monolayer, the magnitude of the indirect transition increases while the direct transition stays much the same. This results in a crossover from an indirect to direct bandgap semiconductor; in the monolayer the direct bandgap is at a lower energy. The evolution of band structure with crystal thickness is illustrated in figure 2.2.

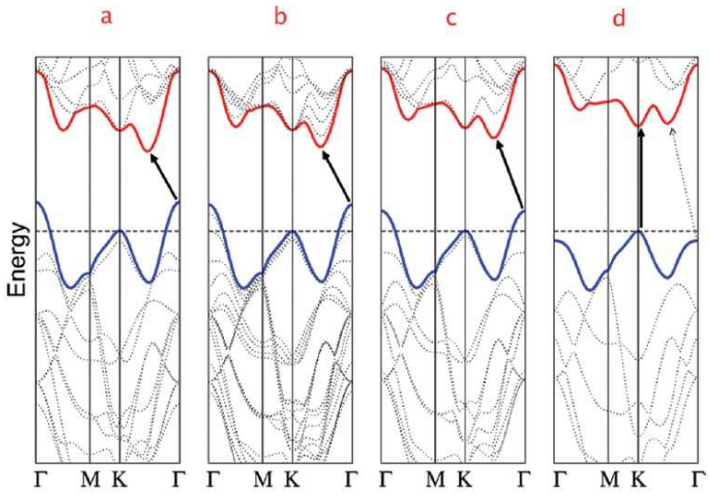


Figure 2.2: The band structures for (a) bulk, (b) 4 layer, (c) bilayer and (d) monolayer MoS_2 are shown, with the lowest energy transitions marked on with solid arrows. Red (blue) solid lines mark the edges of the conduction (valence) band respectively. (a) Bulk MoS_2 has an indirect bandgap. (b), (c) As the number of layers decreases, the magnitude of the indirect bandgap increases, but the direct bandgap does not vary significantly. (d) The indirect bandgap increases further in the monolayer, making the direct transition lower in energy. *Adapted from ref* [2].

2.2 Semiconductor Transport

2.2.1 Field-Effect Transistors at Room Temperature

A field-effect transistor consists of a semiconducting channel separated from a metallic gate electrode by an insulator, and contacted by metallic source and drain electrodes, shown schematically in figure 2.3.

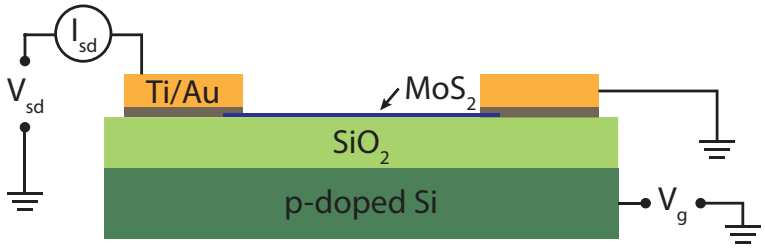


Figure 2.3: Schematic of a MoS_2 back-gated field-effect transistor. Source-drain (V_{sd}) and gate (V_g) voltages control source-drain current (I_{sd}) through the MoS_2 channel. The gate used in this work is highly doped silicon; the source and drain are made of titanium (grey in figure) and gold (orange in figure).

The first transistor was made in 1954 out of silicon [45], which is still a widely used transistor material today [46], with electron mobilities up to 1350 $cm^2V^{-1}s^{-1}$ [47]. As the research field has progressed, other materials have been introduced, outperforming silicon. For example, an intrinsic mobility of $>$100,000 $cm^2V^{-1}s^{-1}$ was estimated for a carbon nanotube field-effect transistor [48]. Thin (10 nm) MoS_2 FETs have achieved mobilities of 700 $cm^2V^{-1}s^{-1}$ [49]. When engineering a FET device, the impact of additional resistance due to the metallic contacts (section 2.2.2) and the choice of contact metal (section 2.2.3) on device performance must be taken into consideration. Important device characteristics at room temperature include the maximum ON current I_{max}, the threshold voltage V_T, and the mobility μ.

Figure 2.4 is a simplified semiconductor band structure demonstrating the effect of V_g on the electron density in the MoS_2 channel. At low V_g, the device is in its OFF state, and no current flows through. V_T is the threshold voltage: for $V_g > V_T$ the device is in its ON state and current flows increasingly with V_g. When a positive gate bias is applied, the energy levels in the MoS_2 are shifted down with respect to the electrochemical potential μ. For large positive gate bias, the conduction band edge will lie below μ, with nearby energy levels available for transport.

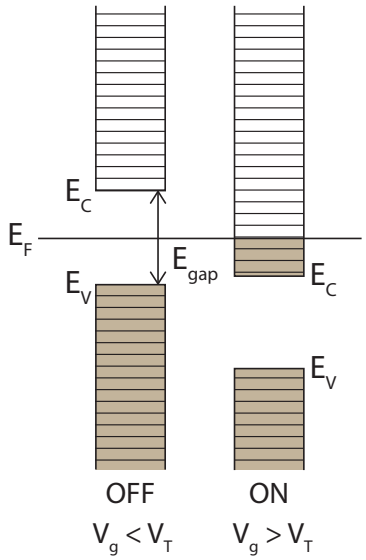


Figure 2.4: A simplified semiconductor band structure showing changes in electron density with gate bias.

Applying a bias V_{sd} between source and drain electrodes shifts their electrochemical potentials with respect to each other so $\Delta\mu = -qV_{sd}$, with q the electron charge. Nearby energy levels will contribute to transport through the channel, with the source (drain) continuously injecting (removing) electrons.

The occupation of energy levels is described by the Fermi distribution, thus only energy levels that lie within a few k_BT of the Fermi level are available for transport:

$$f_0(E-E_F) = \frac{1}{1+\exp[(E-E_F)/k_BT]} \tag{2.1}$$

where $E-E_F$ is the energy relative to the Fermi energy, $k_B = 8.62\times10^{-5}$ eV/K is the Boltzmann constant, and T is the temperature in Kelvin. At room temperature (300 K), k_BT is 26 meV. At low temperature (10 mK), k_BT is 0.86 μeV. As such, the thermal broadening in room temperature measurements can blur out fine details. Low temperature measurements offer higher resolution so that discrete energy levels may be resolved, as demonstrated in figure 2.5 comparing Fermi distributions at 300 K and 10 mK.

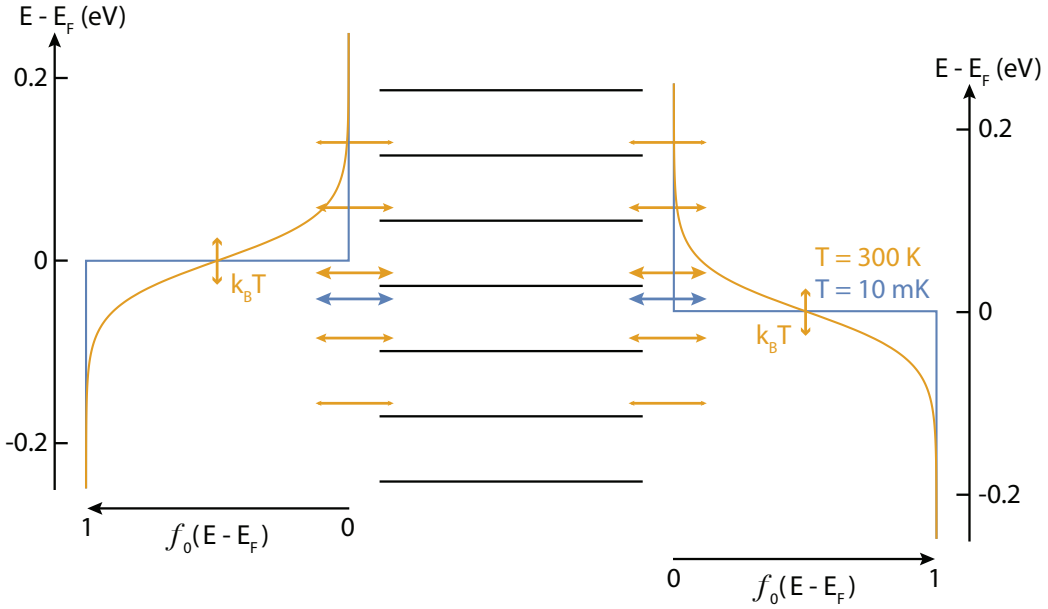


Figure 2.5: Fermi distributions at room temperature (orange) and low temperature (blue), with k_BT marked on for room temperature. Central black lines are energy levels, with arrows indicating possible transport paths. Low temperature measurements allow for resolution of discrete energy levels. There is a small source-drain bias for clarity.

2.2.2 Mobility

Electron mobility gives the speed of electron transport with an applied field. Application of an electric field, E, will cause electrons to move at a drift velocity, v_d, proportional to the force, qE. The velocity depends on the effective mass of the carriers, m, and on the level of scattering through the momentum relaxation time, τ_m [50].

$$v_d = \frac{q\tau_m}{m}E \tag{2.2}$$

Electron mobility, μ, is defined as the ratio of the drift velocity to the applied electric field, $v_d/E = q\tau_m/m$. Factors that can reduce mobility are phonon scattering and impurity scattering [51]: these both depend on temperature.

At room temperature phonon scattering is the dominant process. As the temperature decreases, phonon scattering is suppressed due to smaller lattice vibrations [3], resulting in an initial mobility increase. At very low temperatures, electrons move more slowly and thus the effect of impurity scattering increases. As the temperature decreases further, mobility decreases. Figure 2.6 shows mobility as a function of temperature for a monolayer MoS_2 field-effect transistor [3]. At high temperatures $\mu \propto T^{-\gamma}$ with $\gamma = 0.62 \pm 0.13$.

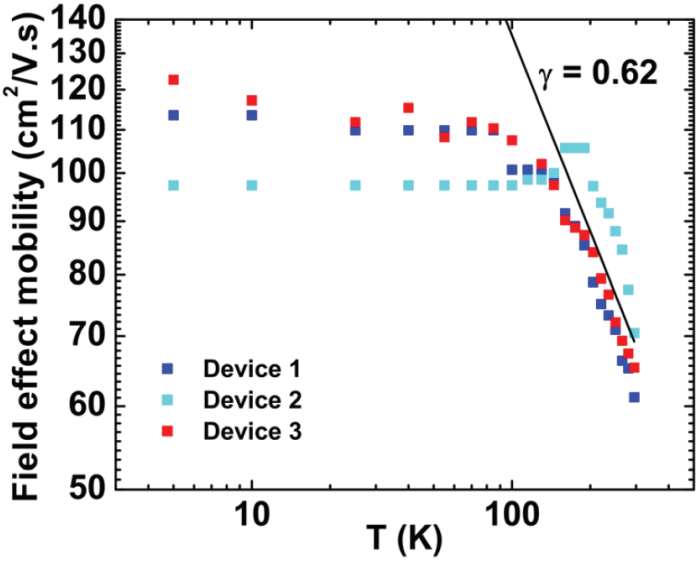


Figure 2.6: Mobility as a function of temperature for three monolayer MoS_2 devices. $\gamma = 0.62$ is a line of fit for $\mu \propto T^{-\gamma}$. *Adapted from ref* [3].

Field-effect mobility μ_{FE} is calculated using the following equation:

$$\mu_{FE} = \left[\frac{dI_{sd}}{dV_g}\right] \times \left[\frac{L}{WC_iV_{sd}}\right] \tag{2.3}$$

in which L and W are the channel length and width respectively, V_{sd} is the applied source-drain bias, dI_{sd}/dV_g is the gradient of the transfer curve when the device is in the ON state, and C_i is the capacitance per unit area:

$$C_i = \frac{\varepsilon_0\varepsilon_r}{d} \tag{2.4}$$

in which $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m is the vacuum permittivity, and ε_r = 3.9 for SiO_2, d is SiO_2 thickness.

This calculation gives a lower limit on the intrinsic MoS_2 mobility, as it does not account for contact resistance. Assuming an additional resistance of R_C at each contact, the total resistance is $R_{channel} + 2R_C$, leading to a reduced source-drain current I_{meas}:

$$I_{meas} = \frac{V_{sd}}{R_{ch} + 2R_C} < I_{ch} = \frac{V_{sd}}{R_{ch}} \tag{2.5}$$

2.2.3 Metal-Semiconductor Junctions

A metal with work function ϕ_M, when brought into contact with a semiconductor with an electron affinity χ_S, will form a Schottky barrier, with height $\phi_B = \phi_M - \chi_S$, as the Fermi levels of the two materials match. This type of junction is shown schematically in figure 2.7.

Using this relation, it should be possible to engineer an ohmic contact by choosing a contact metal with a work function similar to the electron affinity of the semiconductor so that $\phi_B \simeq 0$. However, it has been found experimentally that changing the contact metal has little effect on the Schottky barrier height in MoS_2 devices [28, 29].

Defect states lying inside the bandgap form a charge neutrality level, ϕ_0, to which the Fermi level is pinned, shown schematically in figure 2.8. The level of pinning can be quantified using a factor S, where S = 1 is no pinning (as in

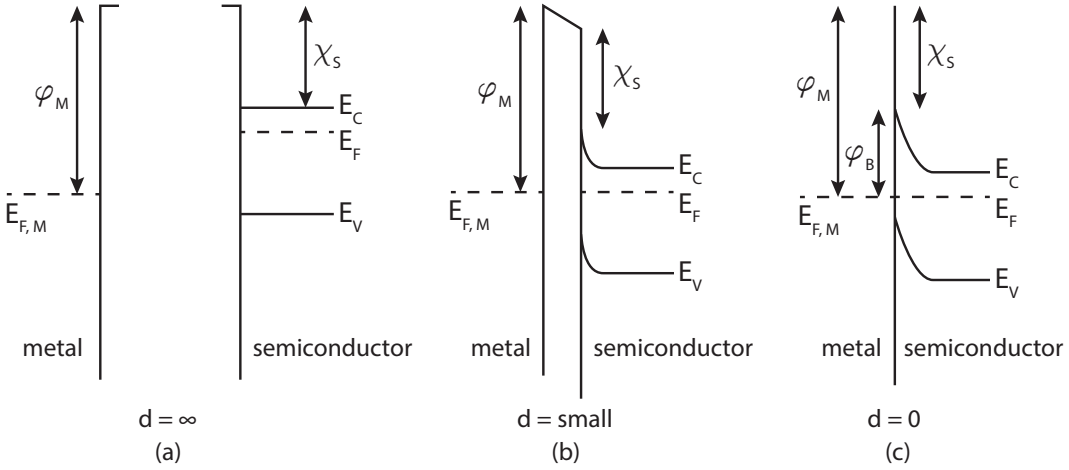


Figure 2.7: Metal-semiconductor junction at different separations, d. ϕ_M = metal workfunction, χ_S = semiconductor electron affinity, ϕ_B = Schottky barrier. E_F = Fermi energy, $E_{C,V}$ = conductance, valence band edges.

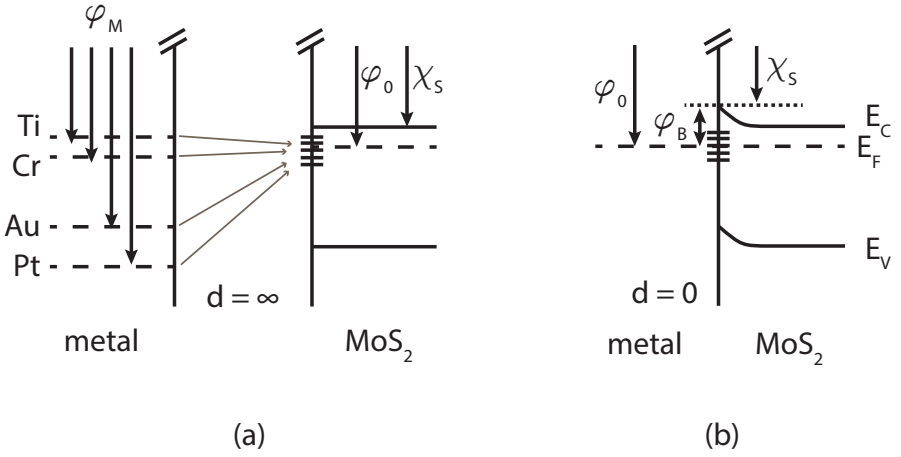


Figure 2.8: An illustration of the effect of Fermi level pinning on the height of the Schottky barrier formed in MoS_2 devices. The Fermi level is partially pinned to the charge neutrality level ϕ_0, leading to only a small dependence of ϕ_B on ϕ_M.

figure 2.7), and S = 0 is fully pinned, showing no change with different contact metals.

The Schottky barrier height can now be calculated as [28]:

$$\phi_B = S(\phi_M - \phi_0) + (\phi_0 - \chi_S) \tag{2.6}$$

2.2.4 Defects in MoS_2

Naturally occurring MoS_2 has a significant proportion of defects. Sulphur vacancies are very common due to their low formation energy, with an approximate density of 10^{13} /cm^2 determined using scanning transmission electron microscopy [28] and conductive atomic force microscopy [31], but these defects seem to have little effect on electron transport.

Defects with metallic behaviour have been observed with an approximate density of 10^{10}-10^{11} /cm^2, reducing the pinning factor S by a factor of 3 from 0.3 (pristine) to 0.1 (defective) indicating enhanced Fermi-level pinning at defects.

Conductive atomic force microscopy (c-AFM) measurements using nanocontacts $<$6 nm^2 showed these defects in positive and negative biases, surrounded by a ring depleted of electrons [31].

Scanning tunnelling spectroscopy (STS), scanning tunnelling microscopy (STM), and X-ray photoelectron spectroscopy (XPS) measurements displayed both n- and p-type conduction at different points across the same sample. XPS data showed a corresponding variation in the S:Mo ratio between 1.8:1 and 2.3:1, suggesting S-poor and S-rich (or Mo-poor) areas [29].

The metallic-like defect states lie inside the MoS_2 bandgap, close to the conduction band, resulting in the widely experimentally observed n-type behaviour. Proposed metallic-like defects include molybdenum vacancies, MoS_2 vacancies, anti-sites, and molybdenum substitution.

Gong et al [30] used density functional theory (DFT) to determine the mid-gap states to be Mo d-orbital character. The suggested mechanism of metal-S interactions resulting in weakened S-Mo bonding partially explains the observed Fermi-level pinning. The presence of defect states, which were not explored in this paper, could explain the further reduction of the pinning factor observed experimentally. Bampoulis et al [31] experimentally verifies this explanation. No structural modification of the top-most sulphur layer is seen in their AFM measurements, and so possible defects are limited to subsurface defects, such as molybdenum vacancies or anti-sites.

McDonnell et al [29] do see structural deformation of the MoS_2. It is suggested that pit formation reduces the strain caused by S-rich areas. However, given that their experiments are carried out on bulk MoS_2 instead of few-layer MoS_2, there could be an alternative explanation for pit formation. Simply, the act of exfoliating the top surface of the bulk crystal in preparation could result in a pitted top surface.

2.2.5 2D Density of States

Current through a device is dependent on the density of states, defined as the number of states per energy per unit area in real space, $\rho(E) = dN/dE$. In a two-dimensional material, the total number of states N_{2D} in a circle of radius k, in k-space, is given by

$N_{2D} =$ spin degeneracy $\times$ valley degeneracy $\times$ area in k-space $\div$ area occupied by one state (2.7)

$$N_{2D} = g_s \times g_v \times \pi k^2 \times \frac{1}{(2\pi/L)^2} \tag{2.8}$$

The electron density (number per unit area, N_{2D}/L^2) gives the Fermi momentum, k_F.

$$n = \frac{N_{2D}}{L^2} = \frac{g_s g_v}{4}\frac{k_F^2}{\pi} \tag{2.9}$$

$$k_F = \sqrt{\frac{4\pi n}{g_s g_v}} \tag{2.10}$$

The density of states in k-space, $\rho(k)$, is given by dN/dk:

$$\rho_{2D}(k) = \frac{dN_{2D}}{dk} = \frac{d}{dk}\frac{g_s g_v L^2 k^2}{4\pi} = \frac{g_s g_v L^2 k}{2\pi} \tag{2.11}$$

This can be converted to the density of states in energy space, $\rho(E)$.

$$\rho(E) = \frac{dN}{dE} = \frac{dN}{dk} \times \frac{dk}{dE} \tag{2.12}$$

dk/dE is calculated from the energy-momentum relation $E = \hbar^2 k^2/2m^*$, with m^* the effective mass.

$$\frac{dk}{dE} = \frac{d}{dE}\sqrt{\frac{2m^*}{\hbar^2}}E^{\frac{1}{2}} = \sqrt{\frac{m^*}{2\hbar^2}}E^{-\frac{1}{2}} \tag{2.13}$$

This gives the density of states per unit area (L^2) in energy space.

$$\rho_{2D}(E) = \frac{1}{L^2} \times \frac{g_s g_v L^2 k}{2\pi} \times \sqrt{\frac{m^*}{2\hbar^2}}E^{-\frac{1}{2}} = \frac{g_s g_v m^*}{2\pi\hbar^2} \tag{2.14}$$

In two dimensions, the density of states is independent of energy.

2.3 Quantum Dots

A quantum dot is an area in which electrons are confined in all dimensions. This spatial confinement results in a discrete energy spectrum similar to that of an atom. In low dimensionality materials such as the transition metal dichalcogenides discussed in this thesis (2D), carbon nanotubes (1D), or molecules (0D), there is some natural spatial confinement. Further confinement can be achieved in a number of ways experimentally, discussed below.

Quantum dots in graphene have been fabricated using graphene oxide as a potential barrier [52]. Growth by molecular beam epitaxy of indium arsenide (InAs) on gallium arsenide (GaAs) spontaneously forms quantum dots due to the small lattice mismatch between the two materials [53]. Electrostatic gating can be used for one- and two-dimensional materials to define a potential well [6, 54]. For transport measurements, a quantum dot must be capacitively coupled to source, drain and gate electrodes, pictured schematically in figure 2.9. The capacitance of the dot is the sum of the capacitances between source, drain and gate electrodes and the dot, $C_\Sigma = C_S + C_D + C_G$.

A dot with N electrons has energy $U(N)$.

$$U(N) = \frac{[-|e|(N-N_0) + C_S V_S + C_D V_D + C_G V_G]^2}{2C_\Sigma} + \sum_{n=1}^{N} E_n(B)$$

where V_i, $i = S, D, G$ are the potential biases applied to source, drain and gate electrodes, e is the electron charge, $E_n(B)$ is the n-th occupied energy level,

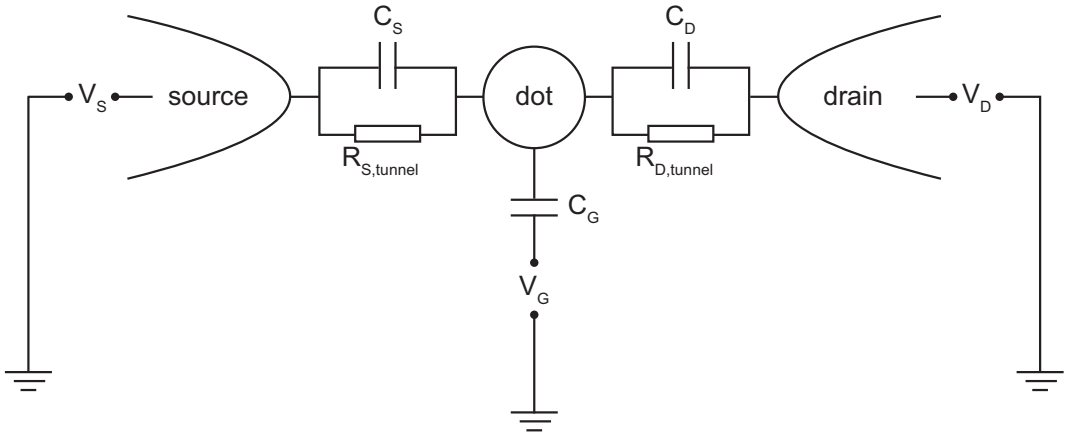


Figure 2.9: Quantum dot schematic. The gate voltage is capacitively coupled to the dot; there are tunnel barriers between the dot and the source, drain. Electron occupation of the quantum dot can be controlled by adjusting source-drain and gate voltages.

dependent on the magnetic field. The electrochemical potential $\mu(N+1)$ is defined as the energy difference between N- and $N+1$-electron states, $\mu(N+1) \equiv U(N+1) - U(N)$.

$$\mu(N+1) = (N - N_0 + \frac{1}{2})E_C - \frac{E_C}{|e|}(C_S V_S + C_D V_D + C_G V_G) + E_{N+1} + g\mu_B B[S_z(N+1) - S_z(N)] \tag{2.15}$$

where g is the Landé g-factor, $\mu_B = 5.79$ eV/T is the Bohr magneton, B is the magnitude of the applied magnetic field in Tesla, and $S_z = \pm 1/2$ is the z-component of the spin, $+1/2$ for spin-up, $-1/2$ for spin-down.

Electrons can tunnel on and off the dot via a tunnelling resistance R_{tunnel}, giving a typical charging time $\Delta t = R_{tunnel} C_\Sigma$. The energy required to add the $(N+1)$-th electron is the spacing between electrochemical potentials, $E_{add}(N) = \mu(N+1) - \mu(N)$.

$$E_{add}(N) = E_C + \Delta E_N + g\mu_B B[\Delta S_z(N+1) - \Delta S_z(N)] \tag{2.16}$$

For a spin degenerate system, $\Delta E_N = E_{N+1} - E_N = 0$ or ΔE, dependent on whether

the electron is added to a half filled energy level, or to an empty level ΔE higher in energy.

The ladder of electrochemical potentials, $\mu(N)$, spaced by E_{add} is shifted with respect to μ_S and μ_D when a gate bias is applied: increasing V_g lowers all $\mu(N)$.

Taking $\Delta E_N = 0$ in zero magnetic field, $E_{add}(N) = E_C = e^2/C_\Sigma$, the charging energy. Using the Heisenberg uncertainty relation $\Delta E \Delta t \geq h$ along with a requirement for the energy uncertainty to be much smaller than the charging energy presents a limit for the tunnelling resistance, $R_{tunnel} \gg h/e^2 = 25.8\ \mathrm{k\Omega}$, for electron number to be well-defined.

The charging energy is related to the capacitance of the dot $E_C = e^2/C_\Sigma$, which in turn is proportional to the dot size. A two-dimensional circular dot of radius r has a capacitance $C_\Sigma = 8\varepsilon_0\varepsilon_r r$. It follows that a smaller dot will have a smaller capacitance and thus a larger charging energy.

A typical 50 nm dot has a charging energy of 11 meV. This energy is smaller than the thermal energy at 300 K, 26 meV, so electrons at room temperature can easily bypass the tunnel barriers, thermally smearing out the zero-dimensional behaviour. To restore quantum dot behaviour, the electron temperature should be reduced until the thermal energy is much smaller than the charging energy, $k_B T \ll E_C$.

2.3.1 Separation of Energy Levels

The separation between energy levels, ΔE_N, can be visualised by modelling an electron on a quantum dot as a particle in an infinitely deep one-dimensional potential well. This is a simple way to treat electron confinement, and can be expanded to fit the quantum dot dimensions.

Solving the Schrödinger equation

$$-\frac{\hbar^2}{2m}\frac{\partial^2}{\partial z^2}\psi(z) = E\,\psi(z) \tag{2.17}$$

for a particle with mass m in an infinitely deep well of width d gives wavefunctions

$$\psi(z) = \sqrt{\frac{2}{d}} \sin \frac{\pi n}{d} z \tag{2.18}$$

and energies

$$E_n = \frac{\hbar^2 \pi^2 n^2}{2md^2} \tag{2.19}$$

for the n-th energy level as illustrated in figure 2.10.

Determining the energy levels of the quantum dot through measurement of the electron transport gives an estimation of the size of the dot, d.

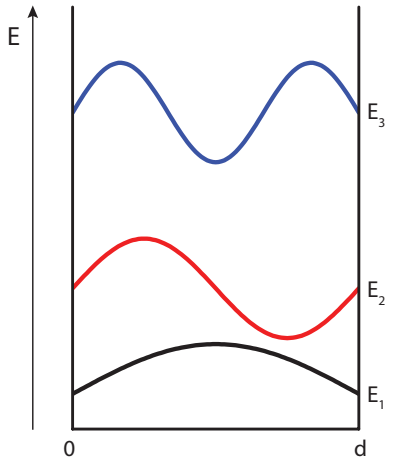


Figure 2.10: Solutions to the Schrödinger equation for an infinite one-dimensional potential well of width d for n = 1, 2, 3.

2.3.2 Differential Conductance

The position of energy levels in the quantum dot can be explored by plotting the differential conductance, dI_{sd}/dV_{sd}, as a function of the gate and source-drain biases. Electron transport on or off the dot can only occur when the electrochemical potential of a transition $N \rightarrow N \pm 1$ enters the bias window $\mu_S - \mu_D$. This has a number of consequences.

For zero bias, $\mu_S = \mu_D$, there is no transport through the dot except for gate bias values at which $\mu_{dot} = \mu_{S,D}$. This happens periodically, at $V_g = (N + \frac{1}{2})|e|/C_g$. When a new state enters or leaves the bias window, there is a step change in conductance, corresponding to a peak in the differential conductance. Figure 2.11

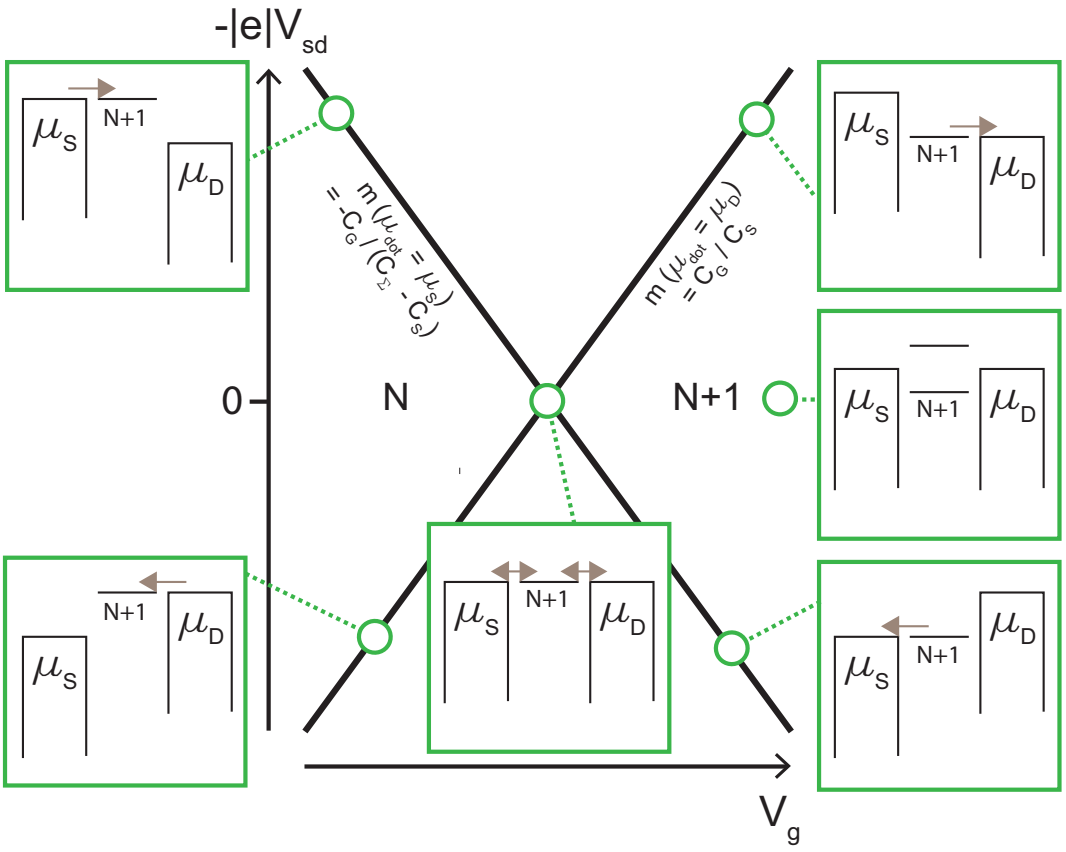


Figure 2.11: Peaks in differential conductance due to the $N \leftrightarrow N+1$ single-electron transition lining up with the source or drain potential. Inset figures show the relative positions of source, drain, and dot electrochemical potentials at different points in the plot.

shows the positions of the dI/dV peaks arising from the transition $N \leftrightarrow N+1$. The positive (negative) gradient corresponds to μ_{dot} lining up with the drain (source). These gradients are dependent on the system capacitances.

With the drain electrode grounded, $V_D = 0$, the electrochemical potential can be simplified to

$$\mu(N+1) = (N - N_0 + \frac{1}{2})E_C - \frac{E_C}{|e|}(C_S V_S + C_G V_G) + E_N + g\mu_B B[S_z(N+1) - S_z(N)] \tag{2.20}$$

$\mu(N+1)$ lines up with the drain when $\mu(N+1) = \mu_D = -|e|V_D = 0$

$$0 = -\frac{E_C}{|e|}(C_S V_S + C_G V_G) + \text{const.} \tag{2.21}$$

$$-|e|V_S = \frac{|e|C_G}{C_S} V_G + \text{const.} \tag{2.22}$$

giving the gradient m_D shown in figure 2.11:

$$m_D = \frac{|e|C_G}{C_S} \tag{2.23}$$

$\mu(N+1)$ lines up with the source when $\mu(N+1) = \mu_S = -|e|V_S$

$$-|e|V_S = -\frac{E_C}{|e|}(C_S V_S + C_G V_G) + \text{const.} \tag{2.24}$$

$$-|e|V_S = \frac{-|e|C_G}{C_\Sigma - C_S} V_G + \text{const.} \tag{2.25}$$

giving the gradient m_S shown in figure 2.11:

$$m_S = \frac{-|e|C_G}{C_\Sigma - C_S} \tag{2.26}$$

The source, drain, and gate capacitances quantify the effect of the applied voltages on the dot potential. The lever arm α_i, (i = S,D,G) is the ratio of the system capacitance C_i to the dot capacitance C_Σ.

Figure 2.12 shows the differential conductance through a single-electron transistor schematically. For each number of electrons on the dot N, there is a diamond-shaped region where there is no change in conductance.

At zero source-drain bias, scanning the gate bias results in peaks in the differential conductance whenever $\mu(N+1) = 0$. Taking $V_S = V_D = 0$, equation 2.20 becomes

$$\mu(N+1) = (N - N_0 + \frac{1}{2})E_C - \frac{E_C}{|e|}C_G V_G = 0 \tag{2.27}$$

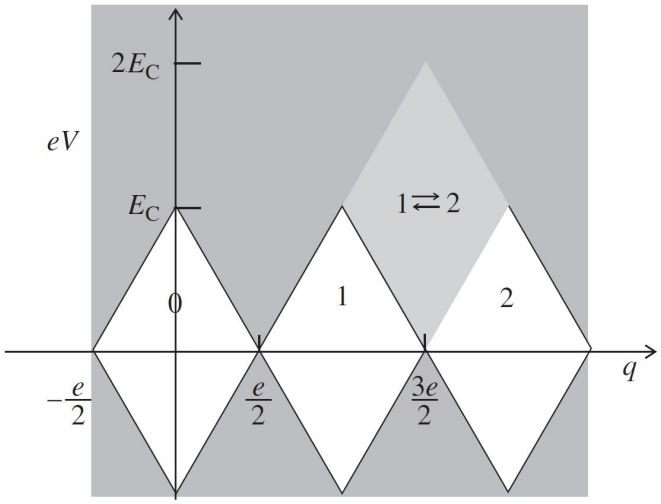


Figure 2.12: A plot of differential conductance as a function of source-drain voltage in eV and gate voltage expressed as a change in charge, q, through a single-electron transistor for N = 0,1,2. White areas correspond to zero differential conductance. *Adapted from ref* [4].

thus

$$V_G = \frac{(N+1/2)|e|}{C_G} \tag{2.28}$$

giving a diamond width

$$\Delta V_G = \frac{|e|}{C_G} \tag{2.29}$$

The tip of the diamond corresponds to the addition energy $|e|V_S = E_{add} = e^2/C_\Sigma$. The ratio of diamond height to width, both of which result in the addition of an electron, gives the gate lever arm α_G.

$$\alpha_G = \frac{C_G}{C_\Sigma} = \frac{|e|\Delta V_S}{\Delta V_G} \tag{2.30}$$

Source and drain lever arms can be extracted using the diamond edge gradients m_S (equation 2.26) and m_D (equation 2.23).

$$\frac{|e|\alpha_G}{m_D} = \frac{C_G}{C_\Sigma}\frac{C_S}{C_G} = \frac{C_S}{C_\Sigma} = \alpha_S \tag{2.31}$$

Using $C_S + C_D + C_G = C_\Sigma$,

$$\alpha_D = \frac{C_D}{C_\Sigma} = \frac{C_\Sigma - C_G - C_S}{C_\Sigma} = 1 - \alpha_G - \alpha_S \tag{2.32}$$

the absolute capacitances C_i are given by

$$C_i = \alpha_i C_\Sigma = \frac{\alpha_i e^2}{E_C} \tag{2.33}$$

2.3.3 Excited States

In cases where there is more than one energy level in the bias window, transitions can occur via either level, increasing the conductance. The excited states lie parallel to the diamond edges in differential conductance plots. Figure 2.13 labels the possible $N \leftrightarrow N+1$ transitions: between the two ground states, between an excited N state and the $N+1$ ground state, and between the N ground state and an excited $N+1$ state.

The mirroring of these states with source-drain bias is due to the two origins of an increase in differential conductance: an additional state to tunnel into (appearing parallel to the source), or an additional state to tunnel out from (appearing parallel to the drain). The current is dependent on the left and right tunnelling rates, $\Gamma_{L,R}$ [4]:

$$I \propto \frac{\Gamma_L \Gamma_R}{\Gamma_L + \Gamma_R} \tag{2.34}$$

If the tunnel barriers between the dot and the left and right contacts are asymmetric, then each excited state will only cause one extra peak, with a gradient parallel to the contact with the shorter tunnelling time. In the limit $\Gamma_L \gg \Gamma_R$, $I \propto \Gamma_R$; in the limit $\Gamma_R \gg \Gamma_L$, $I \propto \Gamma_L$. The resulting differential conductance peaks are shown schematically for both cases in figure 2.14.

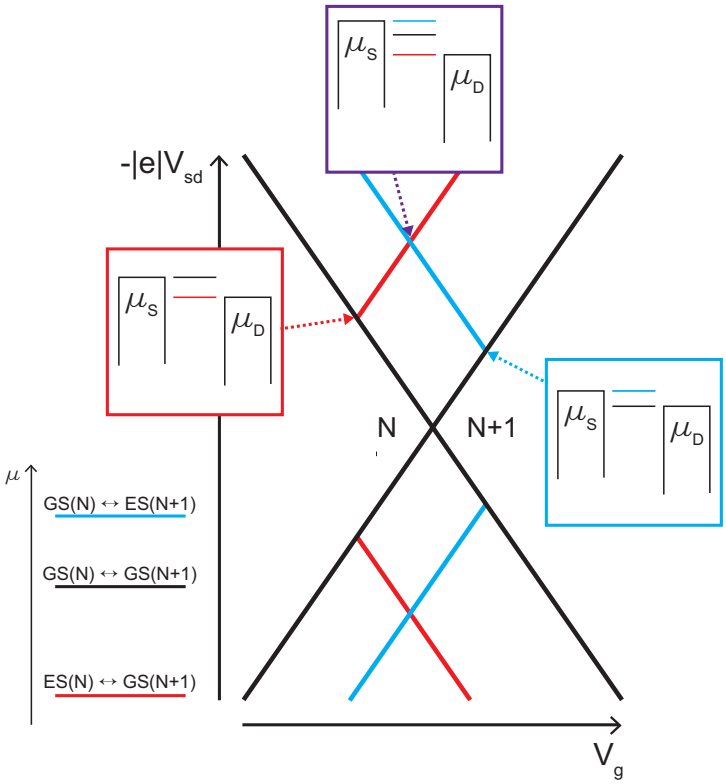


Figure 2.13: At larger source-drain biases, additional states may enter the bias window. At the point that a new state enters, an extra peak in differential conductance appears parallel to the ground state transitions. Inset figures show the relative positions of source, drain and dot electrochemical potentials at key points in the plot. The relative potentials of the three transitions in the plot is also shown. GS = ground state; ES = excited state.

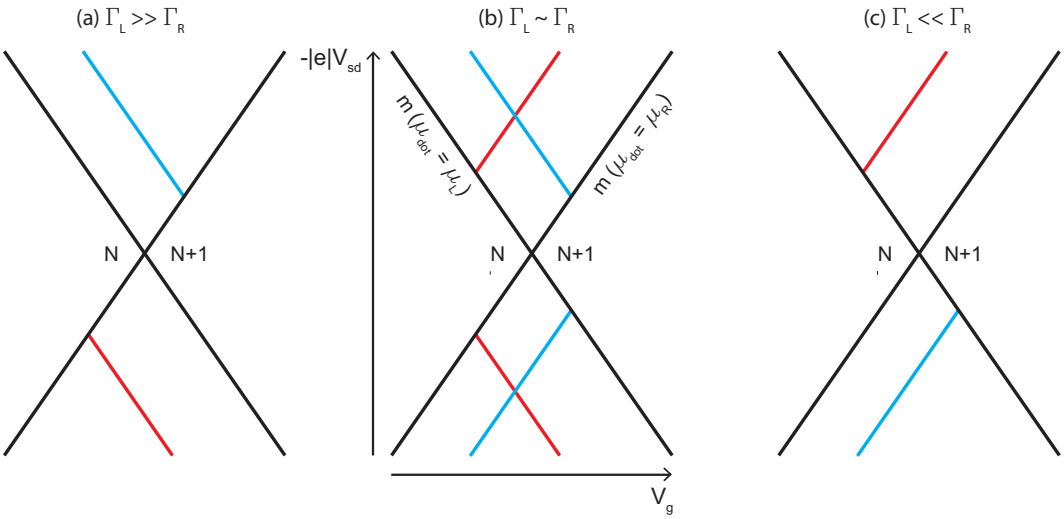


Figure 2.14: Observed excited state transitions for (a) a small left tunnel barrier, (b) roughly symmetric tunnel barriers, and (c) a small right tunnel barrier. $\Gamma_{L,R}$ are tunnelling rates between the dot and the left and right contacts.

2.3.4 Magneto-spectroscopy

If an external magnetic field is applied, each energy level is subject to Zeeman splitting, separated by $\Delta E_Z = g\mu_B B$, with g the Landé g-factor, $\mu_B = 5.79$ eV/T the Bohr magneton and B the applied magnetic field in Tesla. The Landé g-factor can be found by plotting the splitting with magnetic field.

Differential conductance maps obtained with an applied magnetic field can also be used to determine whether N is odd or even. Figure 2.15 shows the transitions seen for odd N.

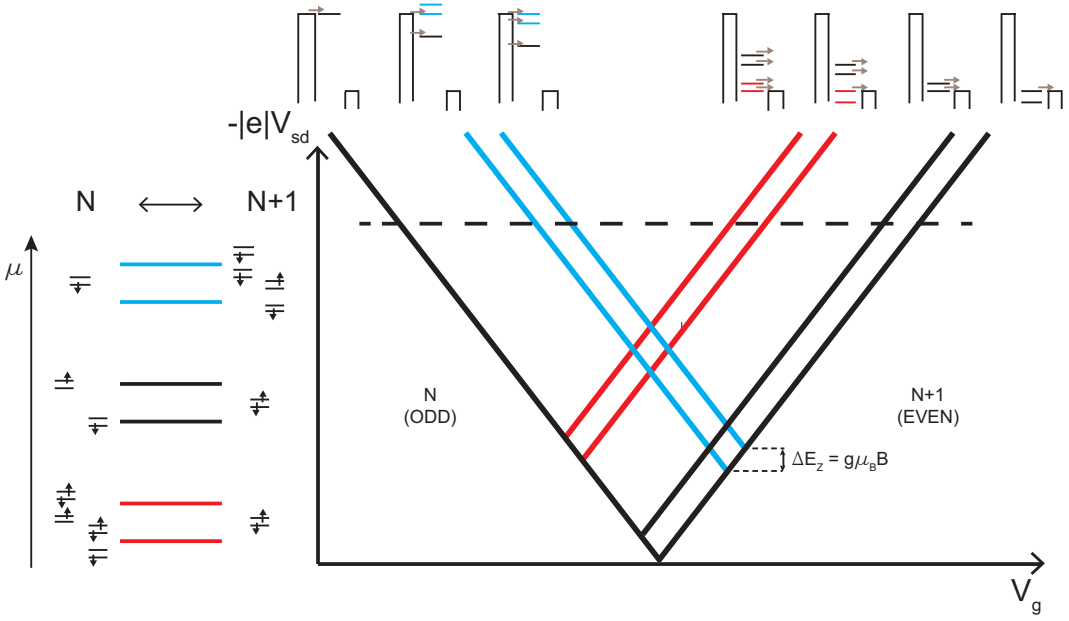


Figure 2.15: Origin of differential conductance peaks seen in a magnetic field. The ladder of electrochemical potentials, μ, on the left show electron configurations for N and $N+1$ electrons corresponding to μ. Source-drain energy diagrams at the top show the relative source, dot and drain potentials for the cross-section indicated by the dashed line.

For transitions to an even dot state (negative gradients in figure 2.15), there are three possible final configurations. Transitions to excited $N+1$ states (figure 2.16(a,b)) are shown in blue in figure 2.15, separated by E_Z; the transition to the $N+1$ ground state appears as a single line. Although there are two possible transition starting points ($\downarrow$ or $\uparrow$), the starting point does not affect the chemical potential of the final state, the $N+1$ ground state.

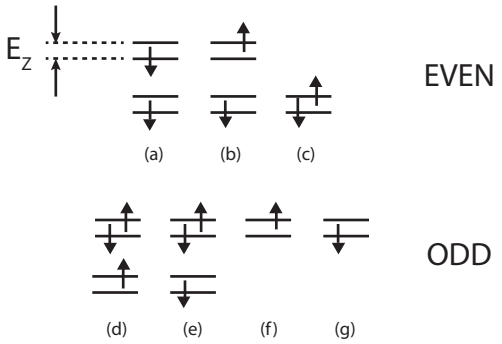


Figure 2.16: Possible electron configurations for (a)-(c) even and (d)-(g) odd dot states.

Transitions out of an even dot state (positive gradients in figure 2.15) pick out four possible electron configurations, shown in figure 2.16(d)-(g).

Chapter 3

Experimental Methods

In this chapter, the theory behind experimental techniques used for this work are covered along with operation details for the equipment used.

Specifically, an exploration of different quantum dot fabrication techniques, use of an atomic force microscope for imaging and lithography, use of Raman spectroscopy for crystal thickness measurements, and use of a dilution refrigerator along with a description of the modifications made to lower the sample temperature are described.

3.1 Quantum Dot Fabrication in MoS_2

Electrons in few-layer MoS_2 are confined to the plane; to form an MoS_2 quantum dot, electrons must be confined in the two remaining dimensions. Currently the primary method for achieving this in semiconducting two-dimensional materials is through local gating, causing band bending [5, 6, 55]. Small electrodes are patterned above the 2-D material with a dielectric layer in between. A bias is applied to an electrode, altering the band structure to cause locally insulating or metallic behaviour. Figure 3.1 illustrates the ideal gating effect for a single quantum dot.

An alternative method is to directly, and permanently, locally modify the material using lithography techniques such as atomic force microscopy [52, 56, 57].

Different quantum dot fabrication techniques are used depending on the desired outcome. Liquid exfoliation of MoS_2 in organic solvents [58] results in isolated quantum dots 2-9 nm in size, suitable for optical experiments. Laser

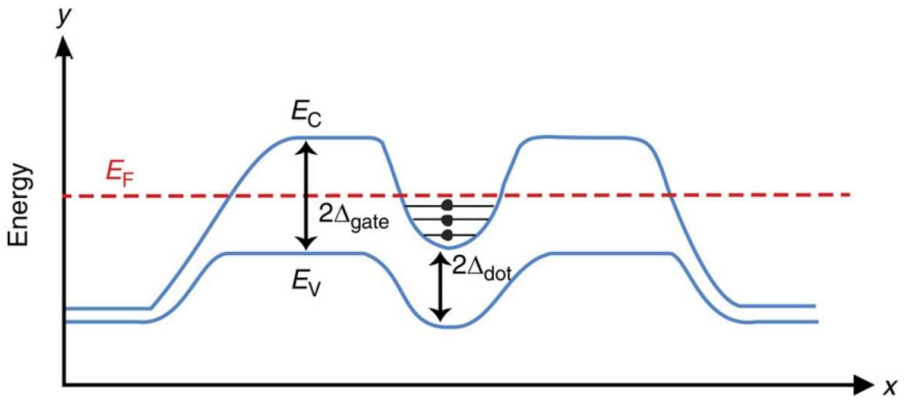


Figure 3.1: An illustration of the change in energy as a function of position across a gate-defined quantum dot. E_V, E_C mark the valence and conduction band edges respectively; E_F is the Fermi energy. Charge can accumulate in the central dot and to the left and right; tunnel barriers in which E_F is inside the band-gap mark the edges of the dot. *Adapted from ref* [5].

ablation [59] produces similarly small MoS_2 quantum dots (1-5 nm) which could also be used for optics. The small size of these quantum dots means they are easily stored in a suspension, and easily dispensed to cover a surface.

Recently, single-electron transport has been seen at T $\sim$1.7 K in a 70 nm radius gate-defined monolayer MoS_2 quantum dot [6], with charging energies $\sim$2 meV. Different gating patterns were used in this work to change the effective geometry between a single and double dot configuration. Figure 3.2 shows differential conductance plots for the single and double dot configurations, measured at T $\sim$1.7 K. Disadvantages of gate-defined dots include a restricted geometry after patterning, low yield, and poor electrostatic definition. In Pisoni et al [6], the patterned dot was 70 nm, but the effective dot size was $\sim$280 nm.

Some of these disadvantages can be overcome by fabricating MoS_2 quantum dots using atomic force microscope lithography, as explored in section 3.3. Lines of insulating MoO_3 are drawn in the chosen design to create a quantum dot. The technique allows repeated dot geometry modification, guided by in situ transport measurements. In addition to this, the level of spatial control allows a finer resolution than gate-defined dots, and the direct local oxidation forms a hard electrostatic barrier, in contrast to the sloping potential present in a gate-defined dot (figure 3.1).

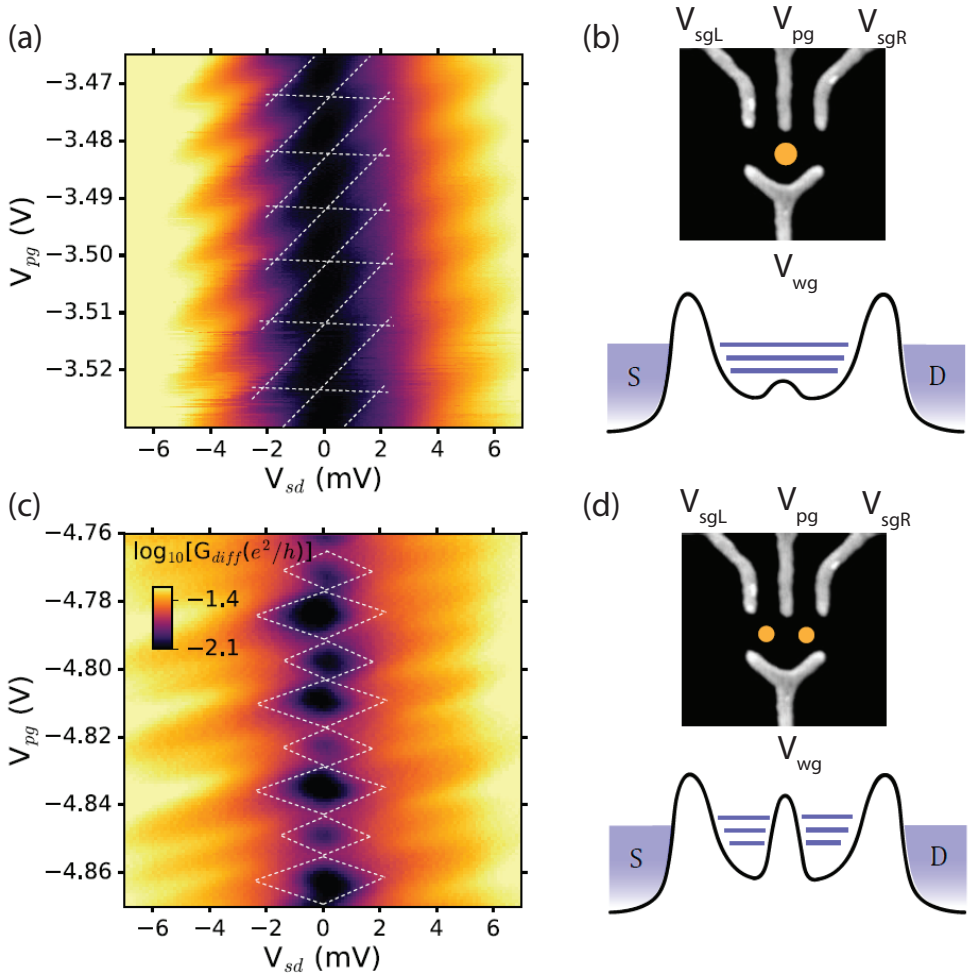


Figure 3.2: (a) Differential conductance as a function of plunger gate voltage (V_{pg}) and source drain voltage (V_{sd}) for a single quantum dot. Scale shown in (c). (b) Single dot configuration shown schematically with the corresponding electrostatic potential landscape. $V_{sgL} = -5.7$ V, $V_{sgR} = -6.1$ V, $V_{wg} = -8$ V. *sgL* and *sgR* are the left and right side gates. (c) Differential conductance as a function of V_{pg} and V_{sd} for a double quantum dot. (d) Double dot configuration shown schematically with the corresponding electrostatic potential landscape, showing the addition of a central barrier. $V_{sgL} = -5.6$ V, $V_{sgR} = -6.1$ V, $V_{wg} = -8$ V. *Adapted from ref* [6].

3.2 Atomic Force Microscopy

3.2.1 Theory

In scanning probe microscopy, a probe on the free end of a cantilever is scanned over a sample to determine the surface properties. The properties are inferred from experimentally dependent tip-sample interactions, such as van der Waals forces, electric and magnetic interactions. In the case of atomic force microscopy (AFM), the primary property measured is the topography, using feedback from changing van der Waals forces, typically measured either in tapping mode or in contact mode. Capillary forces are also present, due to the formation of a water meniscus between the tip and sample. Figure 3.3 shows these two modes, as the tip is approaching the surface and during imaging.

Probes used for tapping mode AFM are typically short and stiff. During imaging the probe oscillates, driven at a frequency close to its resonant frequency, excited by a piezoelectric element in the tip holder. The amplitude of these oscillations is dependent on the probe-surface separation, thus measuring the amplitude gives the topography. If there is a bump (dip) on the surface, the oscillation amplitude will decrease (increase), and a feedback loop will move the tip higher (lower) so that the amplitude returns to its set point as set by the user. Tapping mode tips used for this work were NanoWorld NCH-20/NCHR-20 POINTPROBE® Silicon SPM-Sensors, with resonant frequencies around 320 kHz. NCHR probes have an aluminium reflective coating on the detector side to enhance the laser beam reflectivity for easier alignment.

In contact mode, the probe is swept over the surface and as such probes are typically longer and more flexible than those used for tapping mode. Deflection of the probe as it scans the surface varies depending on the topography. Tip-sample interaction causes the cantilever to bend as the tip approaches the surface, shifting the position of the laser on the photosensors until it reaches a deflection set point defined by the user. If there is a bump (dip) on the surface, the laser position will be raised (lowered), and a feedback loop will move the tip higher (lower) so that the laser returns to its set position. In contact mode a map of the friction is

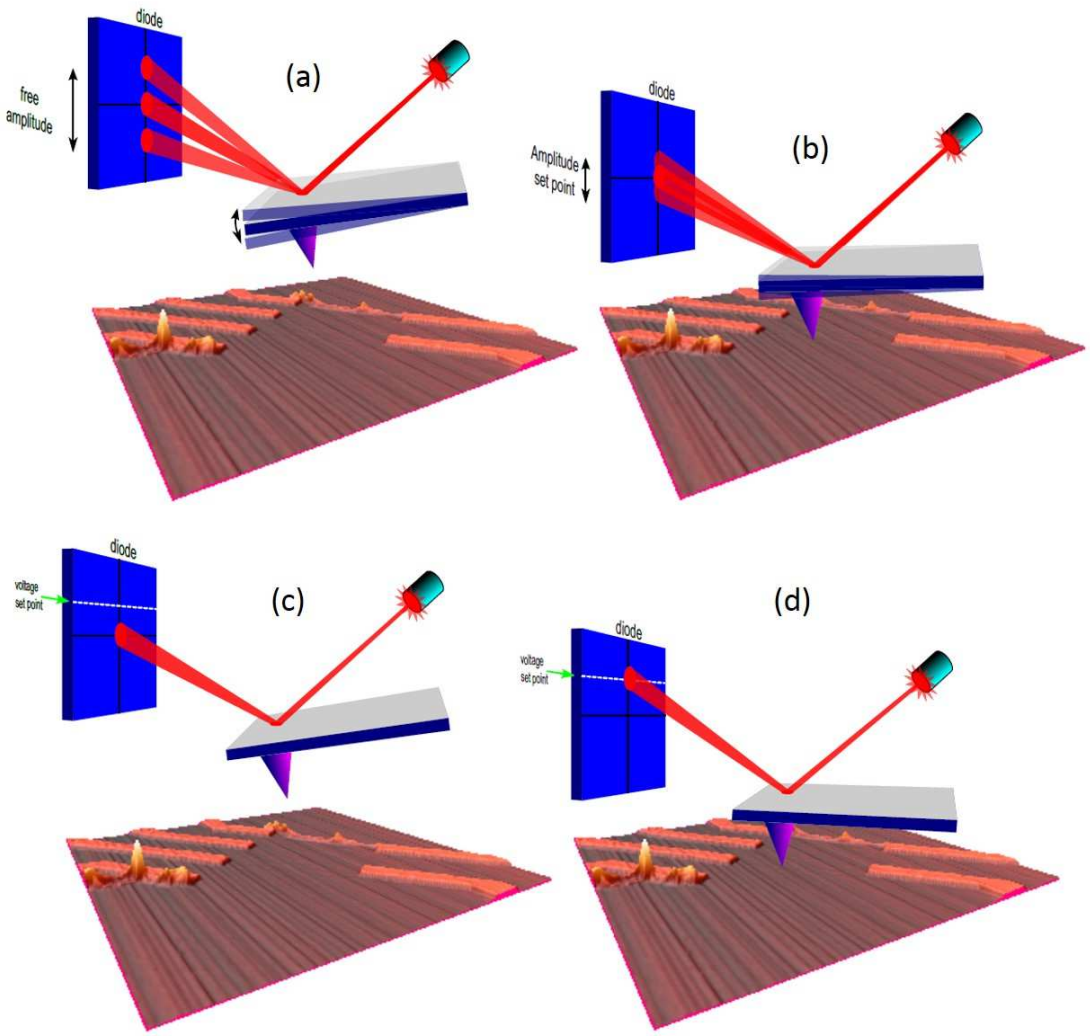


Figure 3.3: Atomic force microscopy schematic. A laser is reflected off the cantilever and hits an array of photosensors, shown in blue. (a) and (b) Tapping mode operation during (a) approach and (b) scanning. Scanning can begin once the amplitude of the laser oscillation on the photosensors reaches a pre-defined amplitude set point. (c) and (d) Contact mode operation during (c) approach and (d) scanning. Scanning can begin once the laser reaches a pre-defined voltage set point on the photosensors. (b) and (d) During scanning, bumps and dips in the surface change the laser position on the photosensors. Any change is fed back to the tip and the tip position is adjusted accordingly. In this way a map of the sample topography is built up. *Adapted from ref* [7].

also produced, showing the lateral deflection of the tip during scanning. Friction images can be clearer than height images in contact mode, as the height images can be noisy. Contact mode tips used for this work were NanoWorld CONTR-20 POINTPROBE® Silicon SPM-Sensors and NANOSENSORS PPP-CONTR-20

POINTPROBE®-PLUS Silicon-SPM-Sensors. The NANOSENSORS probes used n-doped silicon; all contact-mode probes used had an aluminium reflective coating on the detector side.

The mode chosen depends on the type of sample to be imaged. Lateral forces aren't exerted in tapping mode, so it can be used for delicate samples. The tips also last longer as a result. Contact mode is often used to image transition metal dichalcogenides and other low-profile samples as the z-resolution is better. The heights extracted from a tapping mode topography image will depend on the feedback parameters used. Resolution in the sample plane depends on the tip radius: an AFM image is a convolution of the tip with the sample surface. Uncoated tips used in this work typically have a 10–20 nm tip radius.

3.2.2 Operation

The laser is aligned so it hits the centre of the back of the tip of the cantilever. At this point the laser beam will visibly split. The 2×2 photosensor array is then aligned so that the laser hits the centre, maximising the signal.

Relative positions of the tip and sample are found by focussing on each in turn, and the height difference is used as an approximate travelling distance when the tip engages.

For tapping mode operation, the tip is tuned by driving it at a number of frequencies, and plotting the response to find the resonant frequency. Tuning adjusts imaging parameters to fit a particular tip in that environment.

A set point is chosen by the user, depending on the sample properties. In tapping mode, an amplitude setpoint is chosen: a smaller amplitude imparts a larger force. In contact mode, a deflection setpoint is chosen: a larger deflection imparts a larger force.

The tip-sample force can be measured in contact mode by approaching and retracting the tip in one location. An example of the resulting plot is shown in figure 3.4. As the tip approaches the surface, it remains unaffected until it snaps to contact, at which point the repulsive force increases as the tip continues to lower. When the tip is retracted, it stays in contact for longer due to attractive capillary

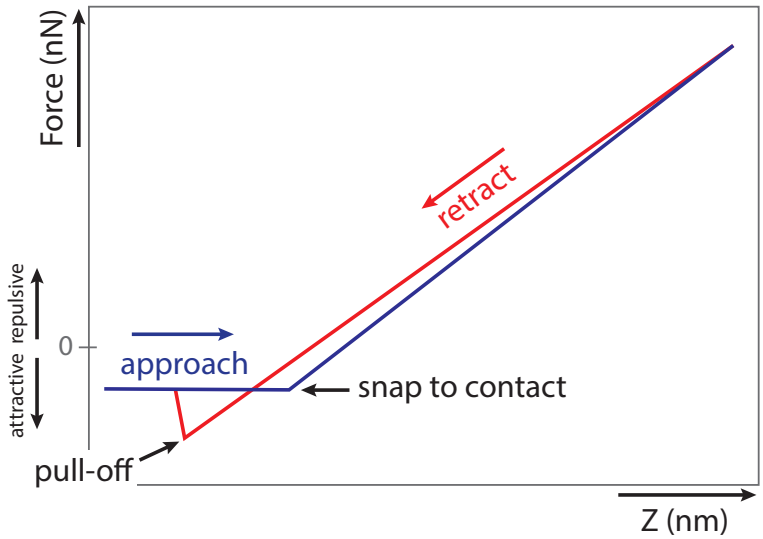


Figure 3.4: A plot of the force as a function of tip-sample separation. As the tip approaches the sample, there is initially no change in the force. At the point marked 'snap to contact', the tip is in contact with the sample and the repulsive force between them starts to increase. The repulsive force decreases as the tip is retracted in the second half of the measurement, and remains interacting with the sample for longer with an attractive force until the 'pull-off' point, at which the tip-sample interaction ceases.

forces. If there is water present, a capillary neck will form between the tip and sample, breaking at the pull-off point.

3.3 Atomic Force Microscope Lithography

In addition to surface imaging, a scanning probe can be used to manipulate the sample surface in a number of ways depending on the tip and sample properties. Thermal probe lithography uses a heated tip [60]; dip-pen lithography deposits material picked up by the tip onto the sample [61]; mechanical lithography uses force to create small scratches [62]; oxidation lithography locally oxidises the sample [52]. The commonality in these techniques is a narrowly spatially defined reaction allowing the flexible patterning of nano-scale structures that can be imaged and altered in situ. A contact-mode AFM tip can also be used to clear loose debris by scanning back and forth over the area [63, 64].

Oxidation nano-lithography has been explored in depth on silicon [65, 66, 67], titanium [68, 69], and more recently graphene [52, 70, 71] amongst other

surfaces [72, 73]. Before work started on this thesis, oxidation nano-lithography was as yet unexplored on transition metal dichalcogenides such as MoS_2. Just as a quantum dot can be defined on a graphene flake by drawing lines of oxide to create potential barriers [52], the same can in principle be done on MoS_2.

Oxidised MoS_2, MoO_3, is an insulator. MoO_3 lines defined using AFM local oxidation can be used as potential barriers to define a small island in the semiconducting MoS_2: a quantum dot. Defining a dot in this way allows the device transport characteristics to be monitored in situ, and the dot walls to be altered. For a small enough island at a low enough temperature, the electronic spectrum will be discrete. Studying this spectrum would reveal properties such as g-factors, and spin-filling.

3.3.1 AFM Lithography Operation

Figure 3.5 is a schematic of the AFML technique. The tip is biased with respect to the sample, and the electric field ionises the water molecules which migrate in accordance with the electric field polarity. A negative tip bias results in local oxidation of the sample.

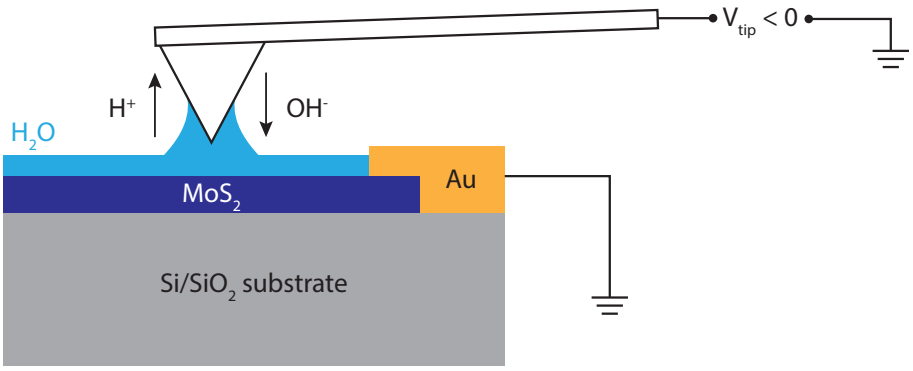
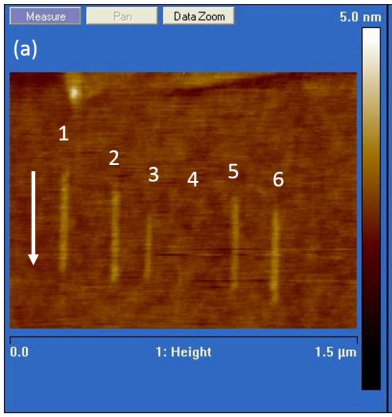


Figure 3.5: A schematic of atomic force microscope lithography. When the tip is close to the surface, a meniscus forms. The electric field resulting from an applied bias polarises a layer of water atop the sample. The negatively biased tip with respect to the sample attracts the oxygen towards the MoS_2 surface, locally oxidising the sample.

In order to test the new AFML set-up, graphene devices were fabricated, and lithography was carried out using parameters known to result in successful oxidation [52]. Graphene oxidation requires a small tip-sample bias, $\sim$4 V, which

can be achieved using the in-built NanoMan software. Figure 3.6 shows the resulting height and friction AFM images of six lines of graphene oxide taken in contact mode, drawn using different tip voltages and speeds. The threshold tip voltage here was -5.5 V: a smaller voltage resulted in no change in the sample. Lines 3 and 4 only appear partially; this is likely due to the wafer lying at a slight angle, resulting in the tip-sample distance decreasing as the line is drawn. Above a threshold tip-sample separation there is no oxidation.



Line number	Voltage /V	Speed /nms^{-1}
1	-6	100
2	-6	50
3	-5.5	50
4	-5.5	100
5	-5.5	10
6	-6	10

Figure 3.6: (a) Height and (b) Friction AFM images are shown of six oxidised lines of graphene on devices fabricated to test the AFML set-up. The tip voltages and speeds are given in the table. All of the lines were drawn to be the same length, and drawn in the same direction, with the direction and intended line length shown by the arrow to the left of the images.

Early lithography experiments carried out on MoS_2 were based on previous AFML work done with graphene [52, 71]. A contact mode tip with a tip radius $<$10 nm was used, and a constant bias ($|V_{tip}| \leq 12$ V) applied to the tip using NanoMan software on a Veeco Dimension^{TM} 3100 AFM. This method was unreliable and had a low yield. Where there was successful oxidation, the lineshape was uneven. The oxidised material also appeared to be very mobile. Figure 3.7 shows AFM images of four oxidised lines on bulk MoS_2, oxidised in contact mode but imaged in tapping mode to avoid moving material whilst imaging. The arrows indicate the length and direction of the tip movement, labelled with the tip voltage used. It can be seen that drawing a small line has a large effect on the surrounding material, forming a mound several nanometres high, increasing in height in a

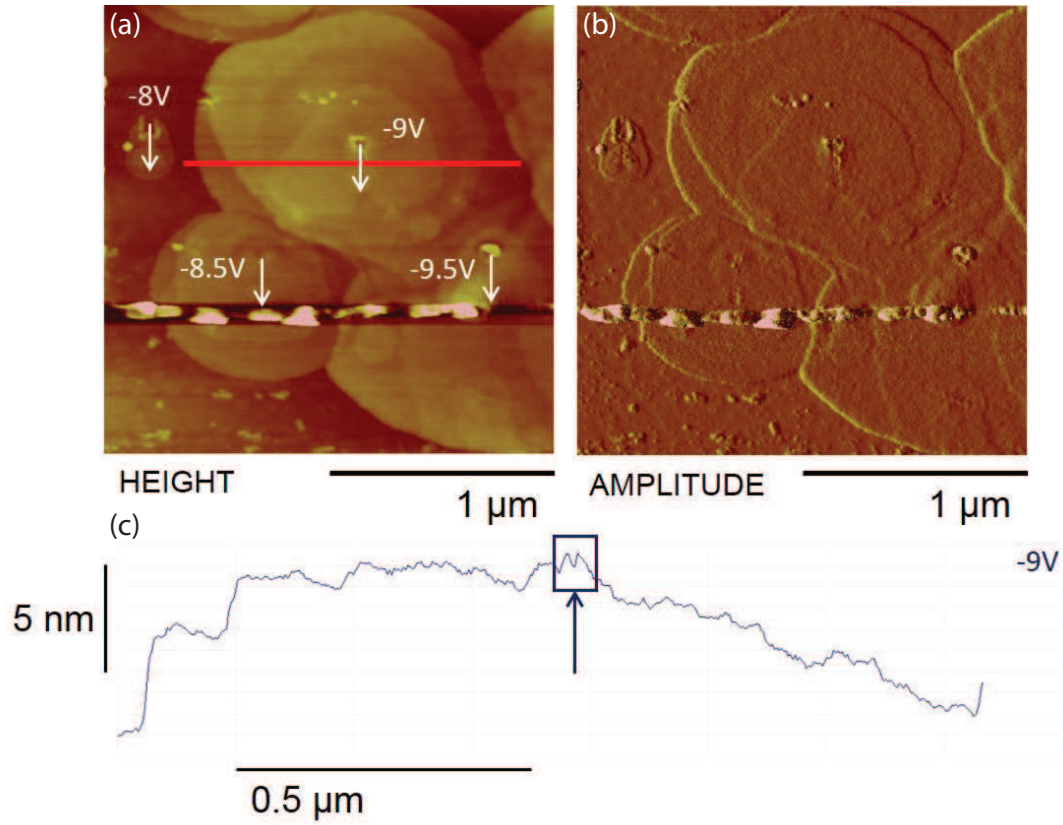


Figure 3.7: (a) Height and (b) Amplitude AFM images, taken in tapping mode, showing areas of oxidised MoS_2 (oxidised in contact mode). The direction and distance moved by the tip during lithography is shown by the arrows. (c) A cross-section through the line drawn at V_{tip} = -9 V, with the central groove picked out.

step-like fashion towards the centre. At the centre, where the line is drawn, there is a groove, deepest at the start of the line.

3.3.2 MoS_2 Oxidation (Garcia group, ICMM)

The Garcia group at the Instituto de Ciencia de Materiales de Madrid (ICMM) in Spain specialises in AFM lithography on a variety of materials, which recently has included MoS_2. In their set-up, described for CVD-grown MoS_2 in Espinosa et al [8], there are a number of differences compared with the method described above. Specifically, lithography is carried out in the presence of ozone, with a tapping mode tip to stabilise the meniscus, a pulsed bias to avoid charge build up, and using code which controls both the tip movement and the applied bias.

Figure 3.8 shows oxidation of monolayer CVD MoS_2 from Espinosa et al [8], with V_{sample} = +54 V, t_{pulse} = 250 μs, and relative humidity RH = 45%.

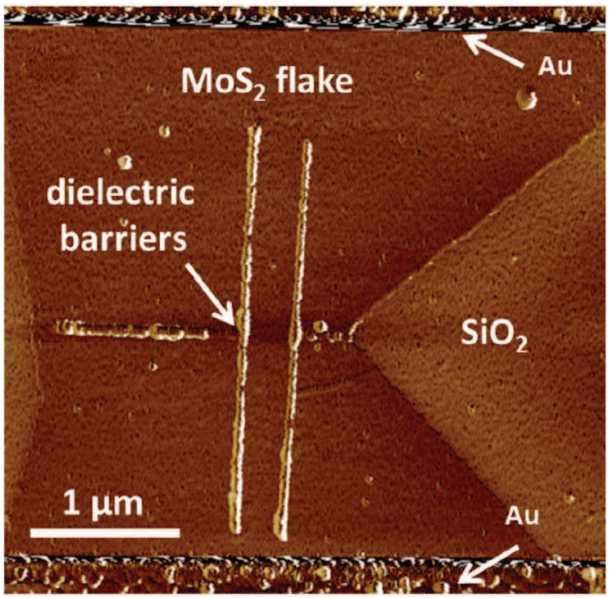


Figure 3.8: AFML oxidation of monolayer CVD MoS_2. *Adapted from ref* [8].

Taking my own devices to the Garcia lithography laboratory used for the above results allowed for a wider exploration of parameters and further understanding of the technique. Figure 3.9 shows a quantum dot drawn on CVD grown MoS_2 during this visit. The lithography was carried out after sample cleaning in contact mode and illumination with ultraviolet light for 11 minutes to create ozone inside the AFM chamber. Lab and chamber relative humidities were measured as 30% and 31% respectively. The sample bias applied was +26.1 V, with a pulse on time of 0.5 ms, and a 3 nm step between pulses.

The resulting oxide width was 25–50 nm, and oxide height on monolayer MoS_2 was $\sim$1 nm. The CVD sample had small triangular bilayer areas; oxidation propagated much more readily on these areas, covering entire bilayer sections. The oxide bilayer height at $\sim$2 nm was roughly double that of the monolayer.

After returning from the Garcia lab, three notable adaptations were made to the original technique shown schematically in figure 3.5: a larger sample-tip bias was applied, $\geq$ 20 V, a pulsed bias was used, and the contact mode tip was replaced by a tapping mode tip with a similar tip radius.

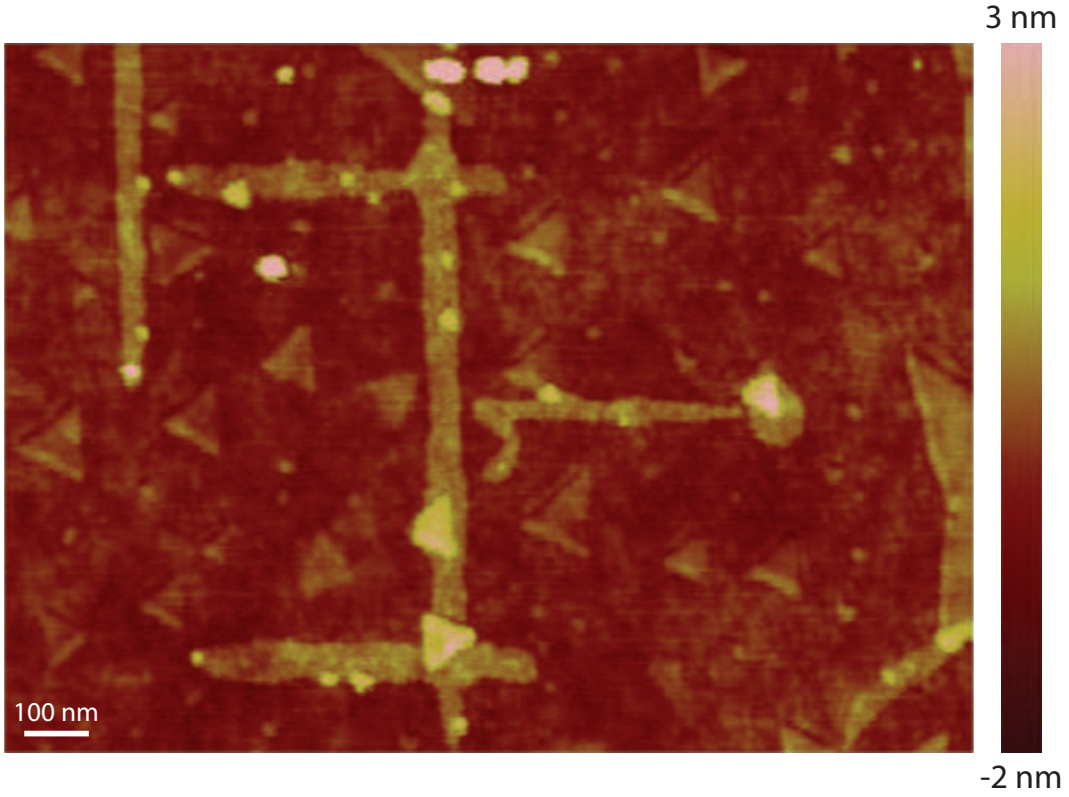


Figure 3.9: Quantum dot drawn on CVD monolayer MoS_2 using ozone-assisted nano-lithography at the Garcia lithography laboratory. Parameters: 11 minutes UV illumination, $RH_{chamber}$ = 31%, V_{sample} = +26.1 V, t_{pulse} = 0.5 ms, step = 3 nm.

3.3.3 Experimental Factors

A number of parameters were explored to identify necessary conditions for successful oxidation of MoS_2. However, despite extensive experimentation, MoS_2 oxidation is still unreliable. In this section, the parameters explored are discussed along with observed or postulated effects resulting from a change.

1. Relative Humidity

Relative humidity (RH) both in the lab and in the AFM chamber is key, as it affects the size of the meniscus formed between the tip and sample. Optimum levels were 30–50%. Drier conditions than this result in no oxidation due to the limited water adsorbed on the MoS_2 surface; wetter conditions result in uncontrollable oxidation.

Hygrometers were placed close to the sample inside the AFM chamber, and

in the AFM lab. Humidity inside the chamber can be increased by the addition of water, or decreased by pumping nitrogen gas into the chamber.

2. Sample bias

Larger tip-sample biases, 25–50 V, are required for MoS_2 compared with graphene. There is a current threshold below which oxidation will not occur; the significantly lower conductivity of MoS_2 therefore requires the application of a larger voltage.

Application of a pulsed or continuous bias was found to change the line shape. A pulsed bias resulted in straighter edges with a more controllable thickness. This could be due to minimised charging effects; a continuous bias can result in a large area being charged up and oxidising, as seen in figure 3.7.

3. Surface cleanliness

The surface cleanliness has an effect on the oxidation: surface debris may affect the electric field. To this end, the crystal can either be contacted using shadow mask evaporation, a resist-free contacting technique (see section 4.1.4), or cleaned using a contact mode tip [63, 64]. Figure 3.10 shows a 10 μm AFM image taken in tapping mode after cleaning a 5 μm area in contact mode. The RMS roughness, R_q, and average deviation, R_a, are given for the two outlined areas, defined below with y_i the distance from the mean and n the number of equally spaced samples taken. The roughness is significantly reduced after contact mode cleaning.

$$R_q = \sqrt{\frac{1}{n}\sum_{i=1}^{n} y_i^2} \tag{3.1}$$

$$R_a = \frac{1}{n}\sum_{i=1}^{n} |y_i| \tag{3.2}$$

4. Temperature

An increased sample temperature may promote the oxidation reaction. The temperature of the lab was measured along with the relative humidity. There could also be localised heating around the tip.

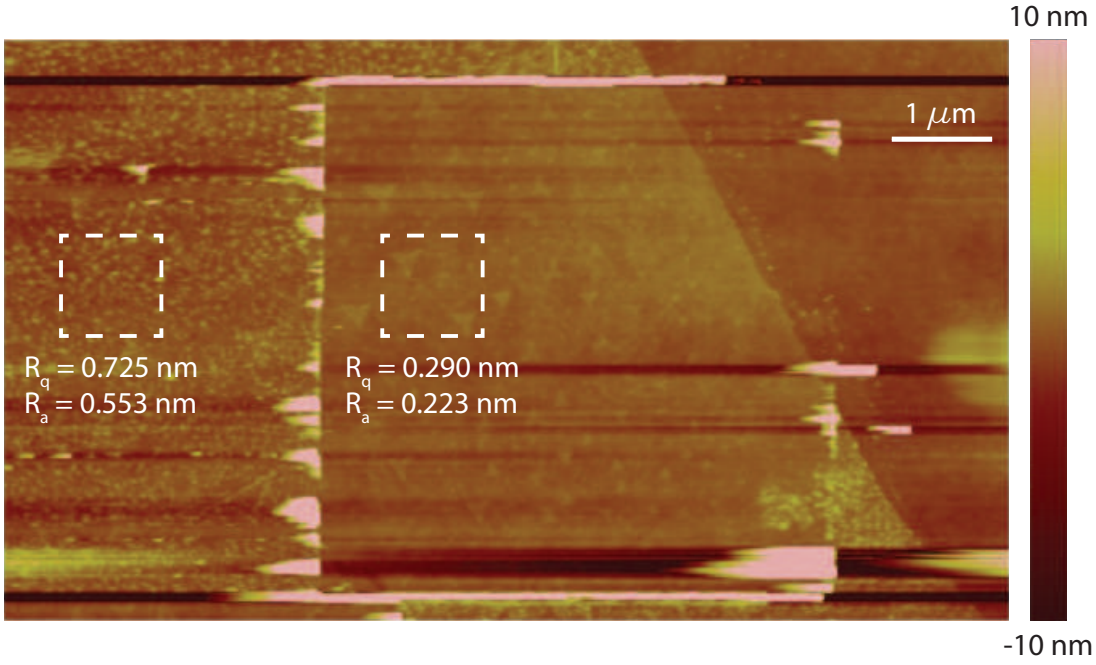


Figure 3.10: 10 μm tapping mode AFM image taken after cleaning a 5 μm area in contact mode. Calculated RMS and average roughness ($R_{q,a}$) values for 1 μm^2 areas inside and outside the cleaned area are given, showing significant improvement after contact mode cleaning.

5. MoS_2 thickness

Lithography was carried out on monolayer, bilayer, and bulk MoS_2. Bilayers appeared to oxidise more readily than monolayers (figure 3.9), and bulk MoS_2 oxidised uncontrollably (figure 3.7).

6. Amplitude setpoint

Different amplitude setpoints can be defined for imaging and lithography. The setpoint can be reduced for lithography to make the tip oscillate closer to the surface. The amplitude of the oscillations will correlate to the stability of the meniscus: large oscillations will cause more variation in the meniscus size, and could result in cycles of meniscus formation and destruction, making it too unstable for lithography.

7. Tip speed

Figure 3.6 shows the effect of tip speed on line thickness for a continuously applied bias: a slower speed results in a thicker line.

For a pulsed bias, a slower tip speed results in smaller distances between

pulses. It should follow that a slower tip speed results in a thicker line for a pulsed bias as well as a continuous bias.

There may be upper and lower limits of tip speed for successful oxidation to occur. A tip moving too slowly may produce a large uncontrollable oxidised area; a tip moving too fast may not oxidise at all, or may leave large gaps in a line, rendering it useless as a potential barrier.

8. Pulse width

Pulse ON time will have an effect on the oxidised diameter due to the build up of charge over time. A longer pulse will increase the diameter; a pulse that is below a threshold time may result in no oxidation.

The pulsed bias was achieved using MATLAB code and a Keithley Source-Measure Unit (SMU). This set-up allowed only rudimentary control of the pulse width. For this to be investigated with finer control, a pulse generator would be required.

9. Exfoliated and CVD MoS_2

Lithography was tried on CVD and exfoliated MoS_2 samples. CVD samples were grown by Maria O'Brien from the Duesberg group at Trinity College Dublin and by the Warner group at Oxford University. There was no obvious difference between CVD and exfoliated samples. However, it was not possible to get transport measurements for CVD MoS_2 devices, as there were electrical shorts between at least one contact and the back gate in every device. It is thought that the oxide is damaged during the MoS_2 growth.

10. MoS_2 defect density

Naturally occuring MoS_2 has been found to be quite defective. Sulphur vacancies are found with an approximate density of 10^{13} cm^{-2} [28, 31]. In addition, metallic-like defects are found with an approximate density of 10^{10} to 10^{11} cm^{-2} [31, 74]. Electronic properties of MoS_2 were found to vary significantly on a mesoscopic scale [31, 74] due to the metallic-like defects. Oxidation success could be linked to the local defect density.

11. Local electric field

The magnitude of the local electric field (LEF) will determine the oxidation success. The LEF depends on the conductivity of the MoS_2, which may explain why graphene is much more readily oxidised at low voltages than MoS_2. The LEF also depends on the contact resistance, R_C, with a higher contact resistance resulting in a lower effective tip-sample bias for lithography. The value of R_C will vary between samples, depending on the crystal properties such as defect density, and the effects of experimental processing such as photolithographic patterning of contacts.

12. Charge traps

If the conductivity is an important factor in the oxidation success, a positive gate voltage can be applied to switch the device on. However, as discussed in chapter 5, the presence of charge traps, particularly in ambient conditions as used in AFM, will result in an increase threshold voltage over time, and therefore a reduced current.

3.3.4 Results

To apply a large enough bias, the AFM electronics were bypassed. A bias was applied directly to the sample using a KEITHLEY 2450 SourceMeter unit, and the AFM tip was grounded separately. Figure 3.11 shows the set-up used. A hygrometer was used to measure the humidity levels inside the AFM chamber using a sensor located close to the sample. MATLAB code was used to apply a pulsed bias, providing rudimentary control over pulse width ($t_{ON} \simeq 1$ ms). The sample was mounted to an insulating rotating stage (figure 3.12(b)). A cantilever holder designed for use with conductive-AFM imaging was used to ground the tip. Figure 3.12(a) shows the cantilever holder, c-AFM module, and a pin grounded through the break-out box.

Figure 3.13 shows a quantum dot drawn on exfoliated MoS_2 using this set-up. The sample bias was +50 V; tip speed 25 nm/s; amplitude setpoint 0.65 V; relative humidity 34% and temperature 27.6 °C. The final line drawn, labelled (3), demonstrates the flexibility of the AFML technique: the dot was easily made smaller by a chosen distance after the previous line, (2), was drawn.

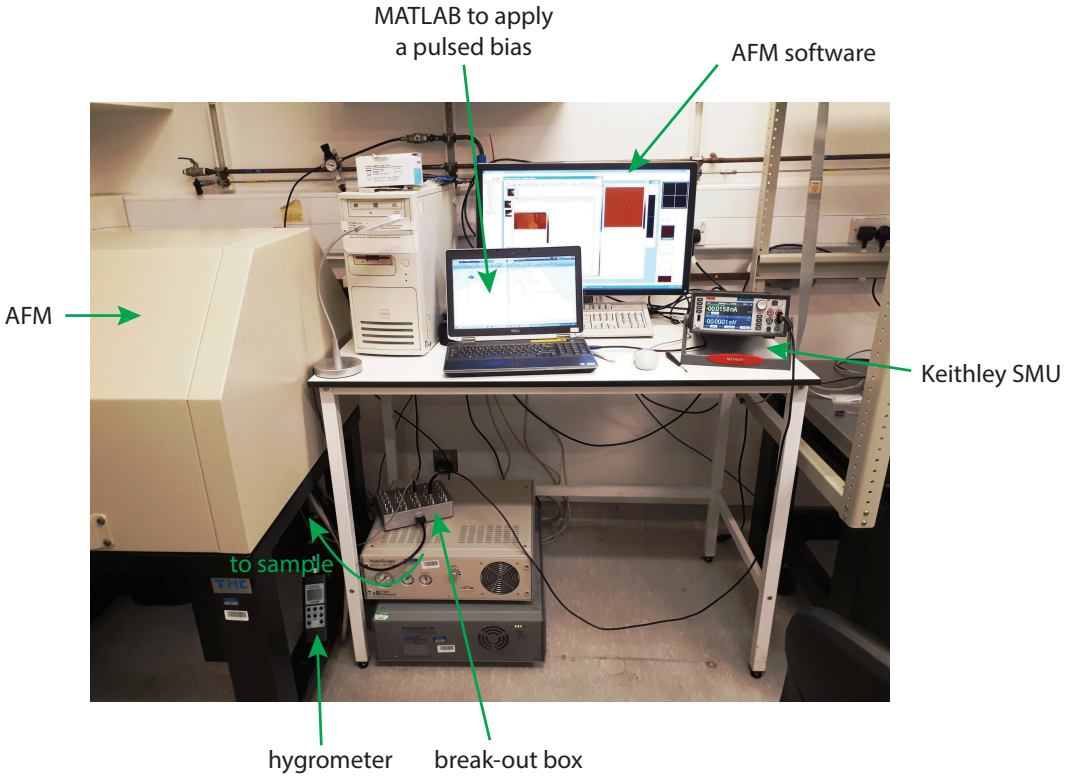


Figure 3.11: AFM lithography set-up. A pulsed sample bias was applied using the Keithley SMU controlled by MATLAB code. The hygrometer measures the humidity inside the chamber.

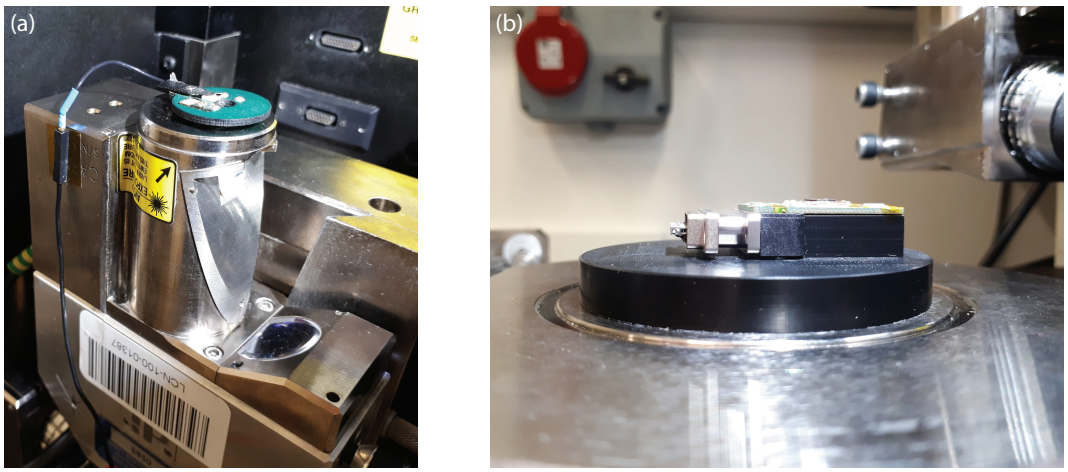


Figure 3.12: (a) An AFM cantilever mounted on a conductive-AFM holder, grounded via the break-out box. (b) Sample mounted on insulating rotating stage in the AFM.

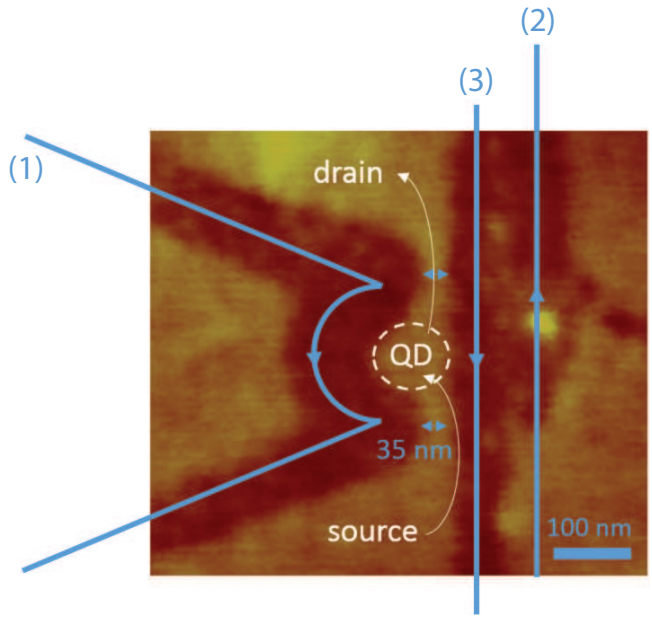


Figure 3.13: Quantum dot drawn on exfoliated trilayer MoS_2. Blue lines show tip movement and direction, with lines numbered in the order they were drawn. Parameters: $RH_{chamber}$ = 34%, V_{sample} = +50 V, $t_{pulse} \simeq$ 1 ms, u_{tip} = 25 nm/s, $A_{set\,point}$ = 0.65 V, $T_{chamber}$ = 27.6 °C.

3.3.5 Transport Measurements

Figure 3.14 shows transfer curves taken at V_{sd} = 0.5 V at different stages of lithography for the device shown. The current is highest before any lithography, as there is current through the trilayer and through the bulk. The first lithography step cuts off the bulk contribution with a line of oxide drawn perpendicular to the direction of current, reducing the current by a factor of 20. The remaining lithography steps formed the quantum dot imaged in figure 3.13 and blocked off the remainder of the trilayer to force current through the dot.

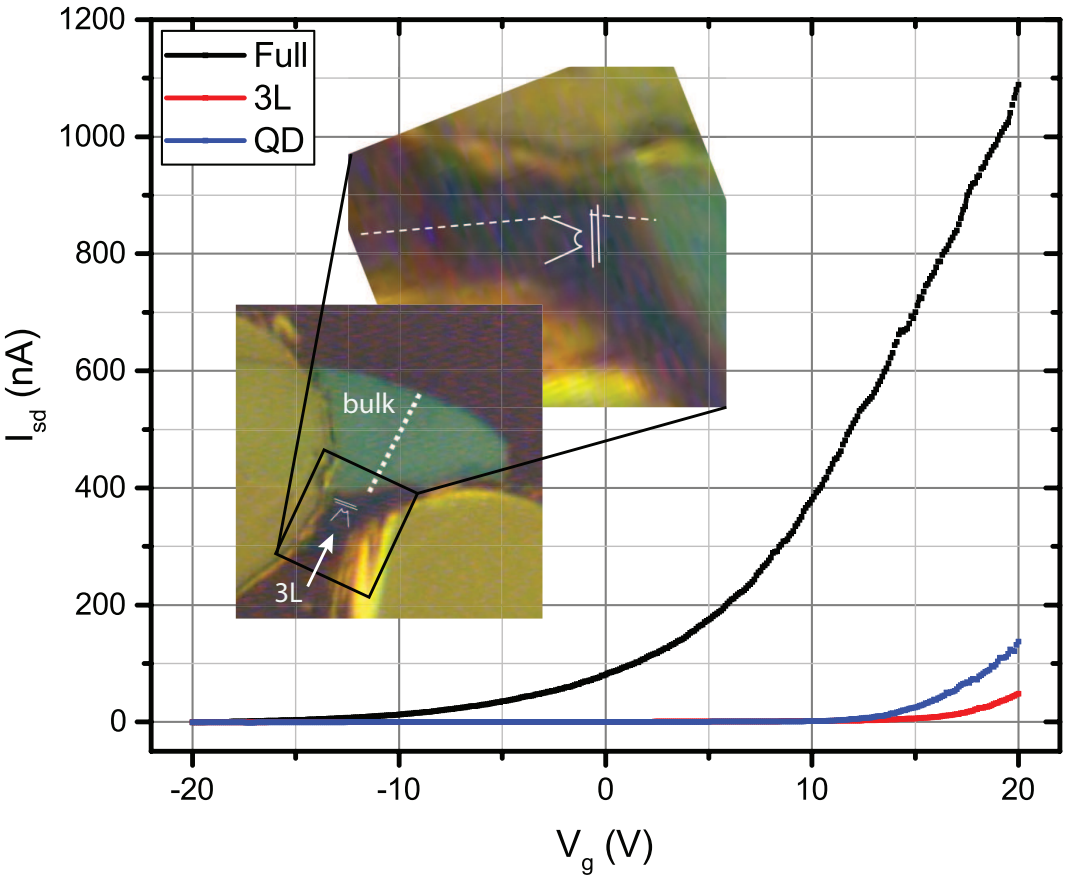


Figure 3.14: Transfer curves at V_{sd} = 0.5 V taken in between stages of lithography for the device shown inset.

3.3.6 Discussion

Unlike experiments carried out on graphene, MoS_2 oxidation lithography was harder to characterise. Many parameters were hard to control, such as humidity, temperature, pulse width, defect density, tip radius, and surface quality. Seemingly

identical lithography attempts would sometimes be successful and at other times be unsuccessful. Further work is required to understand this more fully.

Pulse width is difficult to control as the equipment used is not designed to generate pulses. Voltage pulses were defined by simple MATLAB code switching the Keithley SMU output from $V_{on} = V_{sample}$ to $V_{off} = 0$ V. It should be noted that V_{off} was defined as 0 V, rather than just turning the source on and off, as the latter is not well defined. This method led to a pulse width of $\sim$1 ms.

In addition to this, lithography patterns had to be specially designed because software limitations prevented full integration. NanoMan, part of the standard AFM software, was used to define the pattern, and to set tip speed and amplitude setpoint. MATLAB and NanoMan were started together manually. Lithography patterns had to be designed to allow for over or under exposure at the beginning and end, which would result in excess or no oxidation respectively.

In addition to the parameters already explored, there is some suggestion that dynamic lithography, as practised here, is not as accurate and reproducible as static lithography [9]. For static lithography, the tip stops oscillating while the bias is applied. It is suggested that this allows the meniscus to be stable during lithography. Figure 3.15 shows, experimentally, the difference between static and dynamic lithography.

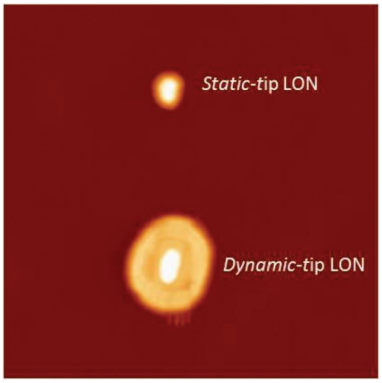


Figure 3.15: AFM image showing a comparison between static and dynamic oxidation lithography on tantalum sulphide (TaS_2). *Adapted from ref* [9].

3.3.7 Further Work

Use of a newer AFM system would allow for full software integration allowing sample bias and tip movement to be controlled centrally. This would allow for more precise operation, and development of a static lithography procedure.

Addition of a pulse generator instead of a standard source-measure unit could be used to explore the effect of pulse width on oxide formation.

MoS_2 is widely studied due to its natural abundance. However, other TMDs appear to be more easily oxidised. Oxidation of WSe_2 in Dago et al [57] uses a sample voltage of +18 V and a pulse width of 0.2 ms. Further study of the parameter space in other TMDs could provide useful insight for MoS_2 lithography.

3.4 Raman Spectroscopy

By illuminating the sample with a laser, the laser photons, if not absorbed, will scatter off the sample either elastically or inelastically. The majority of the photons will undergo Rayleigh scattering, which is an elastic scattering resulting in no change in photon energy. The remaining photons, on interaction with various vibrational modes and other excitations in the sample, will scatter inelastically, resulting in a shift in the energy of the photons. Shifts to higher (lower) energy states are known as Stokes (Anti-Stokes) Raman scattering events. The location and intensity of the shifts seen can be used to give information about the sample.

Raman spectroscopy can be used to determine the number of layers in an MoS_2 crystal. The two dominant peaks seen in MoS_2 spectra result from E^1_{2g} and A_{1g} modes, illustrated in figure 3.16(b) [11]. Figure 3.16(a) shows the peak evolution with layer thickness from monolayer to bulk MoS_2 for three commonly used laser wavelengths [10]. As the number of layers decreases, the two peaks get closer together by a small amount, $\sim$1 cm^{-1} per layer.

Figure 3.17 shows Raman spectra for monolayer, bilayer, and bulk MoS_2, taken using a RENISHAW inVia Raman Microscope, with a 514.5 nm laser, and exposure time of 60 seconds. The silicon peak cannot be seen in the bulk spectrum due to shielding. The separation of the E^1_{2g} and A_{1g} peaks was taken, along with absolute

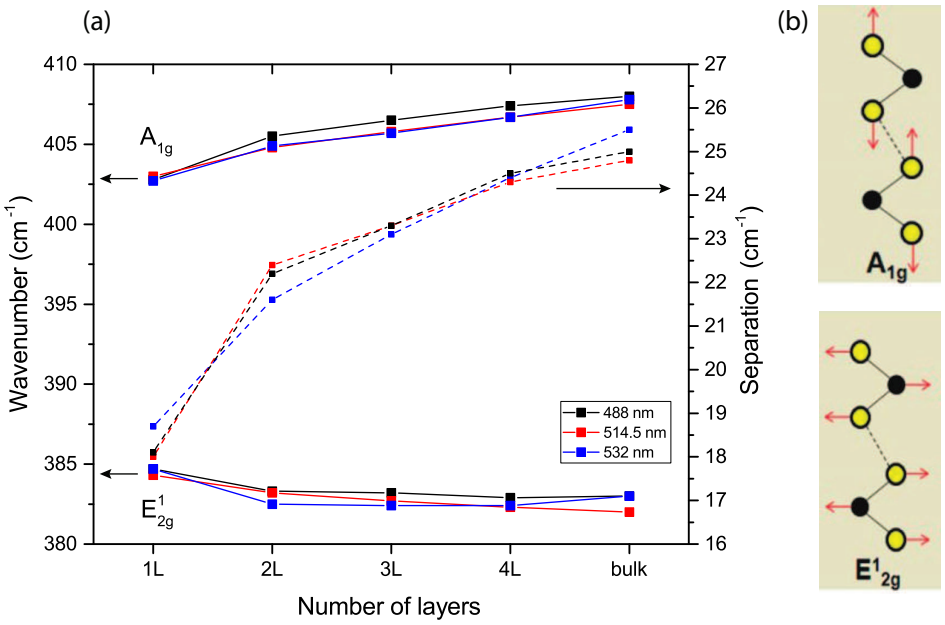


Figure 3.16: (a) Evolution of the E^1_{2g} and A_{1g} MoS_2 Raman peak positions (solid lines) and their separation (dashed lines) as the number of layers increases from monolayer to bulk. Values of the peak frequencies are shown for three common laser wavelengths. *Data from* [10]. (b) Illustration of the two Raman-active modes in MoS_2, showing 2 adjacent layers. Yellow (black) atoms are S (Mo) atoms. *Adapted from ref* [11].

values of the E^1_{2g}, A_{1g} and silicon peak positions to determine the number of layers in the sample. The position of the silicon peak was used to determine the value of any offset in the spectrum.

Raman spectroscopy was used to determine crystal thickness after locating few-layer crystals using an optical microscope. The technique very easily distinguishes monolayers, bilayers, and thicker crystals, but it is difficult to determine the thickness of MoS_2 crystals with three or more layers using Raman. With practise, monolayers and bilayers can be distinguished fairly reliably by eye. MATLAB code was designed to analyse relative contrast between pixels in optical images, but there were difficulties associated with fixing a baseline corresponding to the blank substrate. Confirmation of crystal thickness was achieved using Raman spectroscopy for crystals that would be later used for devices. For a more complete thickness characterisation, the number of layers can be measured using AFM, but this is largely unnecessary for monolayers and bilayers.

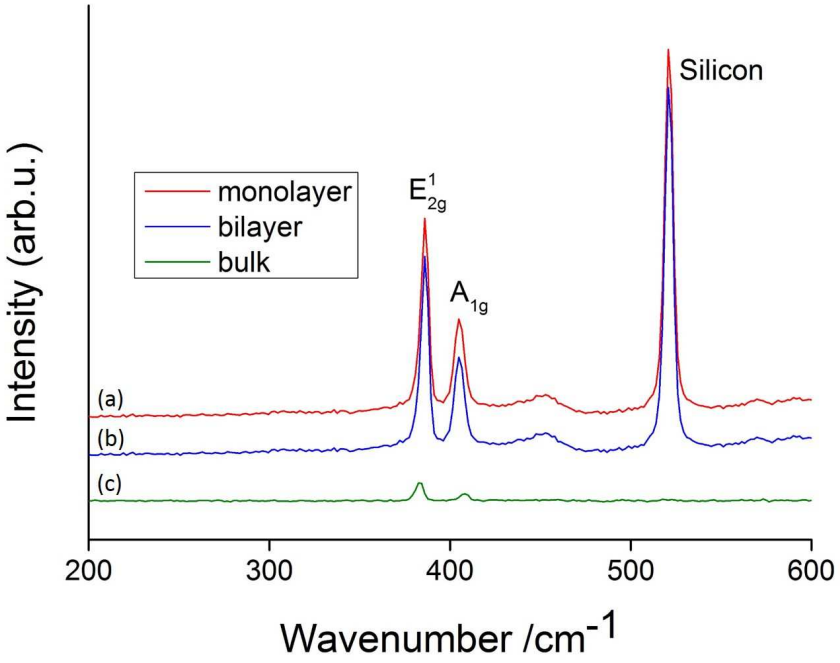


Figure 3.17: Labelled Raman spectra for (a) monolayer, (b) bilayer and (c) bulk MoS_2, taken to determine the thickness of optically-located crystals. Spectra offset in intensity for clarity. The exposure was set to 60s; the wavelength of the laser used was 514.5 nm.

3.5 Dilution Refrigerator

The dilution refrigerator (DR) used for low temperature measurements in this work is a BlueFors LD250, with a base temperature T $\leq$ 10 mK, and a 9 Tesla magnet. The DR was not present at the start of this work; this section covers some of the set-up required such as the addition of filters to achieve a lower electron temperature in the sample.

Other practical contributions such as the design of a cold finger to facilitate magnetic field measurements, and the design of a new sample holder are covered in section 4.2. Diagrams of the code written for data acquisition can be found in section 4.4.

3.5.1 Operation

DRs fall into two main categories: wet and dry. To cool from room temperatures to 4 K, wet fridges use liquid nitrogen and liquid helium; dry fridges use a cryocooler. At low temperatures ($\leq$ 4 K) they function similarly, using pumps and a mix of ^{3}He and ^{4}He to cool. The cooling happens in stages, with ^{3}He being pumped continuously around the system. A schematic of a dilution refrigerator is shown in figure 3.18.

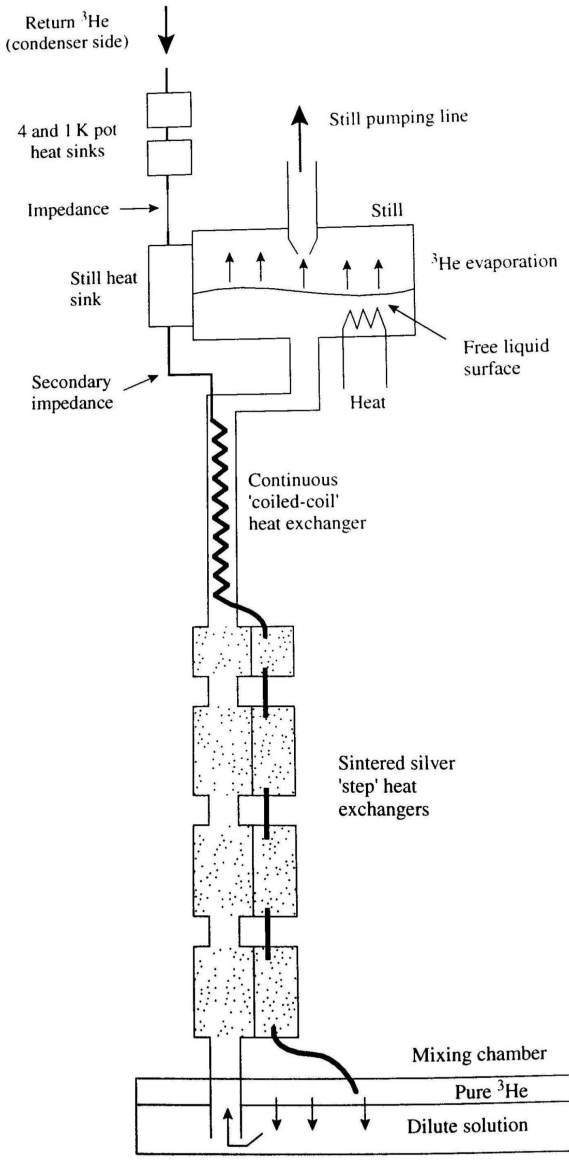


Figure 3.18: A schematic of a wet dilution refrigerator, showing the heat sinks, the still, and the mixing chamber. *Adapted from ref* [12].

Sustainable cold temperatures are achieved by cycling ^{3}He. The mix of ^{3}He and ^{4}He separates at low temperatures (< 0.7 K), into near-pure ^{3}He and a dilute solution comprising superfluid ^{4}He and viscous ^{3}He. Figure 3.19 shows the phase diagram for a ^{3}He-^{4}He mix at low temperatures as a function of ^{3}He concentration. The different behaviours arise because of the extra neutron in ^{4}He, making ^{3}He a fermi fluid and ^{4}He a bose liquid. Due to the mass difference, the pure ^{3}He sits in a layer on top of the dilute solution. In operation, ^{3}He in the mixing chamber flows through the dilute solution: this is an endothermic process so reduces the temperature. This ^{3}He is circulated up to the still, where a small amount of applied heat ($\sim$7 mW) causes it to evaporate. The ^{3}He is recondensed through a series of high impedance lines down to the mix of dilute and pure ^{3}He phases in the mixing chamber.

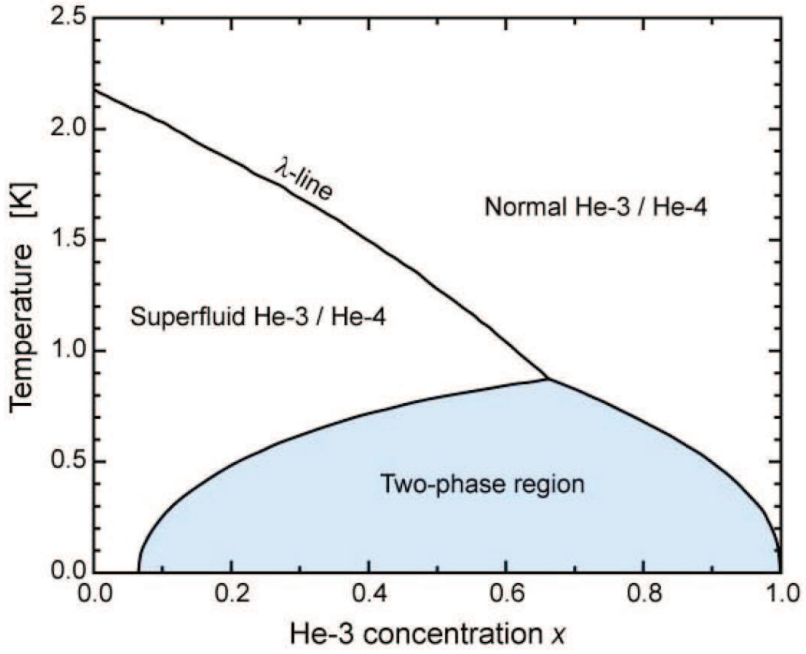


Figure 3.19: ^{3}He-^{4}He phase diagram for temperatures below 2.5 K as a function of ^{3}He concentration, showing the phase separation at low temperature. *Adapted from ref* [13].

3.5.2 Filtering

The effective electron temperature in the sample will be significantly hotter than the mixing chamber if there is insufficient filtering. Filters were added by B. Villis at two stages: a low pass filter at the 4 K plate, and an inductive RC filter on the mixing chamber plate.

3.5.2.1 Low-pass Filter

Copper powder filters based on work done by Mueller et al [75] act as low pass filters, suppressing high frequency noise (f $\geq$ 10 GHz). Figure 3.20 shows the filter mounted beneath the 4 K plate, and its constituent parts. A PCB with meandering pairs of length $>$1 m was covered with a mix of equal parts by mass copper powder (spherical, APS 10 μm) and high resistivity STYCAST 2850FT Blue with low viscosity Catalyst 23 LV. This was enclosed in a copper holder with rubberised ECCOSORB JCS-9 before mounting.

3.5.2.2 Inductive RC Filter

Figure 3.21 shows the inductive RC filter based on a patent by Kuemmeth et al [76]. Each DC line is filtered through a series of low-pass filters (Mini-circuits LFCN-5000, LFCN-1400, and LFCN-80), attenuating frequencies above 5000, 1400, and 80 MHz respectively, and two sets of RC filters (1 kΩ, 3.3 nF and 1 kΩ, 1 nF.)

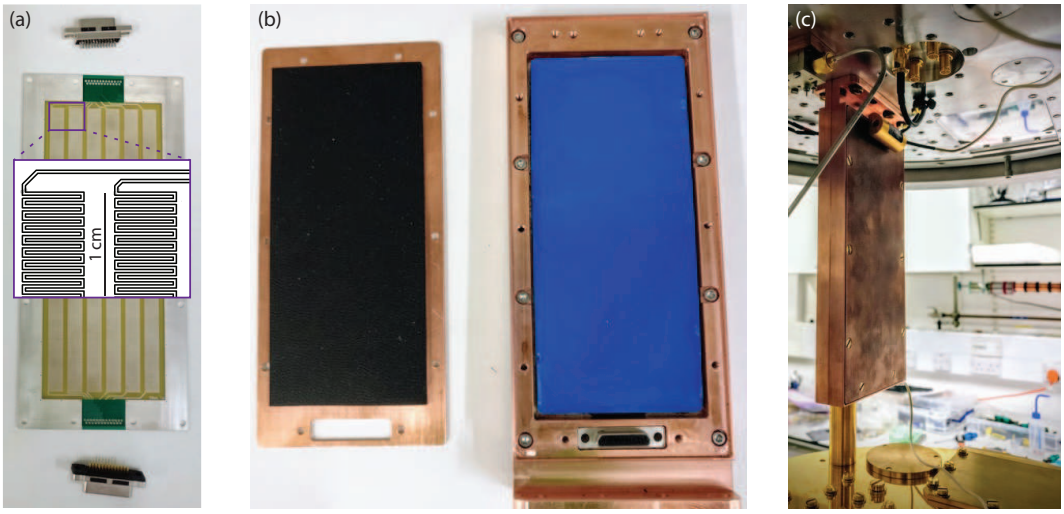


Figure 3.20: Low-pass filter. (a) PCB with meandering pairs, length >1 m. (b) ECCOSORB, STYCAST-copper powder mix, and the copper filter holder. (c) Filter mounted beneath the 4 K plate.

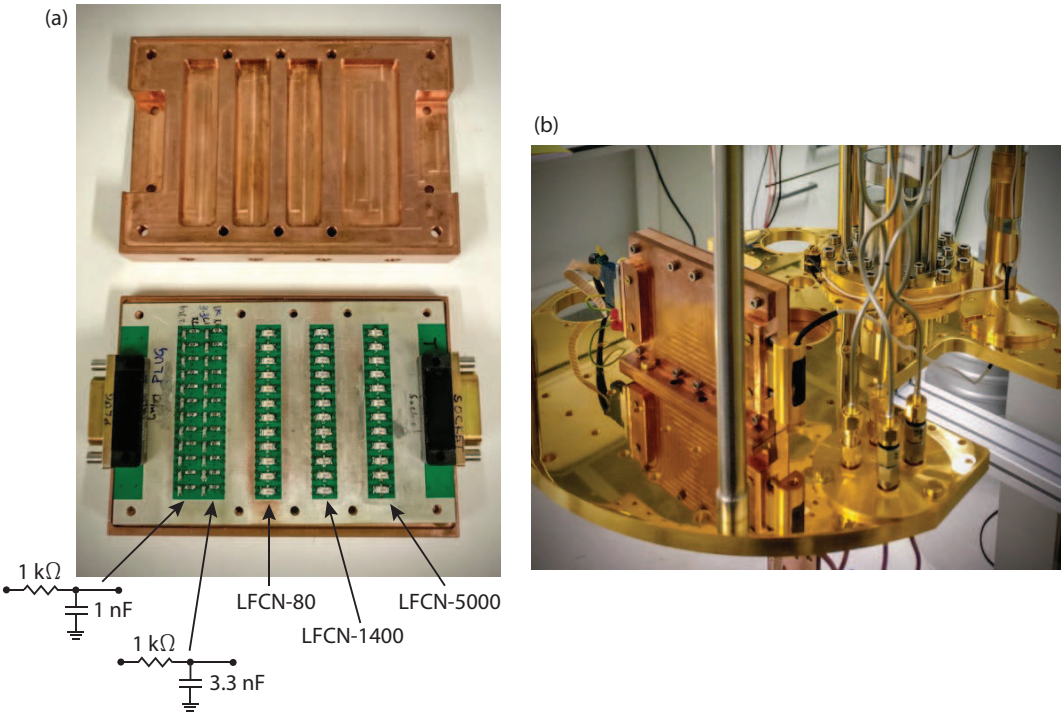


Figure 3.21: Inductive RC filter. (a) PCB with a series of low-pass and RC filters. (b) Filter mounted to the mixing chamber plate.

3.5.3 Measuring Electron Temperature

An energy diagram for a dot with source and drain contacts at finite temperature is shown in figure 3.22. The chemical potentials of the contacts are thermally smeared according to the Fermi distribution. The quantum dot chemical potential $\mu(N+1)$ is assumed to have negligible width due to lifetime broadening, $h\Gamma \ll k_B T$, where Γ is the tunnelling rate.

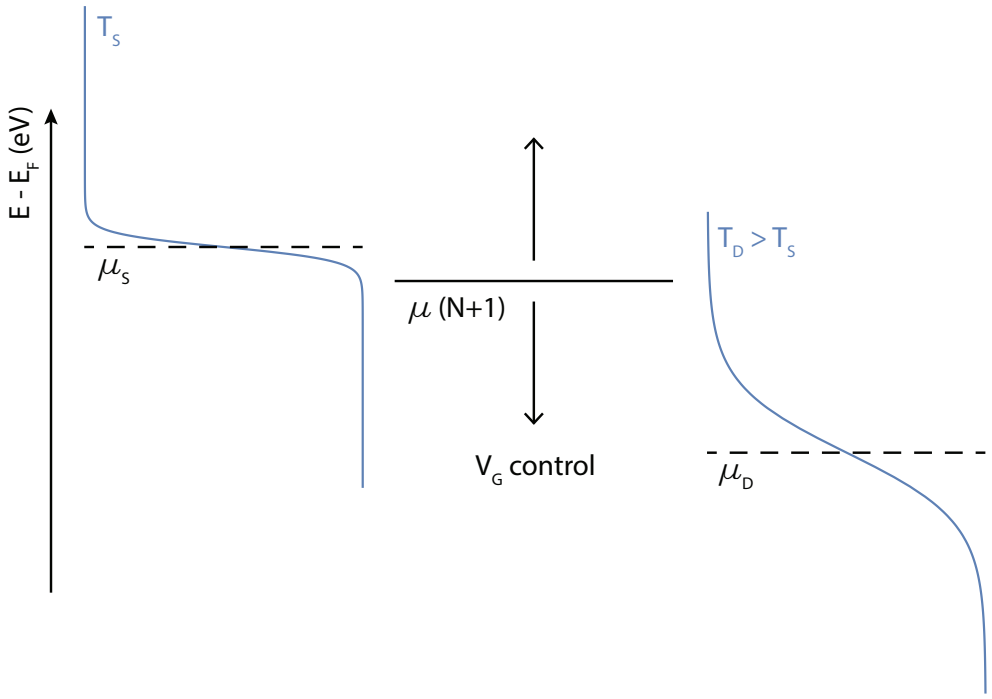


Figure 3.22: The chemical potential of the dot $\mu(N+1)$ of assumed negligible width can be shifted with respect to the source and drain chemical potentials $\mu_{S,D}$ (dashed lines) by changing the gate voltage V_G. As $\mu(N+1)$ is shifted, the Fermi distributions (blue lines) of the source and drain will be mapped out. Here the temperature of the source is taken to be lower than that of the drain, $T_S < T_D$, as seen in the data.

Given a source-drain bias large enough that the thermal smearing from the source and drain do not overlap and small enough that only one energy level appears in the bias window, the temperature of both contacts can be measured by sweeping the gate bias to map the Fermi distributions. The source-drain bias must also be small enough that the effect of increased lifetime broadening with increased bias is negligible. Figure 3.23 shows data from two gate bias sweeps at different source-drain biases.

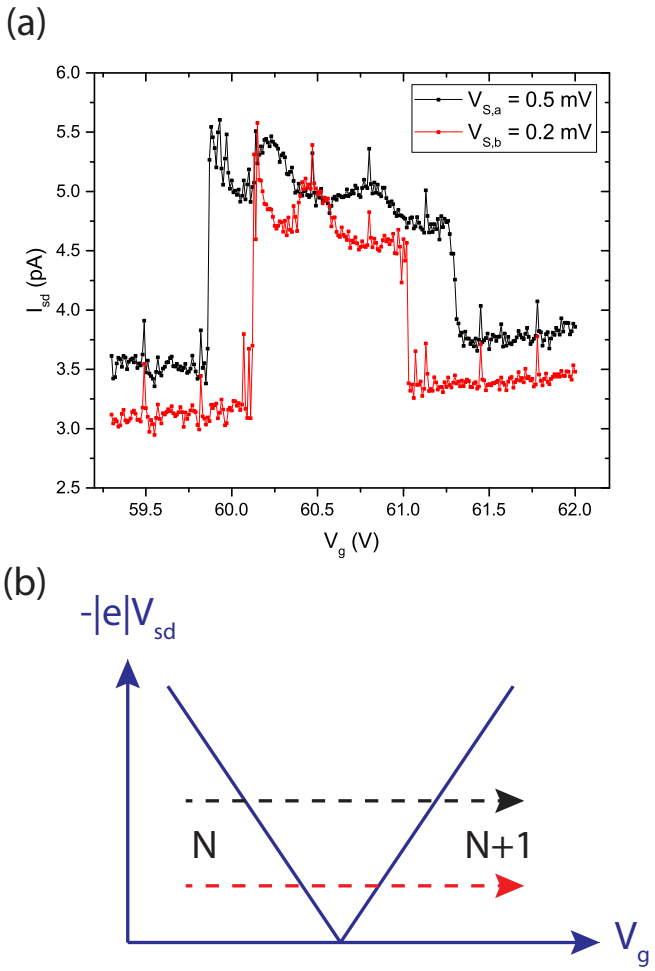


Figure 3.23: (a) Experimental data showing change in current with gate bias measured at two fixed source-drain biases. (b) Schematic showing measurement range in relation to Coulomb diamonds.

The effective temperature of the left and right contacts is extracted using equation 3.3 [77].

$$I_{FD}(V_G) = I_1 \left[\exp\left(\frac{\alpha(V_G - V_{G0})}{k_B T_{L,R}} \right) + 1 \right]^{-1} + I_0 \tag{3.3}$$

I_1 is the step height, I_0 is the offset current, V_{G0} is the gate bias offset and α is the lever arm.

Figure 3.24 shows the data and fits for two source-drain biases. The effective temperature of the right contact, T_R, is larger than that of the left, T_L, possibly due to the connected current preamplifier. The average T_R taken from nine readings was

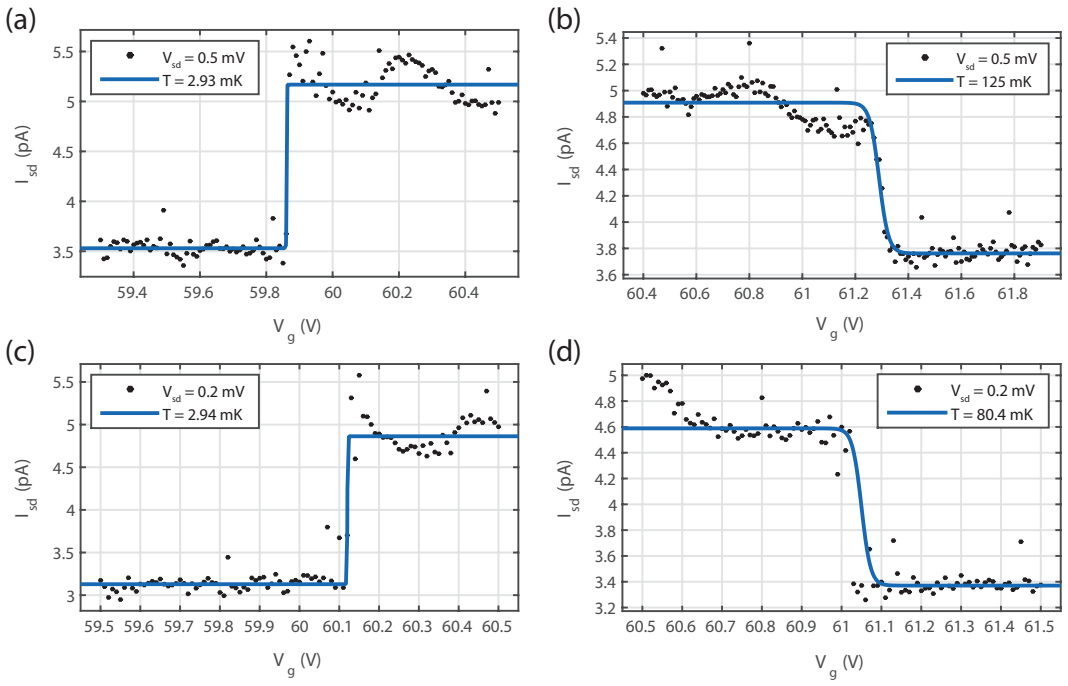


Figure 3.24: (a),(c) T_L and (b),(d) T_R fits using equation 3.3 for data taken at (a),(b) 0.5 mV and (c),(d) 0.2 mV.

107 ± 35 mK. The average T_L taken from the same nine readings was 2.07 mK, with extremely large uncertainties for each fit. The lack of resolution in the gate voltage is responsible for the poor estimation of T_L. For a 200 V range on the SMU, the resolution is 5 mV. T_R defines an upper limit for the electron temperature.

Similar measurements taken on carbon nanotube devices at lower gate biases (and thus finer resolution), estimated the electron temperature to be $T_L = 13 \pm 2$ mK.

Chapter 4

Experimental Details

4.1 Device Preparation

MoS_2 field-effect transistor (FET) devices were fabricated using mono- and bi-layer MoS_2 and WSe_2 crystals. The following section describes the fabrication process. Few-layer crystals are located and their thickness is determined before they are patterned with source and drain electrodes.

4.1.1 Isolating Few-Layer MoS_2 Crystals

Exfoliated MoS_2 and WSe_2 crystals were transferred onto highly p-doped silicon substrates (≤ 0.0015 Ω-cm, boron dopant), topped with a 280 nm thermal oxide. Figure 4.1 shows the mechanical exfoliation process used to isolate few-layer crystals.

A small (3 x 3 x 0.5 mm^2) piece of bulk crystal is placed onto a section of dicing tape for mechanical exfoliation. The tape is stuck and unstuck over the crystal, removing layers. After 5–10 cycles, the tape is left stuck together during the substrate cleaning process.

Sonication for 5 minutes in acetone, then 5 minutes in isopropanol (IPA), removes most of the adsorbed organic compounds from the substrate. After drying with nitrogen gas, N_2, the wafer is placed in a Diener electronic barrel configuration radio-frequency oxygen plasma asher for 20 minutes. After being left to cool, the dicing tape with exfoliated material is opened and immediately placed onto the substrate, avoiding trapping air bubbles beneath the tape. Minimum pressure is

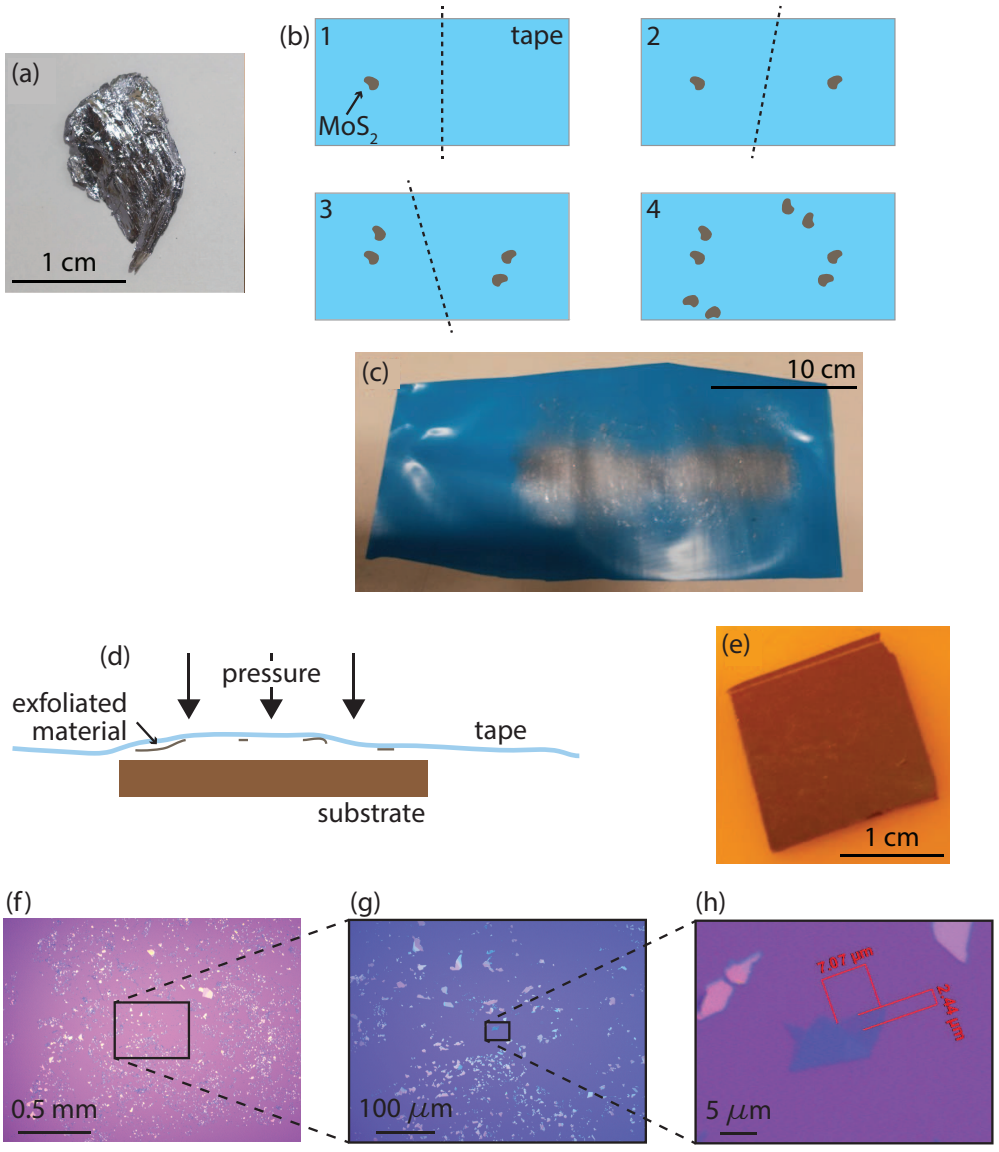


Figure 4.1: Photographs and schematics of the mechanical exfoliation process. (a) Bulk MoS_2. (b) Exfoliation schematic. Sticky tape is used to remove layers from the bulk MoS_2. The tape is folded gently along the dashed lines indicated; when the tape is unfolded, the bulk crystal is cleaved into thinner pieces. (c) After 5–10 cycles of sticking and unsticking the tape, there are a range of different thickness of MoS_2 spread out on the tape. (d) Exfoliated material is transferred from the tape to the substrate by applying a small amount of pressure, taking care to avoid air bubbles beneath the tape. (e) A photograph of exfoliated material on a Si/SiO_2 substrate. (f)-(h) Optical images focussing in on a specific MoS_2 crystal taken at a range of magnifications in order to relocate the crystal at a later date.

used to transfer the material. After 10 minutes, the tape is removed slowly and at a low angle.

Mechanical exfoliation cannot reliably produce a high density of large, isolated few-layer crystals. A number of parameters were explored to increase the density of viable crystals. Below is a list of the improvements made from the initial graphene exfoliation process described in [7].

- Extended substrate cleaning with an oxygen plasma
- Reduced number of sticking–unsticking cycles
- Increased tape resting time between exfoliation and transfer and removal
- Reduced transfer pressure
- Slower tape removal after transfer
- Lower angle tape removal after transfer

4.1.2 Position and Thickness Characterisation

Mono- and bi-layer MoS_2 crystals on a Si/SiO_2 substrate are located using an optical microscope, with the contrast dependent on crystal thickness, SiO_2 thickness, and illumination wavelength. The substrates used in this work have a 280 nm thick oxide layer for optimum contrast when using white light [78, 79]. Optical detection is fast, non-expensive, and non-destructive. Crystal thickness is then verified using Raman spectroscopy (section 3.4) and atomic force microscopy (AFM, section 3.2).

Raman spectra were taken using a RENISHAW inVia Raman Microscope, with a laser wavelength of 532 nm. Separation between the E^1_{2g} and A_{1g} peaks is thickness dependent.

Low force contact mode AFM was used for good z-control; tapping mode AFM was found to exaggerate the height difference.

Figure 4.2 shows optical, Raman, and AFM data for mono- and bi-layer MoS_2.

Suitable crystals were fabricated into field-effect transistors by evaporating metal source and drain contacts; the highly doped silicon substrate is used as a

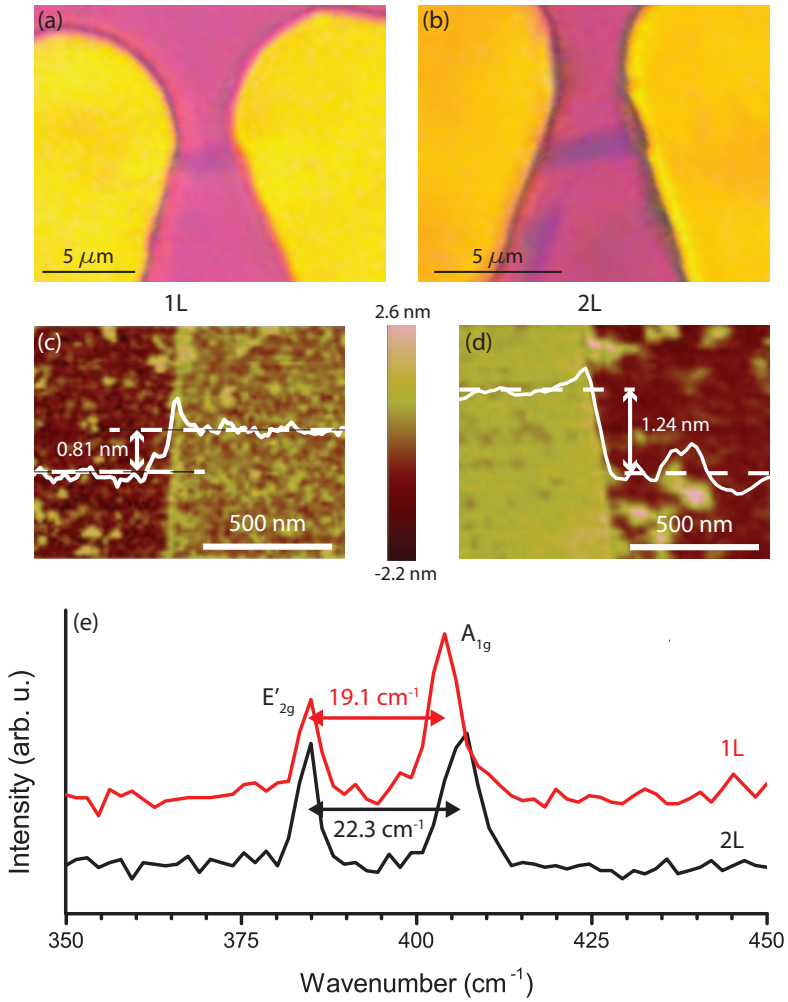


Figure 4.2: (a),(b) Optical images of contacted (a) monolayer and (b) bilayer MoS_2. (c),(d) AFM images showing (c) monolayer and (d) bilayer thickness. Resist residues can be seen in these images, because the crystals were imaged with an AFM after the photolithography process (section 4.1.3). (e) Raman spectra for mono- and bi-layer MoS_2, offset for clarity.

back gate. Source and drain patterning was achieved using two primary methods: photolithography (section 4.1.3), and shadow mask evaporation (section 4.1.4).

A device fabricated using the shadow mask evaporation (SME) technique will have a clean surface and fewer defects making it ideal for atomic force microscopy lithography (section 3.3) and transport measurements. However, SME takes longer, as only one device can be metallised at a time. On top of this, the masks used in SME are etched using a very finely balanced recipe. A small number of masks were successfully fabricated before the deep reactive-ion etcher (DRIE) used to etch the masks was subject to technical difficulties for a number of months. The work was

continued by technical staff in Edinburgh, but they were unable to reproduce masks of a high enough quality.

As an alternative, contacts were patterned using photolithography (PL). The PL technique is significantly faster and more reliable, but results in lower quality devices. Data presented in chapters 5 and 6 is from PL-patterned devices.

4.1.3 Contacting Devices Using Photolithography

The photolithography process is shown schematically in figure 4.3.

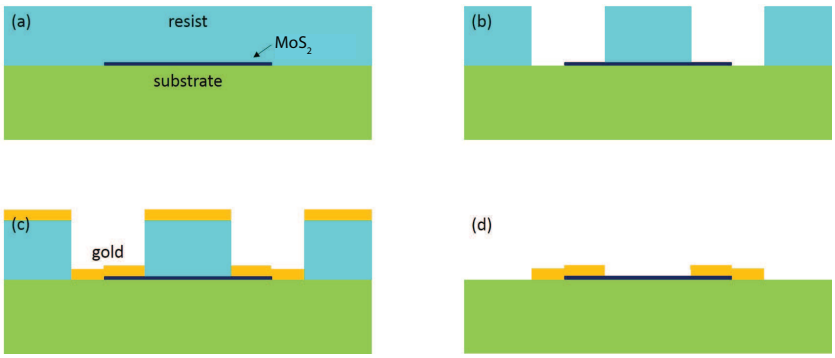


Figure 4.3: A schematic of the photolithography process. (a) A polymeric resist is spun onto the sample. (b). Parts of the sample are exposed to ultraviolet light. When the sample is developed, the exposed areas will be removed. (c) Metal is evaporated onto the sample. (d) The remaining resist is removed during the lift-off stage, leaving behind metal in the exposed pattern.

To selectively metallise the sample, a photo-sensitive polymer, S1818 (from the Shipley Microposit® S1800® series), is spun onto the surface. The crystal is aligned by eye beneath a quartz mask patterned with chromium. The mask and substrate are brought into contact and the set-up is illuminated with ultraviolet light for ∼2.5 seconds. Parts of the sample beneath chromium remain dark and are unaffected. Where there is no chromium blocking the UV light, the polymer chains are shortened. During the 60–75 second development process in MF-26A following exposure to UV light, these shortened chains are removed. The sample is rinsed in de-ionised (DI) water and dried with N_2 gas before loading into an evaporation chamber.

Contacts were formed of 20/70 nm of titanium/gold, evaporated using an Edwards A500 electron beam evaporator. After evaporation, samples were placed

in acetone overnight. This removes the resist, taking with it the unwanted metal. The sample is rinsed in IPA and dried with N_2 gas.

4.1.4 Resist-free Contacting: Shadow Mask Evaporation

Residual resist leftover from the metallisation process can affect atomic force microscope lithography (AFML) [52], scanning tunnelling microscopy (STM), and transport properties [64]. Figure 4.4 shows the increased sample roughness after photolithography. The RMS roughness, R_q, and average deviation, R_a, are given for each image, defined in equations 3.1 and 3.2 in section 3.3.3.

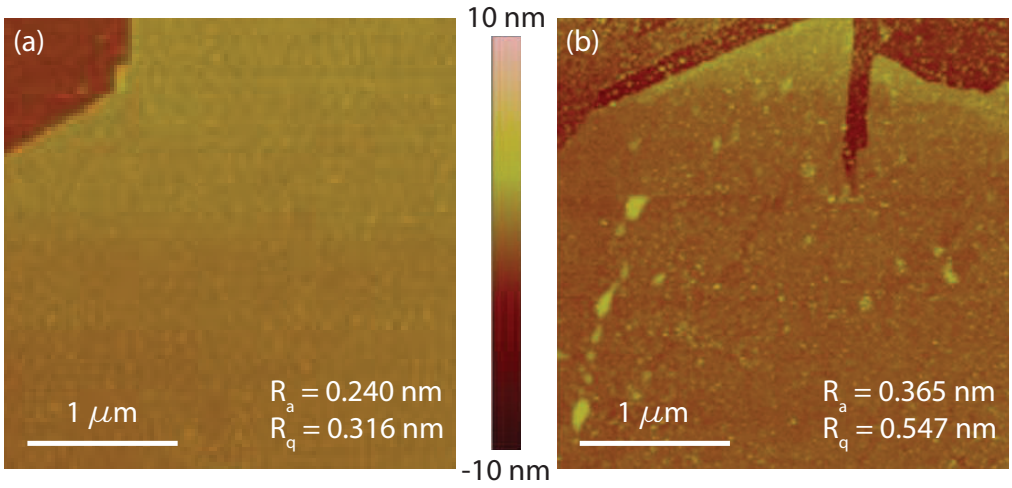


Figure 4.4: AFM images of (a) an unprocessed MoS_2 crystal and (b) an MoS_2 crystal after photolithography, with resist residues. R_a and R_q are the average deviation and RMS roughness respectively.

In AFML (section 3.3), the large voltages applied result in a large electric field forming in the vicinity of the AFM tip ($E \sim 10^6$ Vm^{-1}). Resist residue can weaken the field and make the sharp tips dirty and therefore blunt. These problems can be avoided by using a resist-free contacting method: shadow mask evaporation (SME), shown schematically in figure 4.5.

To create metal contacts, a patterned silicon mask and 2-D crystal are aligned before evaporating onto the sample through the mask. Patterns are etched into thin (150 μm) silicon wafers using photolithography followed by deep reactive-ion etching (DRIE). Details of the fabrication process for the silicon mask can be found in appendix A.

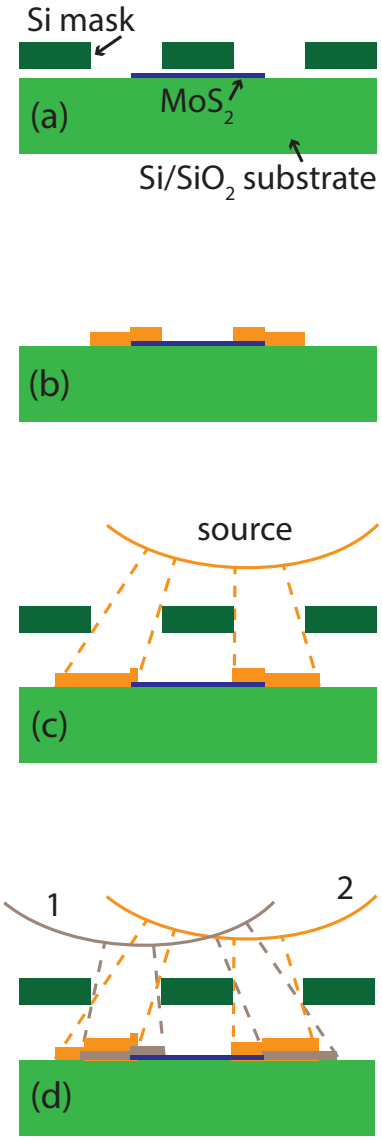


Figure 4.5: (a) The shadow mask is aligned to a crystal. (b) An ideal evaporation. (c) A diagram of the lateral offset caused by having a small source-sample separation in the evaporator in combination with a slightly off-centre source. (d) Diagram for two-layer contacts (e.g. 1 = titanium, 2 = gold). Mis-alignment between the two sources will result in a lateral offset.

4.1.5 MoS_2 Sample Mounting

The devices are mounted with GE-varnish (CMR-Direct) onto a sample holder designed for both atomic force microscopy and transport measurements. For low temperature measurements in the dilution refrigerator, detailed in chapter 6, the sample holder can be mounted either parallel or perpendicular to the magnetic field.

The back gate is connected using silver paste applied by hand with a small gauge wire; source and drain contacts are contacted using a wedge bonder fitted with 25 μm gold wire.

Room temperature transport, detailed in chapter 5, was characterised as a function of measurement speed, bias range and bias stress history, in ambient, under vacuum, and at room temperature after vacuum annealing.

4.2 Sample Holder Design

The sample holder used for this work was required to be transferable from one experimental environment to another, namely: low temperature transport measurements with the holder mounted either perpendicular or parallel to the magnetic field, atomic force microscope imaging and lithography, and room temperature measurements and annealing in a vacuum chamber. A new multi-purpose sample holder was designed, removing the need for re-mounting and re-bonding and thus avoiding device damage.

Printed Circuit Board Design

There are 24 DC lines leading down to the sample. Although only three DC lines are needed per device, PCBs were designed for use with 25 DC lines via a micro-D connector: 24 for the fridge, and ground. Sample mounting space was maximised. Together, this allowed for the cooling and measuring of multiple devices and more accessible bonding. Figure 4.6 is a photo and diagram of the final PCB design, including components used for vacuum annealing, discussed below.

Atomic Force Microscope Requirements

During AFM, the probe, and the head upon which it is mounted, are very close to the surface. The PCB design was required to be low profile. A right-angle

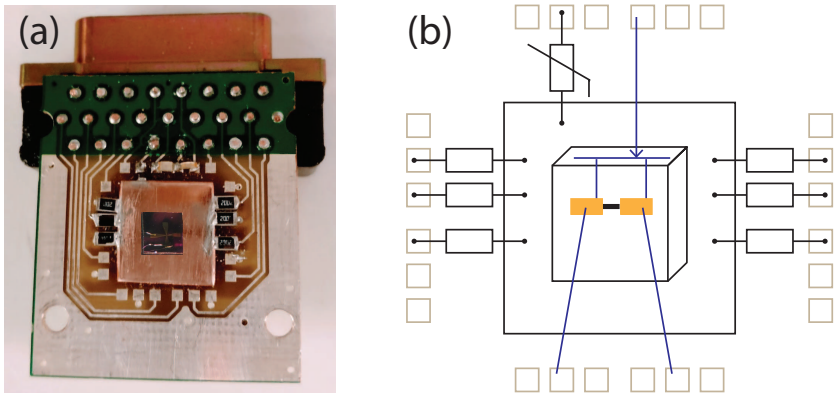


Figure 4.6: (a) PCB with six 20 kΩ resistive heaters, a thermistor, and MoS_2 sample. (b) Component configuration.

micro-D connector was selected, mounted below the board.

Large voltages up to 60 V were applied to the sample during AFM lithography. To bypass the AFM electronics, rated up to 12 V, the AFM tip was grounded separately. A replacement rotating stage (figure 4.7) was designed to match the joint of the standard stage. A step the height of the right angle connector with threaded holes is used to mount the PCB, with low-profile plastic screws. These measures help sample stability during imaging and lithography by removing sources of mechanical vibration.

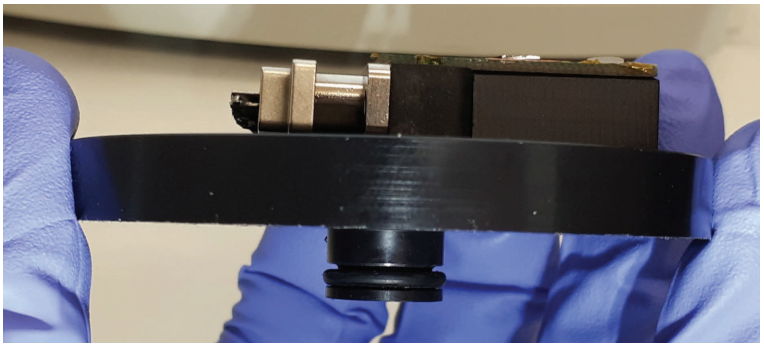


Figure 4.7: Side view of replacement AFM stage made of acetal resin.

Low Temperature Measurement Requirements

In the dilution refrigerator, cooling is achieved in stages (figure 4.8). The final plate is the mixing chamber, at $T \leq 10$ mK. The superconducting magnet is held below here. Samples to be tested in the magnet are mounted to a cold finger which

extends below the plate into the bore of the magnet. The cold finger was made from copper for good thermal conductivity; the design included an array of M3 and M4 holes to suit the different sample holders in use with positioning flexibility.

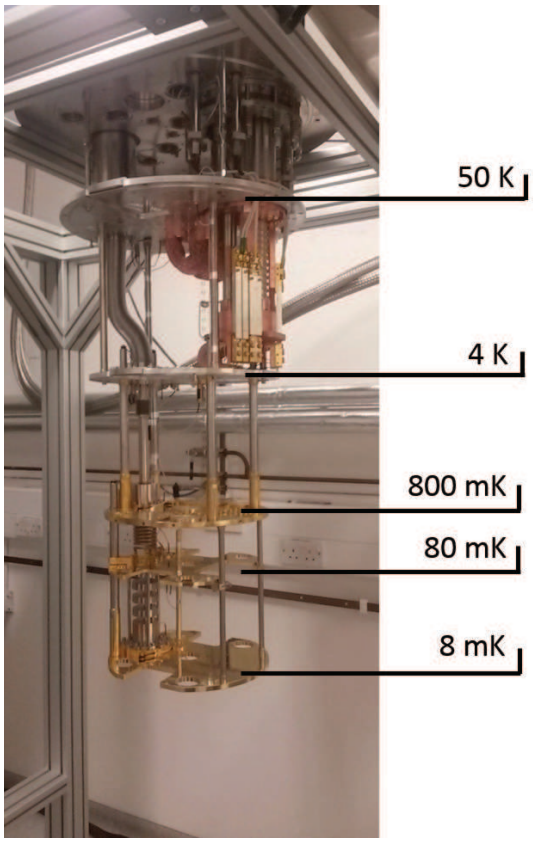


Figure 4.8: Temperatures at different stages in the BlueFors LD250 dry dilution refrigerator.

The cold finger of width $w_{cf} < 2r$ sits centrally in the bore of radius r. Mounting the sample holder parallel to the magnetic field puts a limit on its height $h_{sh} < r$. Mounting the sample holder perpendicular to the magnetic field puts a limit on the holder width $w_{sh} < w_{cf}$ and length $l_{sh} + l_{\text{micro-D connector}} < 2r$. In addition to dimension limitations, good thermal conductivity is required to ensure a low sample temperature.

The finalised design for the sample holder base is shown in figure 4.9(a),(b). Beneath the PCB, copper has been removed to avoid shorts, with a raised platform directly underneath the sample to improve thermal conductivity. Figure 4.9(c) and (d) show the holder mounted to the cold finger parallel and perpendicular

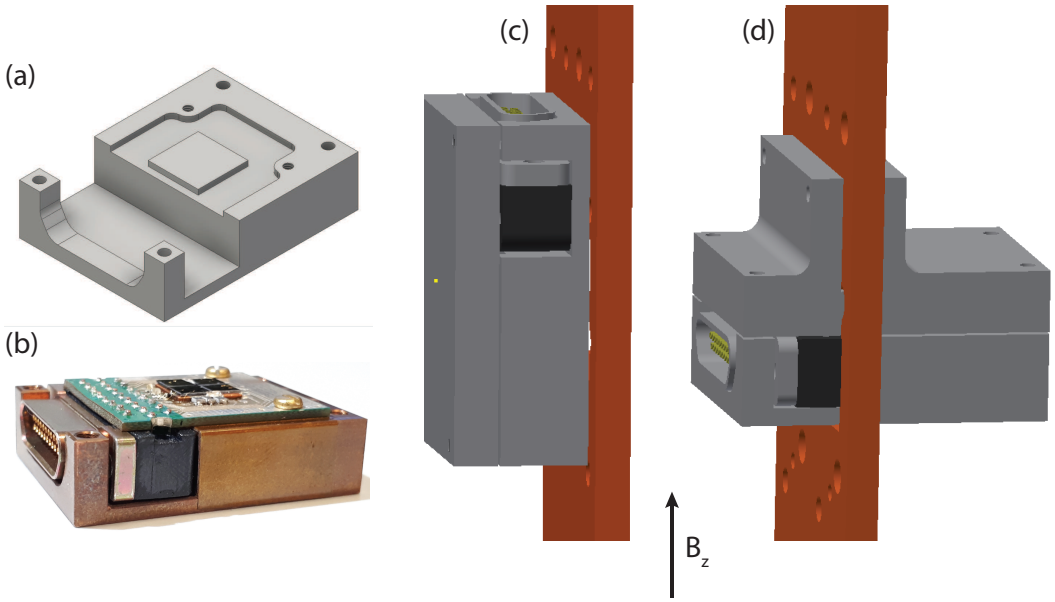


Figure 4.9: Sample holder design. (a) base, with material removed to avoid electrical shorts. (b) sample holder in use, with four devices. (c),(d) sample holder mounted (c) parallel and (d) perpendicular to the magnetic field.

to the magnetic field, respectively. The two configurations require different lids, engineered to improve thermal connection. All parts of the sample holder are made of copper.

4.3 Vacuum Annealing

After pumping to below 5×10^{-7} mbar and taking transport measurements in vacuum, samples were heated by applying a large voltage, ≤ 200 V, to four 20 kΩ resistors connected to the sample substrate. The circuit diagram is shown in figure 4.10. A thermistor mounted on the far side of the PCB was used to record the temperature reached, typically around 140 °C. The resistance of the thermistor used reduced when heated; the temperature dependence is shown in figure 4.11. The temperature-resistance relation for the thermistor can be modelled as:

$$\frac{1}{T} = A + B\ln R + C(\ln R)^3 \tag{4.1}$$

Parameters A, B and C were calculated using known points given on a calibration sheet. During annealing the resistance was measured and the

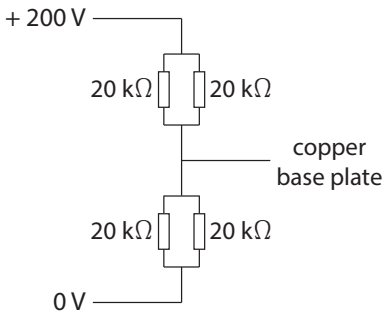


Figure 4.10: Circuit diagram showing the resistive heater configuration used for vacuum annealing.

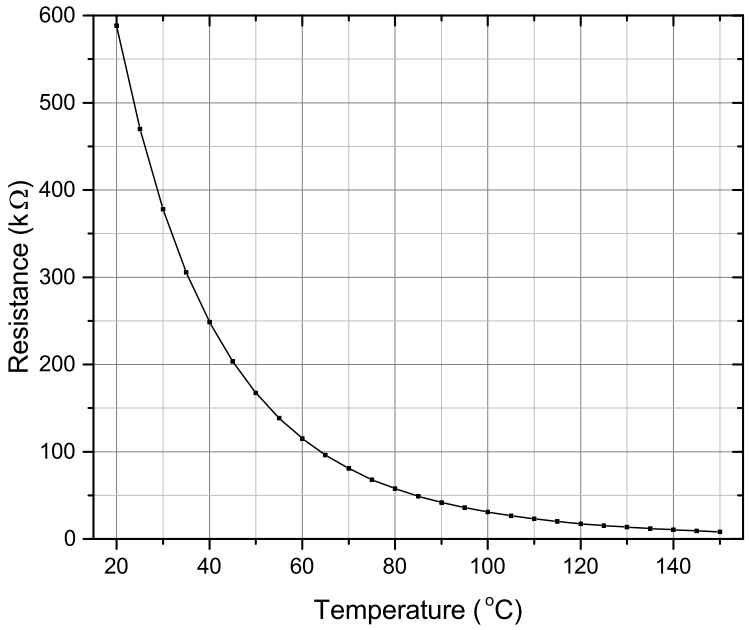


Figure 4.11: Temperature dependence of thermistor resistance. Points on the curve given by a calibration sheet. The curve can be fitted using equation 4.1.

temperature was calculated using equation 4.1. Figure 4.6(b) shows schematically the resistor, thermistor, and sample configuration.

4.4 Transport Measurement Set-Up

Room temperature measurements were carried out using two KEITHLEY SourceMeter® SMU Instruments: 2450 and 2400, with device communications via GPIB. The voltages were applied to the sample via a 25-pin break-out box fitted

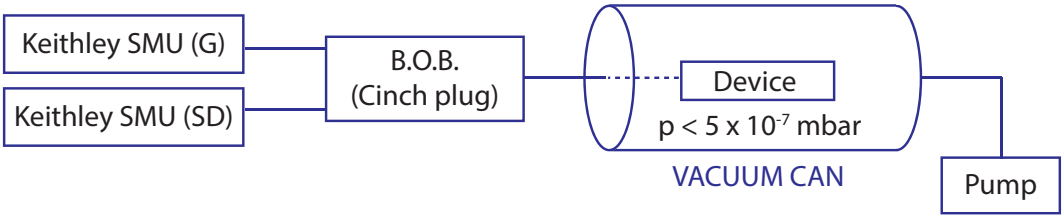


Figure 4.12: Room temperature measurement set-up showing vacuum can used for vacuum annealing. Two Keithley source-measure units are used with a homemade break-out box.

with 50 Ω resistors to ground. A diagram of the set-up is shown in figure 4.12.

At low temperature, the large voltages required for gate biasing were supplied by a KEITHLEY 2450 SourceMeter® SMU Instrument (V_{max} = 200 V). This was also used to measure the gate leakage current. The smaller, more precise, voltages required for source-drain biasing were supplied to each device using a BILT BE2101 module (V_{max} = 12 V). For a 12 V (1.2 V) range, the resolution is 12 μV (1.2 μV).

Source-drain currents were passed through a Stanford Research Systems SR570 low noise current preamplifier, and converted using a KEITHLEY KUSB-3116 data acquisition module (DAQ). A diagram of the low temperature transport measurement set-up, including filters at the 4K and mixing chamber plates as discussed in section 3.5.2, is shown in figure 4.13.

4.4.1 Data Acquisition

Device communication was carried out using MATLAB, following the measurement process for a gate sweep outlined in figure 4.14. Two KEITHLEY SMUs were initialised and then ramped to the initial source-drain and gate biases. Pauses at the minimum gate voltage and before the current measurements in each cycle were lengthened and shortened to test the effects of negative bias stressing and measurement frequency respectively. Gate current was also measured to check for shorts across the gate dielectric.

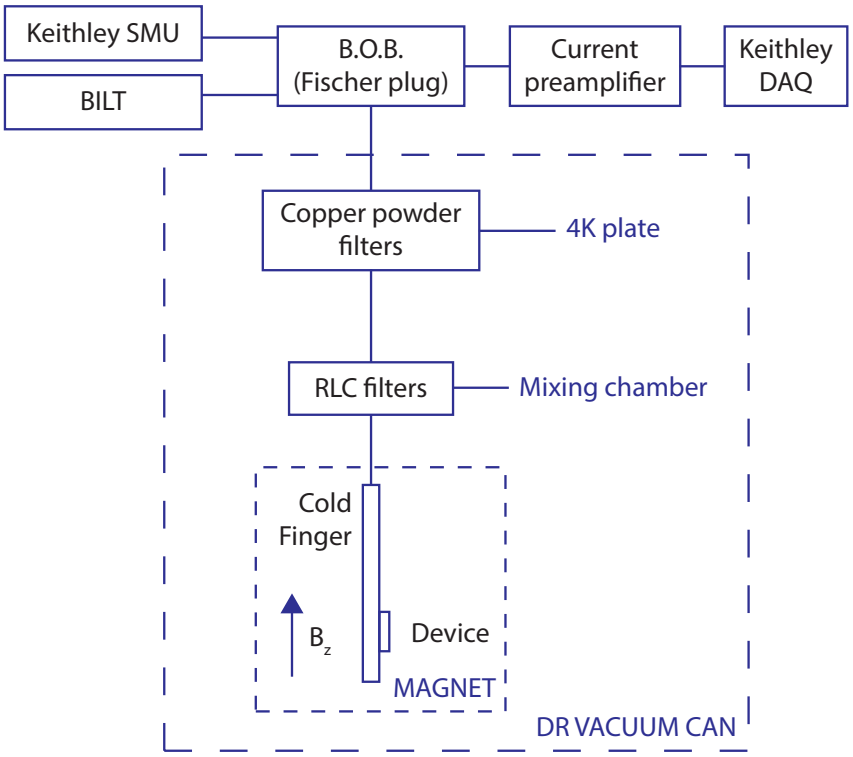


Figure 4.13: Dilution refrigerator (DR) measurement set-up showing the voltage sources (SMU, BILT) and data acquisition (DAQ via a current preamplifier). Inside the DR vacuum can the DC lines are filtered at the 4K and mixing chamber plates (see section 3.5.2). The device, mounted on the cold finger, extends into the centre of the magnet.

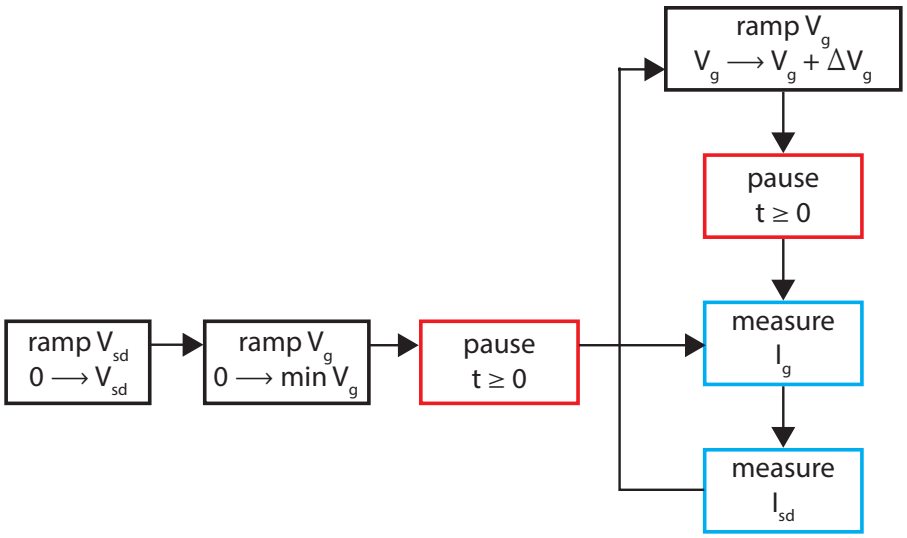


Figure 4.14: Flowchart of the measurement process. A pause after ramping to the minimum gate bias is used to observe the effect of negative bias stressing; a pause after stepping the voltage by ΔV is used to explore the effect of changing the measurement frequency.

Chapter 5

Room Temperature Transport

A full understanding of transport behaviour is important for device application. An ideal device should have predictable and stable current-voltage characteristics, with a high mobility, and low hysteresis in the current as a function of gate voltage.

In order to understand MoS_2 field-effect transistor behaviour, transport at room temperature and low temperature has been studied in this work in detail. Charge traps and defect states heavily influence the transport properties and are explored in more detail here and at low temperature in chapter 6. Figure 5.1 shows a typical transfer curve from one of the bilayer MoS_2 field-effect transistor devices studied in this chapter, along with the analysis done.

Important characteristics are the maximum source-drain current, I_{max}, the forwards and reverse threshold voltages, $V_{T,F}$ and $V_{T,R}$, taken by extrapolating down from the linear region as shown in figure 5.1, the hysteresis (taken as the difference between forwards and reverse threshold voltages), $\Delta V_T = V_{T,R} - V_{T,F}$, and the field-effect mobility, μ_{FE}, proportional to the gradient in the linear region (equation 2.3). It is important to note that calculating the mobility in this way assumes that only the gate bias changes the electric field. However, in measurements of these devices, the electric field is subject to additional modifications due to the changing occupation of charge traps. Forwards and reverse mobilities are recorded to give upper and lower bounds for μ_{FE}.

Transport across MoS_2 field-effect transistors is an area of active research [25, 27, 80, 81, 82]. Environmental factors such as adsorbed water [25], and

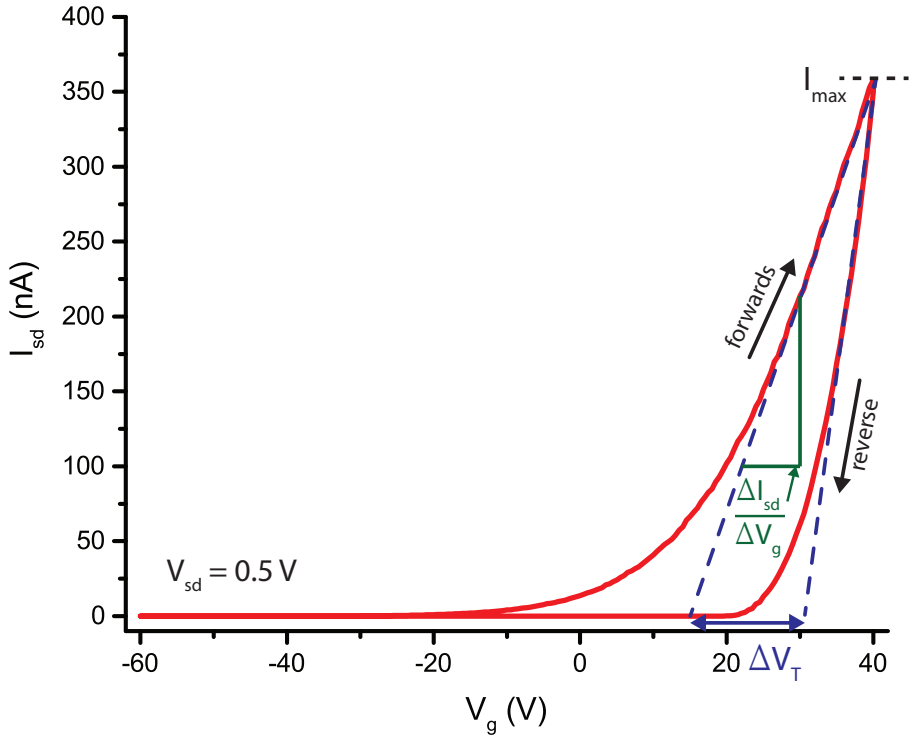


Figure 5.1: Source drain current, I_{sd}, as a function of gate voltage, V_g, with fixed source drain voltage, V_{sd} = 0.5 V: a representative single transfer curve showing the analysis done. Hysteresis is the difference between forwards and reverse threshold voltages; mobility is proportional to $\Delta I_{sd}/\Delta V_g$.

measurement parameters such as voltage ramp rate [82], have been seen to affect device performance. In ambient conditions there is considerable hysteresis seen in the transfer curves of both suspended and supported MoS_2 devices [80]. Increased water adsorption increases hysteresis as seen in a study varying humidity levels [25] and thinner MoS_2 samples show more hysteresis, implying a large surface contribution [80]. Sweep range, sweep direction, sweep rate, and bias stressing history all have an effect on the hysteresis [80, 81, 82].

Attempts have been made, in this work and in the wider literature [25, 27, 82] to remove the hysteresis entirely, with varying success. Pumping on devices and thermal annealing reduce hysteresis but may not remove the effect entirely. Illarionov et al [82] still observed significant hysteresis after annealing at 85 °C under vacuum ($p < 6.7 \times 10^{-6}$ mbar) for 6 days. Roh et al [27] employed two thermal annealing steps for successful hysteresis elimination: the first after

transfer and before contacting; the second after lift-off. Each annealing step was at 400 °C for 1 hour in a H_2/Ar mix. Late et al [25] passivated devices with PECVD (plasma-enhanced chemical vapour deposition) grown Si_3N_4, successfully eliminating hysteresis. Device conductivity also increased by two orders of magnitude. They suspect this is due to the Si_3N_4 thin film preventing water adsorption on the MoS_2 surface. However, the eliminated hysteresis may partly be occurring indirectly, due to the high temperatures and low pressures used. Prior to film growth the device is held at 300 °C at 7×10^{-3} mbar for one hour to remove moisture before deposition; during Si_3N_4 deposition, the device is at 300 °C at 0.43 mbar. Despite the successful elimination of hysteresis using a Si_3N_4 passivation layer, no attempts were made to replicate these results as an uncovered MoS_2 surface is required for AFM lithography (section 3.3).

In this work, mobility, threshold voltage, current, and hysteresis are used to characterise MoS_2 bilayer FETs measured under various experimental conditions. We show that charge traps play an important role and develop a model that qualitatively captures the observed transport behaviour.

5.1 Bilayer MoS_2 Transfer Curves

Room temperature transfer curves were taken for several bilayer MoS_2 devices. A typical measurement is shown in figure 5.1. Measurements were taken in ambient conditions, under a vacuum $< 5\times10^{-7}$ mbar, and at room temperature after annealing in vacuum at T >140 °C for 2–12 hours. Transfer curves for three devices under test (DUTs) at the three stages are shown in figure 5.2. The data shown has been offset by a small amount dependent on the current range set on the source-measure unit.

After pumping, the devices show increased conductance and mobility, and significantly reduced hysteresis, where hysteresis ΔV_T is defined as the difference between threshold voltages recorded for forward and reverse sweeps $\Delta V_T = V_{T,R}$ - $V_{T,F}$. Reduced hysteresis under vacuum has been ascribed to the removal of charge traps in the form of adsorbed water molecules [24, 25].

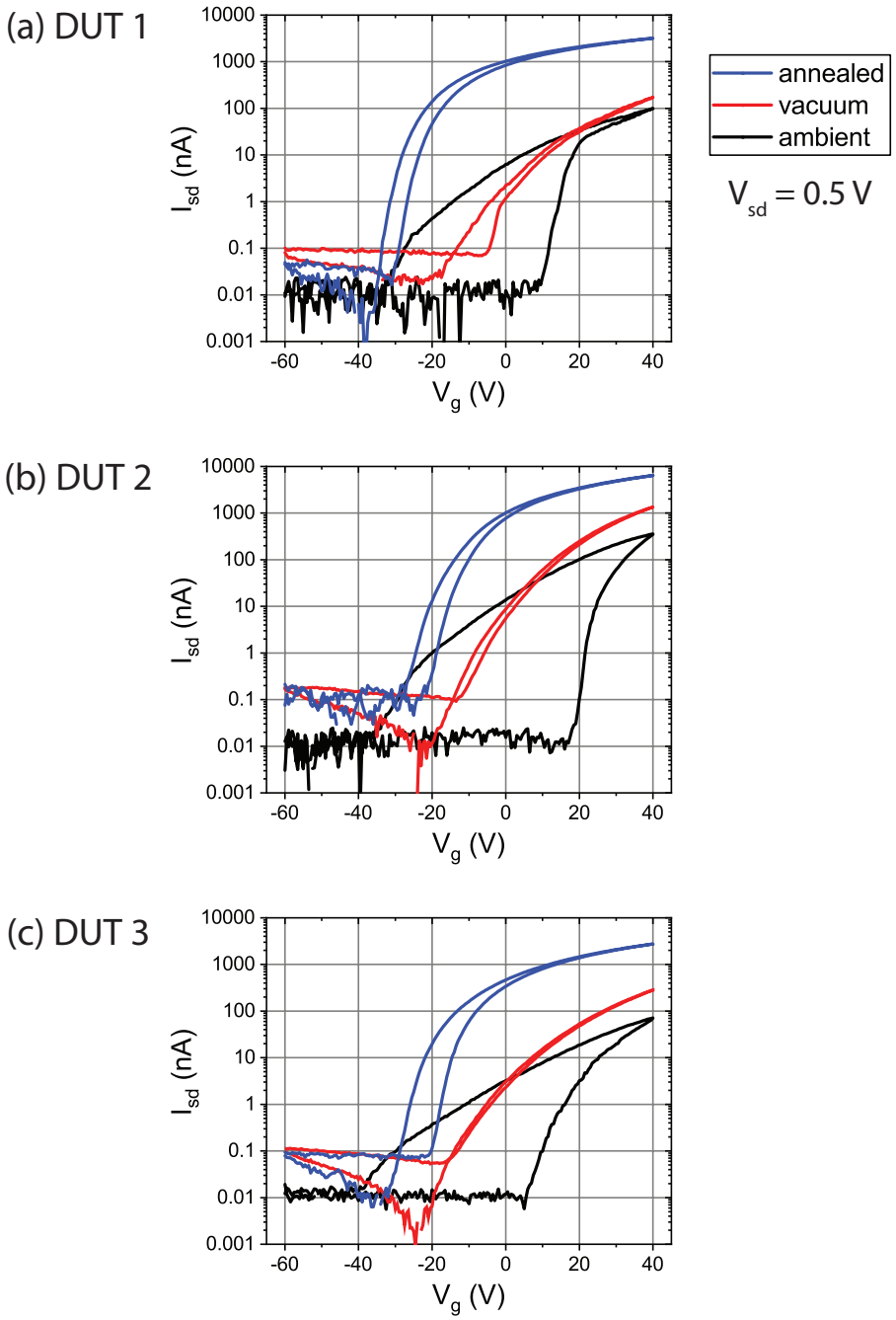


Figure 5.2: Transfer curves in ambient, in vacuum ($p < 5\times10^{-7}$ mbar), and at room temperature after annealing in vacuum at 140 °C for three bilayer MoS_2 devices. V_{sd} = 0.5 V.

In addition, after pumping, some unusual sub-threshold behaviour is seen. Starting from a minimum gate bias of V_g = –60 V, the current decreases sharply before the device turns on at $V_g \simeq$ –20 V. This same shape is seen in all devices, for measurements in vacuum and after annealing. This sub-threshold behaviour may be due to stray capacitances in the system. It should be noted that although the effect appears drastic on a logarithmic plot, the total deviation is on the order of 100 pA, 3-5 orders of magnitude lower than the ON current.

The capacitance arising from the metal electrodes (C_e) may explain the small deviation. Charge is a function of capacitance and bias: $Q = CV$. Differentiating, the current due to the electrode capacitance is

$$I = \frac{dQ}{dt} = C_e \frac{dV}{dt} \tag{5.1}$$

where C_e is a function of the geometry

$$C_e = \varepsilon_0 \varepsilon_r \frac{A}{d} \tag{5.2}$$

Using the vacuum permittivity, $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m, relative permittivity for SiO_2, $\varepsilon_r \simeq 4$, electrode area, $A \simeq 3 \times 10^{-7}$ m^2 and dielectric thickness, $d = 280$ nm, the electrode capacitance is approximately $C_e \simeq 4 \times 10^{-11}$ F. Depending on the ramp rate, dV_g/dt, this yields a current of 80–250 pA.

After annealing, the devices show a further large increase in conductance and mobility, due to the improved metal-MoS_2 contact. There is a negative shift in the threshold voltage, which may be the result of a shift in the charge neutrality level (ϕ_0) defining the Schottky barrier height, $\phi_B = S(\phi_M - \phi_0) + (\phi_0 - \chi_S)$ with ϕ_M the metal work function, χ_S the semiconductor electron affinity, and S the pinning factor (see section 2.2.3). Hysteresis increased for all three devices measured. This behaviour is unexpected, and is discussed further in section 5.3.

5.2 Model

A model based on the charging and discharging dynamics of the charge traps has been developed that qualitatively captures the changes in hysteresis observed in the experimental data. Firstly, an ideal transfer curve, current as a function of gate voltage, has been modelled, discussed in section 5.2.1. Secondly, the effect on the electric field as a result of the changing charge state of the traps during a measurement is modelled in section 5.2.2. A change in effective electric field corresponds to a change in the effective applied gate voltage, thus modifying the ideal transfer curve. The amount of hysteresis changes depending on measurement frequency, charge trap density, and bias range.

5.2.1 Modelling Ideal Transfer Characteristics

To model ideal device transport, three central assumptions are made [83].

1. Ideal gate: no leakage through the gate insulator. The gate leakage was measured as part of the experiments and was negligible.

2. Ideal contacts: no voltage drop at the source or drain. This is unlikely to be true, as there will be some contact resistance. This would cause the sharp step seen between the 'off' and 'on' current states of the transistor (figure 5.3) to be shallower, with a wider gate voltage window for the transition between 'off' and 'on'. As the modifications due to the charge state of the traps are all relative, this does not change the qualitative outcome.

3. Ballistic transport: no electron scattering in the channel. This is also unlikely to be true. All of the models use a normalised current I_{sd}/I_{max}, so even though in practise scattering would lower the mobility, this would not change the qualitative outcome.

Using a further assumption that mobility, μ, is independent of carrier density, the current is directly proportional to the carrier density n_s: $I_{sd}/V_{sd} = |e|n_s\mu$, where e is the electron charge.

The carrier density for electrons in a 2D material is [83]:

$$n_s = \frac{g_s g_v}{(2\pi)^2}\frac{m_c^* k_B T}{\hbar^2}\pi \ln[(1+\exp[\eta_s])(1+\exp[\eta_d])] \tag{5.3}$$

where g_s, g_v are spin and valley degeneracy values, m_c^* is the carrier effective mass (m_c^* = 0.38 m_0 for bilayer MoS_2), and $\eta_i = (E_{Fi} - E_c)/k_B T$ with i = s,d, are source and drain degeneracy terms defining quasi Fermi levels E_{Fi}. E_c is the conduction band minimum.

The sheet carrier density, n_s, can then be plotted as a function of a modified back gate voltage, $V_g - V_T$, where V_g is the applied gate bias and V_T is the threshold voltage:

$$e^{\frac{n_s}{n_b}}\left(e^{\frac{n_s}{n_q}} - 1\right) = e^{\frac{V_g - V_T}{V_{th}}} \tag{5.4}$$

where n_b is proportional to the thermal voltage $V_{th} = k_B T$ and the back gate capacitance C_b,

$$n_b = C_b V_{th}/q \tag{5.5}$$

and n_q is proportional to the quantum capacitance $C_q = q^2 D_0$, with $D_0 = g_s g_v \frac{m_c^*}{2\pi\hbar^2}$ the density of states, as derived in section 2.2.5.

$$n_q = C_q V_{th}/q \tag{5.6}$$

To plot n_s, equation 5.4 is simplified to

$$\frac{n_s}{n_b} + \ln\left(e^{\frac{n_s}{n_q}} - 1\right) = \frac{V_g - V_T}{V_{th}} \tag{5.7}$$

A generalised Puiseux series expansion is used as an approximation for the log term.

$$\ln\left(e^{\frac{n_s}{n_q}} - 1\right) \simeq \ln\left(\frac{n_s}{n_q}\right) + \frac{1}{2}\frac{n_s}{n_q} + \frac{1}{24}\left(\frac{n_s}{n_q}\right)^2 \ldots \tag{5.8}$$

The effect of charge traps is independent of the absolute current, so all modelling and analysis of the behaviour uses normalised current I_{sd}/I_{max}. Figure 5.3 shows the ideal transfer curve evaluated using equation 5.4.

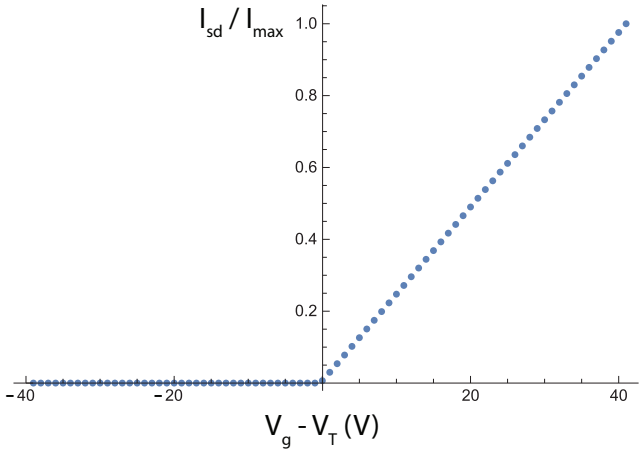


Figure 5.3: Normalised source drain current I_{sd}/I_{max} as a function of gate voltage relative to threshold voltage, $V_g - V_T$. Evaluated using equation 5.4.

5.2.2 Modelling the Occupation of Charge Traps

The charging and discharging of traps as they move with respect to the Fermi level causes the effective electric field to strengthen or weaken. An excess of charged (neutral) traps will result in a stronger (weaker) effective electric field. A charge trap at fixed energy will be shifted with respect to the Fermi energy, E_F, during a gate sweep measurement. Traps well below E_F will be occupied (neutral); traps well above E_F will be unoccupied (charged). A trap with energy corresponding to $V_g = x$ initially above the Fermi level will move below E_F at $V_g = x$, $t = t_F$ on the forwards sweep, and will neutralise with some tunnelling time t_{tunnel}. On the reverse sweep, this state will move back above E_F at $V_g = x$, $t = t_R$. Here there are two possibilities: (1) that it is still charged, or (2) that it neutralised while it was below E_F. In the first case it will remain charged. In the second case, it will charge with tunnelling time t_{tunnel}. In this model, t_{tunnel} is input as a fixed value for all traps at all energies. In practise this is not the case: there are at least two distinct tunnelling times, as discussed in section 5.3.4.

Figure 5.4 outlines the measurement procedure and the expected occupancy

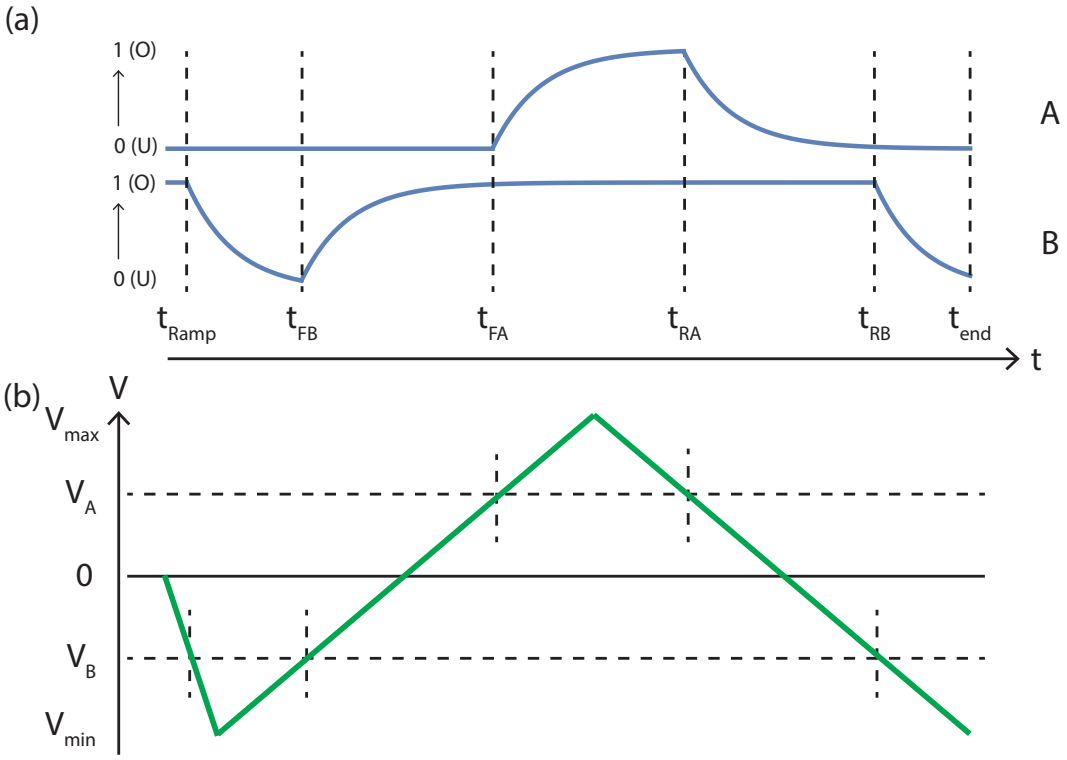


Figure 5.4: (a) The calculated expected occupation over time for the representative trap states A and B. At the starting point, V_g = 0 V, trap state A (B) is above (below) E_F. Trap state A (B) is brought below E_F on the forwards gate sweep at t_{FA} (t_{FB}) and brought back above E_F on the reverse gate sweep at t_{RA} (t_{RB}). Trap state B starts below E_F but is brought above at t_{Ramp} as the gate voltage is ramped from 0 V to the start of the measurement, V_{min}. (b) Gate voltage as a function of time. V_A and V_B are voltages corresponding to states A and B lining up with the Fermi level respectively.

during a gate sweep for states i beginning above (A,i) or below (B,i) the Fermi level.

The total expected number of occupied states at time t is described by $Occ(A,i)$ and $Occ(B,i)$ below.

$$Occ(A,i) = \begin{cases} 0 & t \leq t_F \\ 1 - e^{\frac{-(t-t_F)}{t_{tunnel}}} & t_F < t \leq t_R \\ e^{\frac{-(t-t_R)}{t_{tunnel}}} \left(1 - e^{\frac{-(t_R-t_F)}{t_{tunnel}}}\right) & t_R < t \leq t_{end} \end{cases}$$

$$Occ(B,i) = \begin{cases} 1 & t \leq t_{Ramp} \\ e^{\frac{-(t-t_{Ramp})}{t_{tunnel}}} & t_{Ramp} \leq t_F \\ 1 - e^{\frac{-(t-t_F)}{t_{tunnel}}} \left(1 - e^{\frac{-(t_F - t_{Ramp})}{t_{tunnel}}}\right) & t_F \leq t_R \\ e^{\frac{-(t-t_R)}{t_{tunnel}}} \left(1 - e^{\frac{-(t_R - t_F)}{t_{tunnel}}} \left(1 - e^{\frac{-(t_F - t_{Ramp})}{t_{tunnel}}}\right)\right) & t_R \leq t_{end} \end{cases}$$

The total charge contribution from the traps Q_{trap} is calculated by subtracting the expected occupied states over time from the number of charge traps between V_{min} and V_{eqm}. V_{eqm} is the equilibrium point, taken to be the resting gate bias, V_g = 0 V. Prior to any gate bias changes, it is assumed that all charge traps above V_{eqm} are charged, and all charge traps below V_{eqm} are neutral. This leads to a relative charge contribution, positive (negative) if there are an excess of charged (neutral) traps with respect to the equilibrium position.

The effective electric field is altered by the charge traps: this is modelled as a change in the effective gate voltage: $\Delta V_g = Q_{trap}/C_{trap}$.

5.3 Charge Traps

The charging and discharging of traps as they move with respect to the Fermi level causes the effective electric field to strengthen or weaken. This can cause hysteresis if the measurement time is similar to the tunnelling time between the channel and the trap. In the forwards sweep from V_{min} to V_{max}, charged traps are brought below the Fermi level, neutralising with a tunnel time t_{tunnel}. An excess of charged traps increases the effect of the electric field and thus lowers the forwards threshold voltage. In the reverse sweep from V_{max} to V_{min}, an excess of neutral traps decreases the effective electric field, raising the reverse threshold voltage. Neutral traps raised above the Fermi level will charge with a tunnel time t_{tunnel}.

5.3.1 Measurement Frequency

The amount of hysteresis changes with measurement frequency, as pictured schematically in figure 5.5. Fast sweeps, in which the time taken for the

measurement is much shorter than the channel-trap tunnelling time, have minimal hysteresis: over the course of the measurement, the traps will remain in their initial state. Slow sweeps, in which the tunnelling time is much faster than the measurement time, also have minimal hysteresis: the traps have lots of time to equilibrate over the course of the measurement. Measurements taken at an intermediate speed will have more charged traps (i.e. a stronger effective electric field) on the forwards sweep than on the reverse sweep, leading to hysteresis. In the model, t_{tunnel} is defined as the tunnelling time for a single trap to charge or discharge, and t_{meas} is defined as the number of seconds per volt.

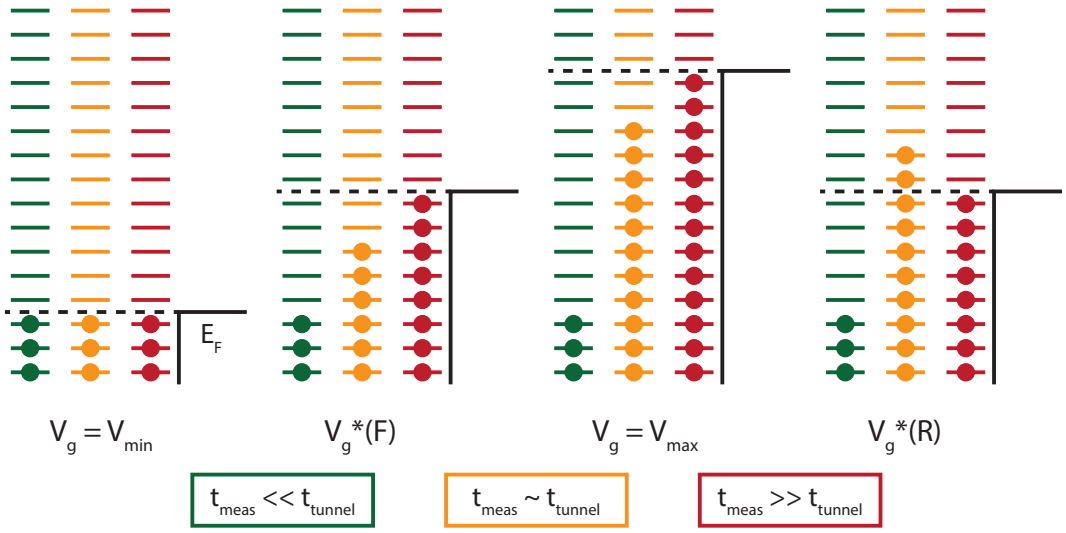


Figure 5.5: Charge trap occupation for fast ($t_{meas} \ll t_{tunnel}$), intermediate ($t_{meas} \simeq t_{tunnel}$) and slow ($t_{meas} \gg t_{tunnel}$) measurements at different gate biases. V_g* is an intermediate gate voltage, $V_{min} < V_g* < V_{max}$, shown for forwards (F) and reverse (R) gate voltage sweeps. Occupied states are neutral; unoccupied states are charged. V_{eqm} taken to equal V_{min} for simplicity.

Figure 5.6 shows the levels of hysteresis in three different devices at varying measurement frequencies between 0.001 and 50 V/s. Over this range, hysteresis increases as the measurement time increases. Slower measurements were not obtained, as the amount of time required to collect one data point was not feasible: a single measurement at a frequency of 1×10^{-4} V/s would take 2.5 weeks. It is expected that the hysteresis would peak and then decrease as the measurement time lengthened, as seen in a monolayer MoS_2/hBN/SiO_2 stack measured in Illarionov et al [82].

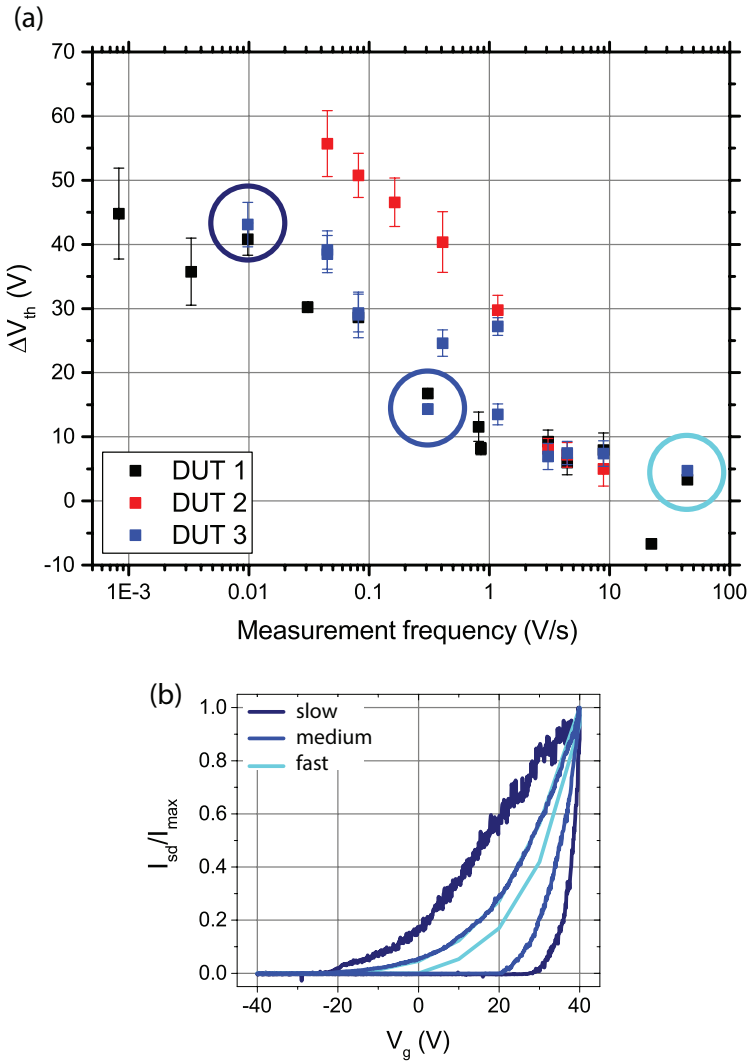


Figure 5.6: (a) Change in hysteresis with measurement frequency for three devices measured in ambient. (b) Three transfer curves for device 3 are picked out across the range of measurement frequencies in (a) with circles.

Figure 5.7 models the effect of measurement frequency on hysteresis for $0.1 \leq t_{tunnel}/t_{meas} \leq 1000$. Hysteresis is largest when the measurement and tunnelling times are similar.

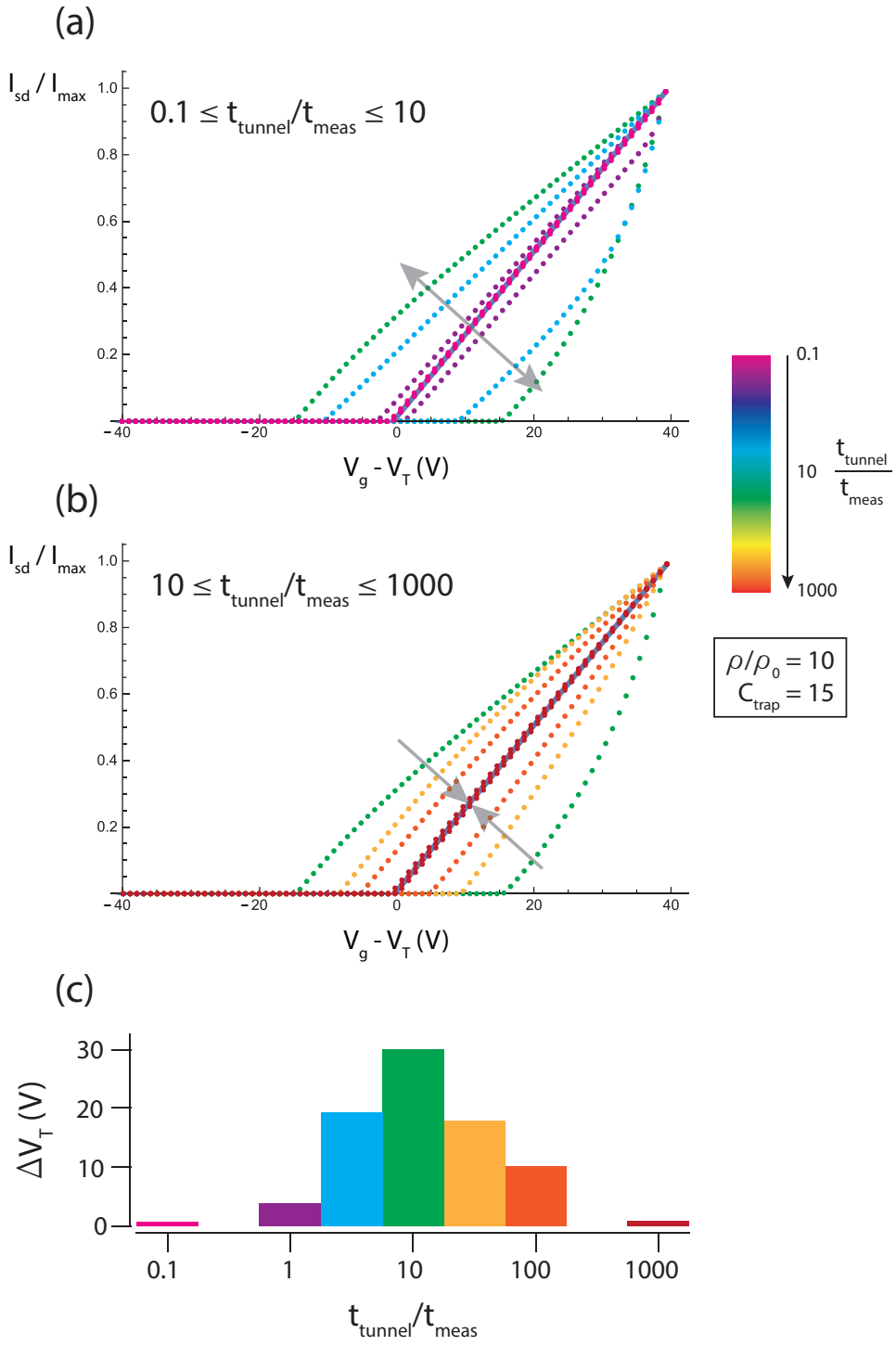


Figure 5.7: (a) Modelled transfer curves for fast to medium tunnelling speeds. As the tunnelling time approaches the measurement time, the hysteresis increases. (b) Modelled transfer curves for medium to slow tunnelling speeds. As the tunnelling gets slower, the hysteresis decreases. (c) Calculated hysteresis $V_{T,R} - V_{T,F}$ at different measurement frequencies. Relative trap density and trap capacitance fixed. Relative tunnelling and measurement times $t_{tunnel}/t_{meas} = 0.1, 1, 5, 10, 50, 100, 1000$.

5.3.2 Trap Density

The density of charge traps will affect the hysteresis: if there are fewer traps, there will be less hysteresis, as shown schematically in figure 5.8, and modelled for a range of trap densities in figure 5.9. The effect is seen experimentally in the measurement frequency data shown in figure 5.10, which reveals an overall drop in hysteresis after pumping. As this corresponds to a lower charge trap density in vacuum, we hypothesize that the origin of the charge traps are adsorbates such as water molecules which would be removed through pumping.

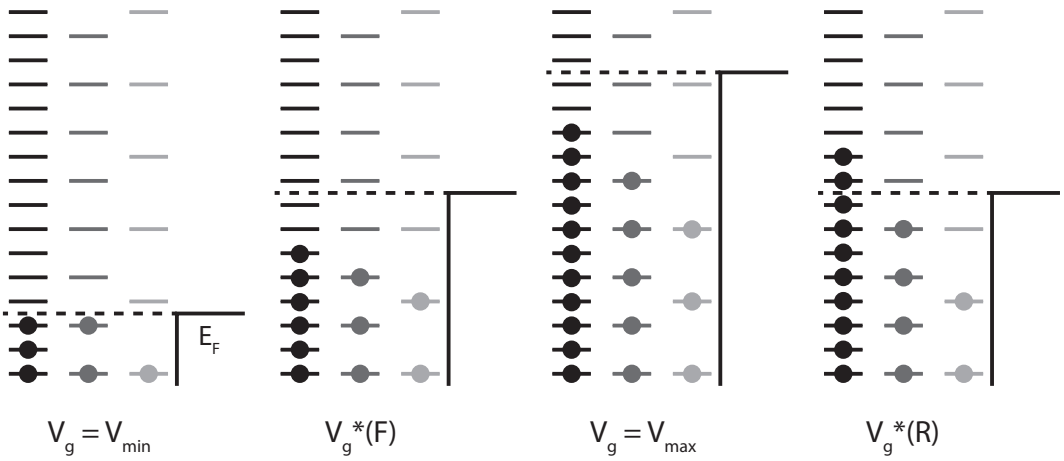


Figure 5.8: Change in charge trap occupation with trap density at different gate biases. V_g* is an intermediate gate voltage, $V_{min} < V_g* < V_{max}$, shown for forwards (F) and reverse (R) gate voltage sweeps. Occupied states are neutral; unoccupied states are charged. V_{eqm} taken to equal V_{min} for simplicity.

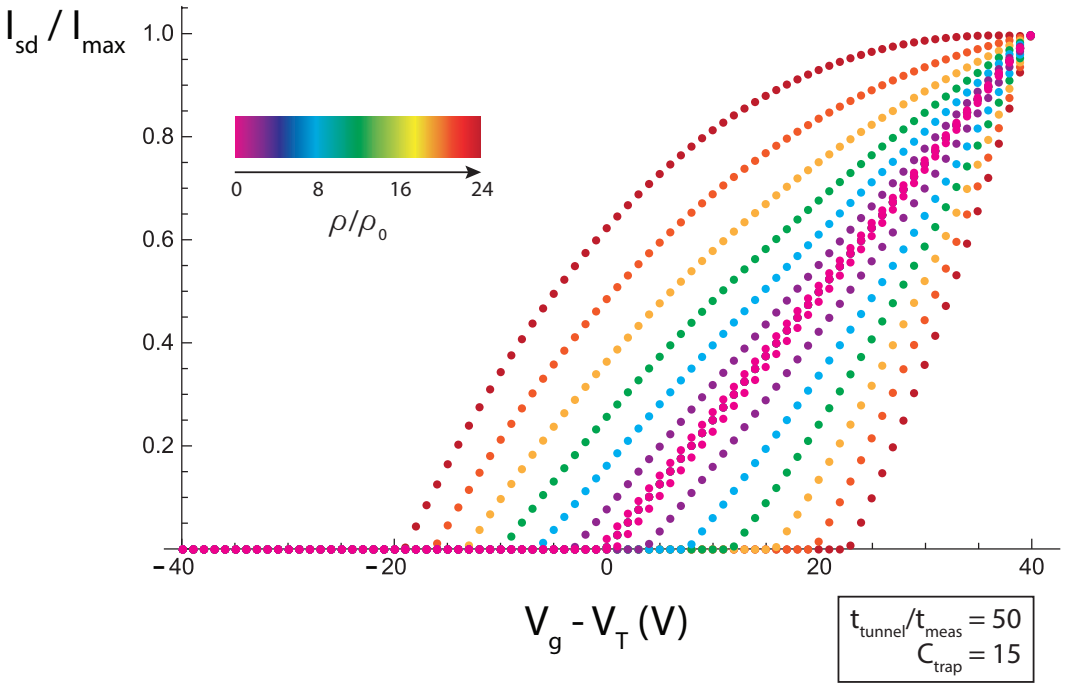


Figure 5.9: Modelling the effect of trap density on hysteresis. As the trap density increases, the hysteresis increases. Trap tunnelling time relative to measurement time and trap capacitance are fixed. Trap densities ρ/ρ_0 = 1, 4, 8, 12, 16, 20, 24.

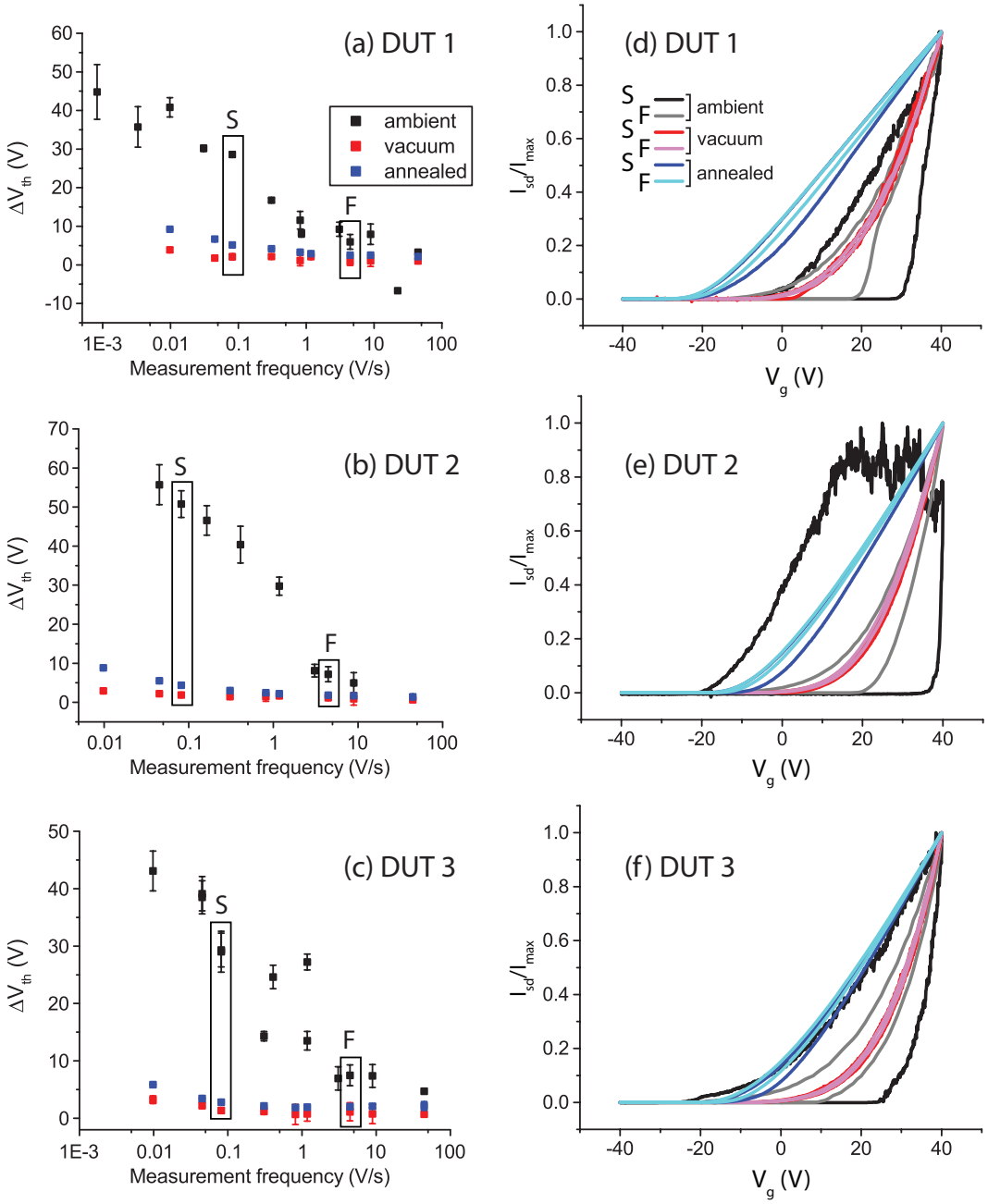


Figure 5.10: (a)-(c) Hysteresis as a function of measurement frequency for three devices in ambient, after pumping, and after annealing, showing a significant overall drop in hysteresis after pumping due to a reduction in the number of charge traps. (d)-(f) Transfer curves for each device, at slow (S, dark colour) and fast (F, light colour) measurement frequencies. These show the change in shape with speed and measurement environment. The corresponding hysteresis points are picked out with rectangles in (a)-(c).

5.3.3 Bias Range

For transfer curves, the gate bias range is defined as $V_{max} - V_{min}$. A larger bias range is expected to result in more hysteresis: during the measurement, charged traps will be below the Fermi level for longer, and will therefore have more time to neutralise before moving above the Fermi level on the reverse sweep. This effect can be seen schematically in figure 5.11(b),(d), a comparison of forwards and reverse charge trap occupations for large and small bias ranges. Figure 5.12 is experimental data showing the change in hysteresis for different bias ranges. Each measurement had the same V_{max} = 40 V, but was started at successively lower V_{min}. It should be noted that the ambient data was recorded on two separate occasions, the first from V_{min} = 0 V to V_{min} = –40 V, the second from V_{min} = –30 V to V_{min} = –60 V. The first overlapping data point at V_{min} = –30 V differs significantly, due to bias stressing history (section 5.3.5).

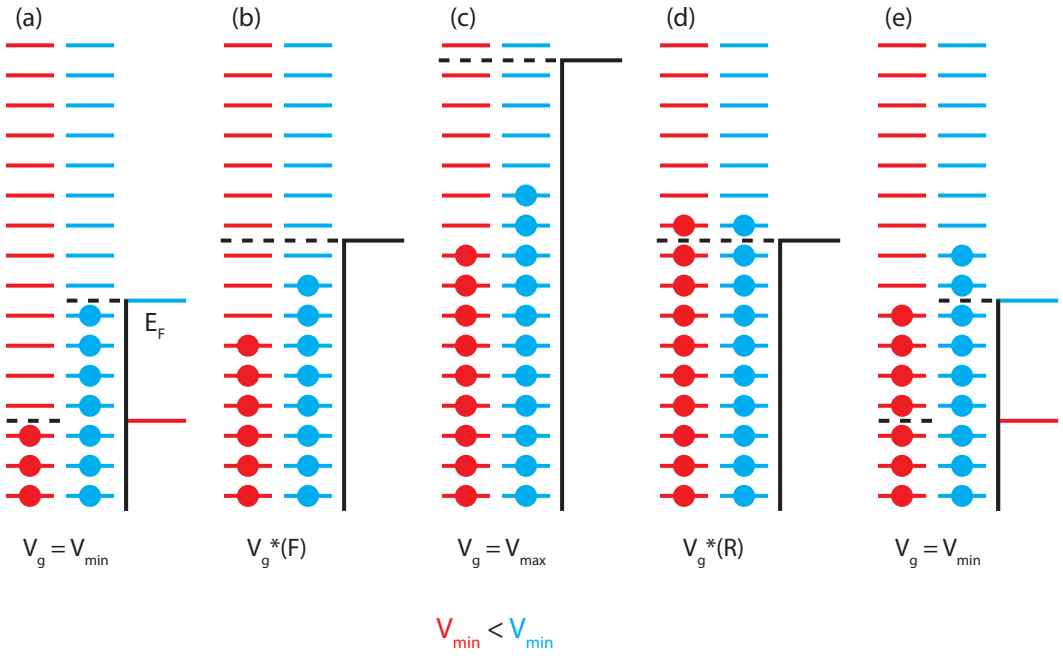


Figure 5.11: Change in charge trap occupation for small and large bias ranges at different gate biases. V_g* is an intermediate gate voltage, equal for the two bias ranges illustrated, $V_{min} < V_g* < V_{max}$, shown for forwards (F) and reverse (R) gate voltage sweeps. Occupied states are neutral; unoccupied states are charged. V_{eqm} taken to equal V_{min} for simplicity.

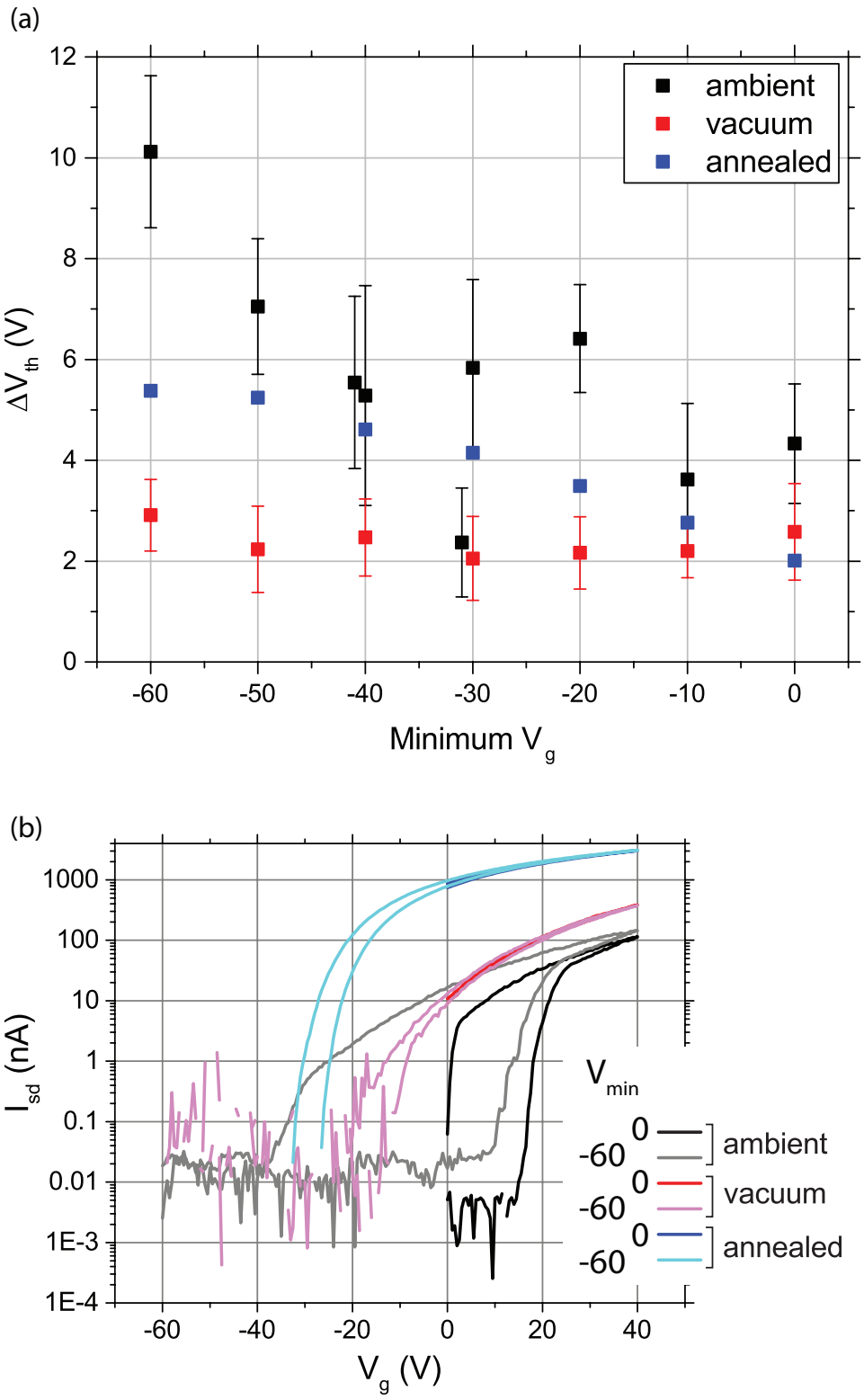


Figure 5.12: (a) Change in hysteresis with bias range for a device measured in ambient, in vacuum, and after annealing. $V_{max} = 40$ V for all runs. (b) Transfer curves plotted on a log scale for clarity for $V_{min} = 0$ V and –60 V from (a). The difference is small in vacuum and after annealing; the clearest difference is between the measurements taken in ambient conditions.

This effect of increased hysteresis with lowering minimum voltage has been modelled in figure 5.13, with the assumption that the equilibrium voltage V_{eqm} = 0 V. Lower forwards threshold voltages correlate with lower V_{min}, due to an increased number of charge traps being spanned. In order to avoid these bias range effects affecting the results, all other measurements were taken between fixed minimum and maximum gate biases.

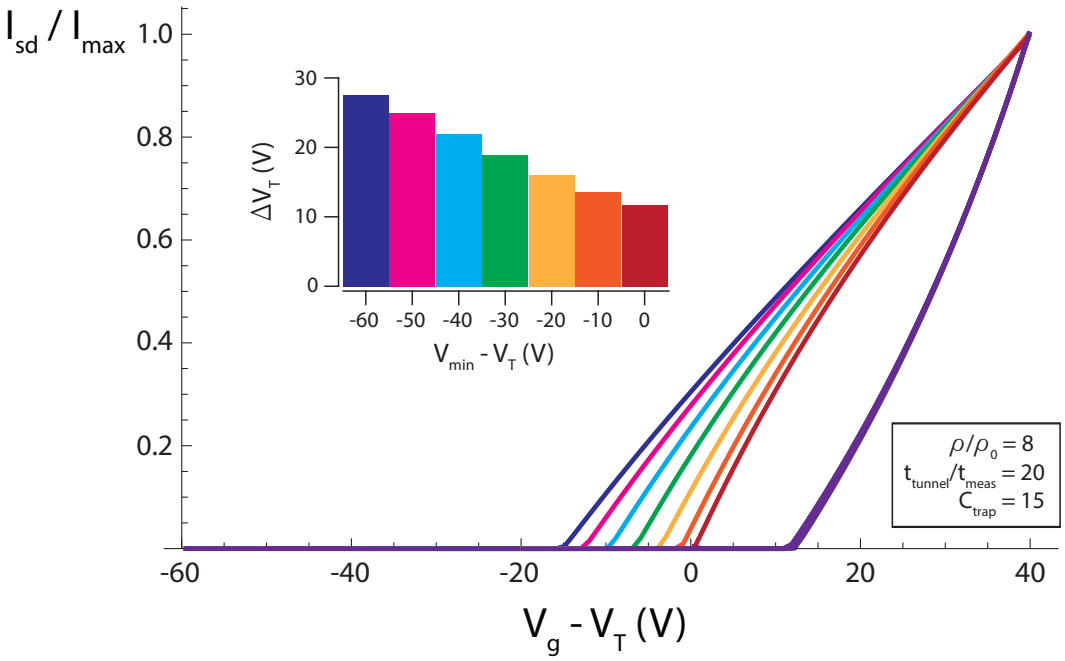


Figure 5.13: A simplified model showing the effect of lowering the minimum voltage on the hysteresis.

In addition to the total bias range, the position of the threshold voltage within the measurement range has an effect on the hysteresis, as modelled in figure 5.14. The figure shows the effect of a changing $V_T - V_{eqm}$, where V_{eqm} is taken to be 0 V, the starting point of the measurement.

The charge contribution from the traps is tied to the equilibrium point: for a fixed V_{eqm}, the change in effective voltage over the course of the measurement will also be fixed. A shift in threshold voltage away from the equilibrium point causes a decrease in hysteresis due to the lower difference between effective electric field at the threshold, the point at which the device turns on. This effect can be seen in figure 5.15, in which three scenarios are depicted: $V_T < V_{eqm}$, $V_T = V_{eqm}$ and

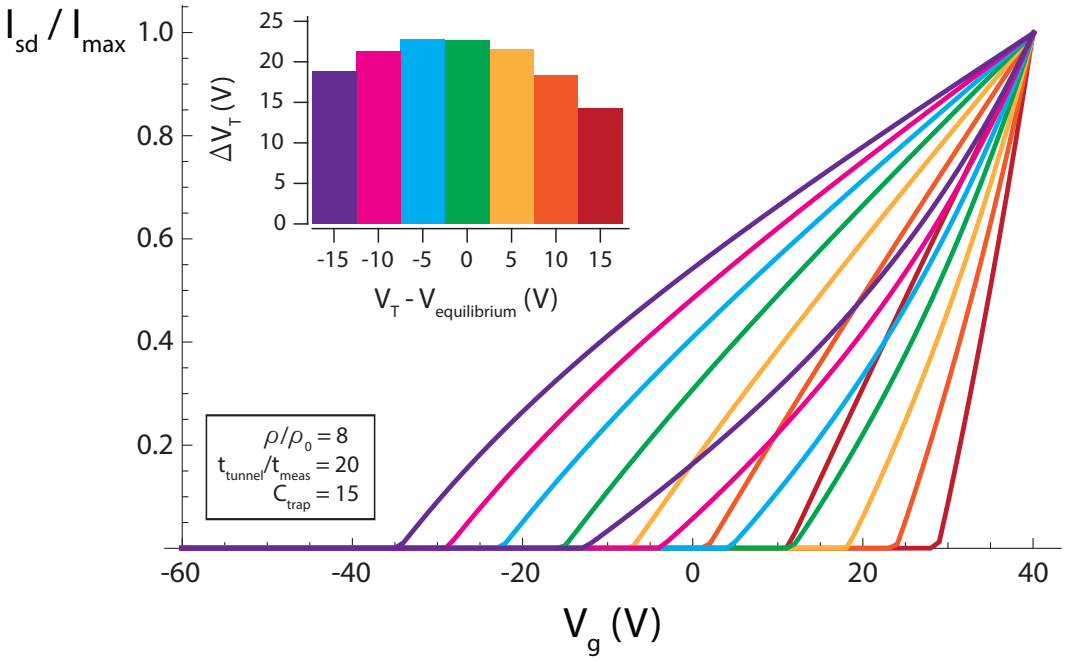


Figure 5.14: A simplified model showing the effect of changing the relative positions of the threshold and equilibrium voltages.

$V_T > V_{eqm}$.

The increase in hysteresis seen after annealing the devices may be due to this effect. Figure 5.16 shows measurement frequency data collected from three devices in vacuum and at room temperature after annealing. Threshold voltages in vacuum are roughly +20 V. Threshold voltages for the annealed devices are 20–30 V lower, bringing them much closer to the equilibrium voltage, which would result in a hysteresis increase. It should be noted that in practice, the equilibrium voltage is expected to be below the assumed value of 0 V due to the bias stressing history (section 5.3.5). This would enhance the effect.

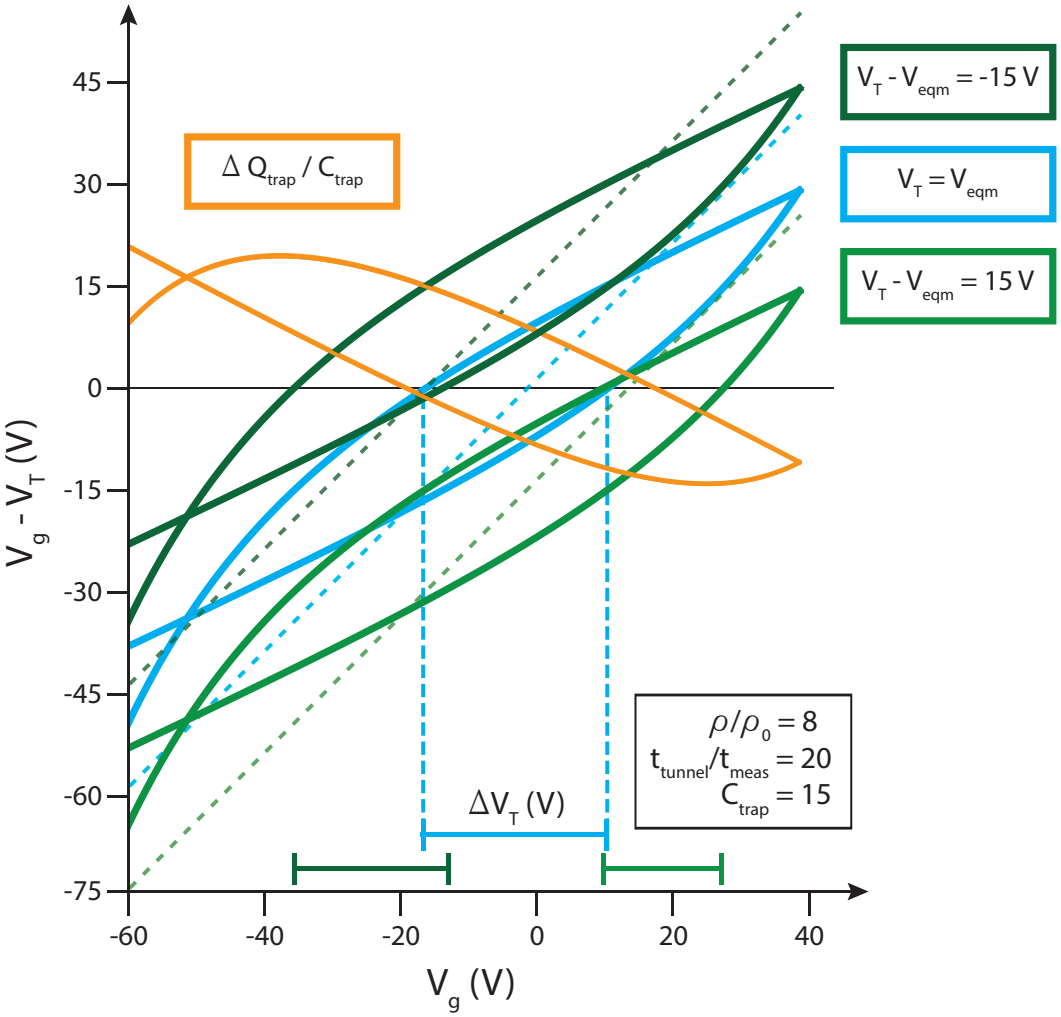


Figure 5.15: Effective modified gate bias as a function of applied gate bias for a device with threshold voltage below the equilibrium ($V_T - V_{eqm} = -15V$), equal to the equilibrium voltage ($V_T = V_{eqm}$), and above the equilibrium voltage ($V_T - V_{eqm} = 15V$). V_{eqm} is taken to be equal to 0 V, the starting gate voltage. Dashed lines show the modified gate bias $V_g - V_T$ without the contribution from charge traps. Solid lines show the effective modified gate bias. The solid orange line shows the contribution from the charge traps, which is the same for all three cases as it is dependent only on the fixed value V_{eqm}, not on the changing value V_T. Hysteresis $\Delta V_T = V_{T,R} - V_{T,F}$ is the separation between forwards and reverse sweeps at $V_g = V_T$, indicated on the plot for the three scenarios.

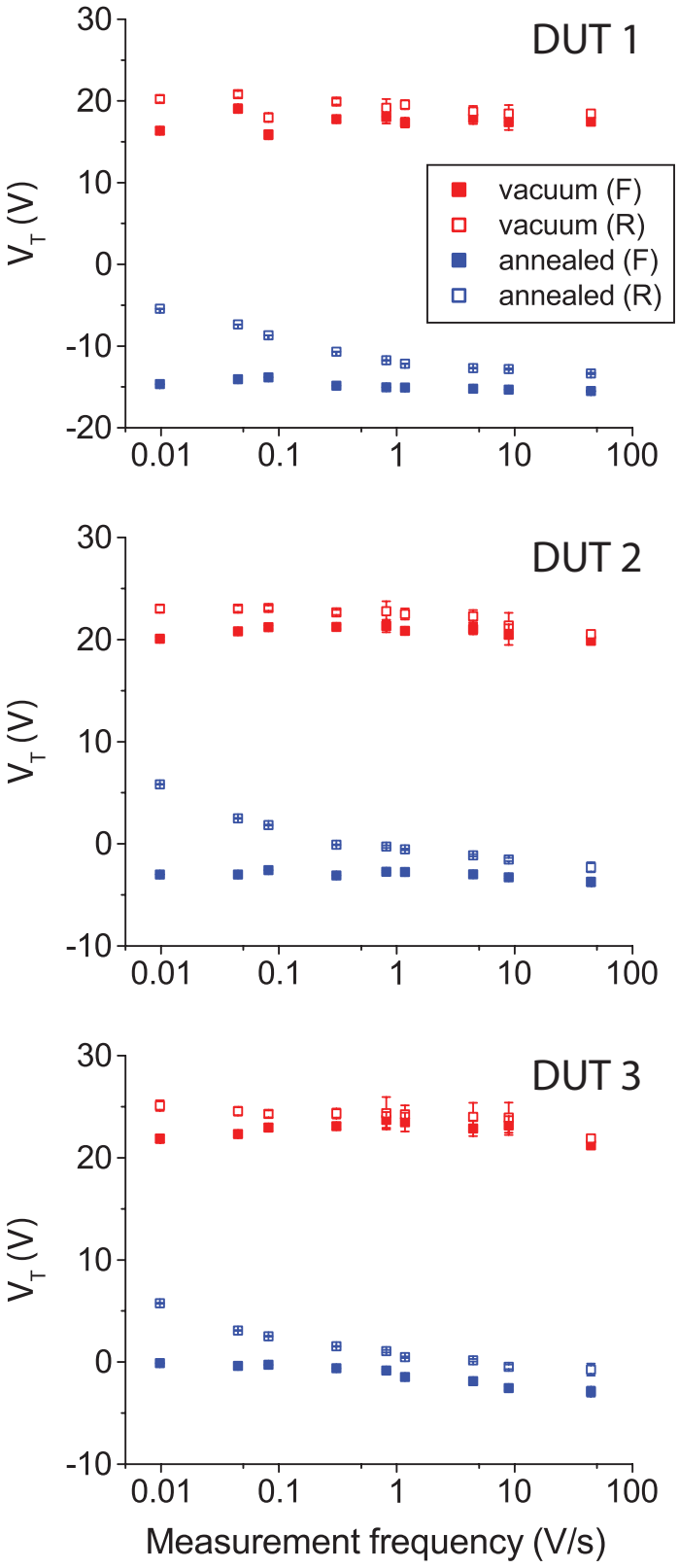


Figure 5.16: Threshold voltages for forwards (F, solid) and reverse (R, open) for three devices measured in vacuum (red) and after annealing (blue), showing increased hysteresis after annealing in all three devices.

5.3.4 Fixed Bias

At a fixed gate voltage above the threshold voltage, the source-drain current will decay exponentially as the charged traps below E_F neutralise, weakening the effective electric field.

Current was measured as a function of time for a fixed source-drain and gate bias (V_{sd} = 0.5 V, V_g = 40 V) in ambient, in vacuum, and after annealing. The gate voltage was ramped over ∼5 seconds from 0 V to 40 V; the current was then measured immediately, and every second up to 6 minutes. Figure 5.17 shows typical data of current against time. Table 5.1 gives the current ratio I(t = 360 s)/I(t = 0 s) for three devices, showing that the drop in current is largest in ambient conditions, and much smaller after annealing.

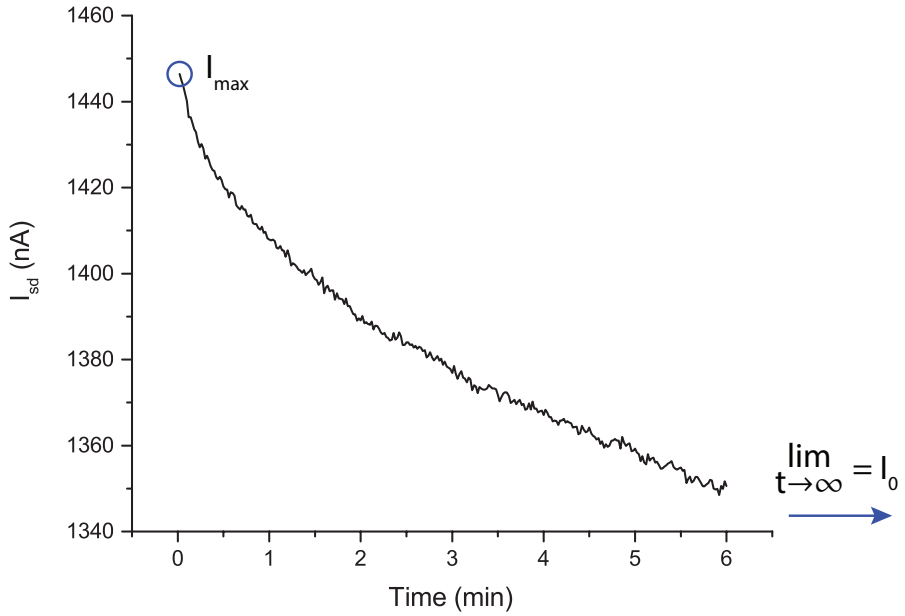


Figure 5.17: A typical measurement of current as a function of time for fixed source-drain and gate biases. The system tends toward equilibrium, at which point the current is equal to I_0.

	DUT 1	DUT 2	DUT 3
ambient	0.424	0.003	0.144
vacuum	0.768	0.838	0.812
annealed	0.935	0.923	0.959

Table 5.1: I(t=360 s)/I(0) for three devices at V_g = 40 V, V_{sd} = 0.5 V.

The current as a function of time can be modelled as

$$I = I_0 + A\exp\left(-\frac{t}{\tau}\right) \tag{5.9}$$

In which the pre-factor A is proportional to the density of trapping states Q, $A = Q\frac{W}{L}\mu V_{sd}$ and τ is the trapping time constant [25, 26]. As $t \to \infty$, $I_{sd} \to I_0$.

Figure 5.18 shows the calculated fitting parameters for measurements of the current over a 6 minute time period taken at fixed source, drain and gate biases V_{sd} = 0.5 V, $V_g = 40$ V for three devices in different environments. After pumping and annealing, the trapping time constant increases and the trapping density decreases. The mobilities used to calculate the trap density, Q, are taken from the average of forwards and reverse mobilities for standard transfer curves measured at 2.2 V/s. This will only give a rough estimate of the trap density.

Trap density is equal to [26]

$$Q = \frac{A}{\mu}\frac{L}{W}\frac{1}{V_{sd}} \tag{5.10}$$

Taking $L = W$ and V_{sd} = 0.5 V, an A/μ value taken from figure 5.18 of 20 nC/cm^2 is equivalent to $20 \times 6.24 \times 10^9 \times 2 = 2.5 \times 10^{11}$ traps/cm^2. Electron charge $|e| = 1.6 \times 10^{-19}$ C, so 1 nC = 6.24×10^9 electrons.

Using equation 5.9, the current was modelled as a function of time for varying trap density and trap tunnelling times (figure 5.19). Measurements of this data are included in the figure for comparison. Qualitatively, the data shows the trap density decreasing and the tunnelling time increasing between ambient, vacuum, and annealed measurements.

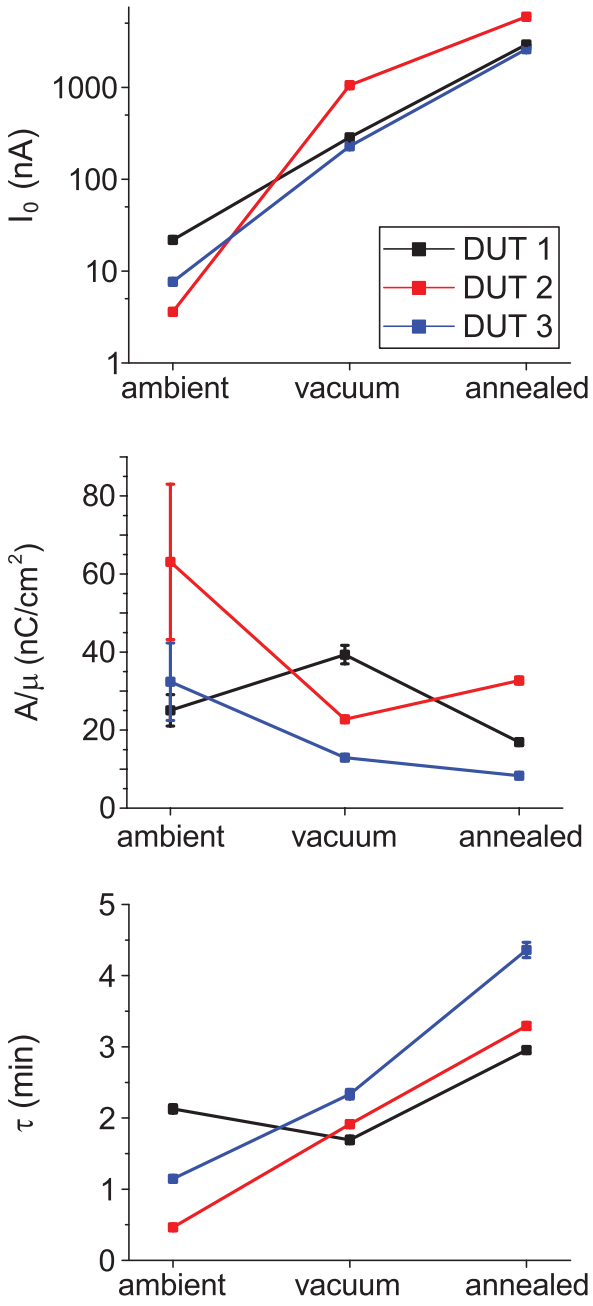


Figure 5.18: Fitting parameters for current measured at fixed source-drain and gate bias for six minutes, fitted using equation 5.9. Three devices are measured in ambient, in vacuum, and after annealing, with $V_g = 40$ V, $V_{sd} = 0.5$ V. (a) Equilibrium current I_0, where $I_{sd} \to I_0$ as $t \to \infty$. (b) A/μ is proportional to the trap density. (c) Effective tunnelling time, τ.

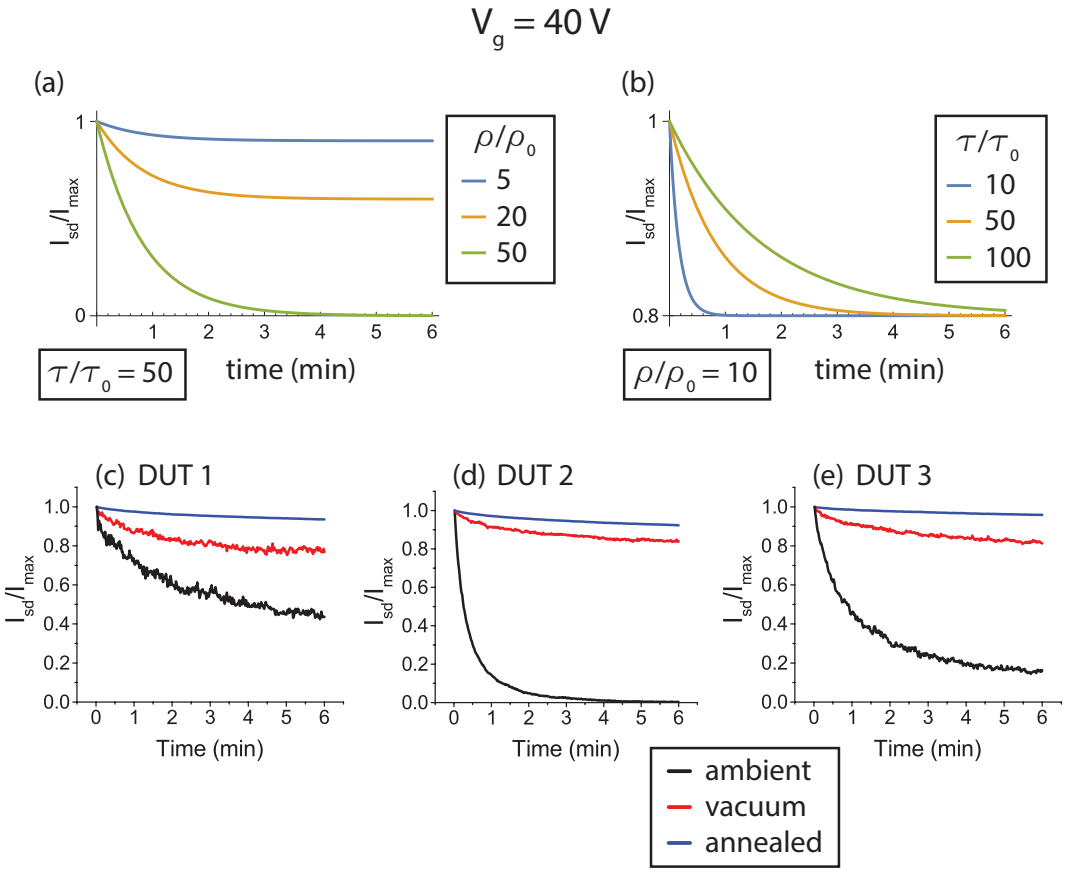


Figure 5.19: (a) Modelled current as a function of time for different trap densities. (b) Modelled current as a function of time for different tunnelling times. (c)-(e) Measured current as a function of time for three devices, measured in ambient (black), in vacuum (red), and after annealing (blue). All at $V_g = 40$ V.

The above analysis assumes a single origin of charge traps. However, representative data shown in figure 5.20 demonstrates that a bi-exponential is a better fit for the experimental data. This suggests there are both fast and slow charge traps present. However, the relatively small contribution of the significantly faster traps leads to unsatisfactory analysis. The increased time constant seen in figure 5.18 may be due to selective removal of fast traps through pumping and annealing, leaving slower traps behind resulting in a longer average trap tunnelling time.

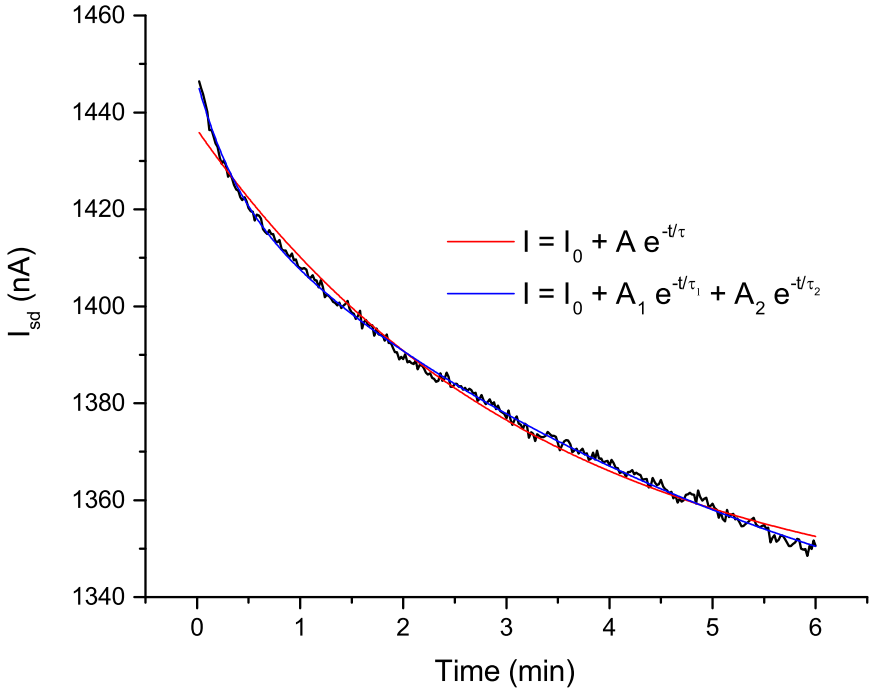


Figure 5.20: Exponential and bi-exponential fits for current as a function of time for fixed biases.

5.3.5 Negative Bias Stressing

The charging and discharging times for the traps were found to be on the order of minutes. This led to difficulties isolating causes for the effects observed, as it takes a long time for the system to equilibrate. This additional effect is called the bias stressing history.

In an equilibrium state, all traps below E_F are neutral, and all traps above E_F are charged. In order to determine how long it would take to reach an equilibrium state at V_{min}, the device was held with $V_g = V_{min} = -60$ V for successively longer durations, taking measurements in between. Figure 5.21 shows the change in forwards and reverse threshold voltages recorded for these measurements, plotted against cumulative time spent at V_{min}. The longer the gate bias is held at V_{min}, the lower the threshold voltages are. This is due to the number of charged traps increasing with time, leading to an enhanced effective electric field. A bi-exponential fits the data well, with time constants $t_1 = 118$ s, $t_2 = 3060$ s. The effects of the bias stressing history are thus difficult to avoid.

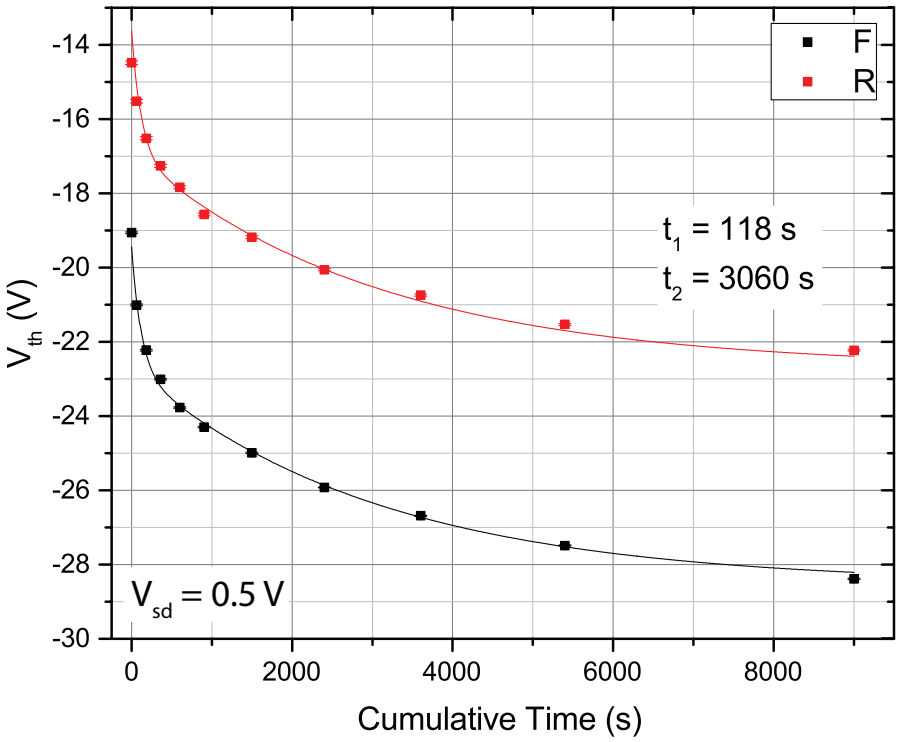


Figure 5.21: Forwards (F) and reverse (R) threshold voltages measured after waiting at $V_{min} = -60$ V for successively longer durations. Fitted with a bi-exponential.

5.4 Discussion

After pumping on devices, the number of charge traps decreases. This is evidenced by a reduction in current loss over time in fixed bias measurements, and a reduced hysteresis in measurement frequency data. The observed hysteresis reduction may also be due to the removal of mobile ions after pumping.

After annealing, fixed bias data indicates a decrease in charge trap density, but observed hysteresis in the measurement frequency data increases. This counter-intuitive result is likely to be a result of a large negative shift in threshold voltage. This shift could arise from a lowered Schottky barrier, ϕ_B, due to a shift in the neutrality point involved in Fermi level pinning, ϕ_0. The effect of the shift is the annealed threshold voltage being closer to the equilibrium voltage and thus more prone to the charging and discharging of the traps.

Chapter 6

Single-Electron Transitions at Low Temperature

Monolayer and bilayer MoS_2 field-effect transistors were cooled to base temperature of a dilution refrigerator (T $\leq$ 10 mK), and the differential conductance, dI_{sd}/dV_{sd}, as a function of source-drain and gate biases was measured. Results from a monolayer device can be found in appendix C: there was evidence of Coulomb blockade, but the device was too resistive to study further. Pisoni et al [6] see Coulomb diamonds at T $\sim$1.7 K in a gate-defined quantum dot with effective radius $\sim$280 nm in monolayer MoS_2.

This chapter contains data collected from two bilayer devices. The first device, discussed in section 6.2, was not annealed. Coulomb blockade is seen but there are no features arising from single-electron transitions.

The second bilayer device studied, discussed from section 6.3 onwards, was annealed before measuring at low temperature, as described in section 4.3. Measurements of this device took place over two periods at base temperature. In the first (second) period, the device was mounted such that the current was perpendicular (parallel) to the applied magnetic field. Similar transport was observed in both measurement periods, with single-electron transitions appearing superimposed onto field-effect transistor-like behaviour. Two further annealed bilayer devices were cooled down, mounted parallel to the magnetic field. These showed qualitatively similar transport.

There was no quantum dot patterning of the device before cooldown, so the single-electron transitions seen are unlikely to be in the MoS_2 channel. They are suspected to arise from defect states at the contacts. Three single-electron transitions are characterised as a function of magnetic field, revealing information about g-factors and spin-filling.

6.1 Field-effect mobility during cooldown

Transfer measurements were taken at regular intervals during the cooldown process to monitor changes in mobility with temperature. Forward and reverse mobilities from two of the devices discussed in chapter 5 are shown in figure 6.1.

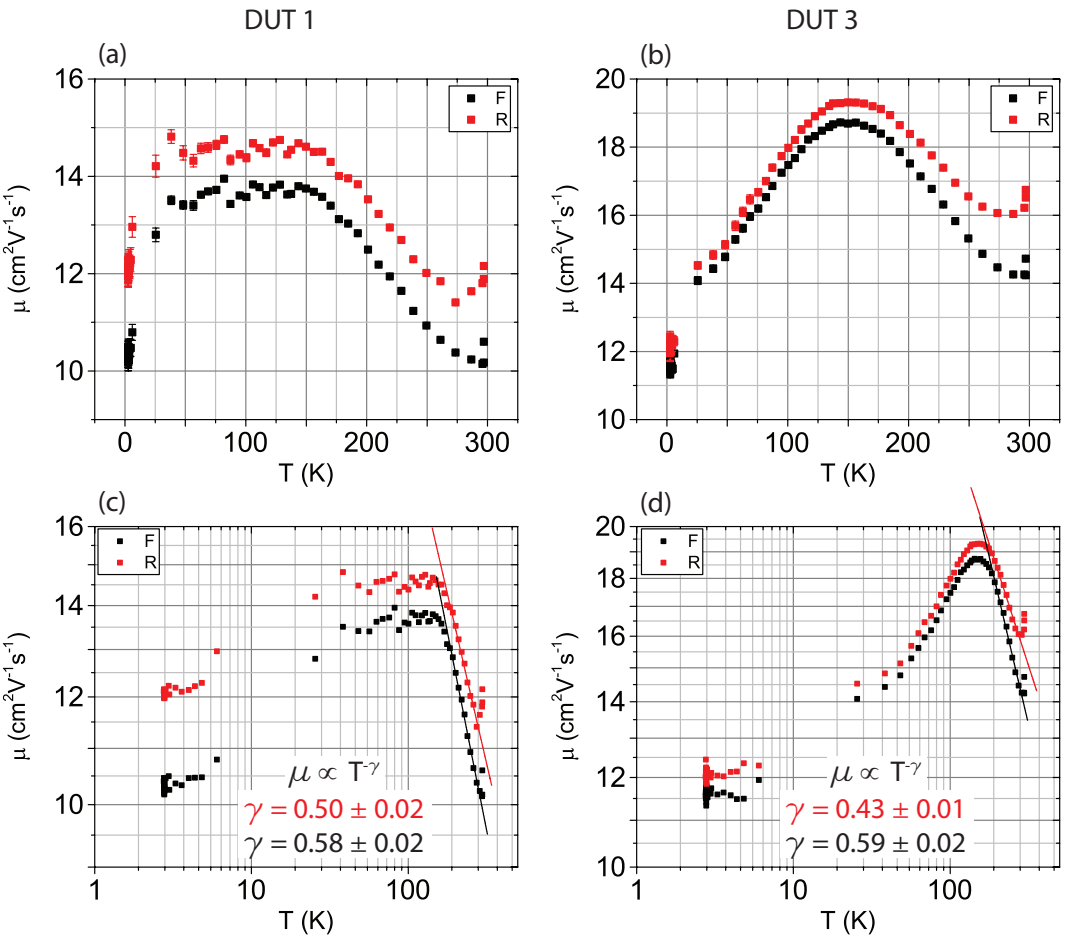


Figure 6.1: Mobility as a function of temperature for (a),(c) device 1 and (b),(d) device 3. (c),(d) Log plots to show $\mu \propto T^{-\gamma}$ fit. Each measurement consists of a forwards run from V_{min} to V_{max}, and a reverse run in the opposite direction. Mobilities are calculated for each direction, labelled F and R respectively.

The plots can be split into three sections, starting at room temperature.

T = 300 K

Devices were annealed outside the dilution refrigerator as described in section 4.3 in order to reach a high enough annealing temperature. Exposure to ambient conditions is known to decrease device performance. Molecules including water adsorb onto the MoS_2, resulting in an increased hysteresis and lower device conductivity. In order to minimise this effect, devices were transferred between the annealing and dilution refrigerator vacuum chambers in under thirty minutes. In the first few measurements recorded at room temperature, the mobility is seen to decrease as a result of the additional charge traps while the DR vacuum chamber is being pumped out before cooling.

150 K $<$ T $<$ 300 K

As the temperature decreases, phonon scattering is suppressed [3], resulting in a mobility increase, with $\mu \propto T^{-\gamma}$. The exponent γ for the two devices ranged from 0.43 to 0.59, as indicated on the graph in figure 6.1.

Assuming phonon-limited scattering, the exponent is calculated to be γ = 1.69 [84]. Assuming charged impurity-limited scattering, the exponent is calculated to be $\gamma = 0.98$ [85]. Experimentally, there are reports of both a strong temperature dependence, $\gamma = 1.4$ [86], and a weak temperature dependence, $\gamma = 0.62$ [3]. These devices also show a weak temperature dependence, so it is assumed that there are several scattering processes, such as substrate phonon scattering and charged impurity scattering.

T $<$ 150 K

As the temperature decreases further, slower moving electrons result in increased impurity scattering, resulting in a mobility decrease. This is not widely seen in other experimental work, suggesting that these devices have an unusually high level of impurities.

6.2 Low Temperature Measurements Before Annealing

Figure 6.2 shows differential conductance maps taken at base temperature with and without a perpendicularly applied magnetic field for a device that was not annealed prior to cooling. Coulomb blockade is observed, but there are no single-electron transitions.

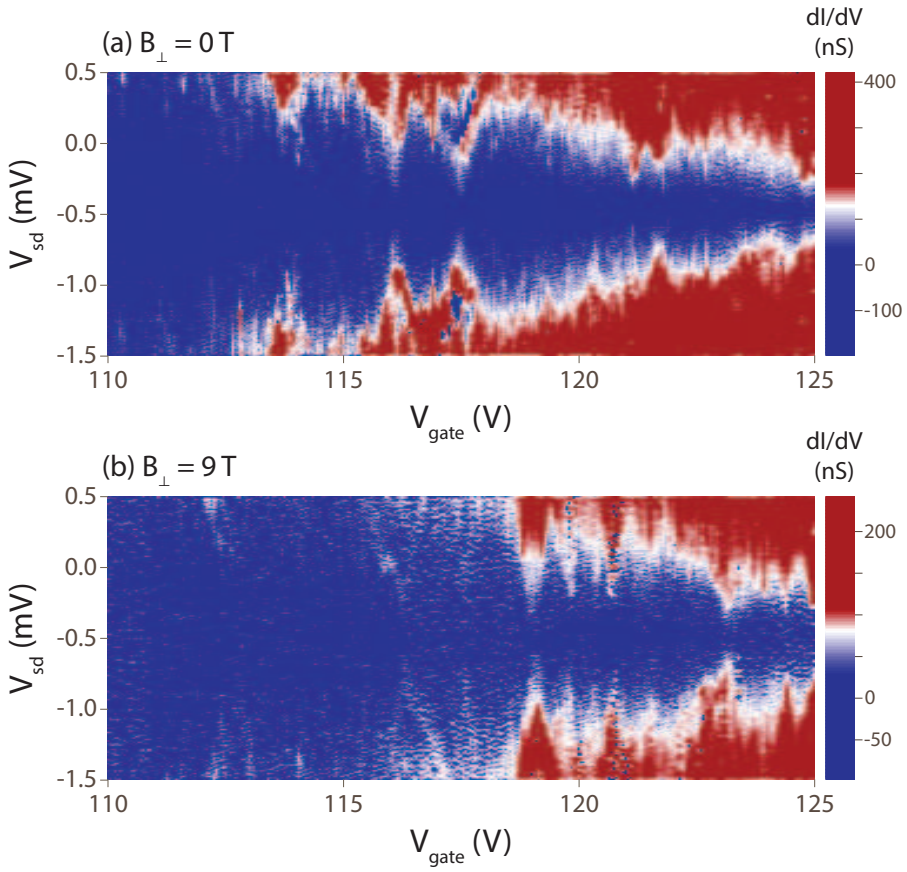


Figure 6.2: Differential conductance maps taken at (a) $B_\perp$ = 0 T and (b) $B_\perp$ = 9 T for a bilayer device which was not annealed before cooling. No single-electron transitions are seen.

6.3 Single-Electron Transitions at Low Temperature

Figure 6.3 shows differential conductance plots for one device over three different measurement ranges. Crosses from single electron transitions arising from zero-dimensional features can be seen superimposed onto transport behaviour

expected from a field-effect transistor. It should be noted that this figure is only intended to give a general overview of the transport in these ranges. Figure 6.3(c) cannot be directly mapped onto figure 6.3(b) due to shifts in energies caused by application of high source-drain biases (up to 10 V). High source-drain biases were applied deliberately to shift transitions that were in the same location away from each other.

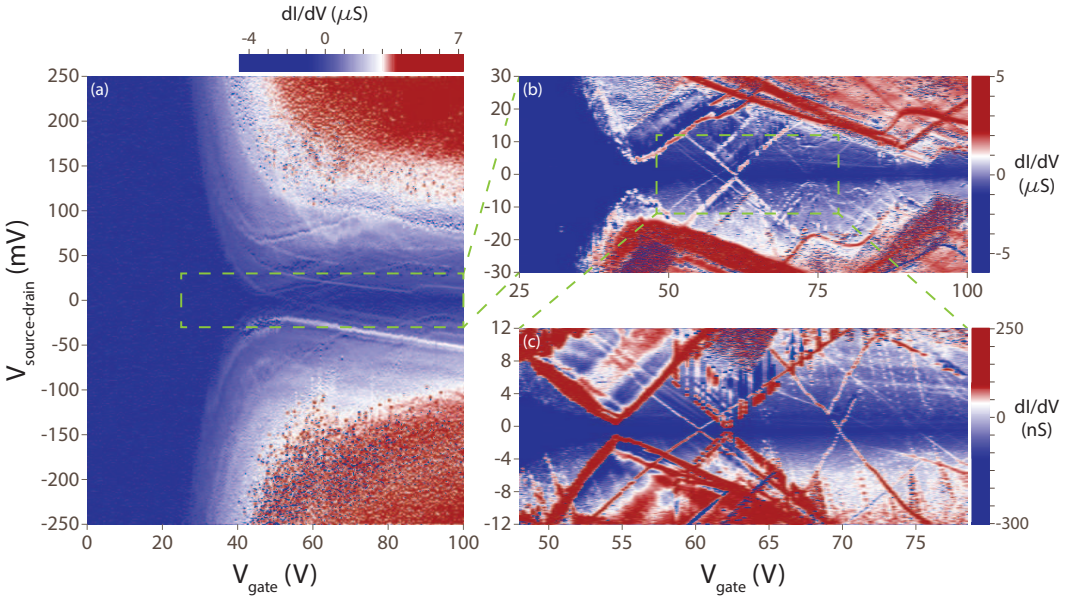


Figure 6.3: Plots of differential conductance as a function of source-drain and gate biases taken at base temperature T $\leq$ 10 mK. (a) Large scale measurement range showing field-effect transistor behaviour. (b) Medium scale as marked out by the dashed box in (a), showing a combination of field effect transistor and zero dimensional behaviour. (c) Small scale as marked out by the dashed box in (b), showing multiple single-electron transitions.

Figure 6.4 shows medium scale differential conductance maps measured at base temperature for two further annealed bilayer MoS_2 devices showing qualitatively similar transport behaviour in comparison to figure 6.3.

The observed single electron transitions are likely resulting from mid-gap interface states. Figure 6.5 shows this transport behaviour schematically. The MoS_2 channel has a comparatively small resistance relative to the mid-gap states at the source and drain metal-MoS_2 interfaces, and thus the latter would dominate the transport behaviour. In addition, the resistances of the source and drain states are likely to be mismatched, such that only one dominates. An assumption made when

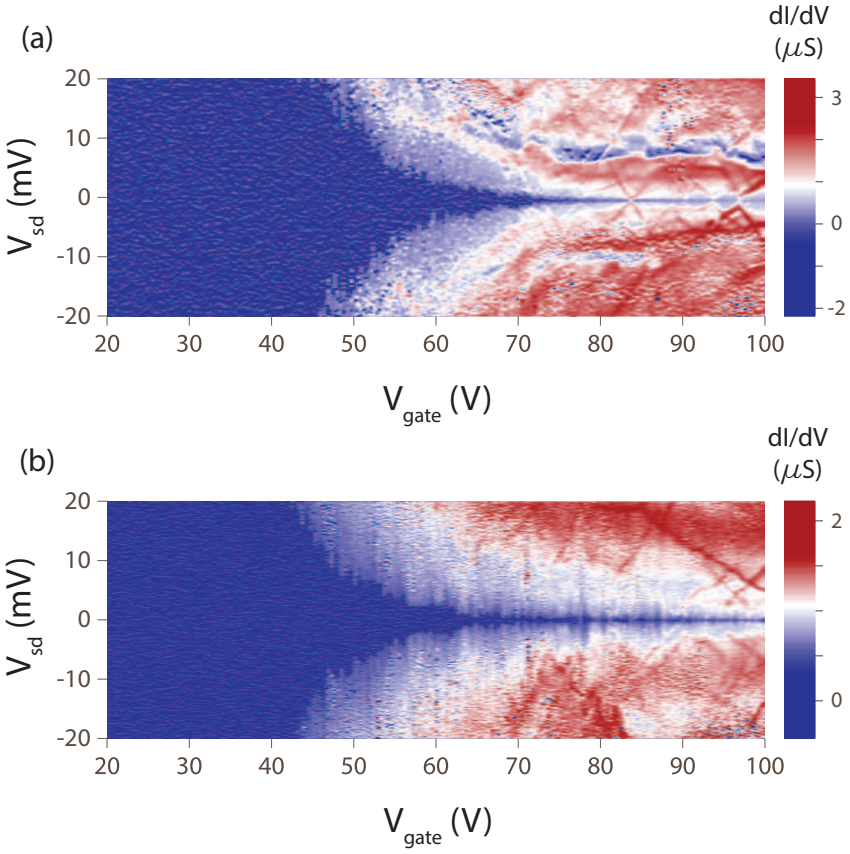


Figure 6.4: Medium scale differential conductance plots as a function of source-drain and gate biases taken at base temperature T $\leq$ 10 mK for (a) DUT 1 and (b) DUT 3 from chapter 5 showing qualitatively similar transport to the device studied in more depth in this chapter (see figures 6.3 and 6.7 for a comparison).

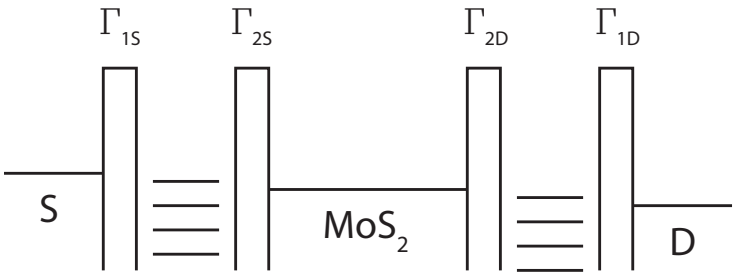


Figure 6.5: An illustration of the transport across the device showing tunnel barriers between the contacts and zero-dimensional mid-gap states ($\Gamma_{1S,1D}$) and between the mid-gap states and the MoS_2 channel ($\Gamma_{2S,2D}$). The mid-gap states dominate the transport at low source-drain biases due to their large resistance in comparison with the MoS_2.

calculating the lever arm is that the voltage drops entirely over one contact, either source or drain. Whilst this is unlikely to be the case, it is a good approximation.

In practise, the lever arm would be scaled by a pre-factor, but it is not possible to determine that pre-factor from this data.

One explanation for the transitions that can be ruled out is the occurrence of naturally-forming MoS_2 quantum dots in the channel. Naturally-forming dots would likely form an array, and thus Coulomb shards would be expected (figure 6.6) [4], which were not observed.

Behaviour of three single transitions all from the same device (figure 6.3) was explored with an applied magnetic field up to 9T to extract g-factors and spin filling information. Transitions A, B, and C are shown in context in figure 6.7. In transition A, the magnetic field is perpendicular to the sample (and the flow of electrons); in transitions B and C, the magnetic field is parallel to the sample.

In order to change the orientation of the current through the device with respect to the magnetic field, the DR had to be brought to room temperature to re-orientate the sample holder manually. Before starting the next cooldown, the device was re-annealed in a separate vacuum chamber as described in section 4.3. This warming, re-heating, and re-cooling process led to a different electrostatic landscape, as shown in figure 6.7 which shows small scale differential conductance maps for the two separate cooldowns required to collect data for transitions A, B, and C analysed below.

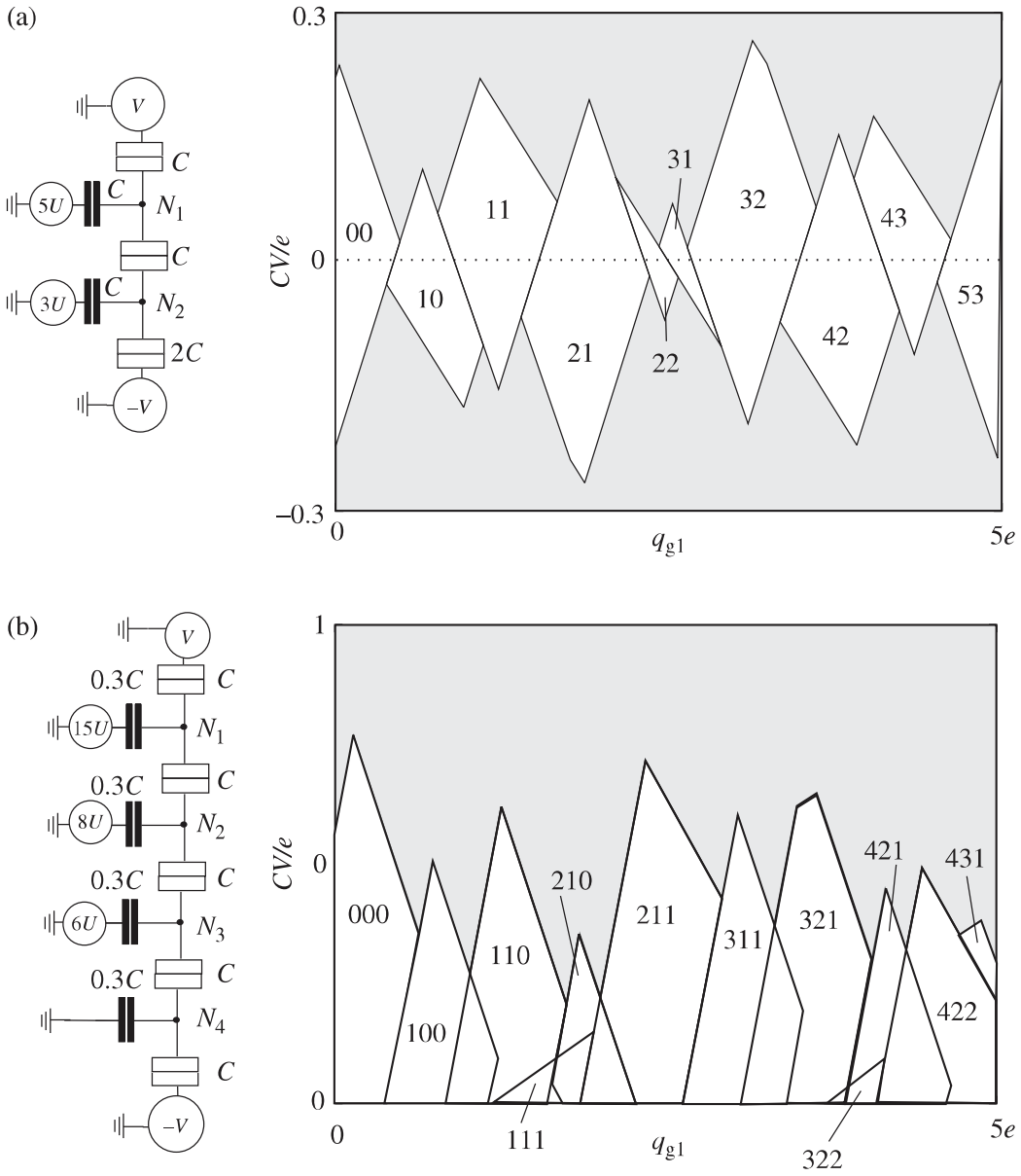


Figure 6.6: Calculated Coulomb blockaded regions for (a) two- and (b) four- quantum dot arrays. Numbers label electron occupation of the islands; *x*U indicates relative dot size. *Adapted from ref* [4].

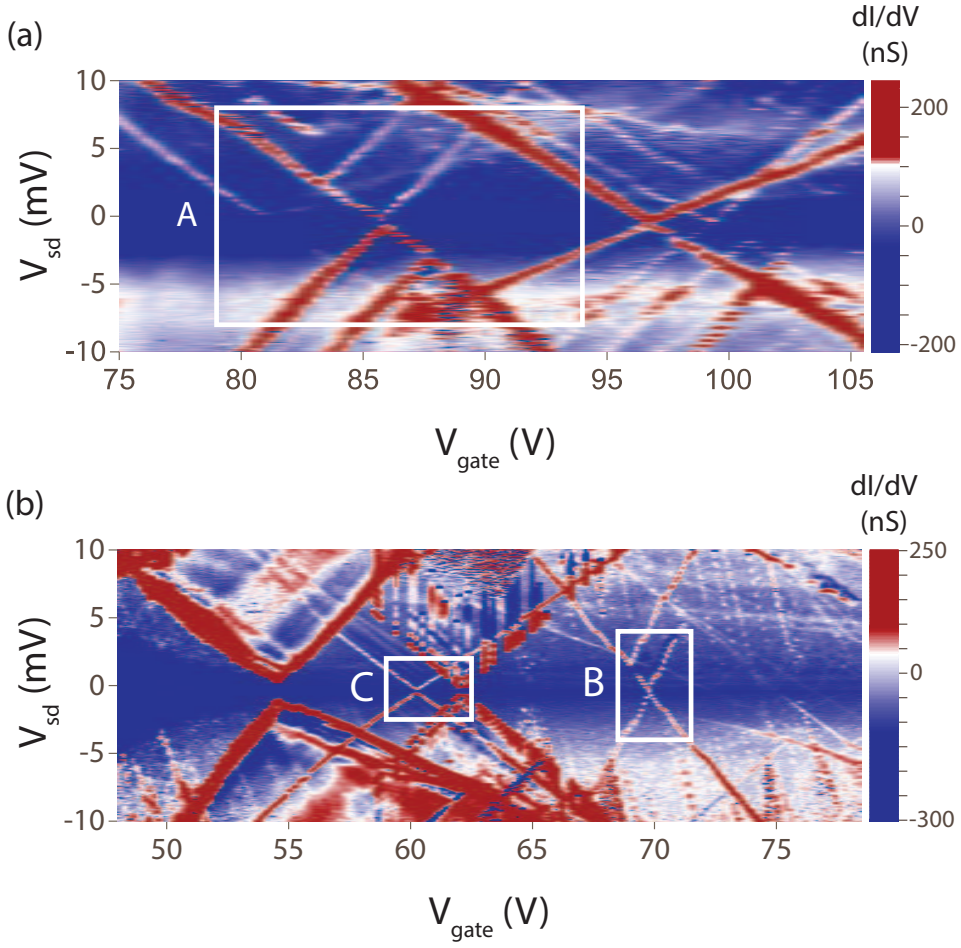


Figure 6.7: Differential conductance maps taken at T $\leq$ 10 mK for the two measurement periods with (a) perpendicular and (b) parallel magnetic field. The three single-electron transitions analysed in the sections below are marked.

6.4 Transition A (perpendicular field)

Figures 6.8 and 6.9 show the evolution of states for transition A in a perpendicular magnetic field. Using theory from section 2.3.3 to determine which states split in a magnetic field, N is determined to be even in this N $\leftrightarrow$ N + 1 transition. The tunnelling rates are asymmetric, with $\Gamma_L \ll \Gamma_R$, resulting in peaks in differential conductance due to excited states only appearing when the excited states line up with the drain (positive gradients).

Differential conductance plots of a single-electron transition give information about the relative positions of the electrochemical potentials which are dependent on the energies of the initial and final states, $\mu(N+1) = U(N+1) - U(N)$. As detailed in section 2.3.4, figure 6.9(c) shows the ladder of electrochemical potentials from figure 6.9(b) with the spin-filling for N and $N+1$ electrons corresponding to energies $U(N)$ and $U(N+1)$ marked for each $\mu(N+1)$. Each line at successively higher source-drain bias corresponds to an additional electrochemical potential of the dot entering the bias window, causing a step increase in conductance.

The energy level separations were 2.51 $\pm$ 0.04 meV, 3.20 $\pm$ 0.06 meV, and 3.11 $\pm$ 0.10 meV, marked in figure 6.9(c). Landé g-factors were calculated for these three states that split in field. These were 2.45 $\pm$ 0.11, 2.26 $\pm$ 0.09, and 1.92 $\pm$ 0.13.

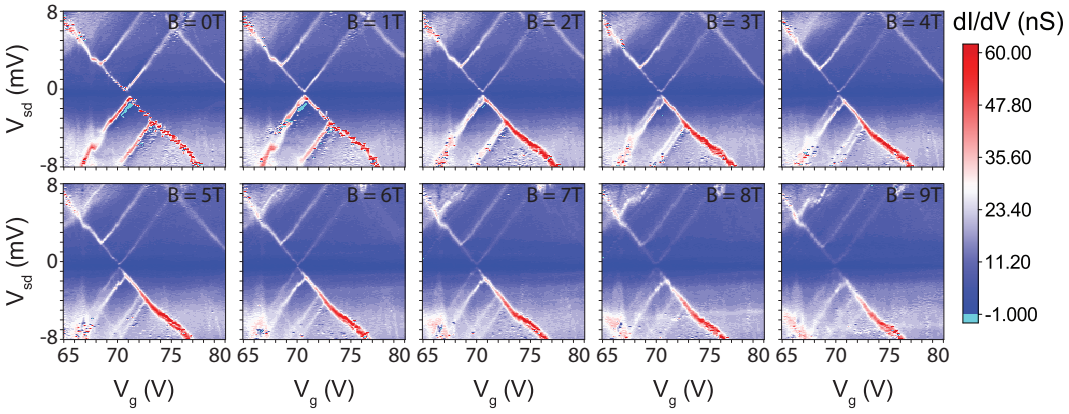


Figure 6.8: Differential conductance plotted as a function of source-drain and gate biases showing the evolution of states in transition A in a perpendicular B field, $B_\perp \leq 9$T.

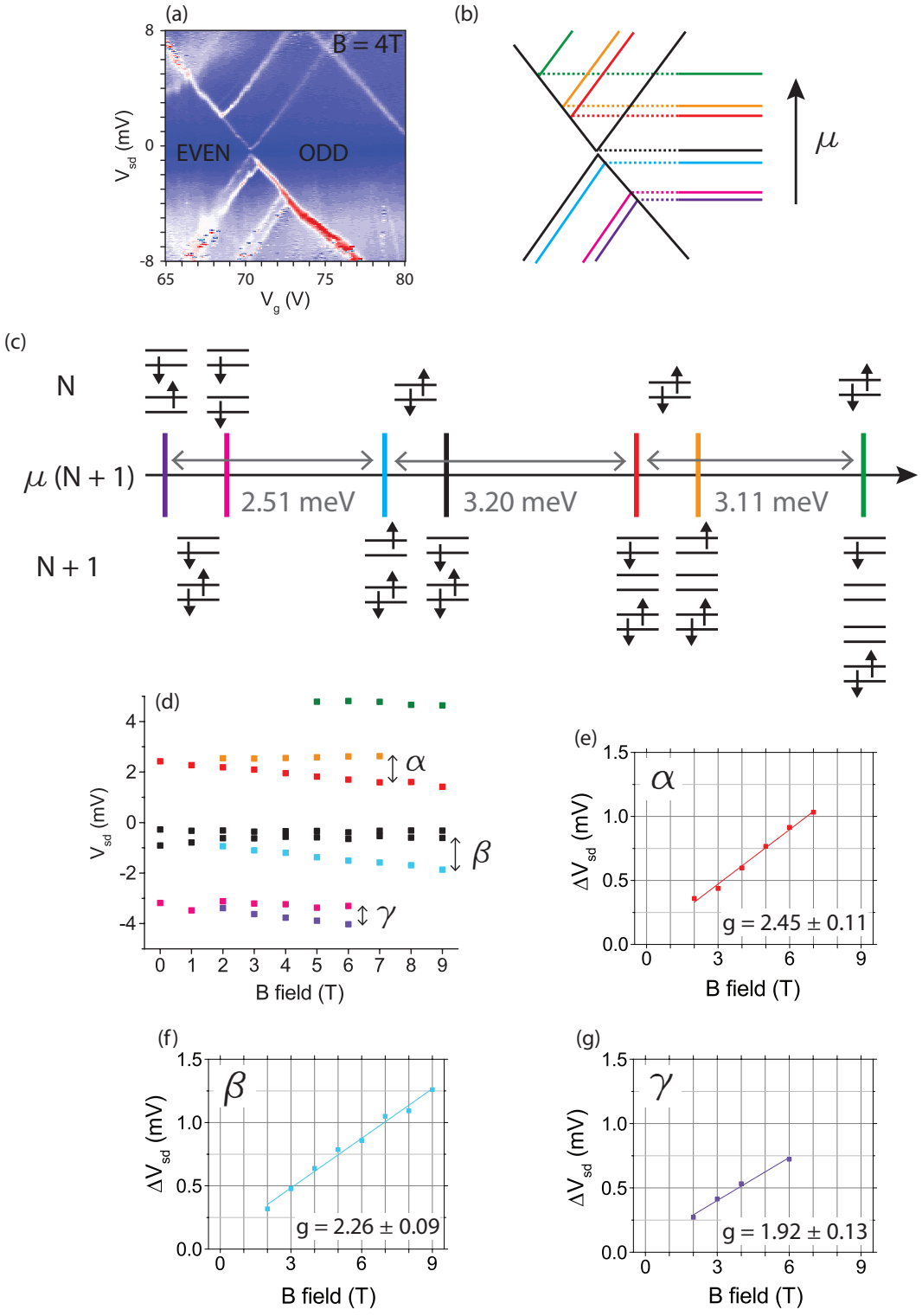


Figure 6.9: (a) Representative differential conductance plot for transition A. (b) Schematic showing observed transitions in (a). (c) N and $N+1$ spin filling corresponding to observed $\mu(N+1)$. (d) Evolution of states in a perpendicular magnetic field. (e)-(g) Plots of energy separation with field for three split states marked as α, β, and γ to extract the Landé g-factor.

6.5 Transition B (parallel field)

Figures 6.11 and 6.12 show the evolution of states for transition B in a parallel magnetic field. Using theory from section 2.3.3 to determine which states split in a magnetic field, N is determined to be odd in this $N \leftrightarrow N+1$ transition. The tunnelling rates are asymmetric, with $\Gamma_L \ll \Gamma_R$, resulting in peaks in differential conductance due to excited states only appearing when the excited states line up with the drain (positive gradients).

The energy level separation between the ground and excited state was 1.79 $\pm$ 0.06 meV, marked in figure 6.12(c). Landé g-factors were calculated for both states that split in field. These were 2.01 $\pm$ 0.17 and 2.07 $\pm$ 0.11. The calculated Landé g-factor for the negative differential conductance was much larger: 6.19 ± 0.72.

The deviation from the behaviour expected for a single-electron transition may be a result of a secondary, larger dot, capacitively coupled to the primary dot, shown schematically in figure 6.10. This may cause the reproducible kinks in the peaks of differential conductance, and the background streaks. We speculate that the streak of negative differential conductance shown in green in figure 6.12(b,d) arises from an electron hopping off the dot to another state nearby, electrostatically blocking the state on the dot leading to a reduction in the conductance with increased source-drain bias. The origin of the strong B field dependence ($g = 6.19 \pm 0.72$) is unknown.

Each state is split by a small, field-independent amount, 0.079 meV for the two lower transitions, and 0.062 meV for the two upper transitions.

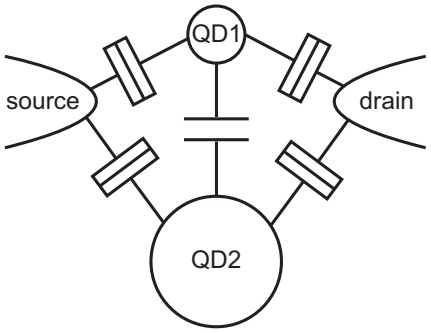


Figure 6.10: Two capacitively coupled quantum dots. The transport behaviour is dominated by the primary dot QD1. The secondary larger dot QD2 causes deviations in the expected single quantum dot behaviour.

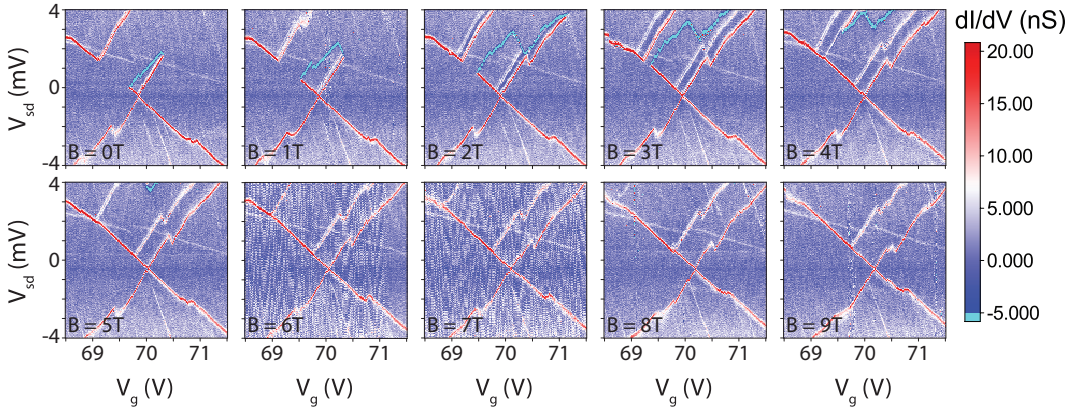


Figure 6.11: Differential conductance plotted as a function of source-drain and gate biases showing the evolution of states in transition B in a parallel B field, $B_{\parallel} \leq 9$T.

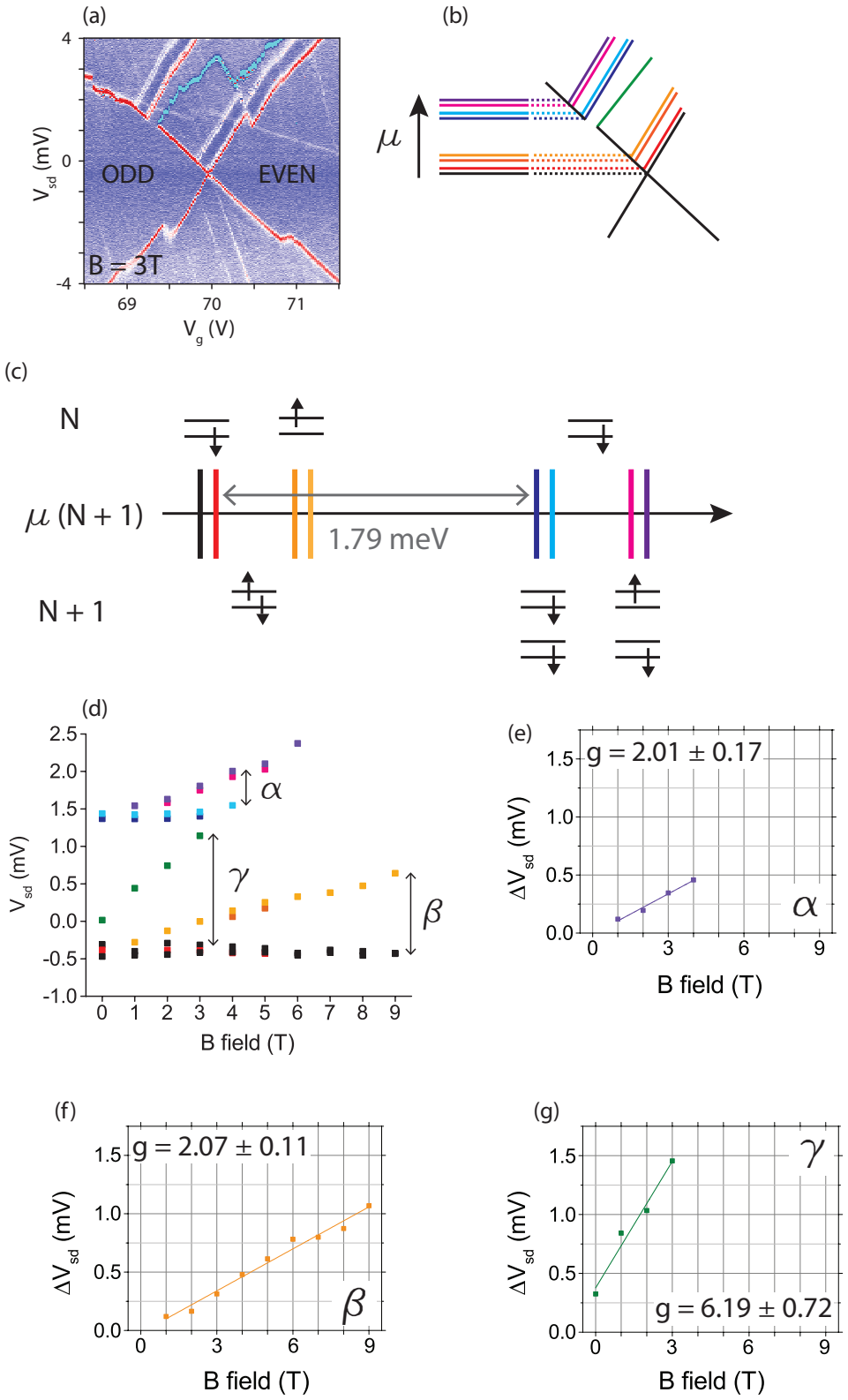


Figure 6.12: (a) Representative differential conductance plot for transition B. (b) Schematic showing observed transitions in (a). (c) N and $N+1$ spin filling corresponding to observed $\mu(N+1)$. (d) Evolution of states in a parallel magnetic field. (e)-(g) Plots of energy separation with field for two split states marked as α and β, and the negative differential conductance (marked γ) to extract the Landé g-factor.

6.6 Transition C (parallel field)

Figures 6.13 and 6.14 show the evolution of states for transition C in a parallel magnetic field. Using theory from section 2.3.3 to determine which states split in a magnetic field, N is determined to be odd in this $N \leftrightarrow N+1$ transition. The tunnelling rates are asymmetric, with $\Gamma_L > \Gamma_R$, resulting in higher intensity peaks in differential conductance when the electrochemical potential of the dot lines up with the source (negative gradient) than with the drain (positive gradient).

Landé g-factors were calculated for the ground state splitting, when the electrochemical potential of the dot lined up with that of the source $\mu(N+1) = \mu_L$, and the drain $\mu(N+1) = \mu_R$. These were 1.32 ± 0.07 and 1.11 ± 0.03 respectively.

The ground state is also split by a small field-independent amount, 0.072 meV. This is a similar energy difference to the field-independent splitting seen in transition B (section 6.5).

The background differential conductance has a rippling pattern, possibly due to electron-phonon interaction as seen in a suspended carbon nanotube device [54].

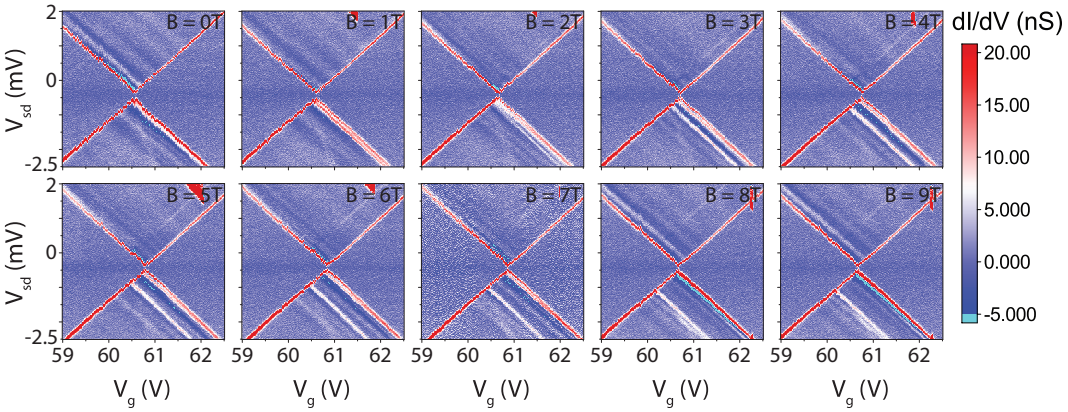


Figure 6.13: Differential conductance plotted as a function of source-drain and gate biases showing the evolution of states in transition C in a parallel B field, $B_{\parallel} \leq 9$T.

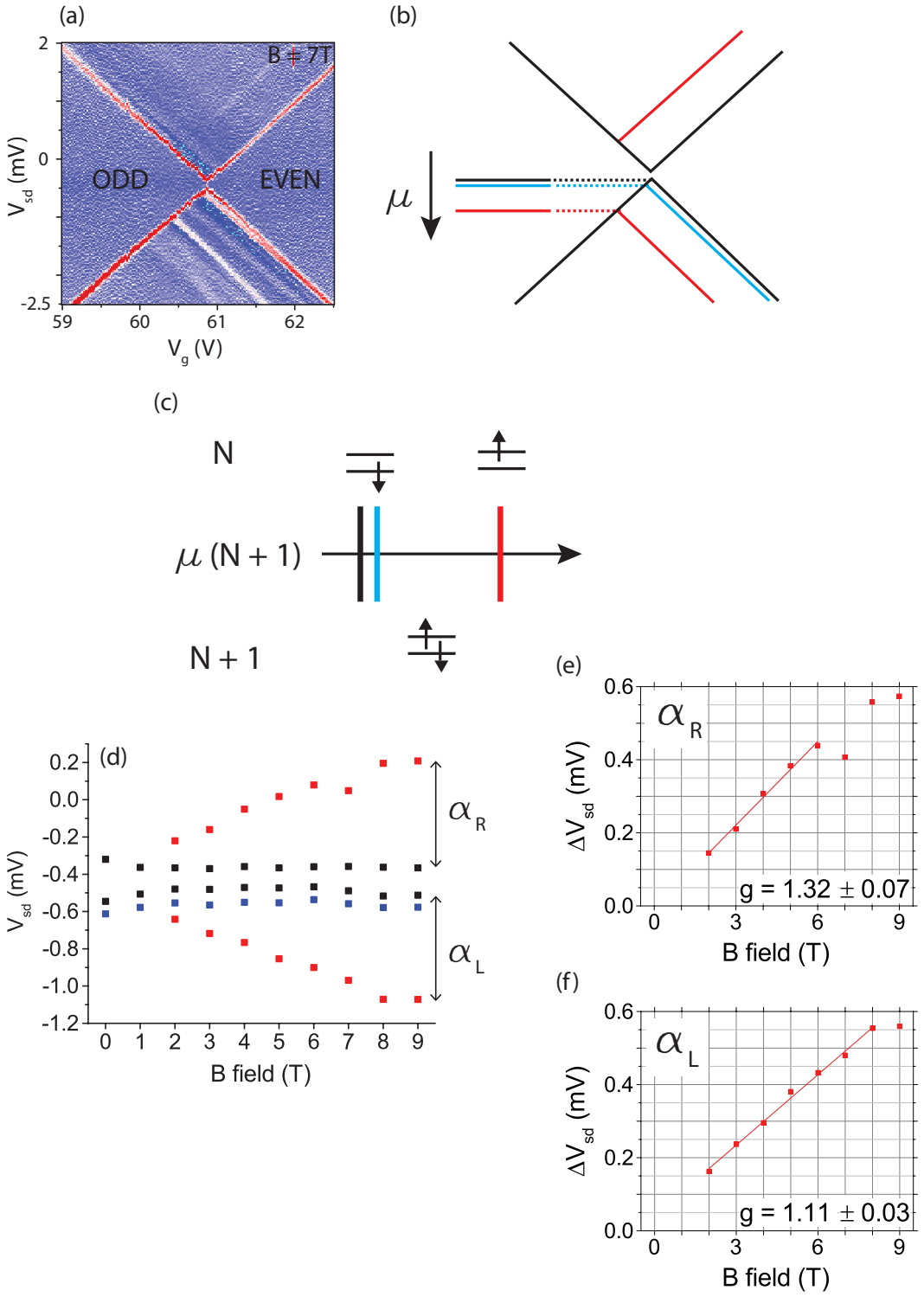


Figure 6.14: (a) Representative differential conductance plot for transition C. (b) Schematic showing observed transitions in (a). (c) N and $N+1$ spin filling corresponding to observed $\mu(N+1)$. (d) Evolution of states in a parallel magnetic field. (e),(f) Plots of the ground state energy separation with field to extract the Landé g-factor. Shifts marked as $\alpha_{L,R}$ correspond to $\mu(N+1) = \mu_{L,R}$.

6.7 System capacitances

Using a single $N \leftrightarrow N+1$ electron transfer, the relative capacitances C_i/C_Σ, i = S,D,G can be determined. However, without the charging energy E_C, the absolute capacitances cannot be experimentally determined.

As an alternative, the self-capacitance of the dot C_Σ or the gate capacitance C_G can be calculated theoretically. In this section absolute capacitances are calculated based on the assumption that the quantum dots have the effective mass of bilayer MoS_2.

Use of the self-capacitance of the dot will tend to overestimate the absolute capacitances [87]. We have assumed that $C_{\Sigma(model)} = C_S + C_D + C_G$, but in practice there will be additional contributions due to capacitive coupling between the dot and other parts of the device, so that $C_{\Sigma(true)} = C_{\Sigma(model)} + C_{add'l.}$. The calculated lever arms are $C_i/C_{\Sigma(model)}$. With $C_{\Sigma(true)} \geq C_{\Sigma(model)}$,

$$\frac{C_i}{C_{\Sigma(model)}} \times C_{\Sigma(true)} \geq C_i \tag{6.1}$$

The gate capacitance can be estimated using the parallel plate approximation, $C_G = \varepsilon_0 \varepsilon_r \frac{A}{d}$, where A is the area of overlap between the two plates (10–15 nm), and d is plate separation (280 nm). This is based on the approximation that $d \ll \sqrt{A}$, which is not the case, so the estimated value of C_Σ is expected to give better predictions than the estimated value of C_G.

The self-capacitance of a sphere with radius R is

$$C_{\Sigma,sphere} = 4\pi\varepsilon_0\varepsilon_r R \tag{6.2}$$

The self-capacitance of an infinitesimally thin conducting disc with radius R can be approximated by using the self-capacitance of an ellipsoid with one of the principal axes taken to 0.

$$C_{\Sigma,disc} = 8\varepsilon_0 R \tag{6.3}$$

$\varepsilon_0 = 8.85 \times 10^{-12}$ F/m is the vacuum permittivity. ε_r is the relative permittivity;

$\varepsilon_r = 4$ for bilayer MoS_2.

The size of a dot is inversely proportional to the mean level spacing for a chaotic dot. Using the excited state energy as a lower limit for the mean level spacing, δ, the dot area was calculated using the following equation [88].

$$\delta = \frac{2\pi\hbar^2}{m_{\text{eff}}A} \tag{6.4}$$

The effective mass is taken to be 0.38 m_0 for bilayer MoS_2. Assuming a circular dot, this yields dots with radii <15 nm.

Relative capacitances, C_i/C_Σ, calculated from the gradients as described in section 2.3.2, are given in table 6.1.

	A	B	C
α_S	0.5484	0.6681	0.5003
α_D	0.4509	0.3303	0.4991
α_G	0.0007	0.0017	0.0006

Table 6.1: Relative capacitances, $\alpha_i = C_i/C_\Sigma$, for transitions A, B, and C, calculated from the gradients in the differential conductance plots.

Table 6.2 shows the extracted system capacitances for two quasi-dots using the three methods described above. The excited state energy was used as a lower limit for the mean level spacing. Transition C is not included in the table because there was no observed excited state.

	A: r = 11.7 nm			B: r = 14.9 nm		
	sphere	disc	|| plate	sphere	disc	|| plate
C_S (aF)	4.428	0.705	35.489	2.854	0.454	41.999
C_D (aF)	2.189	0.348	17.543	2.347	0.373	34.526
C_G (aF)	0.011	1.75 x10^{-3}	0.088*	0.004	5.88 x10^{-4}	0.054*
C_Σ (aF)	6.628*	1.055*	53.120	5.205*	0.828*	76.579
E_C (meV)	24.1	152	3.01	30.7	193	2.09

Table 6.2: Calculated system capacitances for transitions A and B using three different methods: calculating self-capacitance assuming a spherical dot, calculating self-capacitance assuming a disc-shaped dot, and calculating gate capacitance using the parallel plate approximation. Starred capacitances result from the initial theoretical assumption.

The parallel plate approximation can be ruled out based on the estimated charging energies. For both transitions, data was collected for energies well above $E_{C,||}$, where a diamond peak would be expected to be observed. However, no such peak was seen.

6.8 Discussion

Coulomb blockade was seen in monolayer and bilayer MoS_2 devices at low temperature. Devices which were annealed before cooling additionally showed single-electron transitions which we speculate are defect states occurring at the metal-MoS_2 interface. The single-electron transitions were analysed, giving information about the g-factors, spin-filling, and relative system capacitances.

The charging energies were too large to determine experimentally, but estimates were made by assuming an effective mass equal to that of bilayer MoS_2 and taking a lower limit for the mean level spacing. The nature of the defects is unknown, but based on other experimental and theoretical studies discussed in section 2.2.4, they could be molybdenum vacancies, MoS_2 vacancies, anti-sites, or molybdenum substitution [29, 30, 31].

To observe MoS_2 quantum dots, the defective nature of the metal-MoS_2 contact first needs to be improved. Pisoni et al [6] fabricated a clean monolayer MoS_2 gate-defined quantum dot with a $\sim$280 nm effective radius (70 nm patterned radius) using pre-etched hexagonal boron nitride to avoid any defects caused by the device fabrication process. Their device appears to be defect free. Although the defect-free nature of their device is desirable, a fabrication of a smaller quantum dot, measured at lower temperatures, would allow a fuller analysis of MoS_2 quantum dot transport as for the defects in this chapter. Defining a dot using atomic force microscope lithography (section 3.3) would allow for the fabrication of smaller quantum dots defined with a hard electrostatic barrier.

Chapter 7

Conclusions

Lithographically defined quantum dots in MoS_2 have the potential to surpass the current state-of-the-art gate-defined MoS_2 quantum dots [6]. An atomic force microscope lithography technique was developed, with the ability to sharply define electrostatic barriers to create quantum dots that could be measured and altered in situ. Although it was possible to define quantum dot devices, the technique is as yet unreliable and requires further study of the many influencing parameters discussed in section 3.3.

Alongside the development of the AFM lithography technique, room temperature and low temperature measurements of MoS_2 and WSe_2 field-effect transistor (FET) devices were carried out. Although WSe_2 devices were too resistive for further study, room temperature transport measurements of MoS_2 devices revealed a strong dependence on charge trap occupation. We speculate that there are two types of charge trap: adsorbed molecules which are removed in vacuum, and metallic defect states at the metal-MoS_2 interface. Low temperature, $T \leq 10$ mK, measurements of annealed bilayer MoS_2 devices appear to probe individual defect states in the form of single-electron transitions, from which spin-filling and Landé g-factor information can be extracted. MoS_2 monolayer devices were also measured at low temperature but were found to be too resistive.

The work presented in this thesis contributes to the understanding of room temperature MoS_2 FET behaviour, and specifically to the understanding of the dynamics of hysteresis in transfer curves. It also adds to the body of work exploring

the nature of transport-altering defect states through the measurements carried out at low temperature.

In chapter 3 an atomic force microscope lithography technique was developed to define quantum dots in MoS_2 using lines of insulating oxide. Many advances were made including application of a pulsed rather than continuous bias to avoid charge build up, and quantum dots were successfully fabricated. The AFML technique requires further refinement in order to reliably oxidise samples. Improvements could be made to the MoS_2 surface quality by removing dirty processing steps such as photolithography. In addition, the AFML technique can be refined by introducing a pulse generator for more precise voltage pulse definition.

In chapter 5, experimental data and a theoretical model presented together were used to explore changes in transfer curve hysteresis as a result of charging and discharging of charge traps. High charge trap density was seen to result in large hysteresis. A drop in hysteresis after pumping is due to a reduction in the trap density and thus we suspect that a significant proportion of traps are adsorbed molecules that are removed at low pressures. Charge trap tunnelling times on the same time-scale as the measurement time resulted in large hysteresis, explored in a measurement frequency study with gate voltage ramp rates between 1×10^{-3} and 50 V/s. The shifting position of a charge trap equilibrium was noted qualitatively as a negative bias stressing effect which gradually lowered the equilibrium, thus lowering the measured threshold voltages. A sample holder was fabricated to allow in-situ vacuum annealing; annealing devices resulted in a negative shift in threshold voltage which brought the threshold and charge trap equilibrium voltages closer together, thus explaining the unexpected increase in hysteresis.

In chapter 6, devices were studied in a dilution refrigerator with a magnetic field up to 9 T. Spin filling information and g-factors were extracted from three zero-dimensional single-electron transition features probed with an applied magnetic field at low temperature ($T \leq 10$ mK). This adds to the growing area of research into the nature of defect states, which are understood to be molybdenum vacancies, anti-sites, or molybdenum substitution.

To expand on this work, an exploration of electron behaviour in MoS_2 quantum dots would require a new fabrication process which prevents the creation of defects. However, it is unclear whether this is possible. Pisoni et al [6] claim to have defect-free devices, fabricated using hexagonal boron nitride (hBN) sandwiching and an annealing stage at 300°C for half an hour in an inert argon/hydrogen mix. Use of a hBN substrate may better preserve the TMD structure as it is atomically flat. Encapsulation with hBN after annealing will avoid molecule adsorption and prevent further surface degradation; however, encapsulation would not be possible prior to AFML. I suggest a new fabrication process: (1) transfer MoS_2 crystal onto hBN crystal, (2) vacuum anneal the device, (3) immediately outline a quantum dot using AFML and check device transport, (4) vacuum anneal again, and finally (5) encapsulate with hBN. Should this result in defect-free quantum dot devices, low temperature transport measurements would give valuable information about electron behaviour in an MoS_2 quantum dot.

Exploration of other two-dimensional materials, such as tungsten diselenide, WSe_2, is also of interest. WSe_2 is being actively studied for its optical properties [89]: optically active quantum dots are found to occur naturally, possibly due to intrinsic defects. It has been reported by the Garcia group [57] that AFML oxidation of WSe_2 is easier and more reliable than MoS_2 oxidation; thus the developed AFML technique could be used to draw quantum dots in WSe_2 with chosen geometries and locations.

Appendix A

Shadow mask fabrication

Silicon shadow masks are made using photolithography followed by deep reactive-ion etching (DRIE). The optical mask used for photolithography was designed using AutoCAD 2014 and made out of quartz and chromium by Compugraphics (www.compugraphics-photomasks.com). The designs are shown in figure A.1, with four picked out to show the various geometries used. The mask includes two, three, and four-terminal designs with varying tip radii between 0.8 and 130 μm, and varying tip separation between 2 and 20 μm, to accommodate many flake dimensions. Each contact is large: 1.2 mm long, terminating in a 400×400 μm^2 pad. This results in more reliable etching, easier shadow mask alignment to the crystal, easier wire bonding, and a lower probability that there will be loss of contact between the crystal and bond pad.

Photolithography

The photo-resist used is S1818 from the Shipley Microposit® S1800® series. To prepare for photolithography, diced wafers are sonicated in acetone, then IPA, dried with nitrogen gas, and dehydrated at 200 °C for 20 minutes. S1818 is spun on at 4000 rpm for 30 seconds, creating a 1.8 μm thick film. The sample is baked for 60 seconds at 115 °C before aligning the sample to the chromium side of the optical mask using a Karl Suss MJB3 Mask Aligner. The set-up is exposed to UV light, with an exposure time calculated from the UV light power of the mask aligner (20 mW/cm^2), the exposure energy for the photo-resist used (50 mJ/cm^2), and the sample's surface reflectivity. After exposure, the sample is developed in

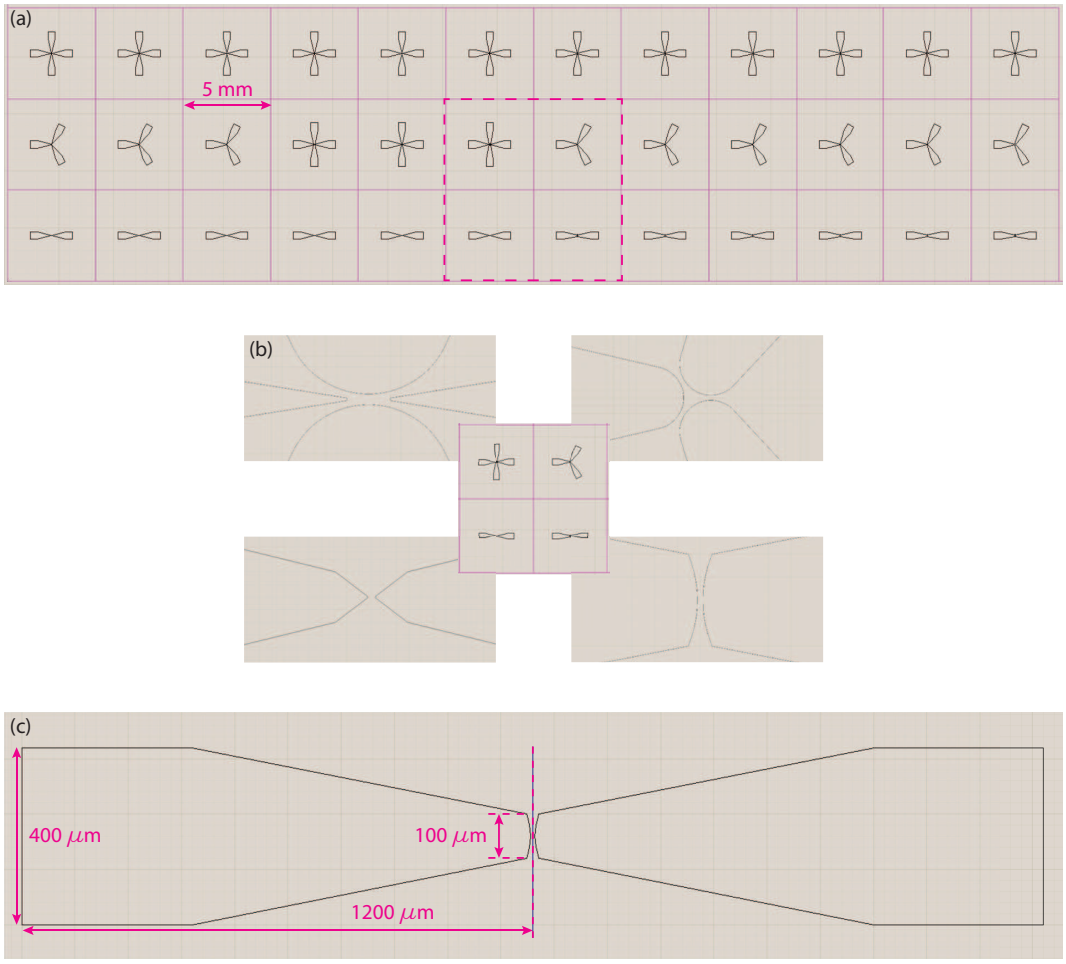


Figure A.1: (a) The pattern for the chromium optical mask, showing the thirty-six shadow mask designs. (b) A close up of four of the designs, showing some of the different tip geometries. (c) A close up of a full two-terminal blunt ended mask showing some features that all designs share: the contacts are 1.2 mm in length, ending in a 400 $\times$ 400 μm^2 pad. Here the radius of curvature of the tip is 130 μm and the contact separation is 10 μm. These values vary between designs.

MEGAPOSIT^{TM} MF^{TM}-26A Developer for 60 seconds, and is finally rinsed in de-ionised water and dried with nitrogen gas. Samples are mounted onto a 6 inch ceramic wafer ready for etching.

Deep Reactive-Ion Etching

DRIE is a two step etch process: isotropic deposition of passivating octafluorocyclobutane, C_4F_8, alternates with anisotropic chemical and physical etching using sulphur hexafluoride, SF_6, and O_2. The passivation layer is sputtered off until the silicon is exposed; the silicon is chemically etched forming silicon tetrafluoride, SiF_4. Each step lasts a few seconds, and together result in a close to vertical etch, even for high aspect ratio features. The etching was carried out on a Surface Technology Systems Inductively Coupled Plasma DRIE. Details of the parameters used are in table A.1. Typically $\sim$200 cycles were required to etch through 150 μm, equating to a silicon etch rate $R_{Si} \simeq 3.1$ μm/min.

Parameter	Deposit	Etch
Cycle Time (s)	5.5	9.0
Power (W)	600	800
Gas 1, flow (sccm)	C_4F_8, 85	SF_6, 130
Gas 2, flow (sccm)	–	O_2, 6

Table A.1: Parameters used in DRIE.

During DRIE the photo-resist is also etched, about 50–100 times slower than the silicon etching. The wafers use for the shadow masks were 150 μm thick. Thinner wafers will etch more successfully and require a thinner photo-resist layer; thicker wafers are easier to handle and less likely to break during fabrication. Etch success is determined by comparing the top-side pre- and post-etch dimensions, and by comparing top- and back-side dimensions post-etch to determine the angular deviation from the vertical. Finer features etch more slowly than large features. Consequently, two-terminal blunt-tipped designs are typically the most successful.

Figure A.2 shows the top- and back-side of two shadow mask designs with different tip radii, etched using the same DRIE recipe. The top-side sits on top of the crystal, and the metal is evaporated from the back-side. Figure A.2(d) showing

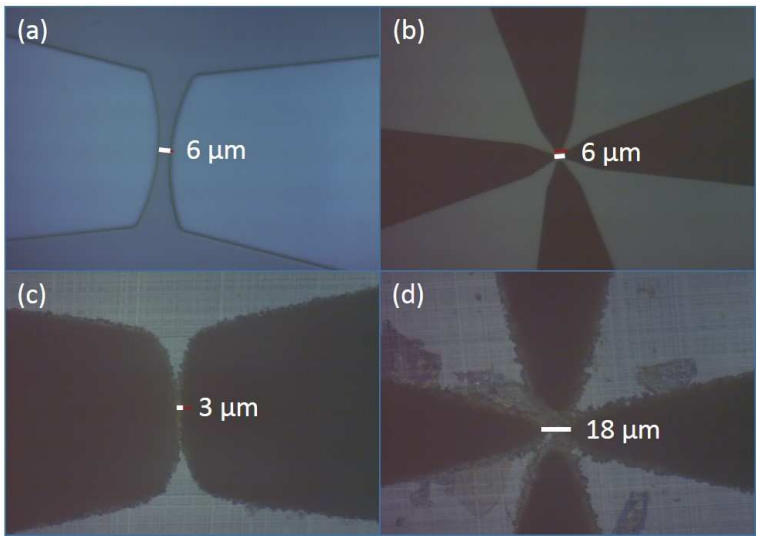


Figure A.2: (a),(b) Top-side and (c),(d) back-side of two different mask designs with the same recipe. (a),(c) show a mask that is suitable for shadow mask evaporation.

the back-side of a fine-tipped four-terminal design demonstrates the slower etching at the tips. The blunt two-terminal design shown was successful, with a deviation of +0.6° from the vertical; the fine four-terminal design was unsuccessful, with a deviation of -2.3° from the vertical.

Aligning

An optical microscope and alignment stage are used to align the shadow mask to the crystal. The sample substrate with the crystal is glued to a fixed base using a water-soluble polymer, Crystalbond^{TM} 555; the back-side of the shadow mask is glued to a thin, flexible, piece of copper with a 3 mm diameter hole to reveal the mask pattern. The top-side of the mask is placed against the sample substrate, and lightly screwed down onto the fixed base. The mask is positioned with tweezers, using the optical microscope to see through the mask onto the sample. Once aligned the mask is tightly screwed to the substrate (figure A.3(a)). If the mask is not in close contact with the substrate, possibly because of a thick crystal nearby the thin crystal of interest, then the area that is contacted with metal may be greater than intended, as shown in an exaggerated way in figure A.3(c). Once aligned satisfactorily, the stage can be moved directly from the microscope to the metal evaporator. If using two metal layers for the contact, care must be taken to align the

metal sources directly beneath the sample, to ensure complete overlap. The effect of slightly mis-aligned sources is shown in figure A.3(d).

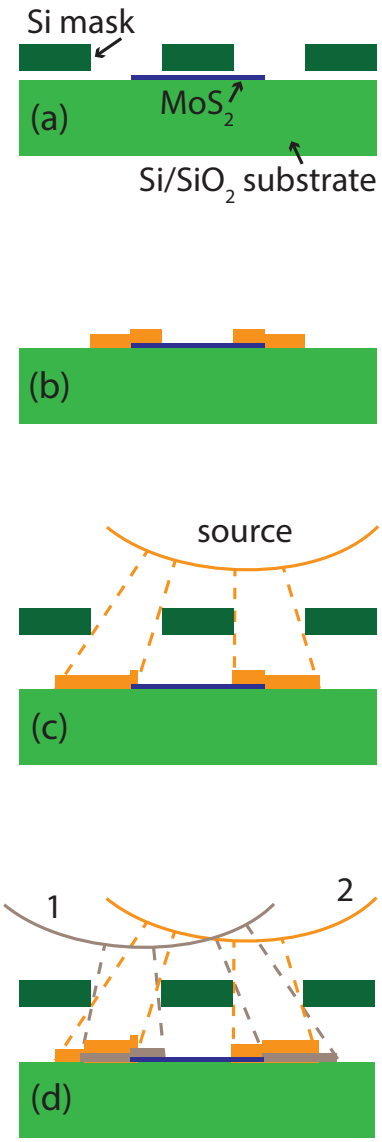


Figure A.3: (a) The shadow mask is aligned to a crystal. (b) An ideal evaporation. (c) A diagram of the lateral offset caused by having a small source-sample separation in the evaporator in combination with a slightly off-centre source. (d) Diagram for two-layer contacts (e.g. 1 = titanium, 2 = gold). Mis-alignment between the two sources will result in a lateral offset.

Appendix B

WSe_2 transport

Preliminary room temperature transport measurements were taken for four few-layer tungsten diselenide, WSe_2, field-effect transistor devices fabricated in the same way as the MoS_2 devices (see chapter 4), using p-type WSe_2 from hq-graphene (http://www.hqgraphene.com/).

Device conductance was low; only one device had a current larger than the noise threshold in ambient conditions $\sim$pA). Pumping on the devices and vacuum annealing to T $>$ 140 $^{\circ}$C reduced the hysteresis and increased the conductivity.

Room temperature measurement after annealing (P3 in table B.1) showed ambipolar behaviour in all of the devices, with a maximum conductance of 170 nS for device D at V_g = 100 V, V_{sd} = 1 V.

Figure B.1 shows transport for device A at V_{sd} = 1 V. Devices B-D were too resistant to do a similar comparison.

The low conductances prevented further study of these devices. Adjusting

	P1		P2		P3	
	p	n	p	n	p	n
A	680.9		22.5		54.2	54.9
B					117.0	212.7
C					1594.8	758.9
D				82.0	298.9	5.8

Table B.1: Device resistances in MΩ from measurements in ambient (P1), under vacuum (P2), and after thermal annealing (P3). V_{sd} = 1 V, $|V_g|$ = 80 V (P1, 2); 100 V (P3). In empty cells, the current was too small to measure.

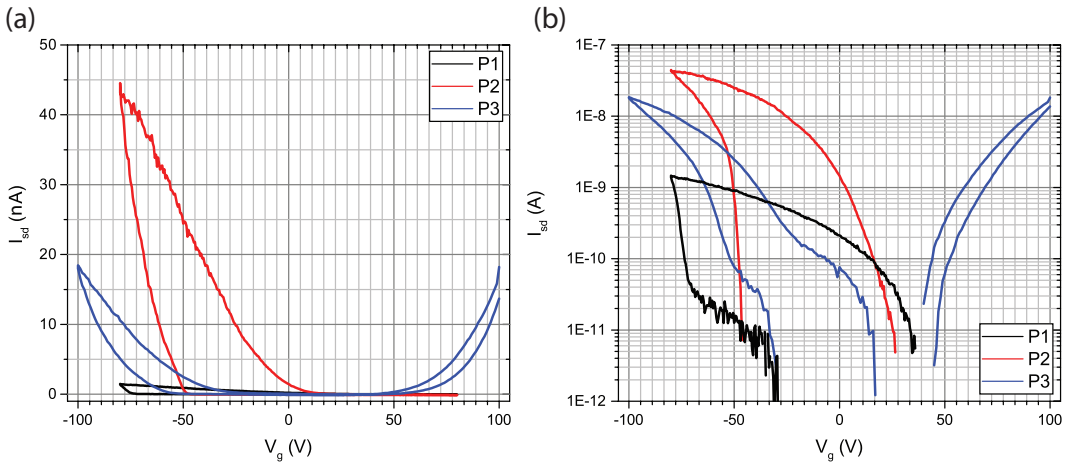


Figure B.1: Transfer curves for WSe_2 device A on a (a) linear and (b) log scale, taken in ambient (P1, black), in vacuum (P2, red), and after thermal annealing (P3, blue).

the fabriction process or starting materials is likely to increase conductance. The contacts were fabricated with titanium/gold, as for the MoS_2 devices. Ti/Au contacts are typically used for n-type devices due to the well-matched metal work function. To increase conductance, n-type WSe_2 can be used instead of p-type, or other metals with larger work functions such as palladium can be used to replace Ti/Au.

Appendix C

Monolayer MoS_2

Devices were also made using monolayer MoS_2, fabricated using the same process as for bilayers. Figure C.1 shows optical, AFM and Raman data for a monolayer MoS_2 device.

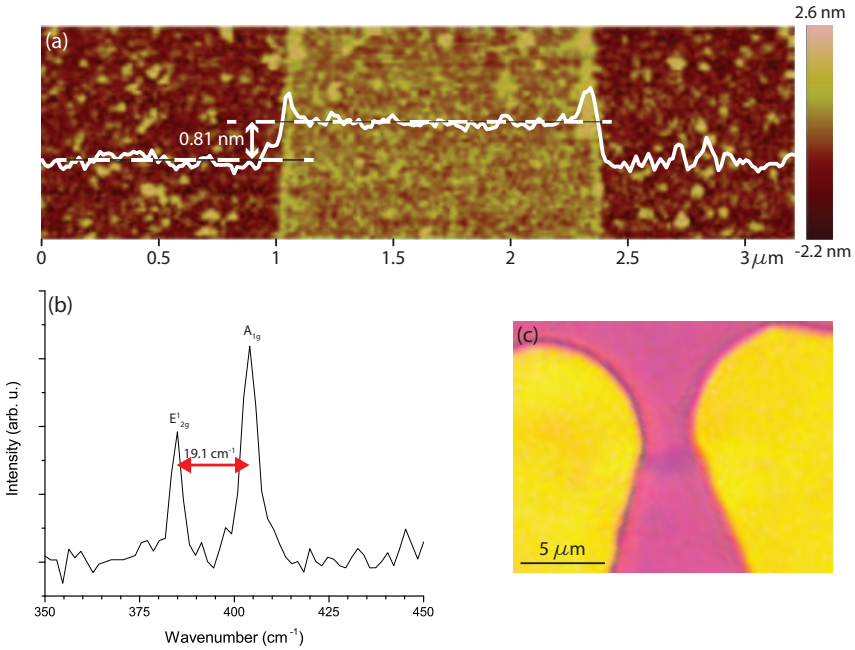


Figure C.1: Characterisation of a monolayer device. (a) AFM image, (b) Raman spectrum, (c) optical image

As the monolayer was cooled to millikelvin temperatures, the threshold voltage increased, and conductivity decreased. A large scale differential conductance map at base temperature (figure C.2(a)) shows a gap that closes with increasing gate bias, with a maximum conductance of 30 nS measured. Higher gate biases were

tested, shown in figure C.2(b). The map shows evidence of Coulomb blockade in the monolayer, with the gap continuing to close. The minimum gap is 20 mV. Testing higher gate biases still was avoided due to the likelihood of it resulting in gate oxide failure.

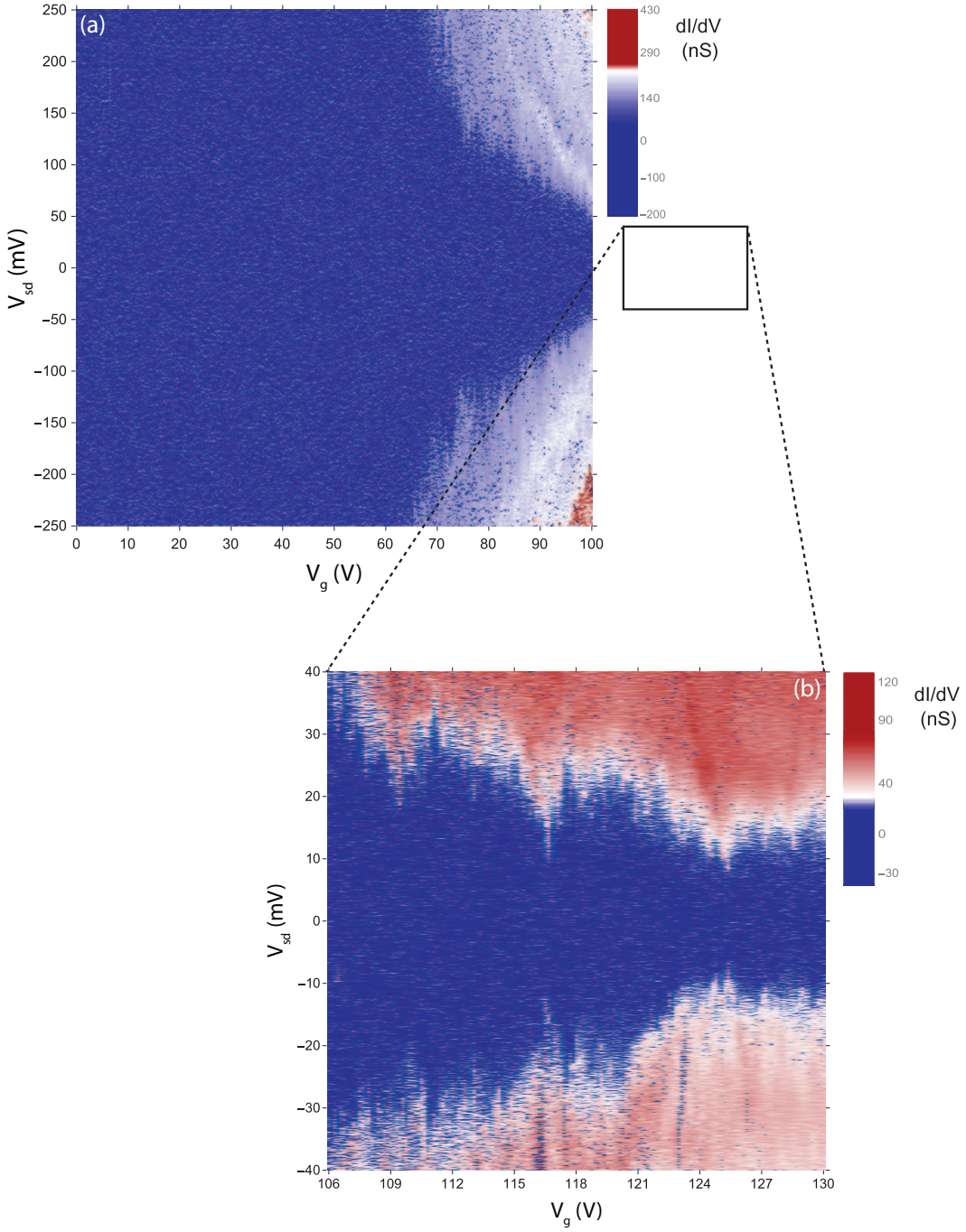


Figure C.2: Large scale differential conductance maps of a monolayer device.

Bibliography

[1] Q.H. Wang, K. Kalantar-Zadeh, A. Kis, J.N. Coleman, and M.S. Strano. Electronics and optoelectronics of two-dimensional transition metal dichalcogenides. *Nature Nanotechnology*, 7:699–712, 2012.

[2] A. Splendiani, L. Sun, Y. Zhang, T. Li, J. Kim, C.-Y. Chim, G. Galli, and F. Wang. Emerging photoluminescence in monolayer MoS_2. *Nano Letters*, 10:1271–1275, 2010.

[3] D. Jariwala, V.K. Sangwan, D.J. Late, J.E. Johns, V.P. Dravid, T.J. Marks, L.J. Lauhon, and M.C. Hersam. Band-like transport in high mobility unencapsulated single-layer MoS_2 transistors. *Applied Physics Letters*, 102(173107), 2013.

[4] Y.V. Nazarov and Y.M. Blanter. *Quantum Transport: Introduction to Nanoscience*. Cambridge University Press, The Edinburgh Building, Cambridge CB2 8RU, UK, 2009.

[5] M.T. Allen, J. Martin, and A. Jacoby. Gate-defined quantum confinement in suspended bilayer graphene. *Nature Communications*, 3(934):1–6, 2012.

[6] R. Pisoni, Z. Lei, P. Back, M. Eich, H. Overweg, Y. Lee, K. Watanabe, T. Taniguchi, T. Ihn, and K. Ensslin. Gate-tunable quantum dot in a high quality single layer MoS_2 van der waals heterostructure. *Applied Physics Letters*, 112(123101), 2018.

[7] R. Puddy. *Transport Spectroscopy of Graphene Quantum Dots Fabricated by Atomic Force Microscope Nano-Lithography*. PhD thesis, Cambridge University, 2013.

[8] F.M. Espinosa, Y.K. Ryu, K. Marinov, D. Dumcenco, A. Kis, and R. Garcia. Direct fabrication of thin layer MoS_2 field-effect nanoscale transistors by oxidation scanning probe lithography. *Applied Physics Letters*, 106(103503), 2015.

[9] E. Pinilla-Cienfuegos, S. Mañas-Valero, E. Navarro-Moratalla, S. Tatay, A. Forment-Aliaga, and E. Coronado. Local oxidation nanolithography on metallic transition metal dichalcogenides surfaces. *Applied Sciences*, 6(250), 2016.

[10] H. Li, Q. Zhang, C.C.R. Yap, B.K. Tay, T.H.T. Edwin, A. Olivier, and D. Baillargeat. From bulk to monolayer MoS_2: Evolution of Raman scattering. *Advanced Functional Materials*, 22:1385–1390, 2012.

[11] C. Lee, H. Yan, L.E. Brus, T.F. Heinz, J. Hone, and S. Ryu. Anomalous lattice vibrations of single- and few-layer MoS_2: Evolution of Raman scattering. *Advanced Functional Materials*, 22:1385–1390, 2012.

[12] G.K. White and P.J. Meeson. *Experimental Techniques in Low-Temperature Physics*. Clarendon Press, Oxford, 4th edition, 2002.

[13] BlueFors Cryogenics. *BF-LD250 Cryogen-Free Dilution Refrigerator System*, 1.4.0 edition, January 2013.

[14] D. Wang, X.-B. Li, D. Han, W.Q. Tian, and H.-B. Sun. Engineering two-dimensional electronics by semiconductor defects. *NanoToday*, 16:30–45, 2017.

[15] M. Akhtar, G. Anderson, R. Zhao, A. Alruqi, J.E. Mroczkowska, G. Sumanasekera, and J.B. Jasinski. Recent advances in synthesis, properties,

and applications of phosphorene. *npj 2D Materials and Applications*, 1(5), 2017.

[16] J.S. Ponraj, Z.-Q. Xu, S.C. Dhanabalan, H. Mu, Y. Wang, J. Yuan, P. Li, S. Thakur, M. Ashrafi, and K. Mccoubrey. Photonics and optoelectronics of two-dimensional materials beyond graphene. *Nanotechnology*, 27(46), 2016.

[17] Y.K. Luo, J. Xu, T. Zhu, G. Wu, E.J. McCormick, W. Zhan, M.R. Neupane, and R.K. Kawakami. Opto-valleytronic spin injection in monolayer MoS_2/few-layer graphene hybrid spin valves. *Nano Letters*, 17(6):3877–3883, 2017.

[18] X. Zhai, W. Gao, X. Cai, D. Fan, Z. Yang, and L. Meng. Spin-valley caloritronics in silicene near room temperature. *Physical Review B*, 94(245405), 2016.

[19] R.-J. Shiue, D.K. Efetov, G. Grosso, C. Peng, K.C. Fong, and D. Englund. Active 2D materials for on-chip nanophotonics and quantum optics. *Nanophotonics*, 6(6), 2017.

[20] R. Frindt. Single crystals of MoS_2 several molecular layers thick. *Journal of Applied Physics*, 37(4):1928–1929, 1966.

[21] P. Joensen, R.F. Frindt, and S.R. Morrison. Single-layer MoS_2. *Materials Research Bulletin*, 21(4):457–461, 1986.

[22] K.S. Novoselov, A.K. Geim, S.V. Morozov, D. Jiang, Y. Zhang, S.V. Dubonos, I.V. Grigorieva, and A.A. Firsov. Electric field effect in atomically thin carbon films. *Science*, 306(5696):666–669, 2004.

[23] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis. Single-layer MoS_2 transistors. *Nature Nanotechnology*, 6:147–150, 2011.

[24] T. Li, G. Du, B. Zhang, and Z. Zeng. Scaling behaviour of hysteresis in multilayer MoS_2 field effect transistors. *Applied Physics Letters*, 105(093107), 2014.

[25] D.J. Late, B. Liu, H.S.S.R. Matte, V.P. Dravid, and C.N.R. Rao. Hysteresis in single-layer MoS_2 field effect transistors. *ACS Nano*, 6(6):5635–5641, 2012.

[26] Y. Guo, X. Wei, J. Shu, B. Liu, J. Yin, C. Guan, Y. Han, S. Gao, and Q. Chen. Charge trapping at the MoS_2-SiO_2 interface and its effects on the characteristics of MoS_2 metal-oxide-semiconductor field effect transistors. *Applied Physics Letters*, 106(103109), 2015.

[27] J. Roh, J.-H. Lee, S.H. Jin, and C. Lee. Negligible hysteresis of molybdenum disulfide field-effect transistors through thermal annealing. *Journal of Information Display*, 17(3):103–108, 2016.

[28] C. Kim, I. Moon, D. Lee, M.S. Choi, F. Ahmed, S. Nam, Y. Cho, H.-J.Shin, S. Park, and W.J. Yoo. Fermi level pinning at electrical metal contacts of monolayer molybdenum dichalcogenides. *ACS Nano*, 11:1588–1596, 2017.

[29] S. McDonnell, R. Addou, C. Buie, R.M. Wallace, and C.L. Hinkle. Defect-dominated doping and contact resistance in MoS_2. *ACS Nano*, 8(3):2880–2888, 2014.

[30] C. Gong, L. Colombo, R.M. Wallace, and K. Cho. The unusual mechanism of partial fermi level pinning at metal-MoS_2 interfaces. *Nano Letters*, 14:1714–1720, 2014.

[31] P. Bampoulis, R. van Bremen, Q. Yao, B. Poelsema, and H.J.W. Zandvliet. Defect dominated charge transport and Fermi level pinning in MoS_2/metal contacts. *ACS Applied Materials & Interfaces*, 9:19278–19286, 2017.

[32] Y. Yang, A.M. Asiri, Z. Tang, D. Du, and Y. Lin. Graphene based materials for biomedical applications. *Materials Today*, 16(10), 2013.

[33] K.S. Aneja, H.L. Mallika Böhm, A.S. Khanna, and S. Böhm. Functionalised graphene as a barrier against corrosion. *FlatChem*, 1:11–19, 2017.

[34] S.P. Surwade, S.N. Smirnov, I.V. Vlassiouk, R.R. Unocic, G.M. Veith, S. Dai, and S.M. Mahurin. Water desalination using nanoporous single-layer graphene. *Nature Nanotechnology*, 10:459–464, 2015.

[35] K. Chen, Q. Wang, Z. Niu, and J. Chen. Graphene-based materials for flexible energy storage devices. *Journal of Energy Chemistry*, 27:12–24, 2018.

[36] D. Ovchinnikov, A. Allain, Y.-S. Huang, and D. Dumcenco. Electrical transport properties of single-layer WS_2. *ACS Nano*, 8(8):8174–8181, 2014.

[37] M. Amani, M.L. Chin, A. Glen Birdwell, T.P. O'Regan, S. Najmaei, Z. Liu, P.M. Ajayan, J. Lou, and M. Dubey. Electrical performance of monolayer MoS_2 field-effect transistors prepared by chemical vapor deposition. *Applied Physics Letters*, 102(193107), 2013.

[38] Y.-M. He, G. Clark, J.R. Schaibley, Y. He, M.-C. Chen, Y.-J. Wei, X. Ding, Q. Zhang, W. Yao, X. Xu, C.-Y. Lu, and J.-W. Pan. Single quantum emitters in monolayer semiconductors. *Nature Nanotechnology*, 10:497–502, 2015.

[39] O. Lopez-Sanchez, D. Lembke, M. Kayci, A. Radenovic, and A. Kis. Ultrasensitive photodetectors based on monolayer MoS_2. *Nature Nanotechnology*, 8:497–501, 2013.

[40] E. Zhang, W. Wang, C. Zhang, Y. Jin, G. Zhu, Q. Sun, D.W. Zhang, P. Zhou, and F. Xiu. Tunable charge-trap memory based on few-layer MoS_2. *ACS Nano*, 9(1):612–619, 2015.

[41] E. Singh, K.S. Kim, G.Y. Yeom, and H.S. Nalwa. Atomically thin-layered molybdenum disulfide (MoS_2) for bulk-heterojunction solar cells. *ACS Applied Materials & Interfaces*, 9:3223–3245, 2017.

[42] M.S. El-Bana, D. Wolverson, S. Russo, G. Balakrishnan, D.M. Paul, and S.J. Bending. Superconductivity in two-dimensional $NbSe_2$ field effect transistors. *Superconductor Science and Technology*, 26:125020, 2013.

[43] W.G. Fisher and M.J. Sienko. Stoichiometry, structure, and physical properties of niobium disulfide. *Inorganic Chemistry*, 19(1):39–43, 1980.

[44] J. Gusakova, X. Wang, L.L. Shiau, A. Krivosheeva, V. Shaposhnikov, V. Borisenko, V. Gusakov, and B.K. Tay. Electronic properties of bulk and monolayer TMDs: Theoretical study within DFT framework (GVJ-2e method). *Physica Status Solidi A*, 214(12), 2017.

[45] M. Riordan. The lost history of the transistor. *IEEE Spectrum*, pages 44–49, 2004.

[46] M. Härting, J. Zhang, D.R. Gamota, and D.T. Britton. Fully printed silicon field effect transistors. *Applied Physics Letters*, 94(193509), 2009.

[47] Y. Cui, Z. Zhong, D. Wang, W.U. Wang, and C.M. Lieber. High performance silicon nanowire field effect transistors. *Nano Letters*, 3(2):149–152, 2003.

[48] T. Dürkop, S.A. Getty, E. Cobas, and M.S. Fuhrer. Extraordinary mobility in semiconducting carbon nanotubes. *Nano Letters*, 4(1):35–39, 2004.

[49] S. Das, H.-Y. Chen, A.V. Penumatcha, and J. Appenzeller. High performance multilayer MoS_2 transistors with scandium contacts. *Nano Letters*, 13(1):100–105, 2013.

[50] S. Datta. *Electronic Transport in Mesoscopic Systems*. Cambridge University Press, 1995.

[51] W.D. Callister Jr. *Materials Science and Engineering*. John Wiley & Sons, Inc., 2007.

[52] R.K. Puddy, C.J. Chua, and M.R. Buitelaar. Transport spectroscopy of a graphene quantum dot fabricated by atomic force microscope nanolithography. *Applied Physics Letters*, 103(183117), 2013.

[53] K.M. Weiss, J.M. Elzerman, Y.L. Delley, J. Miguel-Sanchez, and A. Imamoglu. Coherent two-electron spin qubits in an optically active pair of coupled InGaAs quantum dots. *Physical Review Letters*, 109(107401), 2012.

[54] R. Leturcq, C. Stampfer, K. Inderbitzin, L. Durrer, C. Hierold, E. Mariani, M.G. Schultz, F. von Oppen, and K. Ensslin. Franck-Condon blockade in suspended carbon nanotube quantum dots. *Nature Physics*, 5:327–331, 2009.

[55] M. Javaid, D.W. Drumm, S.P. Russo, and A.D. Greentree. Surface-gate-defined single-electron transistor in a MoS_2 bilayer. *Nanotechnology*, 28(12), 2017.

[56] Y.K. Ryu and R. Garcia. Advanced oxidation scanning probe lithography. *Nanotechnology*, 28(142003), 2017.

[57] A.I. Dago, Y.K. Ryu, and R. Garcia. Sub-20 nm patterning of thin layer WSe_2 by scanning probe lithography. *Applied Physics Letters*, 109(163103), 2016.

[58] D. Gopalakrishnan, D. Damien, and M.M. Shaijumon. MoS_2 quantum dot-interspersed exfoliated MoS_2 nanosheets. *ACS Nano*, 8(5):5297–5303, 2014.

[59] B. Li, L. Jiang, X. Li, P. Ran, P. Zuo, A. Wang, L. Qu, Y. Zhao, Z. Cheng, and Y. Lu. Preparation of monolayer MoS_2 quantum dots using temporally shaped femtosecond laser ablation of bulk MoS_2 targets in water. *Scientific Reports*, 7(11182):1–12, 2017.

[60] S. Gottlieb, M. Lorenzoni, L. Evangelio, M. Fernández-Regúlez, Y.K. Ryu, C. Rawlings, M. Spieser, A.W. Knoll, and F. Perez-Murano. Thermal scanning probe lithography for the directed self-assembly of block copolymers. *Nanotechnology*, 28(175301), 2017.

[61] M. Jaschke and H.-J. Butt. Deposition of organic material by the tip of a scanning force microscope. *Langmuir*, 11:1061–1064, 1995.

[62] X. Jiang, G. Wu, J. Zhou, S. Wang, A.A. Tseng, and Z. Du. Nanopatterning on silicon surface using atomic force microscopy with diamond-like carbon (DLC)-coated Si probe. *Nanoscale Research Letters*, 6(518), 2011.

[63] N. Lindvall, A. Kalabukhov, and A. Yurgens. Cleaning graphene using atomic force microscope. *Journal of Applied Physics*, 111(064904), 2012.

[64] A.M. Goossens, V.E. Calado, A. Barreiro, K. Watanabe, T. Taniguchi, and L.M.K. Vandersypen. Mechanical cleaning of graphene. *Applied Physics Letters*, 100(073110), 2012.

[65] C. Schönenberger and N. Kramer. Nanolithography on hydrogen-terminated silicon by scanning-probe microscopy. *Microelectronic Engineering*, 32:203–217, 1996.

[66] R.V. Martínez, J. Martínez, and R. Garcia. Silicon nanowire circuits fabricated by AFM oxidation nanolithography. *Nanotechnology*, 21(24), 2010.

[67] J.A. Dagata, J. Schneir, H.H. Harary, C.J. Evans, M.T. Postek, and J. Bennett. Modification of hydrogen-passivated silicon by a scanning tunneling microscope operating in air. *Applied Physics Letters*, 56, 1990.

[68] Z. Shen, S. Hou, H. Sun, X. Zhao, and Z. Xue. Local oxidation of titanium thin films using an atomic force microscope under static and pulsed voltages. *Journal of Physics D: Applied Physics*, 37(9), 2004.

[69] T.Y. Kim, E.D. Zitti, D. Ricci, and S. Cincotti. Atomic force microscope nanolithography on titanium: Influence of the anodic voltage waveform on the formation of oxide nanodots. *Superlattices and Microstructures*, 44:670–676, 2008.

[70] L. Weng, L. Zhang, Y.P. Chen, and L.P. Rokhinson. Atomic force microscope local oxidation nanolithography of graphene. *Applied Physics Letters*, 93(093107), 2008.

[71] I.-S. Byun, D. Yoon, J.S. Choi, I. Hwang, D.H. Lee, M.J. Lee, T. Kawai, Y.-W. Son, Q. Jia, H. Cheong, and B.H. Park. Nanoscale lithography on monolayer graphene using hydrogenation and oxidation. *ACS Nano*, 5(8):6417–6424, 2011.

[72] Z.J. Davis, G. Abadal, O. Hansen, X. Borisé, N. Barniol, F. Pérez-Murano, and A. Boisen. AFM lithography of aluminium for fabrication of nanomechanical systems. *Ultramicroscopy*, 97(1-4):467–472, 2003.

[73] J.M. Chen, S.W. Liao, and Y.C. Tsai. Electrochemical synthesis of polypyrrole within PMMA nanochannels produced by AFM mechanical lithography. *Synthetic Materials*, 155(1):11–17, 2005.

[74] R. Addou, L. Colombo, and R.M. Wallace. Surface defects on natural MoS_2. *ACS Applied Materials & Interfaces*, 7:11921–11929, 2015.

[75] F. Mueller, R.N. Schouten, M. Brauns, T. Gang, W.H. Lim, N.S. Lai, A.S. Dzurak, W.G. van der Wiel, and F.A. Zwanenburg. Printed circuit board metal powder filters for low electron temperatures. *Review of Scientific Instruments*, 84(044706), 2013.

[76] F. Kuemmeth and C.M. Marcus. Reducing noise and temperature during measurements in cryostats, March 2015.

[77] D. Maradan, L. Casparis, T.-M. Liu, D.E.F. Biesinger, C.P. Scheller, D.M. Zumbühl, J.D. Zimmerman, and A.C. Gossard. GaAs quantum dot thermometry using direct transport and charge sensing. *Journal of Low Temperature Physics*, 175:784–798, 2014.

[78] P. Blake, E.W. Hill, A.H. Castro Neto, K.S. Novoselov, D. Jiang, R. Yang, T.J. Booth, and A.K. Geim. Making graphene visible. *Applied Physics Letters*, 91(063124), 2007.

[79] M.M. Benameur, B. Radisavljevic, J.S. Héron, S. Sahoo, H. Berger, and A. Kis. Visibility of dichalcogenide nanolayers. *Nanotechnology*, 22(125706), 2011.

[80] J. Shu, G. Wu, Y. Guo, B. Liu, X. Wei, and Q. Chen. The intrinsic origin of hysteresis in MoS_2 field effect transistors. *Nanoscale*, 8(3049), 2016.

[81] K. Cho, W. Park, J. Park, H. Jeong, J. Jang, T.-Y. Kim, W.-K. Hong, S. Hong, and T. Lee. Electric stress-induced threshold voltage instability of multilayer MoS_2 field effect transistors. *ACS Nano*, 7(9):7751–7758, 2013.

[82] Y.Y. Illarionov, G. Rzepa, M. Waltl, T. Knobloch, A. Grill, M.M. Furchi, T. Mueller, and T. Grasser. The role of charge trapping in MoS_2/SiO_2 and MoS_2/hBN field-effect transistors. *2D Materials*, 3(035004), 2016.

[83] M. Chhowalla, D. Jena, and H. Zhang. Two-dimensional semiconductors for transistors. *Nature Reviews Materials*, 1(16052):1–15, 2016.

[84] K. Kaasberg, K.S. Thygesen, and K.W. Jacobsen. Phonon-limited mobility in n-type single-layer MoS_2 from first principles. *Physical Review B*, 85(115317), 2012.

[85] Z.-Y. Ong and M.V. Fischett. Mobility enhancement and temperature dependence in top-gated single-layer MoS_2. *Physical Review B*, 88(165316), 2013.

[86] B. Radisavljevic and A. Kis. Mobility engineering and a metal-insulator transition in monolayer MoS_2. *Nature Materials*, 12(9):815–820, 2013.

[87] R. Hanson, L.P. Kouwenhoven, J.R. Petta, S. Tarucha, and L.M.K. Vandersypen. Spins in few-electron quantum dots. *Reviews of Modern Physics*, 79(1217), 2007.

[88] A.Kormányos, V. Zólyomi, N.D. Drummond, and G. Burkard. Spin-orbit coupling, quantum dots, and qubits in monolayer transition metal dichalcogenides. *Physical Review X*, 4(011034), 2014.

[89] A. Srivastava, M. Sidler, A.V. Allain, D.S. Lembke, A. Kis, and A. Imamoglu. Optically active quantum dots in monolayer WSe_2. *Nature Nanotechnology*, 10:491–496, 2015.