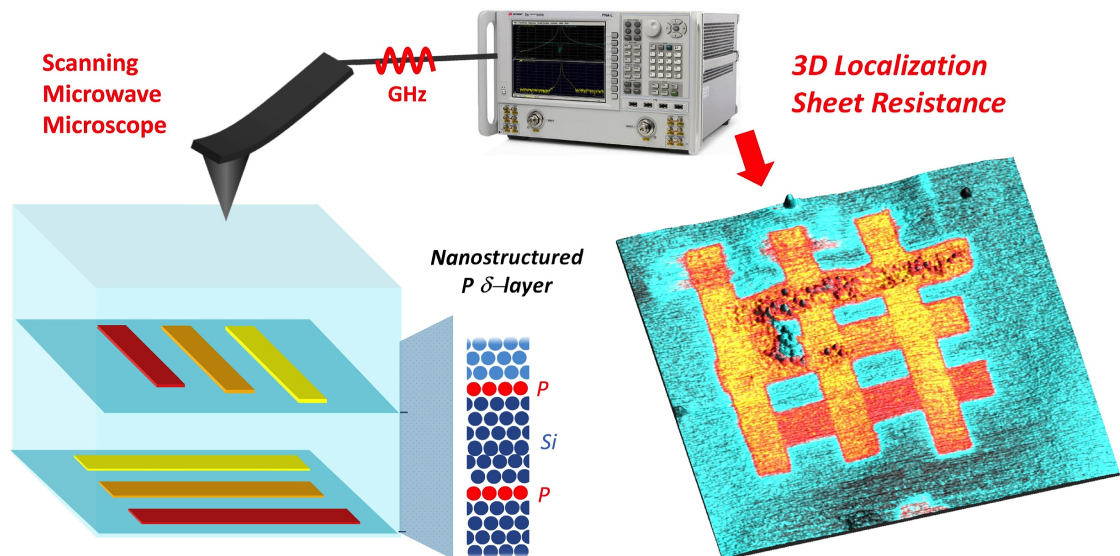
Fabrication and characterization of nanoscale dopant devices in silicon



Alexander Koelker

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Declaration

I, Alexander Koelker, confirm that the work presented in this thesis is my own. Where information has been derived from other sources, I confirm that this has been indicated in the work.

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Abstract

Semiconductor nanostructures consisting of areas of buried dopant atom(s) are crucial components for present and future complementary metal-oxide-semiconductor (CMOS) transistor technologies as well as for emerging quantum computing architectures. This thesis describes electrically contacted nanoscale devices of buried phosphorus in silicon, fabricated using scanning tunnelling microscope (STM) based hydrogen resist lithography, and characterised using scanning microwave microscopy (SMM). The goal is to improve nanoscale device fabrication strategies and develop methods that allow a direct device characterisation for a broad range of applications such as the fabrication of a silicon quantum computer.

At first, a step by step guide for the fabrication strategy that has been developed is presented. The resulting nanoscale devices, consisting of a single layer of phosphorus atoms in silicon (so called δ-layers), are characterised by electrical transport measurements and SMM. The transport measurements enable the study of the sensitivity of conduction to small changes in dopant densities and the determination of the δ-layer 'electronic width', along with the growth quality of the δ-layers.

The second part of the thesis describes the development of a characterisation scheme using SMM that not only enables us to non-destructively image atomically-thin patterned nanostructures buried in silicon, but also extract quantitative parameters such as depth and conductance. This scheme was subsequently applied to extract similar parameters from a three-dimensional (3D) sample, whose complexity and difficulty of fabrication far exceeds any other published 3D P-in-Si structure made using hydrogen resist lithography. We also demonstrate that SMM spectroscopy in conjunction with finite element modelling can be employed to identify the contributions to the measured SMM complex admittance that originate from the substrate, the patterned δ-layer region and the two-dimensional (2D) nature of the two-dimensional electron gas (2DEG). Finally, characterisation is performed on an active P-in-Si patterned device component in the form of a $1\,\mu\text{m} \times 10\,\mu\text{m}$ wire with an in-

plane bias applied along the wire. The full range of scanning probe capabilities of an SMM setup is applied for characterisation, including Kelvin probe force microscope (KPFM) and scanning capacitance force microscope (SCFM).

Impact statement

The details provided here about the fabrication strategy for buried nanoscale dopant devices in silicon will be the basis for future device fabrication activities at LCN, and will also be beneficial for the fabrication community to produce nanoscale devices with highly reproducible performance. This scientific community consists of research groups at universities (UNSW, Australia), national laboratories (National Institute of Standards and Technology, and Sandia National Labs, both USA) and companies (Zyvex Labs, USA and IBM, Zurich). This is a collaborative community, making knowledge exchange straight-forward. For example, I spent six weeks in Zyvex Labs, Dallas, where I worked on programming control software that is now integrated into Zyvex commercial products. I have also given oral presentations about this work at IBM, and at the prestigious International Workshop on Silicon Quantum Electronics. As the research field develops, a broader range of competitive strategies for nanoscale device fabrication will accelerate the progress made within the research area and help to improve methods for the realisation of quantum information processing (QIP) architectures.

The development of a non-destructive metrology tool based on scanning microwave microscopy is a promising step to speed up the current development of three-dimensioal (3D) patterned device structures for the realisation of a surface code quantum computer. The field of quantum technologies currently generates a great deal of interest from within the academic community and beyond. As well as being published in a high impact scientific journal (Science Advances), the work was also of interest to the general public. It was featured in numerous web articles including Phys.org (with 164 likes), IEEE Spectrum, Photonics online, bit-tech and EurekAlert!. One of my industrial collaborators on the SMM research were Keysight Technologies, who are experts in the manufacture of high frequency electronics, and are one of the pioneers of the SMM technique. An important impact of my thesis work was to introduce Keysight to the applications that their technique might have

in the field of quantum technologies and the imaging of integrated circuit components, and discussions with Keysight are on-going. Colleagues at the London Centre for Nanotechnology are planning to extend my work in the direction of reverse-engineering of integrated circuit components for security applications.

My results describing the characterisation of an active P-in-Si patterned device component using three related scanning probe capabilities have the potential to create impact in the academic and commercial sector. As the first measurement of its kind, it opens the way for similar measurements on devices made from different materials and performing different functions. For example, the results here describe the behaviour of a conducting wire, however, components such as in-plane tunnel junctions, capacitors or single electron transistors could be studied alone or in combinations. Semiconductor companies may find it appealing to study their components in operation.

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The last four years have been a very exciting and intense time for me. I would like to express my deepest gratitude for the opportunity of working in such a lively research environment. Not only being responsible for the fabrication of samples for a large group of outstanding researchers (the COMPASSS project), I also got the chance to be part of an initial training network (Marie Curie program) where I could broaden my horizon in an international network of interdisciplinary researchers. I would take the opportunity to dedicate words of gratitude to those who have left a footprint on my way and without which my PhD and this thesis would not have been possible.
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Publications arising

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Chapter 1

Introduction

Since the beginning of transistor technology in the 1950s, silicon has established itself as the primary material for electronic devices. The electrical characteristics of the silicon bulk structure and, in particular, the ability to control the conductivity by doping with group-3 elements like boron, or group-5 like phosphorus (P), opened a broad field of applications. Important components for present and future complementary metal-oxide-semiconductor (CMOS) transistor technology of any integrated electronic device are highly conducting sheets of buried dopant atoms which serve as current vias, capacitance/shielding plates and/or source (S) and drain (D) electrodes [8].

Over the last decades, the semiconductor industry was driven by the ability to increase the computing power of a chip by doubling its transistor density every two years [9]. As a result of this famous relation, known as 'Moors law', todays modern microprocessors contain several billion MOS field-effect transistors (MOSFETs) with a minimum feature size of approximately 10 nm [10, 11]. In the last 15 years, this classical scaling law could only be complied with the invention and introduction of new materials and device structures to retain high device performances of each new technology generation [11]. With decreasing dimension, device performances are significantly influenced by the position and the electrical properties of only a few individual dopant atoms, demonstrated in a three-dimensional (3D) electrostatic potential simulation for a random dopant distribution in a MOSFET (depicted in Figure 1.1). Due to their random distribution in the silicon crystal, a resulting varying threshold voltage in MOSFETs was found to cause a reduced gate control of the device [12–15]. Therefore, the control of single dopant atom placement is highly desirable for a reproducible device fabrication of future MOSFET technology. One possible way to deterministically place donors in silicon has been accomplished by the use of single ion

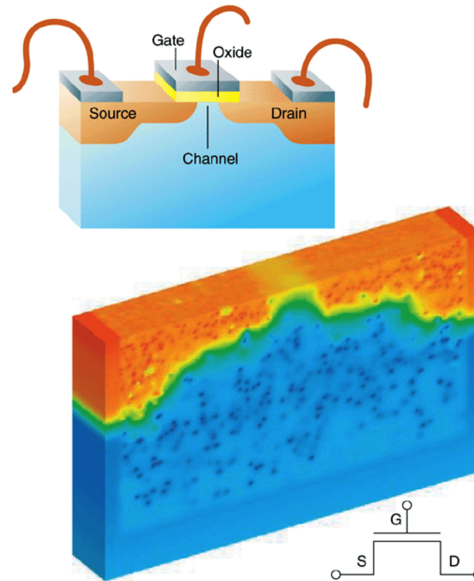


Figure 1.1: 3D simulation of a 30 nm by 30 nm field-effect transistor domain that contains random dopants in the source, drain, and substrate (bulk). The electrostatic potential is color-mapped from red (1 V) through the rainbow to blue (0 V). (Top inset) Schematic diagram of the basic interconnect wiring structure of a field-effect transistor. (Bottom inset) Circuit diagram symbol for a field-effect transistor. (From [13])

implantation [12, 16]. Integrated into a scanning probe tip, single ion implantation is reported to have injected donors into different substrates with a lateral precision of $4-9\,\text{nm}$ while aiming for a subsurface depth of $20\,\text{nm}$ [17]. As discussed below, single donor atoms have also been proposed as possible hosts for quantum bits (qubits) in quantum computing schemes that aim to dramatically increase the computational power compared to classical processors by exploiting the wave-like nature of matter.

1.1 Quantum computation schemes

Since the practical proposal to exploit a quantum mechanical two-level system for computation ([18, 19] and others), a variety of material systems have been investigated for the realisation of a universal quantum computer (QC). A solid state realisation of a QC in silicon was first theoretically proposed by Kane *et al.* [20]. An illustration of his scheme appears in Figure 1.2a). In this proposal, the $S = \frac{1}{2}$ nuclear spins of buried ^{31}P donors in silicon are employed as a qubit because they are extremely well isolated from their environment. At low temperatures the donor electron is recaptured by the positive donor ion similar to a hydrogen atom where the electron wave function is concentrated at the donor nucleus in a 1s orbital. The electron spin $I = \frac{1}{2}$ couples to the nuclear spin via the hyperfine interaction

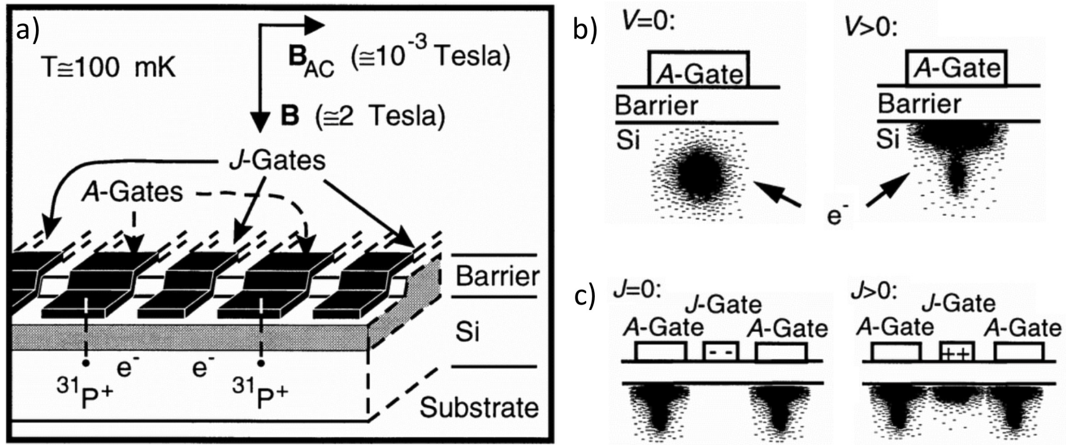


Figure 1.2: a) Illustration of the proposed solid state realisation of a quantum computer in silicon by Kane *et al.*, comprising ^{31}P donors and electrons in a Si host, separated by a barrier from metal gates on the surface. b) 'A gates' control the resonance frequency of the nuclear spin qubits; b) 'J gates' control the electron-mediated coupling between adjacent nuclear spins. (From [20])

and the strength of this interaction can be controlled by precisely aligned top gates. When applying a voltage to the top gate electrodes (A-Gates), the induced emanating E-field spatially shifts the extended wave function of the valance electron away from the nucleus (see Figure 1.2b)) to reduce the hyperfine interaction and its resonance frequency. J-Gates between the donors control the electron-mediated coupling between adjacent nuclear spins (see Figure 1.2c)) while a globally applied AC magnetic field B_{AC} flips nuclear spins at resonance. Besides low temperatures ($\sim$ 100 mK) this proposal requires a very high gate alignment ($\sim$ 10 nm) and atomic precise in-plane donor placement in silicon. The spatial resolution of single ion implementation is not high enough to satisfy the precision demands of this proposal. Since 1998, Kane's theoretical scheme has driven the development of a fabrication technology for the deterministic placement of dopants and the realisation of a read-out architecture for quantum computation in silicon. More recently other proposals for a silicon based QC have been proposed based on ordered arrays [21–23].

An alternative to ion implantation has been developed, using scanning tunnelling microscope (STM) based hydrogen resist lithography (H-lithography) where P donors can be placed with near atomic resolution by selectively removing hydrogen atoms from a passivated silicon surface [24], shown in Figure 1.3. The electron beam of the STM tip is used to break individual Si-H bonds and a subsequent exposure to a background pressure of a precursor gas (PH_3) results in a selective adsorption of the molecules in depassivated areas. The deterministic P donor placement process using STM H-lithography is described

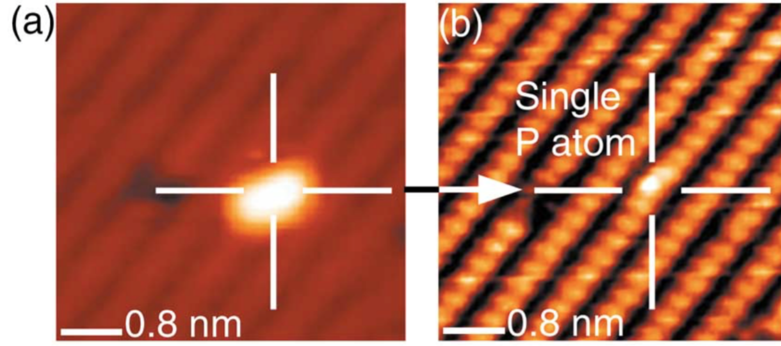


Figure 1.3: STM image of atomically controlled P atom incorporation into Si(001). (a) H-terminated Si(001) with a 1 nm diameter H-desorption point (3 dimers long). (b) The same area after PH_3 dosing and annealing to 350 °C showing a single P atom incorporated at the location defined by the H-desorption point. (From [24]).

in detail in chapter 4. In addition, this method also provides the capability to pattern larger device structures with lateral dimensions ranging from the atomic-scale (angstroms) to microns. Devices can then be fabricated by subsequently encapsulating the patterned P nanostructures with silicon followed by a contacting process. STM H-lithography based device fabrication also provides a powerful tool to investigate the ultimate scaling of conventional semiconductor devices [13, 25].

Over the last decades, STM H-lithography has proved ideal for the definition of laterally confined atomically thin 2D P dopant nanostructures as building blocks for prototype quantum devices. Nanoscale P sheets [26], wires [27, 28], dots [29] and single dopant transistors [30] have all been fabricated. Recent advances have demonstrated control of the exchange interaction of a two-quibit device via in-plane phosphorus doped detuning gates [31]. The patterned nanostructure of this two spin-qubit donor device is shown in an STM micrograph in Figure 1.4F). The successful fabrication of these devices was only possible by the systematic development of a fabrication strategy [27,32], that produces high-quality epitaxially overgrown silicon with a high activation of buried phosphorus dopants while retaining their in-plane confinement [33, 34]. In the first chapter of this thesis, our developed fabrication strategy will be presented, combing STM H-lithography for a precise control of P placement and electron beam lithography (EBL) for achieving high alignment accuracy for contacting.

STM H-lithography in conjunction with PH_3 dosing is a pathway for the fabrication of single atom devices but also provides a new and well-controlled material for systematic studies of two-dimensional lattices. The resulting P sheets are very heavily doped 2D

silicon, called δ-layer, with carrier densities of $\sim 2\times10^{14}\,\mathrm{cm}^{-2}$ [33]. Due to high doping, the carrier densities produced in δ-layers are much higher compared to MOSFETs ($10^{12}-10^{13}\,\mathrm{cm}^{-2}$ [35]), showing high conductivities at low temperatures where even a 1.5 nm wide defined P nanowire shows ohmic transport behaviour [28] (shown in Figure 1.4). In comparison, heavily doped vapor-liquid-solid (VLS)-grown Si wires become highly

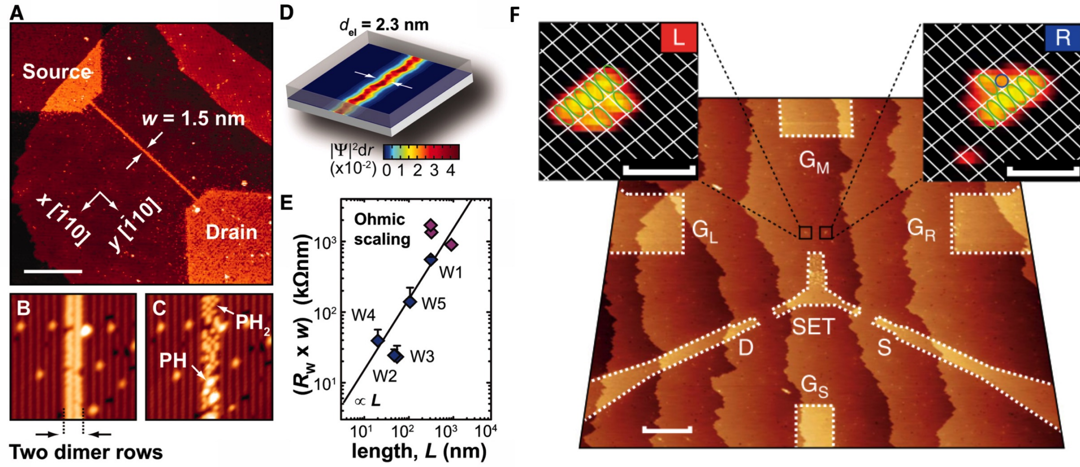


Figure 1.4: (A-C) STM H-lithography defined P dopant wires in silicon, (B) before and (C) after PH_3 dosing. (D) Atomistic NEMO modelling of the electron distribution in a 1.5 nm dopant wire (E) Four-terminal resistances corrected for series resistances and normalised with the lithographic width ($R_W \times w$), plotted versus wire length L (blue and purple diamonds) (From [28]). (F) STM micrograph of a two qubit 2P-P device with independent sequential readout. An STM micrograph of a precision placed two spin-qubit donor device consisting of in-plane control gates (G_L, G_R and G_M) and single-electron-transistor (SET) charge sensor with source (S) and drain (D) reservoirs. The scale bar is 20 nm. The insets show close-up STM micrographs of L and R where the green (blue) circles show fully (half) desorbed silicon dimers. White lines indicate the silicon dimer rows and the scale bars are 2 nm. (From [31])

resistive below a width of 10 nm as a result of surface depletion due to interface states and trapped charges as well as dopant deactivation caused by a dielectric mismatch between wire and its surroundings [36, 37]. Both of these issues lead to a reduction in dopant activation and hence carrier density. These effects cannot be compensated by introducing even higher doping densities because of the limited doping density achievable in VLS-grown nanowires [37]. On the other hand, highly conductive leads are essential for the realisation of a silicon based QC. The conductance in δ-doped wires and layers in the high doping regime, in turn, was found to be very sensitive to minute changes of dopant densities within the δ-layer plane [26, 38]. To investigate these findings, in the first part of chapter 5.3.5 we therefore apply conventional transport measurements to a set of δ-layers to investigate their mobility and carrier density as a function of dopant density in the channel. The extracted

transport parameters also assist in assessing the growth quality of the fabricated δ-layer devices.

Beyond their potential for conventional and quantum electronics, the P δ-layers are of fundamental physical interest because they realise a disordered two-dimensional electron gas (2DEG) with unprecedented high carrier density where quantum contributions to the conductance such as weak-localisation (WL) become significant. In the second part of chapter 5.3.5, we show that this quantum scattering effect, which manifests in an increased conductance, can be exploited as a metrology tool to probe the 'electrical width' of a δ-layer.

In the recent years, surface codes for the realisation of a QC in silicon such as [21] or [22] have been proposed where in-plane leads and interconnects need to be aligned in a 3D architecture with near atomic precision. Substantial challenges arise for their fabrication since precise alignment of a large number of interconnects in 3D requires a complex fabrication process which increases the number of interfaces. That in turn increases the number of defects and trapped charges which can potentially disturb the functionality of the device. A proposal to reduce the number of leads with fewer alignment steps is the Stoneham-Fisher-Greenland (SFG) scheme [39].

In the SFG-scheme the qubit states are encoded in the spin of the donor valence electron and interaction between two qubits (A and B) is mediated not by electrostatic gates but an additional control-dopant located between the qubit-dopants [39]. A schematic is shown in Figure 1.5a). The qubits are separated ($\sim 10\,$nm) such that their donor ground states (1s, Bohr radius of $\sim 2.5\,$nm [42]) do not interact. Since each dopant species has a different optical excitation frequency, the control dopant can be selectively excited by a terahertz pulse, see Figure 1.5b). The resulting excited-state wave function, while still bound, extends over 10 nm [43] through the silicon crystal and creates a spin exchange interaction between the otherwise isolated qubit donors. This alternative proposal requires the precise placement of two dopant species to control qubit interactions or alternatively the ability to selectively control and address the selection frequency of each donor. The COMPASSS[1] (Coherent Optical Microwave Physics for Atomic-Scale Spintronics in Silicon) program aims to implement the SFG scheme. In the appendix A.4, we demonstrate how the orbital extended state can be exploited to probe the proximity of the surface.

[1] http://www.compasss.net

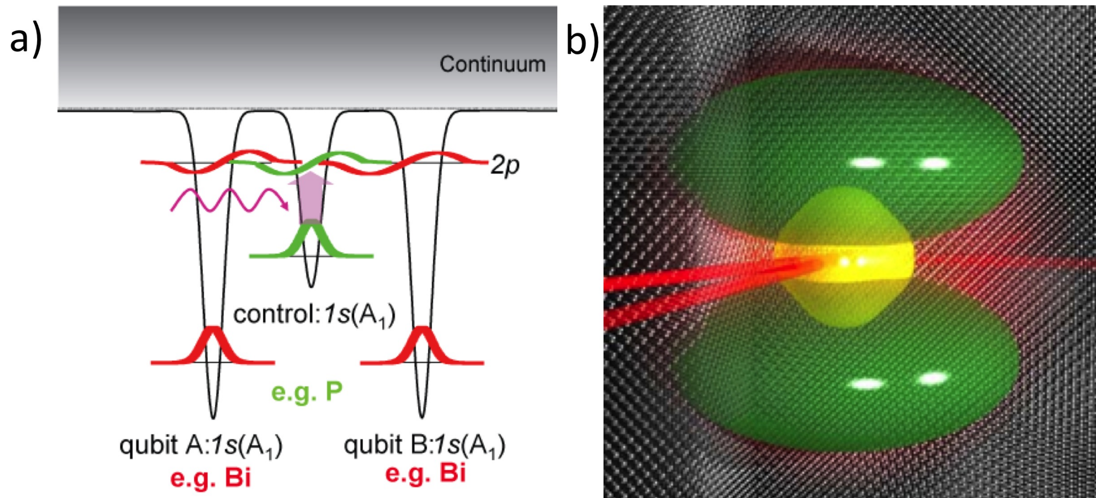


Figure 1.5: Schematic of the SFG-scheme a) The electron spin of each donor atoms serves as a qubit. A control dopant between both qubit donors is optically excited which leads to an spatial extension of the wave function. This turns on a spin exchange interaction of the otherwise isolated qubit electron spins (From [40]).b) Illustration of an donor optically excited by a terahertz pulse (From [41]).

1.2 Characterisation tool for buried δ-layers

Until now, the characteristics of buried dopant nanostructures could only be inferred via indirect and/or destructive techniques, or correlated with the performance of the final electronic device; this severely limits engineering and manufacturing of real-world devices based on atomic-scale lithography. When buried shallow enough ($\sim 20\,\mathrm{nm}$) dopant nanostructures can be resolved via scanning electron microscopy (SEM) which provides enough imaging contrast to determine their position in the xy-plane. Besides inevitably charging the surface region and the patterned nanostructures during electron scanning, SEM can not provide any quantitive or qualitative measure of the device characteristics. Consequently, non-invasive imaging and electrical characterisation of buried nanostructures, with precise lateral and depth resolution, would be of great value for the development and inspection of integrated circuits and quantum devices [2]. These buried nanoscale structures challenge techniques aimed at determining electrical and geometrical properties of subsurface devices. In chapter 6, we use scanning microwave microscopy (SMM) to image and electronically characterise 3D phosphorus nanostructures fabricated via STM-based lithography. The results suggest that SMM could be applied to aid the development of fabrication processes for surface code quantum computers. In chapter 7, we apply three different operational modes of an advanced SMM setup to study buried nanostructures and a powered P nanowire. We demonstrate how an additional DC bias can be employed to extract spectroscopic properties

such as carrier density and contact potential.

In the following, scientific background (chapter 2) and setup (chapter 3) will be briefly introduced for the STM which is the essential fabrication method used in this thesis. Additional theoreticqual background on the silicon substrate and δ-layer properties is summarised. A more detailed introduction and background is provided in the beginning of each results-chapter specifically. The results are presented in chapter 4-7, namely a step by step sample fabrication guide, sample characterisation by transport measurements and SMM studies. The thesis finally concludes with an outlook on possible improvements in the device fabrication strategy and future experiments (chapter 8).

Chapter 2

Methods and scientific background

The essential experimental method used in this thesis is the scanning tunneling microscope (STM) that exploits a quantum mechanical tunneling current to probe both, topographical and electronic properties of metals and semiconductors down to the atomic scale. Since its invention by Binnig and Rohrer in 1982 [44], STM has established itself as invaluable for investigating the real space electronic structure of conducting surfaces. This STM is utilised here as a lithography tool to write atomically sharp features in silicon. The concept and theory of STM is briefly summarised in the following section to understand the fundamental working principle of the method. For an extensive elaboration of the technique is referred to excellent text books [45, 46]. A brief introduction to silicon bulk and its surface properties is presented as well as a literature background on electrical properties of δ-layers.

2.1 Concept of scanning tunneling microscopy

The schematic setup of an STM appears in Figure 2.1a). A very sharp metallic wire (tip) is precisely approached to the surface of a conducting sample. The tip is mounted on a piezoelectric tube, which allows picometer-precise movements in all directions. At a sufficient small tip-sample separation (approximately a few Angstrom), an applied bias voltage between tip and sample allows electrons to travel from the tip through the insulating vacuum gap into the sample or vice versa, depending on the direction of the applied voltage. This transport process occurs despite the fact that the sample and tip are not in mechanical contact, and the electrons do not possess enough energy to overcome the potential barrier between the tip and the sample. This quantum mechanical 'tunneling' effect (see next section) is the origin of this current flow between tip and sample and enables STM.

The tip is scanned line-by-line over the sample in the xy-plane while the tunnel current is recorded. To account for unintended tip crashes with the surface (illustrated in Figure

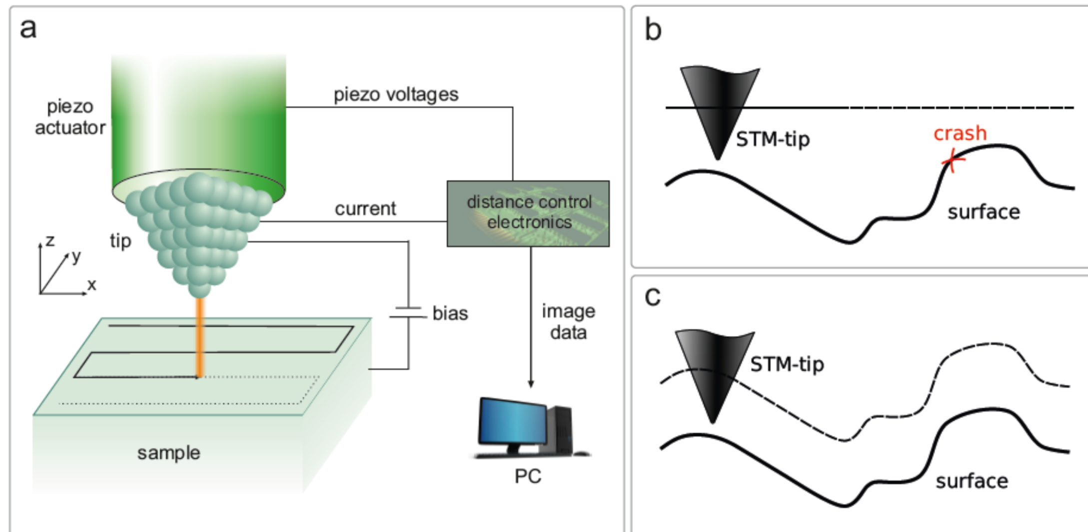


Figure 2.1: Schematic setup of an STM. When the tip is scanned line by line over the sample, whilst the current is measured, an image of the topography is generated. The tip is actuated by piezoelectric tubes, which allow picometer-precise movements (from [47]).

2.1b)), the current is set to a constant value (Setpoint current) whilst scanning. To maintain a constant current value, the z-movement of the tip is controlled via a feedback loop that responds to local variations of the current flow between tip and surface by applying a voltage to the z-piezo. The applied voltage serves to withdraw (extend) the tip from (to) the surface such that the current is kept constant. In this 'constant current' operation mode, the physical changes in tip-height to maintain a constant current value are rendered as a two-dimensional topography image of the surface. The term 'topography' is a bit misleading since topographic and electrical characteristics of the surface are contained in the signal. In the second main 'constant height' operation mode, the z-axis (height) is kept at a constant value and from the varying tunneling current an image is generated, sketched in Figure 2.1c).

2.1.1 The tunnel process

To understand the quantum mechanical tunneling process, the wave-like nature of a particle has to be taken into account to describe the non-classical propagation of an electron through a vacuum barrier such as the gap between a tip and sample surface. In the wave picture, a free particle with mass m and energy E is described as a wave function with a probability distribution $\psi(z)$. For a simple description of the quantum mechanical tunneling we use a one-dimensional (1D) tip-sample model (Figure 2.2) where the height of a piecewise potential $U(z) = \Phi$ for $0 \leq z \leq D$ and zero outside, is equal to the work function of the

sample Φ_S and the tip Φ_T. The particle solution of the 1D-time-independent Schrödinger equation in the classical forbidden region $0 \leq z \leq D$, as depicted in Figure 2.2b), is given as

$$\psi(z) = \psi(0)e^{-\kappa z} \quad , \quad \text{where} \quad \kappa = \frac{\sqrt{2m(U-E)}}{\hbar} \tag{2.1}$$

is the decay constant and $\hbar$ is the Plank constant. Assuming the applied bias $eV << \Phi$ then $U - E \simeq \Phi$. Hence, the amplitude of the quantum mechanical wave function $\psi(0)$ decays exponential along z into the vacuum (see Figure 2.2b)) and the strength of the decay is mainly determined by the barrier height Φ.

Before applying a positive voltage to the sample, the Fermi level E_F of sample and tip

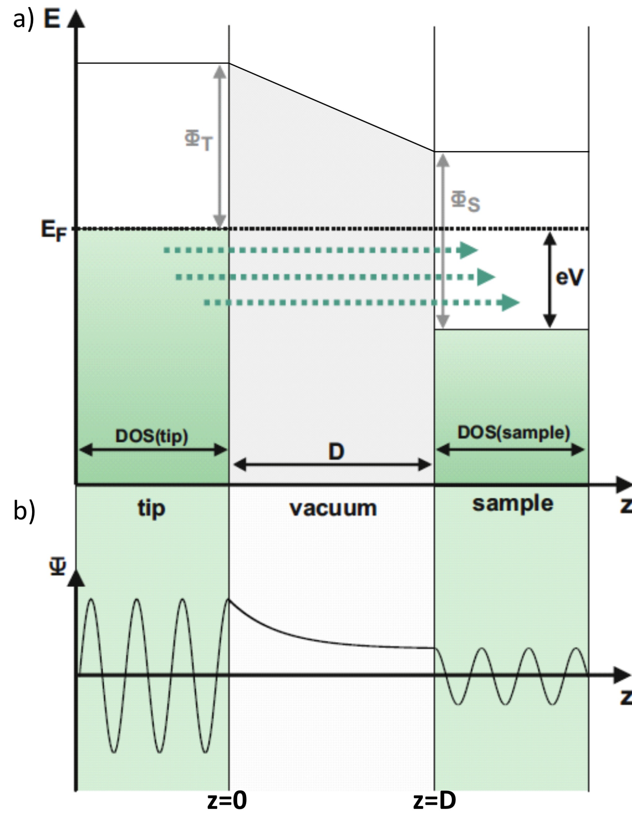


Figure 2.2: a) Energy diagram of the tip-sample junction. Work function Φ_T of the tip and the sample Φ_S form a trapezoidal barrier of width D. b) The propagating incoming wave ψ is oscillating within the classically allowed region and decays exponentially into the classically forbidden barrier. Beyond the vacuum barrier the oscillating continues with smaller amplitude (slightly modified from [47]).

are aligned on the same level. The applied bias voltage shifts the Fermi level of the sample down and accordingly all states in the energy interval eV contribute to the tunnel current as indicated in Figure 2.2a).

The estimated tunneling current I_T at the sample surface is directly proportional to the sum of all states within the energy interval eV by

$$I_T \propto \sum_{E_n=E_F-eV}^{E_F} |\psi_n(D)|^2 = \sum_{E_n=E_F-eV}^{E_F} |\psi_n(0)|^2 e^{-2\kappa D}\,. \tag{2.2}$$

The main reason for the atomic resolution of an STM is the strong dependence of the tunnel current on the distance between sample and tip. The decay of current is exponential in z, which means that a change of 1 Å in distance, results in a current change of about one order of magnitude (assuming a work function $\Phi_{\text{eff}} \approx 5\,\text{eV}$ [46]). To understand a bias dependent current flow we have to consider the availability of states in the sample that can be occupied by electrons ρ_S, referred to as the local density of states (LDOS). For a metallic tip the LDOS are considered to be constant in energy and neglected in this simple model. For small bias variations ε, such that the density of states does not vary significantly, the LDOS of the sample is defined [46] as

$$\rho_S(z,E) := \frac{1}{\varepsilon} \sum_{E_n=E-\varepsilon}^{E} |\psi_n(z)|^2\,. \tag{2.3}$$

We can express Equation 2.3 in terms of the LDOS of the sample at the Fermi level and at the position of the sample surface by

$$I_T \propto \frac{1}{\varepsilon} \sum_{E_n=E_F-\varepsilon}^{E_F} |\psi(D)|^2 \cdot eV = \rho_S(D,E_F) \cdot eV\,. \tag{2.4}$$

According to this simple one-dimensional model the STM effectively probes the LDOS of the sample surface at the Fermi level by scanning the tip at a constant current. When the electrons tunnel from the tip into the empty states of the sample as depicted in Figure 2.2a), the STM acquires an image of the unoccupied states of the sample (empty states imaging). In opposite bias direction, the electrons tunnel from the filled states of the sample into the tip (filled state imaging).

For the model we have assumed small bias voltages, constant tip LDOS and no thermal contributions to the occupation of states. A more sophisticated theoretical description of the tunnel current like the modified Bardeen approach of Tersoff and Hamann [48], shows qualitative agreement with this simple 1D-model and will not be discussed here.

2.2 Silicon bulk and surface properties

Silicon is the most commonly used material in the semiconductor industry due to is thermal stability and its ability to control the amount of free carrier via impurity doping which determines the conductive properties of devices. As a consequence, the group-4 element has been studied extensively for the development of micro-electronic components such as transistors and processors. When forming a crystal structure, each atom develops covalent bonds to four neighbouring atoms by hybridising into sp^3 orbitals. This results in a diamond type face-centred-cubic (fcc) Bravais-lattice structure with a two-atom basis (positions at (0,0,0) and ($\frac{1}{4}$,$\frac{1}{4}$,$\frac{1}{4}$) Miller indices) [49].

All work in this thesis has been performed using the Si(100) surface as a sample substrate. A suitable flat silicon Si(100) surface for STM experiments is obtained by cutting the crystal along the (100) plane. Figure 2.3 displays a schematic with the principle orientations of a silicon surface. Note that (100) and (001) are crystallographically equivalent notations. The ideal Si(100)-1×1 surface is illustrated for a perfect cut along the (100) plane,

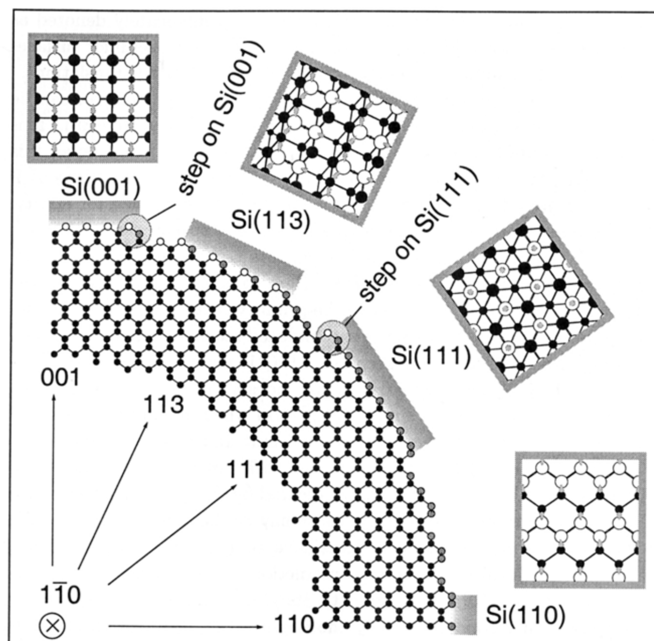


Figure 2.3: Schematic view of the possible low index faces of of Si. Surface atoms are white, bulk atoms black and dangling bonds are gray (from [50])

shown in Figure 2.4a). Each atom on the surface of this ideal crystal structure exposes two broken bonds, due to missing neighbouring Si atoms, making it highly reactive and energetically unfavourable by causing a large free energy. The half filled sp^3 orbital that is protruding from the surface are referred to as 'dangling bond' (DB). The atoms undergo a

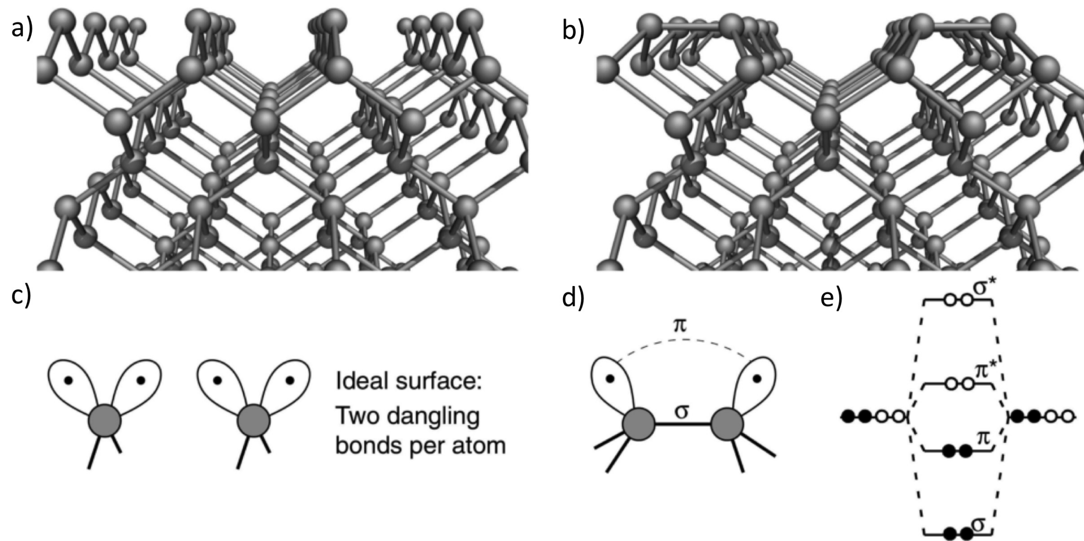


Figure 2.4: Schematic of the ideal and reconstructed Si(001) surface. (a) The ideal Si(001)-1×1 surface (b) and after surface reconstruction forming Si(001)2 × 1. (c) Each atom of the ideal Si(001) surface has two dangling-bonds. (d) Si atoms pair up to form σ-bonds, and a weakly coupled π-bond. (e) Energy level diagram showing the interaction between the four dangling bond orbitals of two Si atoms, producing two bonding orbitals, σ and π, and two anti-bonding orbitals, σ^* and π^* (from [51]).

rearranging process to minimise the free energy by reducing the DB density which leads to a reconstructed super-structure. This process is called 'reconstruction'. The 2×1 surface reconstruction is formed when two surface atoms pair up to form a direct σ-bond and a weakly coupled π-bond [52], shown in Figure 2.4b). The terminology $m \times n$ (*e.g.* in Si (100)-2×1) refers to the unit cell (unit mesh) in terms of bulk lattice vectors. These silicon dimer display a characteristic row formation on the surface with one DB per surface atom. In addition to the σ- and π-bonds, σ^* and π^* anti-bonding states are emerging at higher energies in the energy level diagram, shown in Figure 2.4e). Note that the equivalent σ-bond and σ^*-bond states in bulk silicon correspond to the valance band and conduction band edges of silicon bulk.

2.3 Electrical properties of δ-layers

This section summarises electrical properties obtained from published theoretical calculations of both δ-layers and lithographically defined P nanowires by focusing on the effect of varying donor density, 2D confinement and temperature on their band structure.

Lightly doped semiconductor such that the Fermi level lies within the $3k_B$T range from the band edges, are called non-degenerately doped semiconductor [53], like the silicon bulk

substrate of our devices ($n_{bulk} = 2.5 \times 10^{14}\,\text{cm}^{-3}$). At low temperatures the carriers in non-degenerately doped silicon freeze out and the substrate becomes insulating. Instead, bulk doping above the metal-insulator density ($n_{\text{MIT}} \sim 3 \times 10^{18}\,\text{cm}^{-3}$ [54]) results in an overlap of the donor wave functions which leads to the formation of impurity bands.

For PH_3 saturation δ-doped silicon, typical 0.25 ML of P coverage equals an average dopant separation of $d_p < 1\,\text{nm}$ which is smaller than the Bohr radius of a single donor ($a_B \sim 2.5\,\text{nm}$ [42]), giving rise to 2D impurity sub-bands with quantised energy levels. Experimentally, the electronic band structure was identified by using resonant tunneling spectroscopy [55, 56] and angle resolved photo emission spectroscopy (ARPES) [57, 58]. Various theoretical studies have been published using different modelling methods to compute the electronic band structure of δ-layers buried in silicon, such as density functional theory (DFT) and pseudo-potential methods [38, 59–65].

Lee and Ryu *et al.* used a fully atomistic theoretical treatment by applying the tight-binding code NEMO-3D [66] to understand the impact of vertical and in-plane donor placement in 2D δ-doped sheets on electron transport. The band structure of δ-doped layers and lithographically defined wires were calculated by taking into account both the high dopant density and discrete nature of the doping [38, 67]. From the energy dispersion relation $E(k)$ of the band structure it is possible to determine the number of the impurity sub-bands and the density of states (DOS) below the Fermi energy. The electron occupation of these sub-bands during transport together with the mobility of the carriers mainly govern their conductance. Figure 2.5a) compares the equilibrium band structure of a 0.25 ML P δ-doped layer plotted together with the band structure of the pure silicon structure (without δ-layer) in [110] and [100] direction. It was found that the δ-doped layer creates a sharp electrostatic V-shaped confinement in the z-direction (as displayed in Figure 2.5b)). The screened donor potential creates a very narrow quantum well, where 96% of the charge is confined vertically within 21 monolayers ($< 3\,\text{nm}$) from the donor positions, leaving the donor charges in the δ-doped layer highly screened [38]. The high attractive potential of the dopants pulls down several silicon bands from the conduction band into the band gap. Hence, the 2D band structure of the δ-layer exhibits two Γ- and one Δ-valley below the Fermi level, creating a set of donor impurity bands at $E_{1\Gamma} = -401\,\text{meV}$, $E_{2\Gamma} = -375\,\text{meV}$ and $E_{\Delta} = -249\,\text{meV}$, respectively [67]. These sub-bands and the Fermi level ($E_F = -115\,\text{meV}$) reside well under the silicon bulk conduction band minimum (CBM). The sub-bands can be understood as the

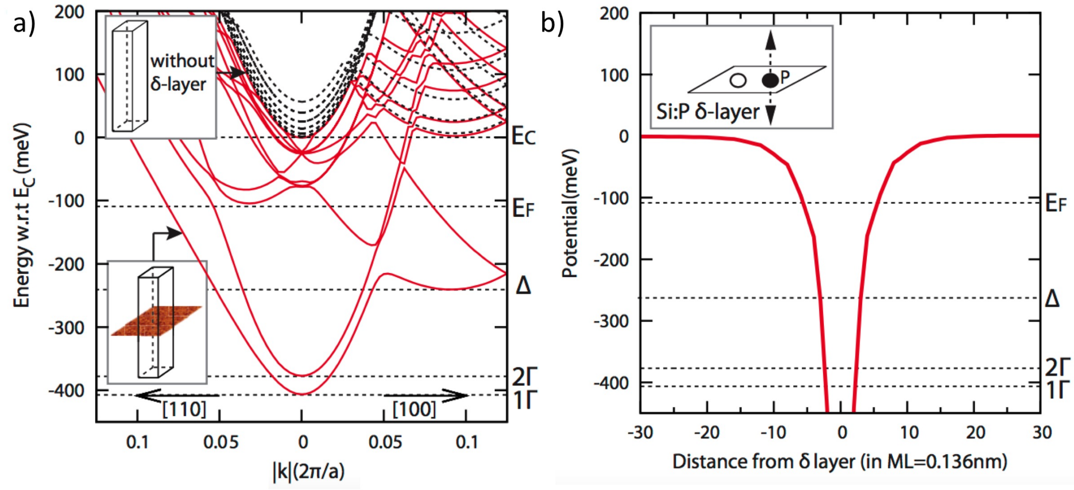


Figure 2.5: (a) Bandstructure of the 0.25 ML-doped Si:P 2D d-layer: (a) the equilibrium bandstructure of a 0.25 ML-doped 2D Si:P δ-layer where the Γ, Δ-valleys are observed below the Si bulk CBM. (b) sharp V-shaped potential profile plotted along confinement direction ([001]) passing through impurity site (from [38]).

projection of the six bulk silicon conduction band valleys into the xy-plane. For example along the [001] direction the two out-of-plane Si bulk conduction band ellipsoids at the Γ point ($k = 0$), marked in dark colour in Figure 2.6, are projected into the $k_x - k_y$ plane. They form the 1Γ and 2Γ sub-bands and exhibit a valley splitting (VS) of $\sim 26\,\text{meV}$ [67] due to their strong confinement in z. From the four Δ-valleys parallel to the (001) plane only one

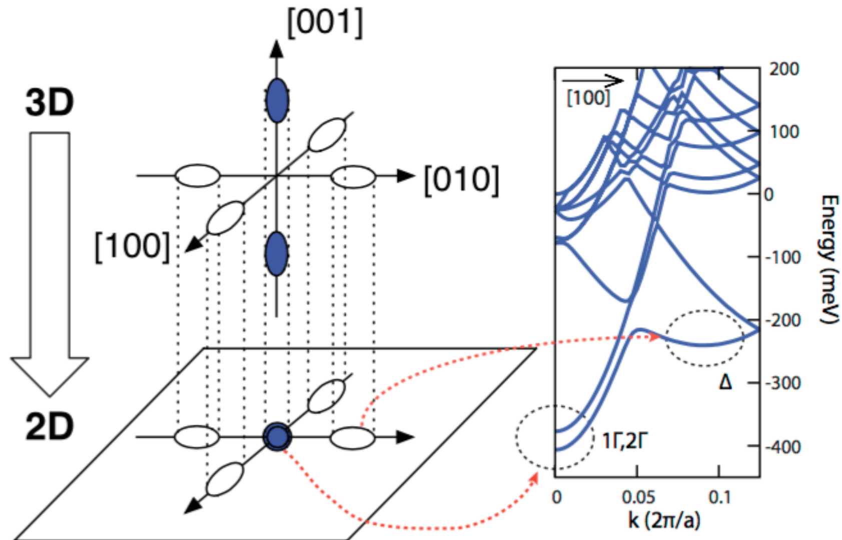


Figure 2.6: Band projection diagram for the highly confined 2D δ-layers. Two valleys (dark) along the z-confinement direction and one Δ-valley parallel to the (001) are projected to the Γ-point and Δ-valley into the $k_x - k_y$ plane (from [38]).

is observed in the [100] direction.

2.3.1 Sensitivity to dopant density and disorder

The position of the δ-layer valley minima is critically dependent on the dopant density within the δ-doped sheet. With increasing dopant density the electrostatic potential enhances and more electrons have to occupy the sub-bands to maintain charge neutrality [38]. The stronger electrostatic attraction of the screened Coulomb potential leads to a higher confinement of electrons in the δ-layer plane, causing an increase in VS and a further downshift of the sub-bands, as shown in Figure 2.7a). A random in-plane disorder was found to cause

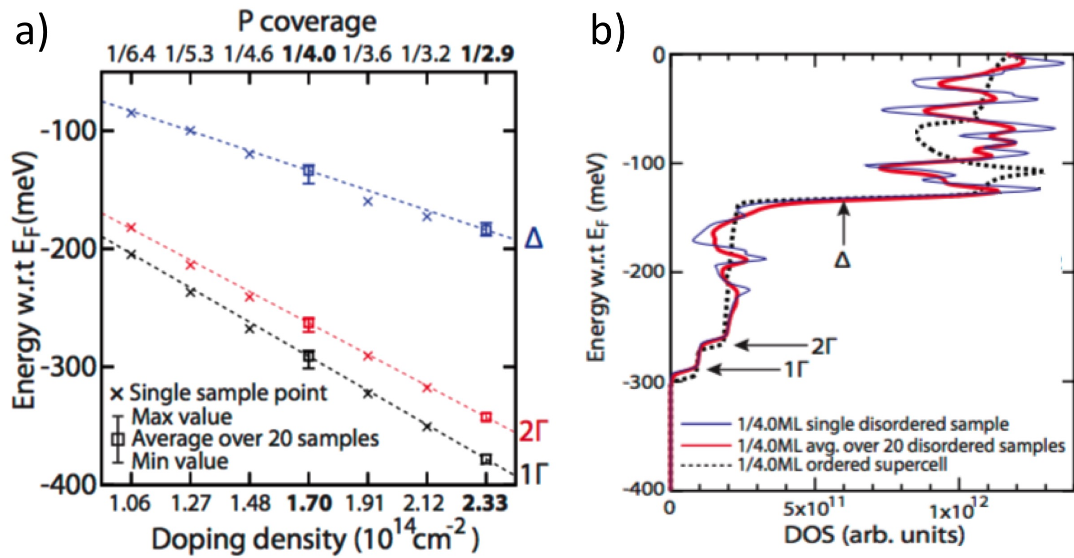


Figure 2.7: a) Valley minimum values of different doping densities plotted with respect to the Fermi level. b) DOS comparison between ordered (dashed line) and disordered Si:P δ-doped layers (solid lines). For disordered cases, the DOS for single sample (blue) and the DOS averaged over 20 samples (red) are indicated.(From [38])

only little change in the positions of the 1Γ-, 2Γ- and Δ-valleys as can be seen in the DOS comparison between ordered (dashed line) and disordered δ-doped layers (solid lines) in Figure 2.7b). The sudden increase in DOS at $E \sim -130\,\text{meV}$ results form the turn-on of the Δ-band which provides a much higher density of electron states due to its larger effective mass compared to the Γ-bands ($m_l = 0.91 m_e > m_t = 0.19 m_e$).

2.3.2 Vertical dopant spreading

Lee *et al.* also modelled the effect of vertical dopant spread on the δ-layer sub band energy and their VS which provides an estimation of the electrical confinement in z, depicted in Figure 2.8. Dopant segregation occurs during Si encapsulations and results in a reduced

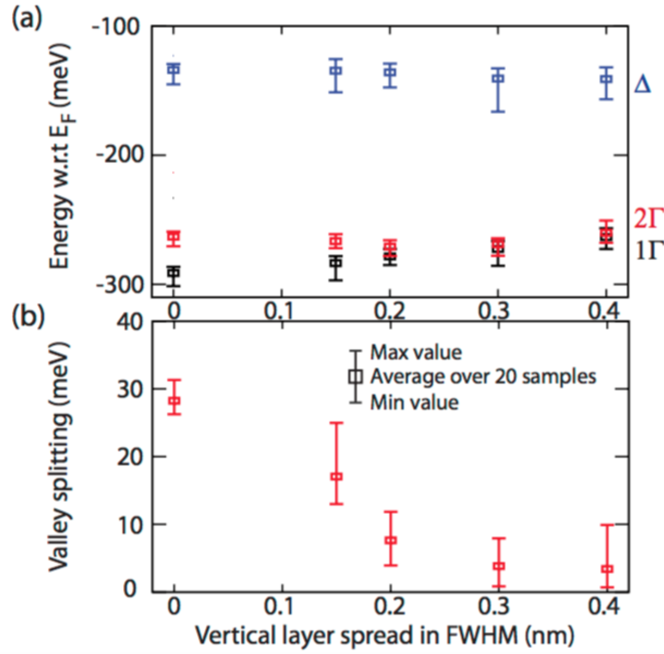


Figure 2.8: (a) 1Γ, 2Γ and Δ valley minimum values are plotted with respected to the Fermi level vs vertical impurity segregation. Statistical samples of vertical segregation of dopant atoms with a nominal 0.25 ML doping is considered. (b) Valley splitting as a function of vertical segregation (From [38])

confinement of the originally in-plane dopant profile. They used a gaussian distribution to model the dopants spread with a varying full width at half maximum (FWHM) profile, assuming a vertical segregation of no more than 7 ML (or 0.81 nm). A vertical dopant spreading results in a reduction of dopant density in the layer which allows the impurity bands to rise slightly in energy (compare with Figure 2.8a)) and leads to a significant decrease in VB of the Γ-valleys. By the time, the maximum limit of vertical segregation of δ-doped layers encapsulated at low temperatures of 250 °C has been experimentally determined to be 0.58 nm [68]. Based on new data on δ-doped silicon [69] and our own observation from δ-layer dopant profiles obtained with SIMS, these values are too small and a larger spreading would result in an increasing rise in impurity band energy.

2.3.3 Room-temperature characteristics

For experiments on δ-layers at room-temperature (300 K), their impurity sub-band characteristic behaviour at elevated temperatures is of critical importance. The temperature dependence of the charge screening in P δ-doped layers is described in [70] using again the tight-binding code NEMO-3D. Calculation suggest that the position of the δ-layer donor-

band minimum is only slightly shifted compared to low temperature (4.2 K) e.g. for Γ_1 being still situated at -367 meV with a Fermi-level located at -87 meV. In addition, calculations from Hwang *et al.* suggest that phonon scattering plays a small role at RT due to a high Fermi temperature ($T_F \sim 700$ K) at densities of $\sim 10^{14}$ cm^{-2}. Impurity scattering still dominates the mobility even at RT [71]. This is promising for δ-layer transport experiments at RT where conduction in the band gap can be expected via donor impurity bands.

2.3.4 Nanowire

Theoretical calculations for a 1.5 nm wide P nanowire point out the effect of a reduced electrostatic potential on the donor sub-band energy due to the narrower doping region, depicted in Figure 2.9. With the reduction of physical dimensions the bands of the nanowire reside closer to the Si bulk CBM as compared to the 2D planar doping. Stronger quantisation of the energy levels results in a total of two Γ and two Δ-valleys in the [110] transport direction and an increase in VS. The DOS profile in Figure 2.9 exhibits multiple peaks at

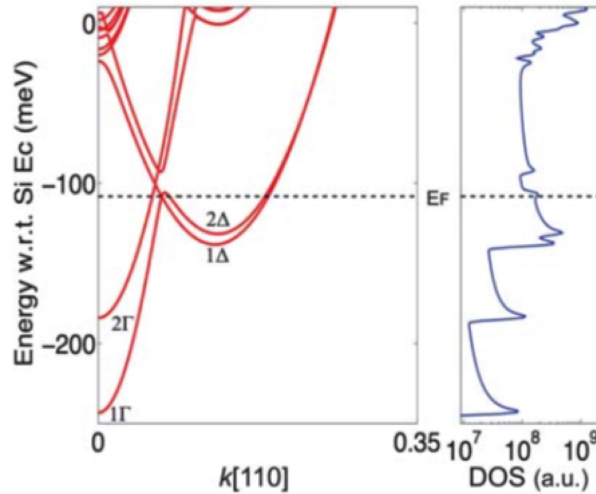


Figure 2.9: (Band structure and DOS profile of the 0.25 ML-doped, 1.5 nm wide Si:P nanowire oriented along the [110] direction: (a) the equilibrium bandstructure and DOS profile of a 0.25 ML-doped, 1.5 nm wide [110]-oriented Si:P nanowire. Donor bands are shown below the Si bulk CBM (From [67])

sub-band minima indicating that even for 1.5 nm wide P wire the 0.25 ML doped channel is metallic [28]. With decreasing dopant density the Fermi-level shifts closer to the donor band minimum until the heavy Δ-valley is completely depleted at a doping density of 0.0156 ML ($\sim 10^{13}$ cm^{-2}) [67]. These theoretical calculations have been experimentally verified [28, 30] and it could be shown that the channel resistance fluctuations due to dis-

order in the channel are not high enough to stop electron propagation [28]. These result demonstrate that the metallic behaviour of these 2D δ-doped nanowires is stable enough to serve as Ohmic interconnects and gates for the control of atomic-scale devices in quantum computing architectures.

Chapter 3

Experimental setup

3.1 Setup of variable temperature scanning tunnelling microscope

The setup for the complex sample fabrication was an ultra-high vacuum (UHV) Omicron variable temperature scanning tunnelling microscopy (VT-STM) system [72]. It was used for the preparation of flat Si(100)-(1×2) and for subsequently performing STM H-lithography. An overview of the current setup appears in Figure 3.1 which consists of three major parts, the load-lock, the preparation chamber, and STM chamber with the actual STM unit. In preparation and measurement mode the STM and preparation chamber are continuously pumped by ion pumps and titanium sublimation pumps, enabling noise re-

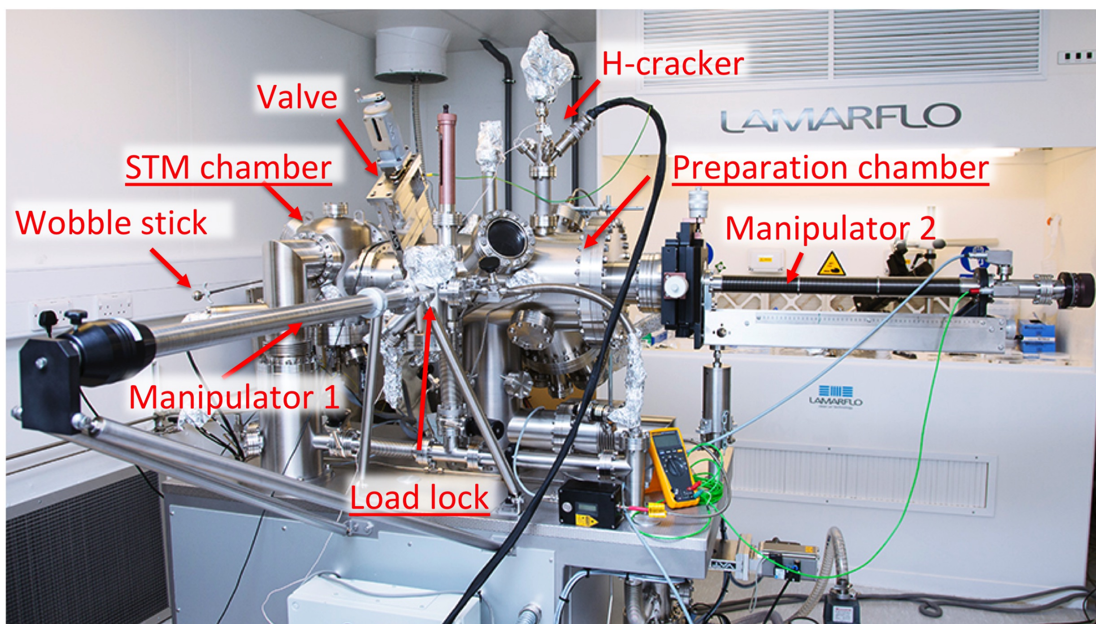


Figure 3.1: Overview of the Omicron VT-STM system with its three major parts: Preparation chamber, STM chamber and load lock.

duced measurements while effectively pumping. In addition, the UHV-mounting frame was standing on eight active damping units, which canceled out low frequency oscillations, while high frequency oscillations were suppressed by the passive magnetic damping in the VT unit stage. A sequential set of pumps, starting with a rotary pump and a turbo pump created a pre-vacuum, allowing the load lock to be purged separately. The preparation chamber can be separated from the STM chamber via a gate valve to prevent contamination of the STM and the ion pump during sample preparation. The sample was loaded into the preparation chamber and from the preparation chamber into the STM chamber using an x,y,z-manipulator, that can be rotated 180°. A Tectra hydrogen cracker unit provided atomic hydrogen for an efficient silicon passivation. The preparation chamber was equipped with an Impac pyrometer for temperature control of the sample and a sublimation silicon source (SUSI) from MBE Komponenten to encapsulate patterned samples with silicon of extreme high purity (see Figure 3.2a)). After sample preparation the sample holder was transferred into the STM chamber which was equipped with a long-distance microscope for a precise tip positioning on the sample. A capsule filled with PH_3 was attached to the VT chamber and a leak valve enabled precise dosing onto the silicon substrate surface (Figure 3.2b)+c)).

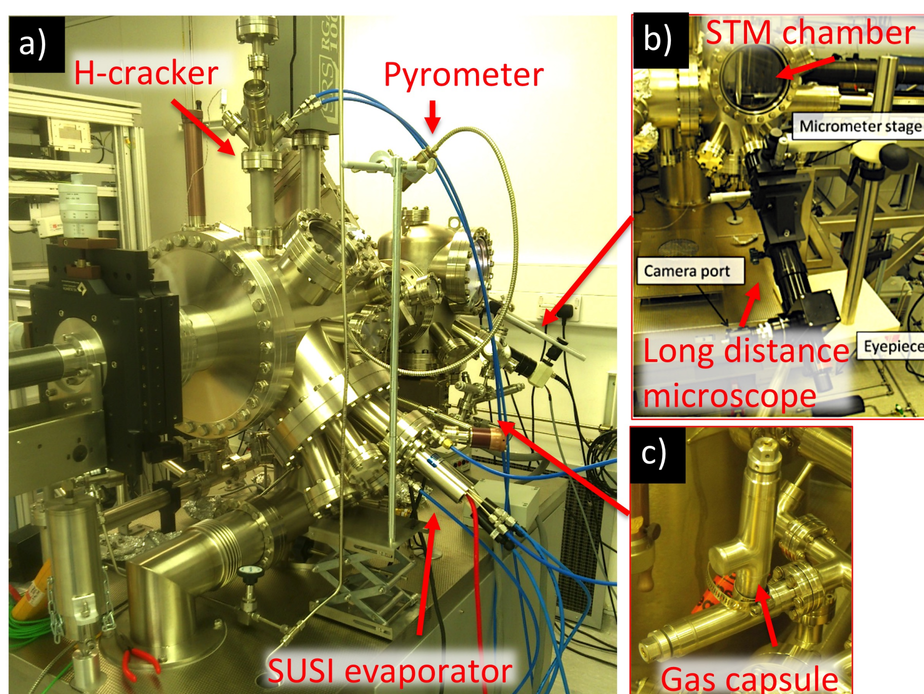


Figure 3.2: a) Side view on the VT-STM system which is equipped with a hydrogen cracker unit, a pyrometer for temperature control of the sample and a silicon sublimation source (SUSI). b) A long-distance microscope for high precision tip alignment and c) a PH_3 gas capsule is mounted on the VT STM chamber (From [73]).

The Omicron VT scan head including the magnetic damping system is shown in Figure 3.3a). A 'carousel' situated at the front part of the STM chamber provided storage space for up to 12 tip or sample holders. After tip and sample have been transferred into the VT-STM stage using a wobble stick, the tip can be automatically approached using shear stack piezos for coarse motion and the Omicron piezo-tube step motor for fine tip movements, shown in Figure 3.3b). The available fine piezo scan area was approximately $18\,\mu\text{m} \times 18\,\mu\text{m}$. The

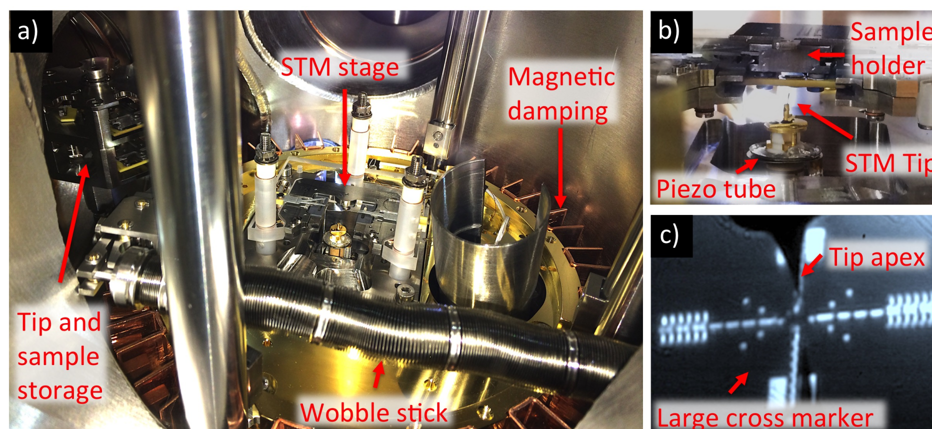


Figure 3.3: a) VT-STM scan head, b) side view of a loaded sample holder inside the STM stage and c) view through the long-distance microscope onto the sample surface comprising a fiducial etched marker system for tip alignment (From [73]).

STM control and measurement software used for scanning and lithography was Matrix 3.1 as well as 'Zyvector' from Zyvex labs.

Figure 3.3c) depicts the view though the long-distance microscope onto the sample comprising deep etched large fiducial cross markers for a high precision tip alignment. The tip apex is positioned over the centre of the large alignment cross and after approaching the surface, the electron beam of the tip can be utilised to break H-Si bonds on a passivated silicon surface to pattern nanostructures of arbitrary shape.

STM tips were prepared by an in-house electrochemical etching from 99.98% pure polycrystalline tungsten wire with a diameter of $d = 0.25\,\text{mm}$. Sharp tungsten tips with a hyperbolic cone shape can be made by electrochemical etching in potassium hydroxide (KOH) solution [74, 75]. Once introduced into UHV the tip was outgassed overnight at $\approx 150\,^{\circ}\text{C}$ and during STM measurements further treated by tip voltage pulses up to $U = 8\,\text{V}$ to obtain highest imaging resolution.

Chapter 4

Development of an STM hydrogen lithography device fabrication strategy

4.1 Introduction

In the endeavour of continuing miniaturisation of electric elements in the semiconductor industry but also for the fabrication of devices for the quantum information technology, control over the location of individual atoms is a desirable requirement for future fabrication and characterisation tools. Scanning probe microscopy (SPM) is the only method that offers atomically precise characterisation and manipulation of single atoms on semiconductor surfaces. To exploit the unprecedented resolution of SPM for device fabrication, a deposition strategy has been developed to control atomic precise donor placement in silicon. Using STM hydrogen (H) lithography Schofield *et al.* [24] demonstrated that a single phosphorus (P) atom can be placed in silicon (Si) with near atomic precision. The fundamental procedure that provides atomically precise control of P donor placement in silicon using STM hydrogen lithography is illustrated in Figure 4.1. In the placement process atomic hydrogen atoms on a passivated Si(100)-2$\times$1 surface are selectively desorbed by the electron beam of the STM tip [76] (see 1. in Figure 4.1). Exposing the patterned surface to a background pressure of PH_3 results in adsorption of the PH_3 molecules exclusively within the depassivated regions [77, 78] (see 2. in Figure 4.1). An activation anneal *e.g.* for 2 min at 350 °C incorporates the P atoms into the silicon lattice (see 3. in Figure 4.1) while a subsequent Si encapsulation prevents the nanostructures from oxidation. (see 4. in Figure 4.1). This procedure allows patterning of arbitrary dopant structures below silicon surfaces. To utilise hydrogen lithography methods for device fabrication, contacts and gate electrodes have to be fabricated ex situ in a cleanroom environment and aligned to the buried STM patterned

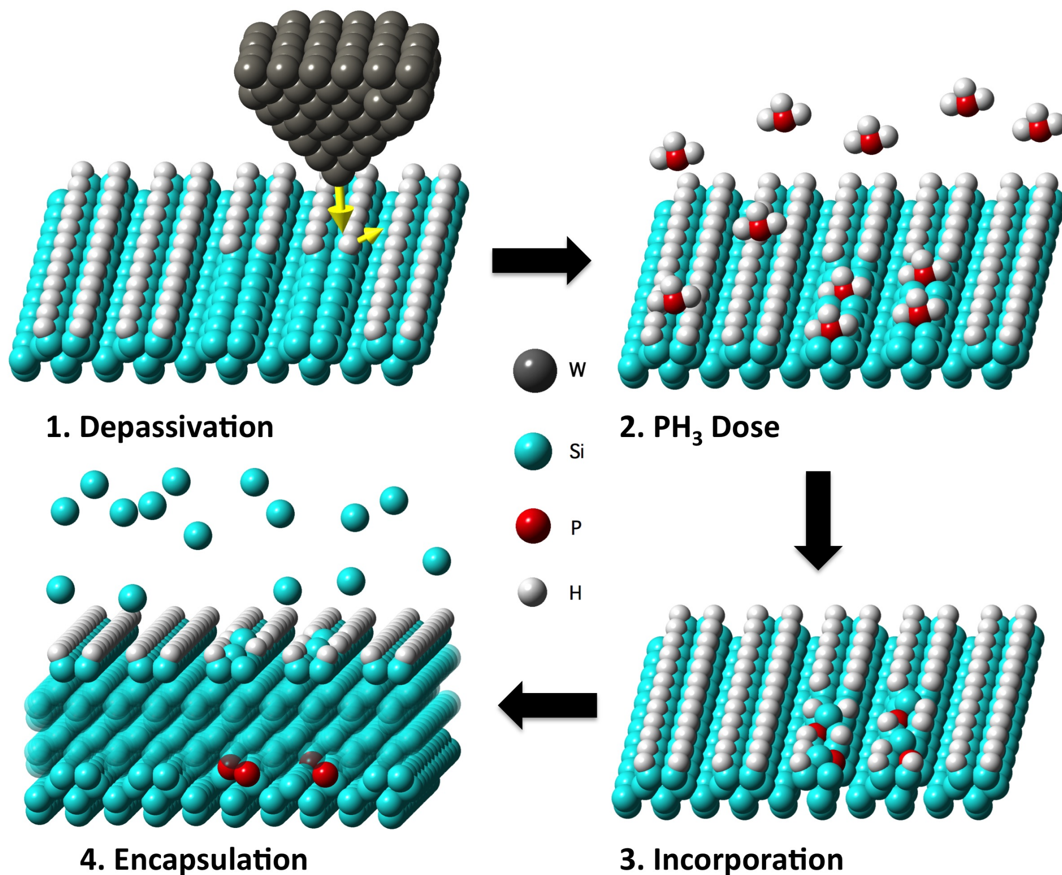


Figure 4.1: STM hydrogen lithography process 1) Hydrogen depassivation: An electron beam from an STM tip depassivates the H-terminated Si(100) surface 2) PH_3 Dose: Adsorption of the PH_3 molecules exclusively within the depassivated regions 3) Incorporation: Annealing the sample to 350 °C incorporates P into silicon lattice 4) Si overgrowth: Donor nanostructure is encapsulated with silicon via molecular beam epitaxy.

P nanostructures (further labelled 'patterned nanostructures'). Different approaches have been undertaken to contact STM patterned devices outside UHV [79–87]. In fact, contacting buried patterned nanostructures of atomic scale to macroscopic contacts on the silicon surface has been reported to be very challenging [79, 85, 86, 88, 89] due to a very high alignment accuracy and the requirement of ultra-high vacuum (UHV) compatibility of the device fabrication strategy.

In addition, the relocation of written features in UHV after re-approching the surface between various STM fabrication steps needs to be facilitated. Thus, the employment of a marker system on the micron scale is crucial. Several pre-patterned methods to facilitate marker systems on the silicon surface have been investigated, including the deposition of different metals such as nickel [90, 91], microscopic patterns of titanium disili-

cide ($TiSi_2$) [80, 81], metallic marks of cobalt and tungsten (W) [79, 84], silicon nitride (SiN) [79], and the deposition of gold (Ag) [82, 83]. A strong requirement on the strategy is thermal stability of the pre-patterend marker system. The standard silicon UHV surface preparation procedure to obtain an atomically pristine and flat reconstructed Si(100)-2×1 silicon surface on large length scales involves heating steps to $\sim$ 1250 °C. At these high temperatures, the native oxide sublimates from the surface and carbon contamination is removed [92]. Even high melting point materials (*e.g.* titanium) that survive the subsequent high-temperature anneal display significant diffusion on the Si(100) surface (up to 500 nm) when annealed to 900 °C [80, 81]. As a result, metal markers were found to deteriorate the surface at the atomic scale, causing either an undesirable 2×n surface reconstruction (*e.g.* induced by already small amounts of nickel contamination [93]) or the formation of trenches around the metal marker along with a high defect density on the surface [80,84,94]. Another method for pre-UHV marker deposition employs ion implantation [85, 86] and the integration of both metal alignment marks and ion-implanted contacts [87] that attracted a lot of interest in the recent years. In general, the use of pre-patterned ion-implanted markers require a low temperature sample preparation process in UHV ($\sim$ 700 °C), which reportedly results in an insufficiently low surface quality, unsuitable for STM lithography [85, 86]. However, a modified pre-UHV cleaning procedure in conjunction with a modest 800 °C anneal in UHV for oxide removal, has been recently developed that demonstrates reproducible preparation of atomically clean silicon on small length scales and low surface contamination [87].

One of the most successful STM device fabrication strategies, initially developed by Ruess *et al.* [88], employs a deep etched marker system defined by electron beam lithography (EBL) or photo lithography to relocate and electrically contact the patterned nanostructures. Electrical measurements have proven that the fabrication scheme is a robust and successful way to contact buried patterned nanostructures ex situ, resulting in first STM fabricated dopant structures, such as wires [26, 28, 95], quantum dots [96] and more recently single donor [30] and few donor devices [31]. Pre-patterning the initial silicon surface with a deep etched marker system strategy is compatible with UHV, although the flashing process does slightly distort the shape of the markers due to step migration in silicon at elevated temperatures [73, 88]. Contamination of the sample substrate induced in the pre-UHV marker fabrication is a general concern for the quality of the silicon surface and performance of the

final device. EBL and photo lithography processes typically require the use of an organic resist, which in turn is a source of carbon. It is well known that residues of carbon causes strong pinning on the Si surface [51, 97, 98], and hence it is critical to completely remove any traces of resist before loading the sample into UHV system to avoid surface contamination. Thus, in order to exploit high resolution STM patterning for device fabrication, the criteria for the fabrication strategy are (i) UHV compatibility and (ii) thermal stability of deep etched marker to survive high temperature silicon preparation steps. (iii) The marker system should enable us to locate the active writing area in the STM chamber and (iv) provide a subsequent high precision EBL alignment. (v) The marker fabrication procedure should not introduce any type of contamination to the substrate. (vi) In addition, the ex situ contacting procedure should produce devices of good ohmic conduction down to the buried patterned nanostructures.

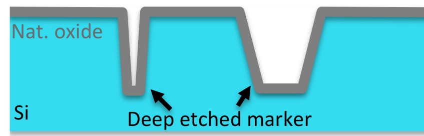
In this chapter a detailed complete description of the STM device fabrication strategy we have developed is presented, which is based on previous strategies developed at the University of New South Wales (UNSW)) [88] as well as initial PhD work from Philip Studer at UCL [73]. The successful implementation of this STM device fabrication strategy at the London Centre for Nanotechnology (LCN) led to the fabrication of a variety of devices during the course of this work.

Parts of the fabrication strategy are to be included in the supplementary materials section of a paper due to be submitted on electrically detected orbital excitation of P dopants in a silicon δ-layer [Matmon, Koelker *et al.,* to be submitted].

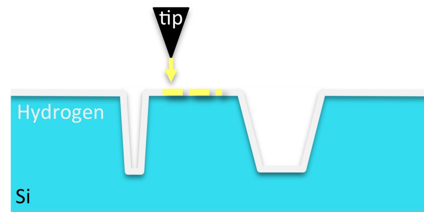
4.1.1 Process flow of the fabrication strategy

The process flow of our fabrication strategy steps are schematically shown in Figure 4.2. In the first fabrication pre-UHV step (1), a fiducial marker system is deep etched into the silicon wafer substrate. The fiducial marker system enables us to position the STM tip into the active writing area and allows a subsequent precise EBL alignment for electrical contacting. Studies have shown that markers etched deeper than > 300 nm survive the high temperature anneal steps required for STM lithography fabrication [73, 88]. Despite a smearing out of the edges due to enhanced silicon diffusion, the deep etched marker are still well resolvable for EBL alignment and produce sufficient contrast for identification in the scanning electron microscope (SEM) [73, 88]. Thus, we aim for an optimal marker depth of ~ 350 nm. In the second fabrication step (2), the diced samples are introduced to UHV, cleaned by flash an-

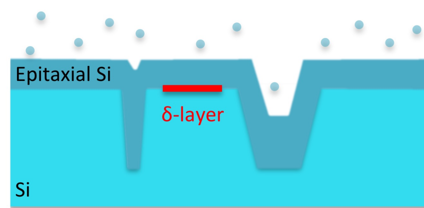
1. Pre-UHV: Marker fabrication



2. UHV: Cleaning and STM-hydrogen lithography



3. PH_3 dosage, incorporation and Si encapsulation



4. Post-UHV:-Contacting and wire bonding

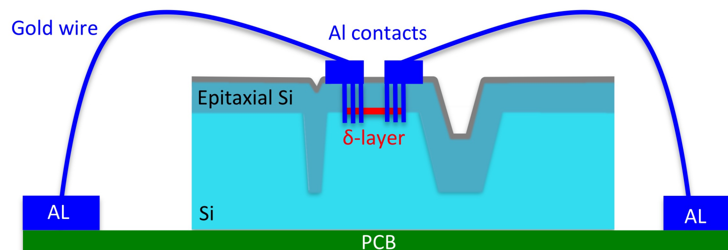


Figure 4.2: Schematic process flow of the fabrication strategy steps, consisting of: (1) the fabrication of a pre-UHV fiducial marker system,, (2-3) STM H-lithography and the deposition of phosphorus in UHV and (4) a post-UHV contacting process.

nealing procedure at high temperatures and the marker system is used to position the STM over the active writing area. Subsequently, nanostructures are patterned onto the silicon surface using STM H-lithography. The third step (3) involves the deposition of phosphorus by employing PH_3 as precursor exclusively adsorbing in previously patterned regions. After P activation and incorporation, the nanostructured δ-layer is encapsulated with layers of epitaxial silicon deposited from a silicon sublimation cell. The sample is unloaded from UHV and in the fourth step (4), the buried patterned nanostructures are electrically contacted to the outside world using deep etched vias and the aligning of macroscopic Al contacts on the

surface. Finally, the sample is wire bonded to a printed circuit board (PCB).

The whole fabrication strategy involves a variety of fabrication techniques and experimental methods, too detailed to be fully explained in this thesis. Instead, only the most crucial methods and principles for a successful patterning and contacting of nanostructured P regions will be discussed for each step of the fabrication strategy.

4.1.2 Design for a fiducial deep etched marker system

The design of the marker system determines the number of devices per sample, the alignment precision and hence, the quality and performance of the final device. The marker layout can be adjusted to the varying specifications of the desired final device, but in general it should provide an easy positioning of the STM tip over the active area with help of a long-distance microscope in UHV, and a straight forward EBL alignment with high precision in the cleanroom. The main goal of the marker fabrication is to transfer the pattern from a chrome mask into the substrate to a certain depth of $\sim 350\,\mathrm{nm}$ without losing sharpness of the profile edges of the features. During the marker fabrication, we try to minimise contaminating the substrate sample during the etch process. The computer-aided drafting (CAD) design for a pre-patterned fiducial marker system shown in Figure 4.3 has been initially designed by Phillip Studer and slightly modified over time. The CAD design of the

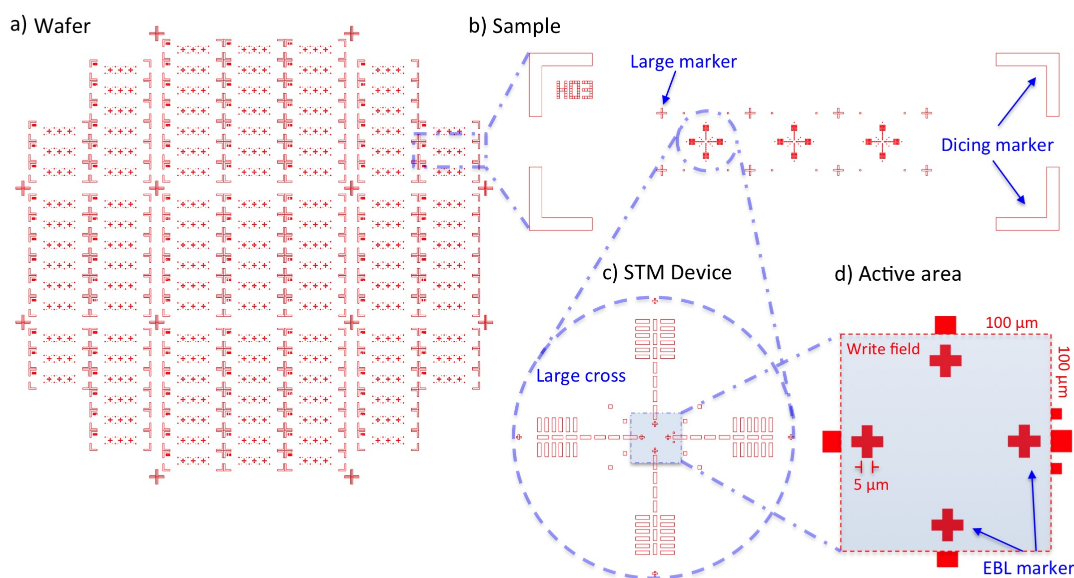


Figure 4.3: CAD design for a pre-patterned fiducial marker system. a) A single 4-inch wafer consisting of 120 samples of $2.6 \times 10\,\mathrm{mm}$ dimensions. b) Three STM devices can be fabricated on each silicon sample. c) Every STM device region comprises of a large cross for optical alignment in the STM. d) In the centre of each cross, the active area of the STM device of $100\,\mu\mathrm{m} \times 100\,\mu\mathrm{m}$ is located between a set of four small cross marker for a precise EBL write field alignment.

fiducial marker system is designed to fit 120 samples of 2.6 mm $\times$ 10 mm dimensions onto a single 4-inch wafer (Figure 4.3a)). The sample dimensions are determined by the size of the Omicron VT-STM sample holder, shown in the inset of Figure 4.7. We found 2.6 mm as the optimal width for the sample, shown schematically in Figure 4.3b)). By exceeding a sample width of 2.6 mm, the sample does not fit accurately into the contacting foil between the two studs of the holder, resulting in a bad contact, such that induced stress during heating can cause the foil to break and the sample to loosen. For a smaller width, the microscopic Al contact pads (250 μm $\times$ 400 μm) that will be aligned onto the surface will suffer from contamination arising from edge effects during resist spin coating which could also cause shorting of the contacts. Each sample pattern is comprised of dicing markers at the edges, a sample number and three large crosses for optical alignment in the STM using an optical long-distance microscope (Figure 4.3b)). In the centre of each cross (see Figure 4.3c)), the active area of the STM device of 100 μm $\times$ 100 μm is located between a set of four small cross marker for precise EBL write field alignment (see Figure 4.3d)).

We will now go step by step through the whole marker fabrication process using the CAD design of the fiducial marker system and explain challenges and processes of the device fabrication. Note, in order to not interrupt the presentation of the device fabrication strategy flow, methods used will only be explained when its necessary for understanding the fabrication procedure.

4.2 1. Pre-UHV fiducial marker fabrication

The first step of the fabrication strategy starts with an unboxed 4-inch silicon wafer and finishes with clean diced substrate samples comprising a fiducial deep etched marker system.

4.2.1 Optical lithography mask

Various photo lithography masks of the fiducial marker system design have been fabricated by Photronics Ltd and JD Photo-Tools, shown in Figure 4.5. The 4-inch chrome mask consists of a soda lime glass substrate plate patterned by a laser-beam. During the optical lithography process, the impenetrable chrome layer will block the ultra-violet (UV) light and the positive resist will only be exposed at the unpatterned regions of the mask. In positive photoresist, the polymer breaks down after reacting with UV light and becomes soluble in a developer solvent. A key parameter for the quality of the mask and resulting resolution of the optically defined marker pattern is the minimum feature size of the mask

design. In our case, the minimum feature size is the width of the four small alignment crosses for precise EBL alignment of $5\mu m$ in the active STM writing area, see Figure 4.3d). As we will see in the following section 4.5.1, a constant width of all crosses is crucial for obtaining a high EBL alignment accuracy. In the EBL automatic alignment process, the write field is aligned to the EBL mask determining the marker position on the sample. By line-scanning over the sides of the crosses, the centre of the write field on the sample is calculated from the edge detection of all four crosses. Hence, the quality of the chrome mask can already significantly influence the alignment accuracy at this early stage of the device fabrication.

4.2.2 Optical lithography process

The process flow of the optical lithography steps are shown in Figure 4.4. The first batches

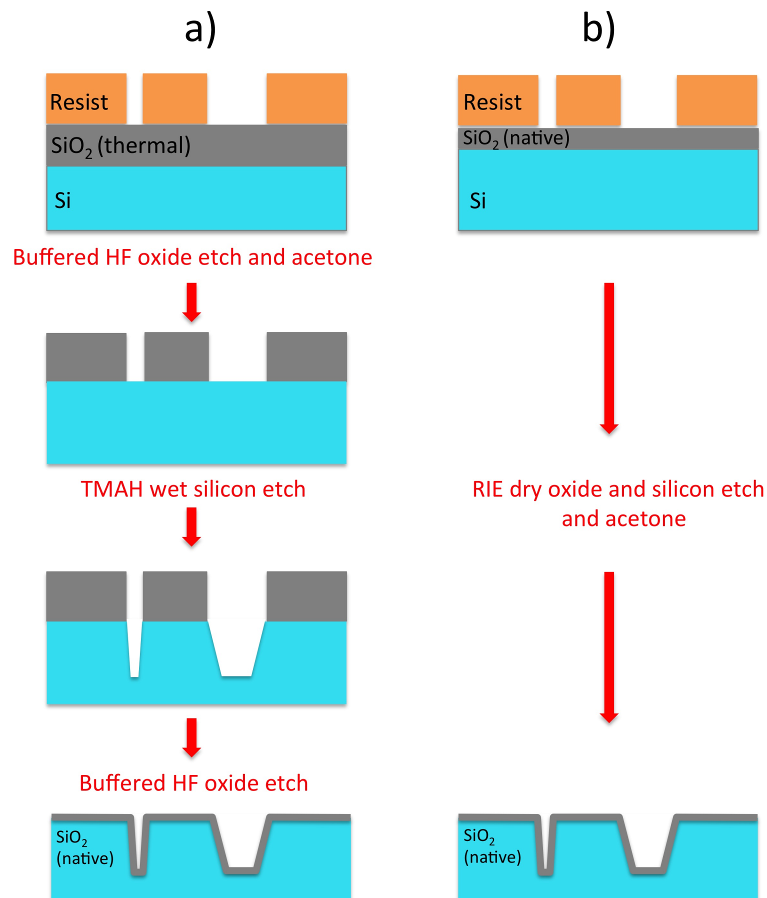


Figure 4.4: Process flow of the optical lithography process. a) When employing a thermally grown oxide as protection layer, the fiducial marker system is transferred into the silicon substrate by chemical wet etching using an HF oxide etch and a subsequent TMAH silicon etch. b) Alternatively the patterned structure can be transferred to the silicon substrate using reactive ion etching (RIE) and only using the native oxide as protection layer.

of samples, such as the dilute δ-layer sample (see section 4.5), have been fabricated by using a thermally grown oxide as protective mask (Figure 4.4a)) and subsequently etching silicon employing tetramethylammonium hydroxide (TMAH), following the fabrication strategy from Ruess *et al.* [88]. This has the advantage that any organic or metal contamination introduced during the fabrication of the registration marker will be removed with the final HF lift-off before introducing the sample to UHV. However, samples that have been fabricated by using only the native oxide as protection layer and subsequent direct RIE etching displayed no significant difference in contamination level, while avoiding chemical wet etching (Figure 4.4b)).

As first step the wafer is carefully cleaned after a three step wet-chemical cleaning cycle. First, a sulphuric peroxide-hydrogen peroxide $H_2SO_4 : H_2O_2$ (3:1) acid bath for 10 minutes removes any organics form the initial wafer surface. Second, a buffered hydrofluoric acid (HF) 10:1 dip for 60 s lifts off the native silicon oxide and a final 10 minutes clean in a RCA-2 $H_20 : HCL : H_2O_2$ (6:1:1) mixture removes any metal contamination. The RCA-2 clean [99] is the industry standard for removing metal contaminants on semiconductor surfaces. After each cleaning step, the wafer is careful rinsed in deionised (DI) water and blown dry with a nitrogen gun. A high quality thermal oxide is grown at $T = 1100\,^{\circ}\mathrm{C}$ for ~ 1.45 h under continued direct oxygen flow in a HiTECH wafer furnace, with a 1h temperature ramp and fall time. The result is a 120 nm thick thermal oxide, confirmed by a MM-16 spectroscopic ellipsometer and prevents a direct contact between the photoresist and the silicon sample. Directly before spin coating, the wafer was kept for 5 min at $220\,^{\circ}\mathrm{C}$ in an oven to undergo a dehydration bake which removes adsorbed water from the surface and increases the photoresist-to-wafer adhesion. We found that the use of hexamethyldisilazane (HDMS) as an extra adhesion layer does not significantly increase the quality of the resist after spin coating. In order to minimise any source of contamination before introducing the sample to UHV, we decided not to make use of HDMS primer.

The 4-inch wafer is spin coated with positive high viscosity MICROPOSIT S1805 resist [100] and rapidly spun at 4000 rpm for 30 s to produce a uniformly thick layer, see Figure 4.5a). To achieve a vertical resist profile, the thickness of the resist should be minimised to limit the effect of under/over cutting resulting in a positive/negative sidewall slope of the developed pattern. For dry plasma etching the resist thickness should not fall below < 500 nm because comparable reactive ion etch rates of resist and silicon could lead to an

effective etch of the whole wafer. The wafer is then pre-baked to drive off excess photoresist solvent at 115 °C for 60 s on a hotplate. This results in a homogenous resist thickness of (525 ± 10) nm, monitored with a DektakXT surface profiler after developing. We used a Quintel Q4000-6 mask aligner to position the wafer underneath the mask and expose the resist in vacuum contact mode to UV light with intensity of $\sim 10\,\mathrm{mJ/cm^2}$, optimised for resists sensitive to 365 nm wave length. After 60 s in standard MF 26A developer and DI rinse, the mask design has been transferred into the resist, a second post-exposure bake at 115 °C for 60 s solidifies the remaining photoresist by producing a durable protecting layer for future process steps like wet or plasma etching.

Figure 4.5b) shows optical microscope images of the small crosses for EBL alignment of varying exposure times after developing. Based on the resist and the intensity of the UV

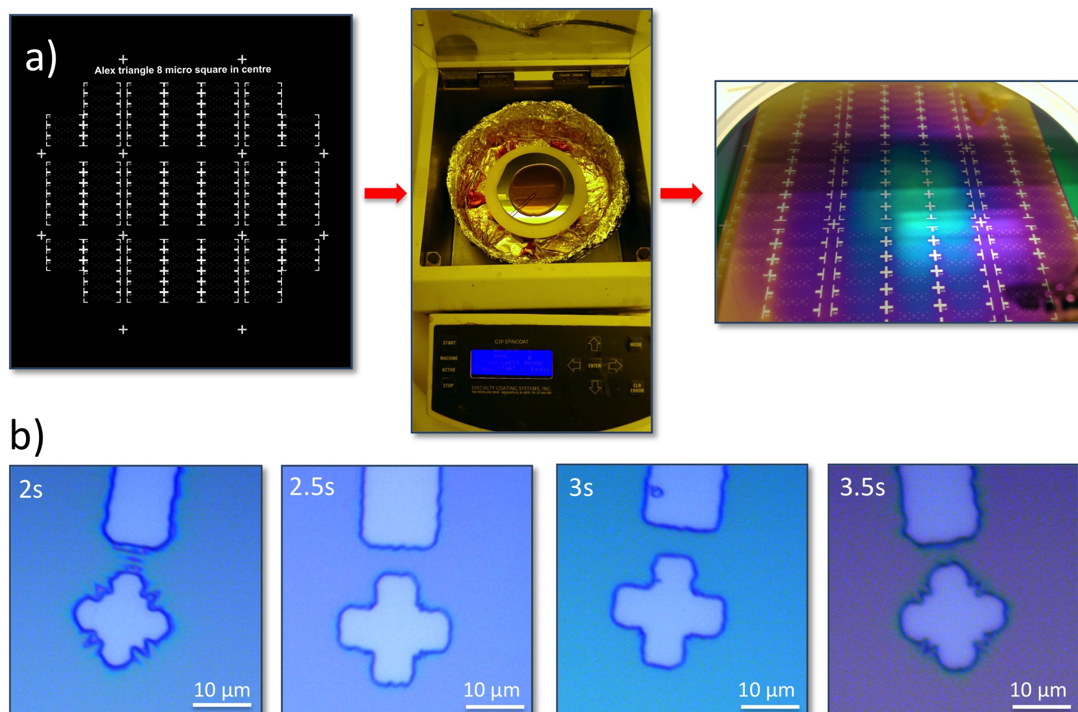


Figure 4.5: Photo lithography process. a) Pattern of a fiducial marker system are transferred into the substrate from a 4″ inch chrome mask (JD Photo-Tools) by spin coating positive high viscose resist onto the wafer and exposing the samples to UV light. b) Microscope images of the small crosses for EBL alignment after developing for varying exposure times.

light, the optimal exposure time can vary. Overexposure results in a smearing out of the feature edges while for an underexposed resist the break down process of the polymers has not been completed all the way down to the SiO_2 interface (normally reflected in a different colour appearance of the pattern in the optical microscope image after developing), accom-

panied with the sharpening of feature edges, as can be seen for a 2 s exposure in Figure 4.5b). The optical lithography defined patterns are first transferred into the thermal silicon oxide by dipping the wafer into buffered HF and subsequently into silicon via TMAH etching by using the thermally grown oxide as a mask (process details appear in section A.1.1 in the appendix). In Figure 4.6a) optical microscope images show the small crosses for EBL alignment for different exposure times after TMAH etch and subsequent resist removal. For

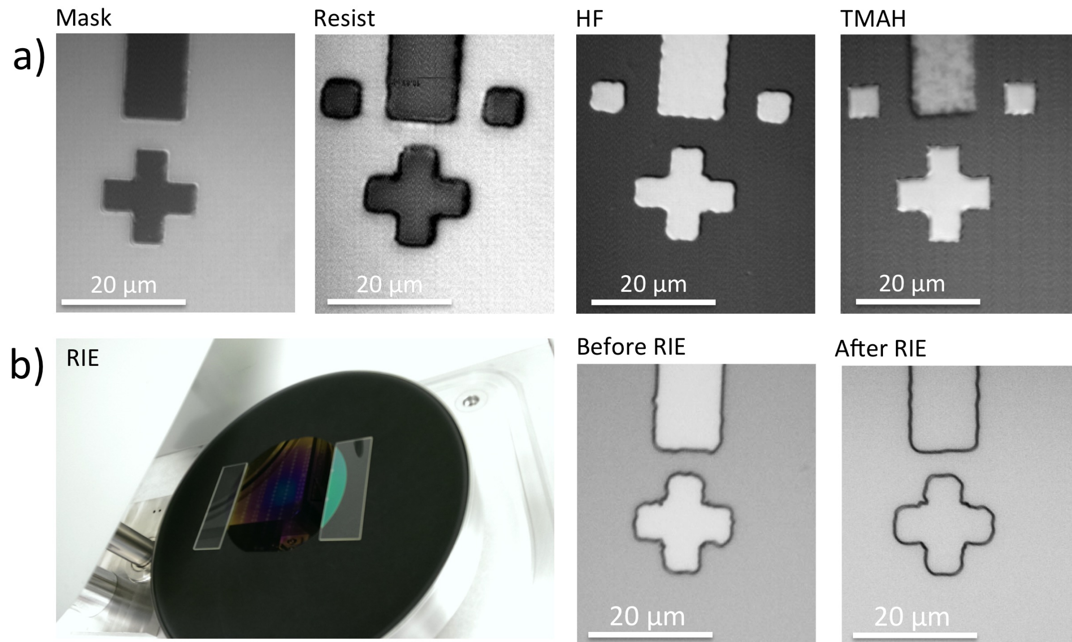


Figure 4.6: Optical microscope images of a small cross for EBL alignment (3 s UV exposure time) at different steps of the marker fabrication process using a) wet etch or b) dry RIE to transfer the fiducial marker system into the substrate.

a targeted marker depth of ~ 350 nm, we obtain an average profile depth (silicon plus oxide) of (520 ± 12.3) nm for an average etch time of (5.44 ± 0.46) min. A problem arising for TMAH wet etching is a varying etch rate for different samples and a non-uniform etch over the whole wafer area, which limits the reproducibility for TMAH etched samples.

4.2.3 Reactive ion etching of fiducial marker system

Alternatively, the patterned structure can be transferred into the silicon substrate using reactive ion etching (RIE) and only using the native oxide as protection layer (as shown schematically in Figure 4.4b)). After cleaning, dehydration bake and optical lithography, the wafer is etched using an Oxford Plasma Pro NGP80 optimised for the etching of layers of silicon, silicon oxide, silicon nitride and similar layers. In RIE, a strong oscillating radio frequency (RF) electric field ionises the gas molecules of the etchant and creates a reactive plasma.

The electrons are accelerated to the electrically isolated platter and build up a large negative voltage, typically around a few hundred volts. The positive ions in the plasma drift to the platter and react with the sample either chemically or by transferring kinetic energy (sputter) which knocks off material from the surface. The wafer is weighted with glass plates on the side which prevents the wafer to move on the graphite cover plate during the etch process, see Figure 4.6b). Process parameters for a homogenous effective SiO_2/Si etch have been investigated by measuring the effective etch depth as a function of varying partial gas pressure (and gas type), RF power and etch time. Homogenous and vertical etch profiles have been achieved using CHF_3 at 58 standard cubic centimeters per minute (sccm) and SF_6 at 25 sccm with a RF power of 150 Watt and a platter bias of 536 V, resulting in an effective etch rate of $(84.4 \pm 1.8)\,\mathrm{nm/min}$. Before and after each RIE etch process, the RIE chamber is cleaned for 15 min in a standard O_2 plasma. The wafer is sonicated in acetone for 5 min to remove the resist and subsequently in IPA to dissolve traces of acetone. IPA evaporates quickly and is used for cleaning beakers and the silicon surface. In optimal condition, RIE produces a very anisotropic etch profile caused by the reactive ions being mostly delivered vertically to the sample surface, in contrast to TMAH isotropic etching, which results in an unavoidable undercutting of the patterned areas. When the etch-depth to feature-size ratio is small, this effect is less significant. On the other hand, RIE can introduce contaminants, especially when choosing heavy etchants at high power. Therefore, it is very important to develop an optimal RIE etch recipe for every desired etch depth, in this case a low power etch which caused a slow etch rate as described above, worked very well for transferring the marker patterns $\sim 350\,\mathrm{nm}$ into the substrate.
Next, a protective S1805 resist layer is spin coated on the wafer to protect the surface during the dicing process. We use the DAD 3230 disco dicing saw for an automated cutting of the wafer. A silicon blade minimises the risk of sample contamination, compared to nickel blades. Typical cutting widths of $\sim 70\,\mu\mathrm{m}$ are obtained. Before loading the processed sample into UHV, it is cleaned in acetone and IPA for $\sim$ 10 minute, which removes the photo resist from the surface. Note that no additional chemical cleaning was needed at this stage of the fabrication to obtain contamination free silicon surfaces after UHV preparation. For samples with thermally grown oxide, an HF dip is performed directly before introducing the sample to vacuum. After optimal process parameters have been found to create suitable fiducial markers of sufficient quality and depth, subsequently Si(100) wafers of different

dopant species and substrate concentrations have been patterned and diced into samples which are then used for further device fabrication processes.

4.3 2. UHV preparation and STM hydrogen lithography

The second step of the fabrication strategy comprises of cleaning and preparing the diced silicon samples in UHV and subsequently performing of STM hydrogen lithography of patterned nanostructures. In this section in addition to the fabrication steps for the device fabrication strategy, a detailed background on STM hydrogen lithography will be presented. Obtaining clean and atomically flat reconstructed silicon as starting substrate is essential to achieve a high quality hydrogen terminated surface. Furthermore, a detailed understanding of the hydrogen desorption mechanism is the basis for controlled and precise STM lithography.

4.3.1 Sample preparation for STM hydrogen lithography

The patterned nanostructures were fabricated using an Omicron VT-STM system with a base pressure of less than 2×10^{-10} mbar of which the setup has been introduced in section 3.1. In this thesis, diced samples with a size of 10 mm $\times$ 2.6 mm from an n-type, arsenic doped, Si(100) wafer were mainly used as substrate, with a sheet resistivity of 15 Ωcm, corresponding to a dopant density of $n_D = 2.5 \times 10^{14}\,\text{cm}^{-3}$ as confirmed by SIMS measurements. The Si crystals were grown by the float-zone technique, which has the advantage of a producing crystals with a very low impurity concentration. After pre-UHV cleaning as described above, the sample is then mounted onto a VT-STM omicron molybdenum sample holder (shown in inset of Figure 4.7) and loaded via load lock into the preparation chamber. The sample is mounted between two contact electrodes on the sample holder, where the holder potential is floating with respect to ground. In UHV, a direct current heating stage is used to apply a voltage across the sample, causing current to flow through the sample, subsequently heating it up. Low doped Si is not conducting at room temperature and needs to be radiatively pre-heated to $T \sim 300\,°\text{C}$ before switching to direct current heating. The sample temperature has been calibrated with an Impact infrared IGA 50-LO plus pyrometer with an assigned uncertainty of $\pm 10\,°\text{C}$. For preparation, cleaning and hydrogen passivation of Si in ultrahigh vacuum we are using a slightly modified standard process after [92], involving an overnight degas at $T \sim 600\,°\text{C}$ and a high temperature flash anneal procedure to obtain a flat and clean Si(100)-2$\times$1 surface with a low defect density ($< 1\%$) [101]. Multiple flash an-

neals to $T = 1230\,°C$ by direct current heating serve to sublime the surface oxide and remove traces of carbon contaminants [97]. By limiting the flash time to 10 seconds with a rapidly cooling to $T \sim 300\,°C$ between flashes, the pressure does not exceed $< 2 \times 10^{-9}$ mbar. The pressure increase during flash anneals is a measure of the outgasing/subliming material from the surface but also from all regions that will be heated by the high temperature radiative heating of the sample during flash periods. When this temperature surpasses the overnight degas temperature of $T \sim 600\,°C$, increased material diffusion onto the surface along with material adsorption from outgassing components (*e.g.* the sample manipulator) result in increased contamination forming on the highly reactive silicon surfaces. We found that a thorough degas of the sample holder at $T \sim 600\,°C$ is crucial for obtaining surfaces of low contamination background, pointing towards the sample holder as a main source of surface contamination. The final flash anneal procedure before H-termination is shown in a timeline in Figure 4.1. After cooling slowly ($\sim 25\,°C$ per minute), the sample is kept at $T = 325\,°C$

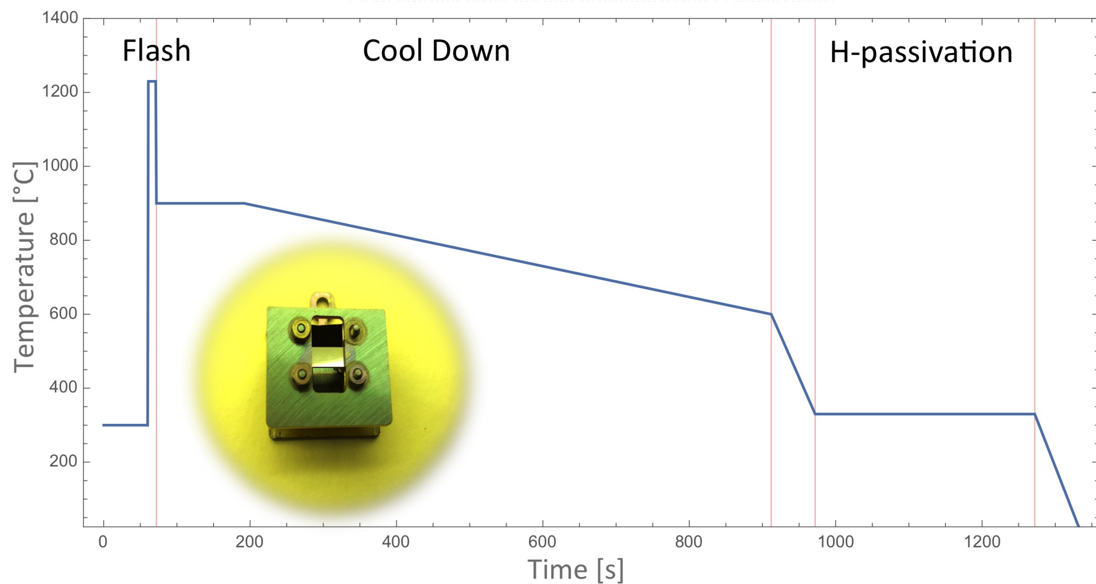


Figure 4.7: Final flash sample anneal preparation procedure for flat Si (100)-2×1 and subsequent hydrogen passivation. A combination of annealing and flash anneals to $T \approx 1230$ °C is crucial to form a flat defect free Si (100)-2×1 surface [101]. After the last flash cycle, slowly lowering the temperature at rates of $\approx 25\,°C$ per min from 900 °C to 600 °C results in the formation of large silicon terraces. The sample is then kept at $T \sim 325\,°C$ during hydrogen passivation. The Omicron VT sample holder with mounted sample is shown in the inset).

for 5 min during hydrogen passivation. Passivation is achieved by exposing the sample to atomic hydrogen with a partial pressure of $\sim 5 \times 10^{-7}$ mbar, which is generated using a commercial Tectra H_2 cracker unit following a standard process [102] (Passivation parame-

ters: Emission current $I_{Emission} = 36\,\text{mA}$, Filament current $I_F = 6.6\,\text{A}$; Voltage $U = 1.2\,\text{kV}$). The filament of the hydrogen cracker is switched off after 5 min and the sample is transferred to the sample stage in the VT-STM chamber for hydrogen lithography patterning. The resulting reconstruction of the hydrogen-passivated silicon surface is dependent on the substrate temperature during atomic hydrogen exposure [103]. There are mainly two distinct surface phases on the passivated silicon surface, the monohydride Si(100)-2×1:H and dihydride Si(100)-1×1:H phase, shown in schematic diagrams in Figure 4.8 (From [51]).

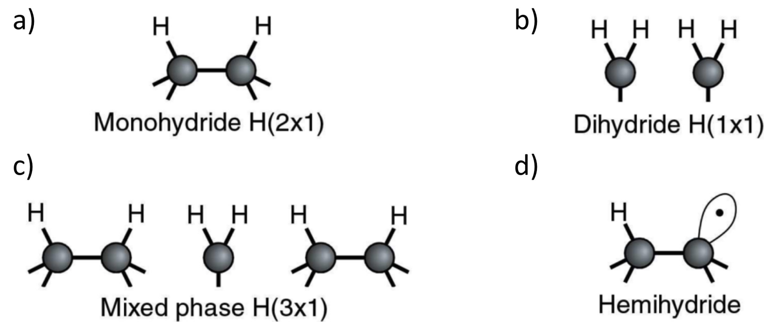


Figure 4.8: Schematic diagrams of Si(001) H-termination. (a) Monohydride Si(001)-2×1:H, (b) Dihydride Si(001)-1×:H, (c) Si(001)-3×1:H mixed phase of monohydride and dihydride and (d) Hemihydride which consists of a single H atom bound to a Si dimer with a dangling bond on the other side of the dimer at very low H coverage (From [51]).

The monohydride phase (Figure 4.8a)) is formed by breaking the Si dimer π-bond such that a single hydrogen atom bonds to each end of a silicon dimer. The formation of the dihydride phase (Figure 4.8b)) results in the bonding of two H atoms to a single Si atom via the breaking of the σ-bond between the Si dimer [104]. Mono and hemihydride phase can co-exist in a Si(001)-3×1:H mixed phase (Figure 4.8c)). The hemihydride consists of a single H atom bound to a Si dimer with a dangling bond on the other side and appears at very low H coverage (Figure 4.8d)). The monohydride phase is more stable and inert, resulting in higher desorption temperature of $\sim 550\,^\circ\text{C}$ compared to $\sim 400\,^\circ\text{C}$ for the dihydride phase, as determined by temperature-dependent hydrogen desorption studies [105, 106]. The monohydride phase is therefore the most desirable reconstruction for the formation of STM-patterned devices. The ideal substrate temperature for obtaining a monohydride surface reconstruction in our system was obtained at $T \sim 325\,^\circ\text{C}$, which is slightly lower compared to $\sim 350\,^\circ\text{C}$ on other systems [26].

To approximately position the tip over the central location of the active writing area, which is defined using a large deep etched fiducial cross marker, we use a long-distance optical mi-

croscope mounted onto the outside flange inlets of VT chamber, shown in Figure 3.2. The shallow EBL alignment cross markers are scanned by STM to identify the exact location of the tip with respect to the four crosses. To avoid tip crashes when scanning over deep etched marker regions, a large feedback loop gain ($\sim 5-10$) at a low setpoint current ($I \sim 20\,\mathrm{pA}$, $U \sim -2\,\mathrm{V}$) and a fairly slow scan speed ($\sim 1000\,\mathrm{nm/s}$) are adjusted for a quick response of the tip height to changes in topography. In the resulting large scale $13\,\mu\mathrm{m} \times 13\,\mu\mathrm{m}$ filled state STM topography image of a $\sim 350\,\mathrm{nm}$ deep etched cross marker in Figure 4.9a), the cross edges appear to be blurred out due to high temperature preparation and non optimal imaging parameters, only allowing an approximate estimation of the exact position. Once

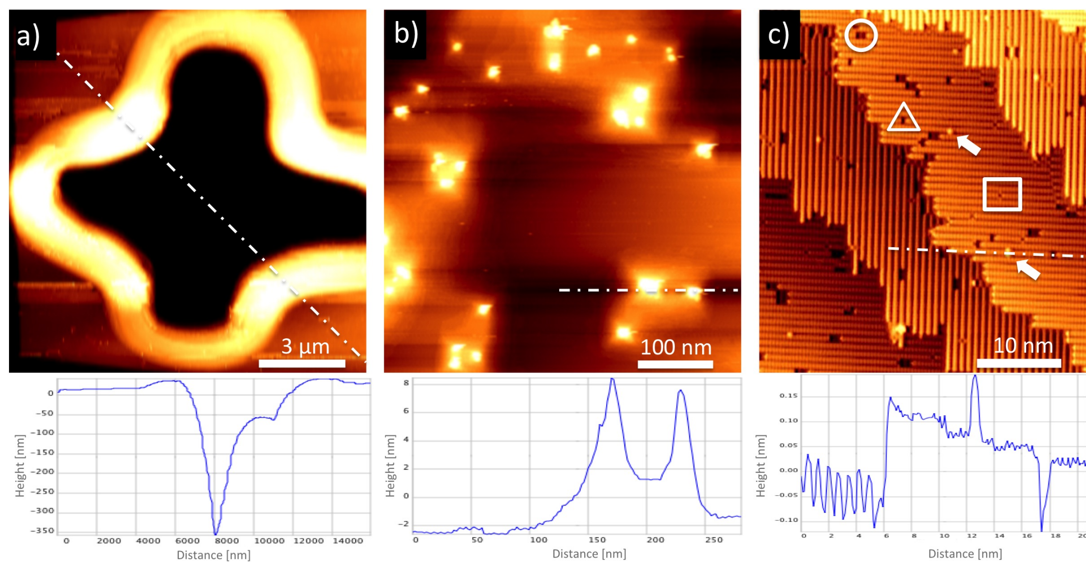


Figure 4.9: STM filled state topography images and line profile of a) an EBL alignment cross marker, b) a $0.5\,\mu\mathrm{m} \times 0.5\,\mu\mathrm{m}$ large area scan, demonstrating pinning of silicon terraces induced from carbon contamination and c) a clean hydrogen passivated Si(100)-2×1:H silicon surface ($40\,\mathrm{nm} \times 40\,\mathrm{nm}$) with typical surface defects.

the location of the tip with respect to the cross markers is determined, the tip is positioned over the actual writing area in the centre of the $100\,\mu\mathrm{m} \times 100\,\mu\mathrm{m}$ write field for performing STM hydrogen lithography. A large scale image is first obtained (here $0.5\,\mu\mathrm{m} \times 0.5\,\mu\mathrm{m}$) to check for large scale carbon contaminations, as shown in Figure 4.9b). A typical signature of carbon contamination on the surface is the pinning of silicon terraces by forming silicon hillocks, possibly induced from carbon defects during flash anneal [51, 97, 98]. On this sample, a large carbon contamination density leads to the formation of a rough surface with a nominal silicon carbide (SiC) pyramid height of $\sim 8\,\mathrm{nm}$. As mentioned earlier, sources of carbon contamination could be diffusing atoms from the sample holder or the sample itself,

indicating an insufficient degassing and/or cleaning of the holder or the resist from the sample. A small scale image is acquired to determine the quality of the hydrogen passivated silicon surface, shown in Figure 4.9c).

Five silicon terraces are visible in the 40 nm $\times$ 40 nm filled state topography image, displaying the monohydride Si(100)-2$\times$1:H reconstructing consisting of dimer rows with common single dimer vacancy defects (VD) (triangle) and double dimer vacancy defect complex 1+2 DV (circle) as well as surface reconstructed dihydride Si(100)-3$\times$1:H (square) [26, 107]. The density of double dimer vacancy defects 1+2 DV provides a measure of the amount of metal contamination on the sample surface, since the occurrence of the so called 'split-off dimer' on Si(100)-2$\times$1 is generally related to metal contamination with minute amounts of Ni or W [108, 109]. Large spherical protrusions indicate the presence of dangling bonds (DB), which are individual missing hydrogen atoms on the passivated Si(100)-2$\times$1:H surface with a nominal height of ~ 0.08 nm (white arrows) [110]. These unsaturated Si p-orbitals remain protruding into the vacuum, leading to an increased tunnel current at negative bias which results in a strong contrast in filled state STM topography images. The dangling bond rate per area also gives an indication about the quality of the hydrogen passivation. As we will see in section 4.4, single DB are known to be practically inert to the adsorption of PH_3 molecules and even a large DB density on the surface will not cause unintended phosphine adsorption in unpatterend passivated silicon regions.

4.3.2 STM hydrogen lithography process

The fundamental procedure that provides atomically precise control of P donor placement in silicon using STM hydrogen lithography was sketched earlier in Figure 4.1. In the following sections, we will go through each step of the STM hydrogen lithography procedure (including a detailed critique of the topic) by highlighting critical aspects for a controlled and successful fabrication strategy.

4.3.3 Hydrogen desorption mechanism

The passivated Si surface [104, 111–113] and the hydrogen desorption mechanism [114–119] have been studied extensively. For controlled hydrogen depassivation, two distinct mechanisms have been found to cause the Si-H bond to break, first demonstrated for hydrogen adsorbed on Si(111) by Becker *et al.* [120]. In field emission (FE) mode, field-emitted electrons cause a direct electronic excitation of the Si-H σ-bond to the σ^* antibonding state [78], as verified by electronic structure calculations [121]. When the energy of inci-

dent electrons is high enough for inducing direct electronic excitations (~ 6.5 V), hydrogen atoms are desorbed with a constant yield of $\sim 2.4 \times 10^{-6}$ H-atoms per electron, independent of the current [78]. When the energy of incident electrons falls below the electronic threshold energy, desorption becomes several orders of magnitude smaller and is strongly dependent on current and voltage, indicating that many electrons are involved in the low voltage excitation process [78, 122]. Model calculations [123] indeed suggest that a high current density under the STM tip produces multiple-vibrational excitations through inelastic electron tunnelling. The amount of vibrational energy transferred to the Si-H bond is critically dependent on the vibration lifetime τ of the excitation of the bond ($\tau_{Si} = 10^{-8}$ s for Si(100)-2×1:H [124]). By using multiple-vibrational excitation for hydrogen depassivation at low applied voltages (< 5 V), STM hydrogen lithography with atomic precision (AP) is possible [78]. In contrast to FE mode, it is found experimentally that the yield in AP mode is at least 100 times worse [125], making the depassivation of a larger areas very time consuming. Hence, we operate in FE mode for depassivating large areas (*e.g.* for the fabrication of large saturation dosed contact pads) and in AP mode when performing sharp atomic precision lithography.

4.3.4 Controlled single hydrogen lithography

Demonstrating control of single depassivation events in AP mode is a crucial requirement for the precise placement of single P donors. In Figure 4.10, filled state topography images and corresponding monitored feedback signals (bias, current and tip height) show the occurrence of a single H desorption event while performing lithography in AP mode along a vertical line over the centre of the Si-H dimer rows. In two subsequent lithography scans H depassiavtion is observed only for the second scan (black line), the feedback signal (topography and current) for the vertical line lithography scan without desorption event is shown as a reference (grey and pink). When the tip sample bias (blue) is ramped up from $U = -2.5$ V imaging condition to $U_{litho} = 4$ V for H-lithography, the tunnel current (black) increases which in turn leads to a retraction of the tip from the surface to maintain a constant tunnel current, visible as a large current peak at ~ 0.18 s. When all depassivation parameters have been reached (4 V, 1 nA, 2 mC/cm) the tip is scanned at a speed of 5 nm/s along the indicated vertical dimer pathway as depicted in the inset of the Figure 4.10. A depassivation event is detected by a peak in tunnel current of $\Delta I = 0.5$ nA (at 0.65 s) and a corresponding feedback induced increase in topography of 0.04 nm (red). No second desorption event

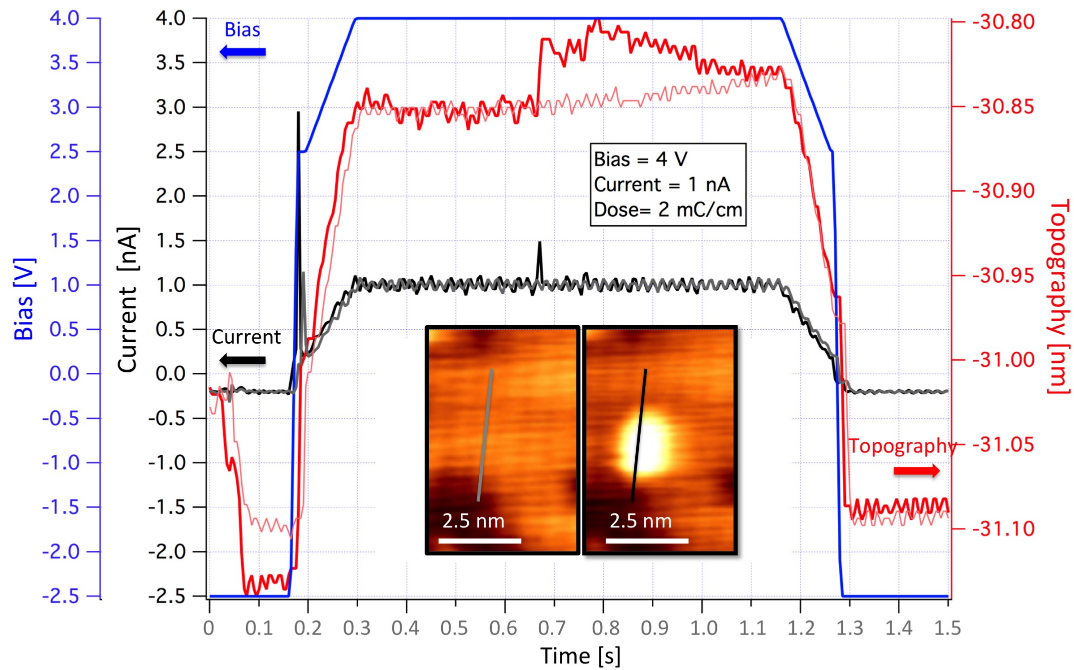


Figure 4.10: Filled state topography images (inset) and corresponding monitored feedback signals (bias, current and tip height (topography)) show the occurrence of a single H desorption event while performing lithography in AP mode along a vertical line over the centre of the Si-H dimer rows. In two subsequent lithography scans, H depassivation is observed only for the second scan (black line), the feedback signal for the vertical line lithography scan without desorption event is shown as reference (grey).

occurs so the continuous topography path maps the spatial extension of the DB till the bias voltage is transversed back to negative scanning parameters. Ideally, for controlled single H depassivation, electron injection should be interrupted to avoid consecutive excitation of adjacent Si-H bonds after the detection of a desorption event. Feedback-controlled STM H-lithography methods have been developed by Lyding *et al.* [126] and automated by Møller *et al.* [119], taking the state of the tip into account. Similar protocols for atom-precision lithography have been developed by Randall *et al.* at Zyvex Labs [125]. As part of a two month secondment at Zyvex labs, I developed an atom-precision protocol code that interrupts the electron injection after the detection of a desorption event. Zyvex has made this code freely available to all users of its commercial 'Zyvector' STM hydrogen lithography control unit.

We used the increase in tunnel current caused by a desorption event as a trigger for the execution of our protocol. In the protocol, the tip was retracted from the surface, current setpoint and bias ramped down, once the detected current setpoint exceeded an adjustable current threshold percentage, during lithography. Thus, the electron flux per area and time

after the detection of a desorption event is minimised.

The functionality of the protocol is demonstrated for a single desorption event in Figure 4.11a), where after a detected current increase of 50% (black curve), the bias is ramped down to 1 V and the tip is retracted (red curve) from the surface. A lower setpoint current of 0.2 nA was adjusted to minimise the possibility of electron injection causing additional unintended excitation processes. Subsequent to H desorption detection, a topography filled state STM image reveals the depassivation of a single H atom (inset a) in Figure 4.11). In contrast to the vertical scan mode presented above, the tip rests over the centre of a H-Si dimer, waiting for a desorption event to occur. Using the developed protocol, controlled H

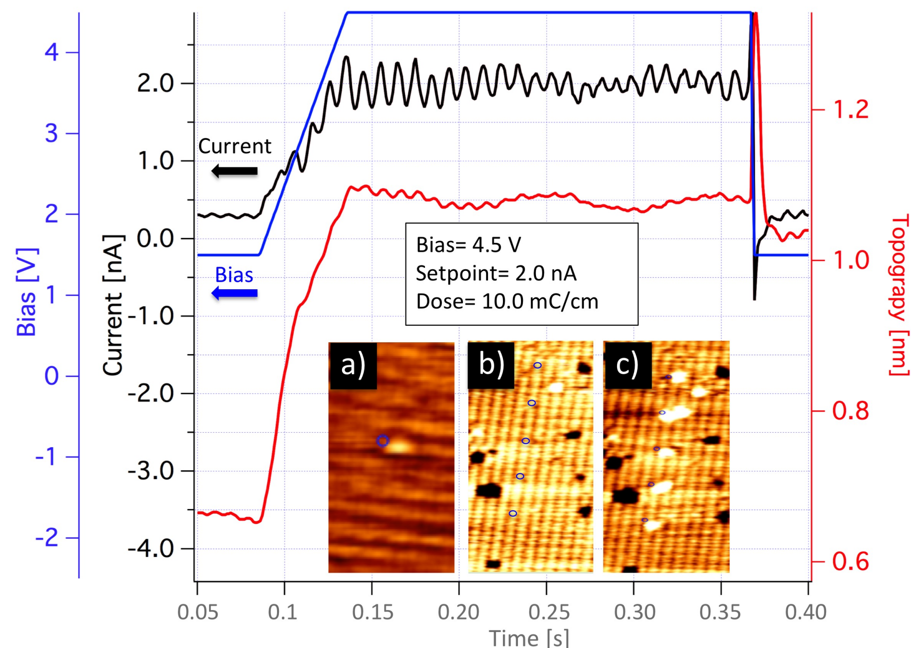


Figure 4.11: Controlled H depassivation for a) a single desorption event and b)+c) a set of five DB along a vertical line.

depassiation for a set of five DB along a vertical line (inset b) and c) in Figure 4.11 and for a 4×5 array (not shown) has been achieved. Unfortunately, the image resolution was not sufficient enough to determine the configuration of the depassivation event. Hence, for a detailed systematic analysis on how to improve the atom-precision desorption protocol, stable and sharp tips are necessary requirements. Using our protocol, the success rate for detecting, triggering and confirming physical single H depassivation is critically dependent on the tip geometry and current threshold that triggers the execution of the protocol. By actively monitoring the STM feedback signal and controlling the desorption parameters

during patterning, individual atoms can selectively and 'autonomously' be desorbed. The implementation of an atom-precision lithography protocol in convolution with a detailed study of controlled single H depassivation on Si(100)2×1:H will be the subject of future experiments at LCN.

4.3.5 Test patterning for optimised hydrogen lithography

Prior to writing our lithographically defined patterned nanostructures we performed test lithography to determine the optimal depassivation parameters for both lithography modes described above. Tip sample interactions in both modes should be minimised to avoid tip modifications during the depassivation process. For controlling the movement of the tip across the surface to pattern arbitrary device areas, Omicron MATE scripts were first used for STM H-lithography. At a later stage of device fabrication, the Zyvector STM hydrogen lithography control unit was implemented using a Python based lithography software. The advantage of the Zyvex lithography software is that it can run pre-installed protocols that automatically correct for piezo creep and align the grid of the lithography mask to the real Si lattice on the sample. This ensures both a small piezo creep during lithography and a defined depassivation path along the centre of the silicon dimer row.

We performed test line lithography by varying voltage, set point current and dose (current/tip speed) along a vertical scan line to establish optimal desorption parameters for both desorption modes and for every tip directly before preforming lithography. In Figure 4.12 filled state topography images display the passivated Si(100)2 × 1:H silicon surface after depassivating a set of vertical scan line in AP and FE mode by varying lithography desorption parameters (voltage, current and dose). The bright features are single Si dangling bonds produced by hydrogen desorption, dark regions are Si dimer vacancy defects. In Figure 4.12a) the desorption pathway was chosen perpendicular to the dimer row direction to determine the desorption spread. Best depassivation parameters that cause a complete and confined depassivation along the vertical line in AP mode were obtained for high tip sample bias of 4.5 V (Line 3, 6 and 9), higher dose rates of $2\,\mathrm{mC/cm}$ and $4\,\mathrm{mC/cm}$. With a constant setpoint current of 2 nA the dose is determined by the tip speed of $10\,\mathrm{nm/s}$ and $5\,\mathrm{nm/s}$ respectively. By using AP lithography mode, sharp lines with dimer resolution (0.384 nm) can be produced as presented elsewhere [24, 28, 78].

In contrast to AP depassivation, in FE mode the width of the depassivated line increases due to the field emission effect and the effective line width can vary between $2-10\,\mathrm{nm}$,

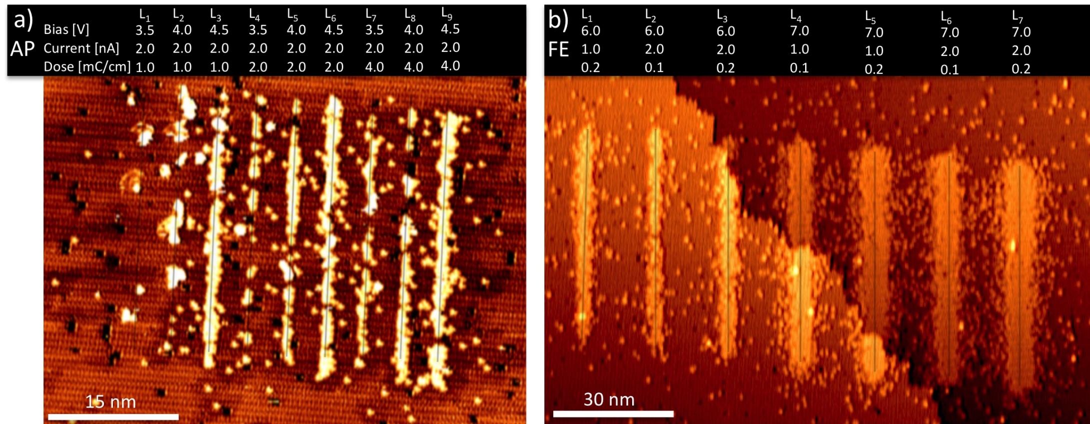


Figure 4.12: Filled state topography images of the passivated Si(100)2 $\times$ 1:H silicon surface after depassivating a set of vertical scan lines in AP a) and FE b) mode by varying lithography desorption parameters (voltage, current and dose).

depending on the geometry of the tip apex and the applied bias. A set of seven vertical desorption lines, shown in Figure 4.12b) demonstrate the bias dependent width of the depassivated line region when using FE mode lithography. The line width of the depassivated region increases when raising the bias from 6 V to 7 V, while a variation of current setpoint and dose parameter display only a small change in depassivation line width. This also holds for higher voltages of $8-9$ V, demonstrated in Figure A.1a) in the appendix. For a constant current and hence constant electron flux, we found that the main parameter for FE depassiation is the tip speed during depassivation, more precisely the exposure time per Si-H bond at a constant electron flux. Independent of the tip geometry, optimal depassivation parameters for FE mode have been determined as $7-9\,\mathrm{V}, 1-2\,\mathrm{nA}, 0.1\,\mathrm{mC/cm}$. Patterning large regions in FE mode requires a trade-off between minimising writing time by using large bias and dose for a large depassivation width and the avoidance of large electric fields causing tip-sample modifications whilst performing lithography. All devices presented in this thesis were fabricated by performing lithography in FE mode.

For a controlled depassivation of larger areas, the tip was programmed to follow the path of a serpentine. The optimal line spacing has to be determined to minimise writing time. For large patterns (*e.g.* contact pads of $4.5\,\mu\mathrm{m} \times 4.5\,\mu\mathrm{m}$), writing times can easily exceed a few hours as will be demonstrated in section 6.8.4. In Figure 4.13a)+b) topography images show two depassivated squared regions where the line spacing of a serpentine pattern was varied from 15 nm to 7 nm, respectively. Both patterns were written using FE depassivation parameters of $U_{Litho} = 7.5\,\mathrm{V}$, $I_{Litho} = 2\,\mathrm{nA}$ and dose$= 0.2\,\mathrm{mC/cm}$, but only the serpentine

pattern with line spacing of 7 nm displays complete depassivation. After the optimal line spacing has been determined, any arbitrary structure can be lithographically patterned with a complete depassivation as shown for two 200 nm × 200 nm squares in Figure 4.13c) with an even smaller line spacing of 4 nm. A magnification of the region between both nanos-

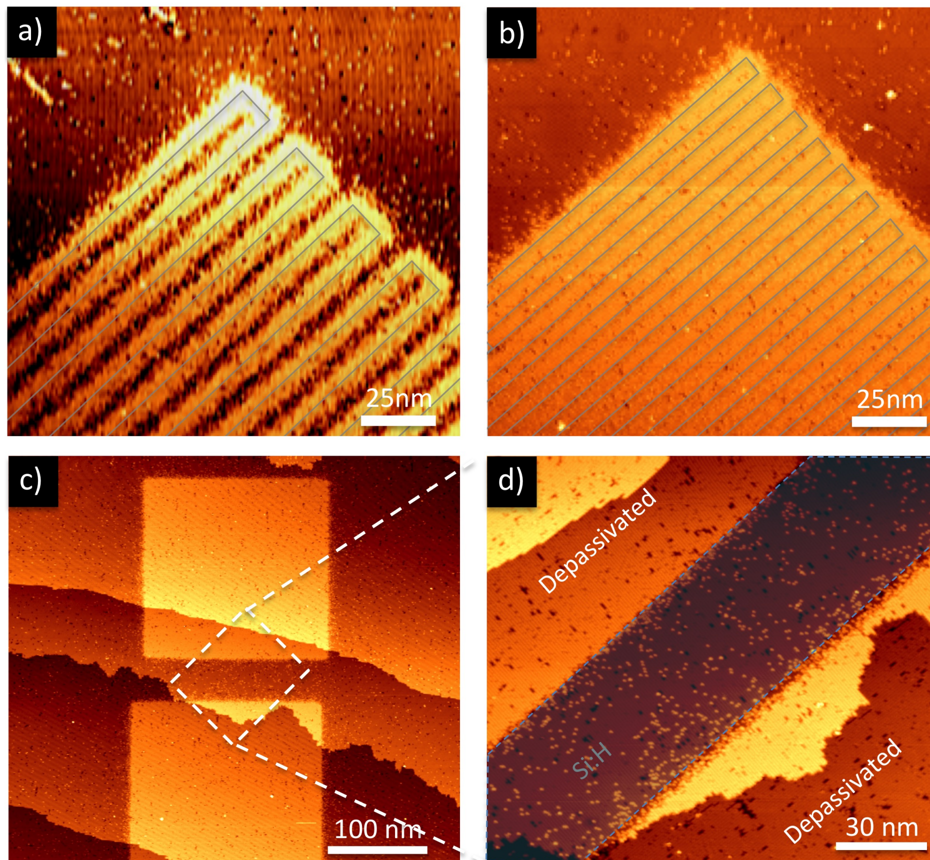


Figure 4.13: STM filled state topography images of depassivated squares where the line spacing of a serpentine pattern was varied from 15 nm a) to 7 nm b) respectively, to determine an optimal line spacing for complete depassiavtion to minimise writing time. c) The surface area of two 200 nm × 200 nm squares with a serpentine line spacing of 4 nm was successfully depassivated, a magnification of the region between both squares confirms complete depassivation within the nanostructured region.

tructures confirms complete depassivation within the nanostructured region.

4.4 3. Phosphine adsorption and silicon encapsulation

Exposing the patterned hydrogen resist to a background pressure of PH_3 results in adsorption of the PH_3 molecules exclusively within the depassivated regions [77] (see 2. in Figure 4.1). During dosing, the STM tip is retracted 50 steps ($\sim 70\mu m$) from the surface to avoid screening of the depassivated area by the presence of the tip and subsequently the surface is exposed to PH_3 by opening the leak valve between VT chamber and PH_3 capsule.

In the following section, the surface chemistry of PH_3 molecules on the clean Si(100)-2×1 surface is summarised which determines the maximum achievable dopant density within a δ-layer and/or patterned P nanostructure. Preparation parameters such as incorporation anneal and encapsulation temperature have significant impact on the dopant profile and electrical properties of the final device. Hence, understanding the consequences of varying preparation parameters for the final device performance is crucial to continuously improve the growth quality and the effectiveness of the fabrication steps. In order to fabricate devices of controlled P dopant density, the extraction of a dose calibration curve is of great importance.

4.4.1 Dissociation process of phosphine

The dopant precursor gas phosphine adsorbs on the clean reactive depassivated Si(100)-2×1 surface in a succession of well understood dissociative processes [127] which are governed by the availability of bare silicon sites on the silicon surface and can be observed on a time scale of minutes by STM [30]. A combination of STM experiments [128] and density functional theory [129] have revealed the dissociation mechanism for a low PH_3 coverage on the Si(001) surfaces, depicted in Figure 4.14a) (from [127]). The PH_3 molecule initially binds to one end of the Si-Si dimer and rapidly dissociates at room temperature to form a one-dimer-wide PH_2+H structure, which undergoes further dissociation to form a PH+2H structure. In the final dissociation step, a three-dimer-wide P+3H structure is formed in which P occupies an end-bridge site between dimers [127]. The surface species present after a low dose of 1.65×10^{-5} L of PH_3 onto the native Si(100)-2×1 surface are shown in a filled state topography image in Figure 4.14b). P atoms in three different states of dissociation appear as asymmetric PH_2+H, centered PH+2H and U-shaped P+3H configuration on the surface. In addition to the PH_x species, native surface defects of the Si(100)-2×1 surface are labeled where the physical explanation for the presence of the C-defects (Cd) is still under debate. In the final dissociation step, P is incorporated into the surface layer by ejecting a silicon adatom. This reaction becomes activated at temperatures of around 650 K [130, 131] by forming a so called 'Si-P heterodimer' structure [24, 131]. The formation of an Si-P heterodimer is demonstrated for a low dosed surface after annealing to 600 °C, shown in Figure 4.14c). In the low dose regime, enough bare silicon surface sites are available for the dissociation process of the PH_3 molecule. Depending on the incorporation anneal temperature it can be approximated that up to 100% (*e.g.* for 350 °C) of the adsorbed PH_3

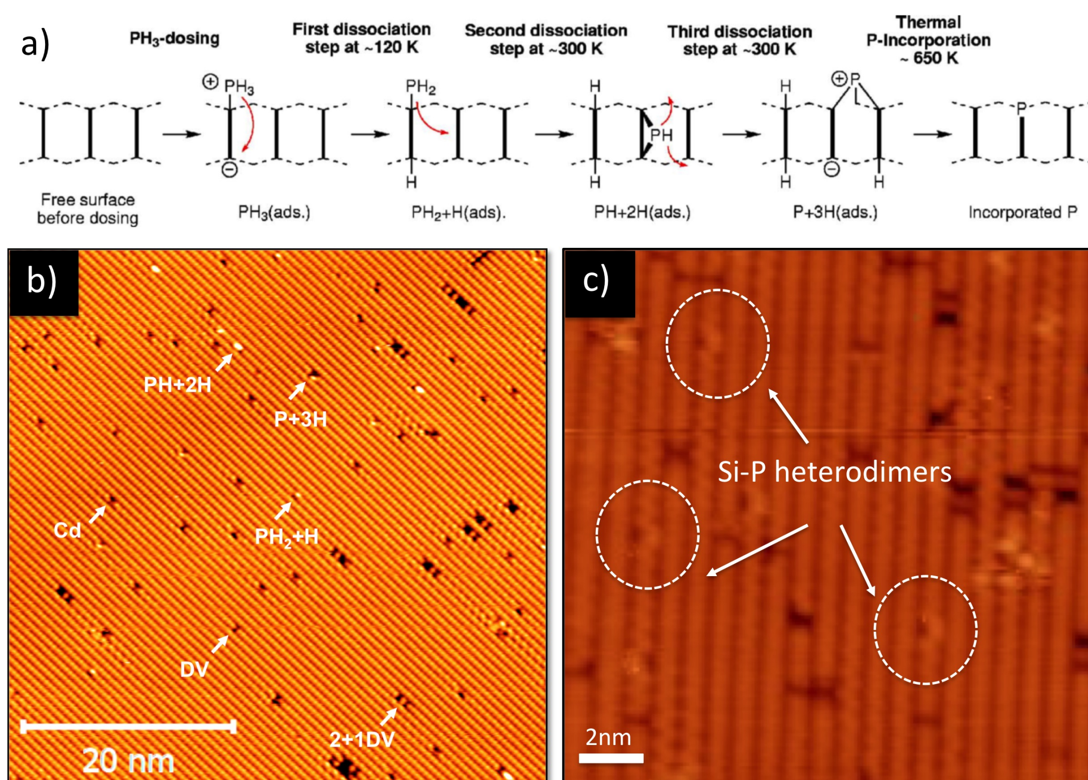


Figure 4.14: a) Outline of the dissociation mechanism of low-coverage PH_3 on the Si(001) surface as revealed in previous work using STM images and density functional theory (From [127]). b) A 50 nm × 50 nm filled state STM image shows the Si surface immediately after PH_3 dose of 1.65×10^{-5} L showing different PH_x species and native silicon surface defects (image provided by Taylor Stock). c) An incorporation anneal of a similarly low dosed silicon surface results in the incorporation of P into the Si lattice by the ejection of Si atoms and formation of Si-P heterodimers.

molecules are incorporated as P donors into the silicon lattice [33, 34, 132].

4.4.2 Phosphorus coverage calibration

To control the effective P coverage in depassivated silicon regions, a PH_3 dose calibration was carried out to assign the exact coverage (in atoms per area) to the corresponding dose measured in Langmuir, which is the partial PH_3 pressure multiplied by the exposure time t_{exp} (1 Langmuir $= 1 \times 10^{-6}$ Torr × s $= 1.33 \times 10^{-6}$ mbar × s). In order to obtain a calibration dose curve for the low coverage regime, a set of 60 high resolution STM images of over 15 different dosages on clean Si(100)-2×1 has been evaluated as part of a summer project conducted by Alice Shipley supervised by Taylor Stock. To determine the accurate dosage, the pressure was measured as a function of time throughout dosing (opening of the leak valve) and the pressure peak was numerically integrated, as an example see Figure 4.15. Due to step edges, large defects or varying image quality, the best method to determine the

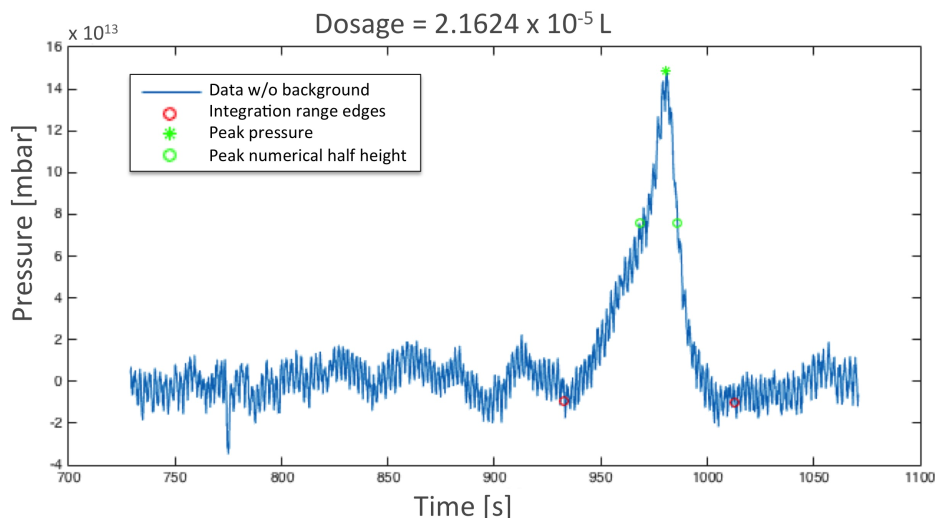


Figure 4.15: Determination of the accurate PH_3 dosage in the low coverage regime. Pressure measured as a function of time throughout dosing. The pressure peak was numerically integrated, yielding a dose of 2.1624×10^{-5} L

corresponding coverage is to simply count P species on the surface from obtained STM topography images by hand. For example a PH_3 dose of 1.65×10^{-5} L (see also Figure 4.14a)) results in the adsorption of 13 P atoms in 3 different states of dissociation on a $50\,\text{nm} \times 50\,\text{nm}$ area. The number of dopants corresponds to a P coverage of $5.2 \times 10^{12}\,\text{cm}^{-2}$. Scanning the same surface area subsequently helps to identify and differentiate PH_x species from defects, other contaminations and from each other due to the dissociation process of PH_3 at room temperature over time. Measurements were repeated multiple times for each value of dose. The average value for the coverage is plotted against the integrated dose values in Figure 4.16a). A linear fit yields $y = (8.6 \pm 0.4) \times 10^{15} \frac{\text{cm}^{-2}}{\text{L}} \text{x} + (4.3 \pm 0.4) \times 10^{11}\,\text{cm}^{-2}$.
The fit reveals that the zero dose coverage with closed leak valve is still $4 \times 10^{11}\,\text{cm}^{-2}$. To investigate if the zero dose coverage originates from PH_3 molecules present on the surface or features mistakenly counted as PH_x species, the feature density of three subsequent images of the clean silicon surface at zero dose have been evaluated over time. We obtained an increasing feature density of $3 \times 10^{10}\,\text{cm}^{-2}$, $4 \times 10^{10}\,\text{cm}^{-2}$ and $6 \times 10^{10}\,\text{cm}^{-2}$ from subsequently taken topography images, respectively. For this extreme low coverage regime only $3-6$ features per $50\,\text{nm} \times 50\,\text{nm}$ image are counted, corresponding to a feature density of $\sim 1 \times 10^{10}\,\text{cm}^{-2}$. However, the feature on the clean silicon surface can be clearly identified as PH_x species and the increasing dopant density with time suggests a slightly leaking leak valve. Since the zero dose is cumulative over time and higher coverages in this data set

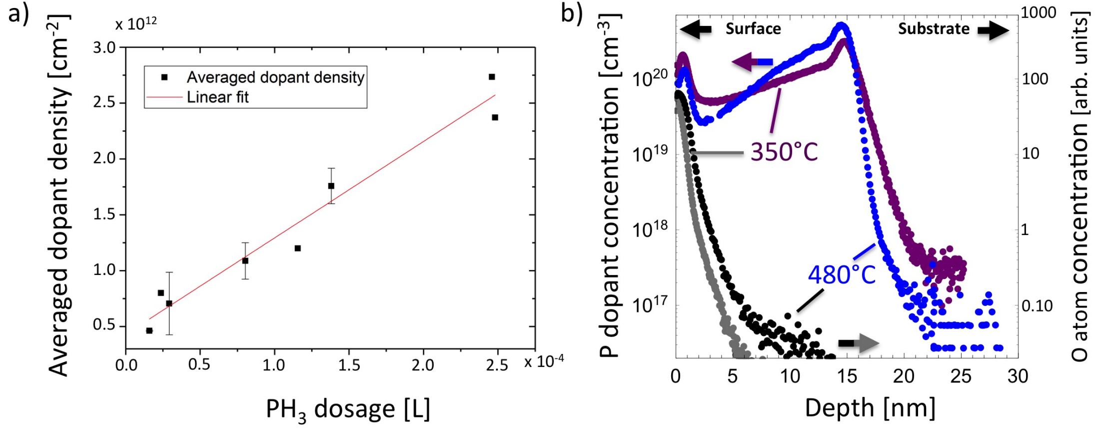


Figure 4.16: a) Average dopant density plotted against integrated dose values. A linear fit yields $y = (8.6 \pm 0.4) \times 10^{15}x + (4.3 \pm 0.4) \times 10^{11}$. Data evaluated by Alice Shipley. b) High depth resolution secondary ion mass spectroscopy (SIMS) profile obtained on a δ-doped sample exposed to a saturation dosage of $(0.450 \pm 0.004)\,\mathrm{L}$. After dose the samples were annealed at 480 °C (blue) and 350 °C (purple) respectively. Followed by Si encapsulation with 15 nm of silicon. Shown are the P and O dopant concentrations as a function of depth.

were obtained from successive dosing, this slope of the calibration curve is estimated to be slightly higher. We therefore assigned an uncertainty of $\Delta \mathrm{u} = \pm 1 \times 10^{15} \frac{\mathrm{cm}^{-2}}{\mathrm{L}}$ to the slope of the calibration curve, yielding as good estimate of

$$y = (8.6 \pm 1.4) \times 10^{15} \frac{\mathrm{cm}^{-2}}{\mathrm{L}} \mathrm{x} \tag{4.1}$$

for the calibration curve in the low coverage regime.

In contrast to the isolated dissociation process of PH_3 molecules for low coverages, the limitations of available silicon surface sites at high coverages determines the extent to which PH_3 can dissociate [26]. As a consequence, the saturation-dosed surface displays a disordered alloy of PH_2 + H and PH + 2 species. Details of the PH_3 dissociation process at high coverage and the reported effect of a varying incorporation anneal temperature on the dopant density is provided in section A.1.3 in the appendix. For dose calibrations in the high P coverage regime, STM is not the ideal tool, since the counting of individual incorporated P dopants after an incorporation anneal is challenging, as can be seen in Figure A.2c) in the appendix. Instead, the dopant density can be extracted from secondary ion mass spectroscopy (SIMS) profiles obtained on δ-doped samples.

In SIMS, a sample is sputtered with a primary beam of ions (here Cs^{+}) and the secondary ions formed during the sputtering process are detected in a mass spectrometer. This way

the element specific concentration as function of depth can be extracted from a sample. The obtained SIMS profiles of two unpatterend saturation-dosed δ-layers are shown in Figure 4.16b). The samples were exposed to a saturation-dosage of $(0.450 \pm 0.004)\,\mathrm{L}$, annealed at 350 °C and 480 °C and subsequently encapsulated with 15 nm of silicon at 250 °C. The SIMS profiles has been acquired by EAG Laboratories, using a high depth resolution (HDR) SIMS setup with a quadrupole mass spectrometer. A low beam energy of 500 eV was applied to achieve high depth resolution with an accuracy better than 2% and a dopant concentration precision of approximately $5-10\%$ (values provided by EAG). The measured dopant distribution of the 350 °C and 480 °C annealed δ-layer displays a Gaussian profile with a FWHM of $d_{\mathrm{FWHM}} = 2\,\mathrm{nm}$ peaking at the encapsulation depth of $(14.74 \pm 0.01)\,\mathrm{nm}$ and $h = (14.45 \pm 0.01)\,\mathrm{nm}$ with an additional segregation tail towards the surface and a P peak in the oxide region. The effects that are causing P segregation and diffusion out of the confined δ-plane will be discussed in section 6.7. Here we extract the saturation P coverage by integrating over the P profile of both δ-layer and obtain a 2D dopant density of

$$n_{480,sat} = (2.43 \pm 0.24) \times 10^{14}\,\mathrm{cm}^{-2} \quad \text{and} \quad n_{350,sat} = (1.91 \pm 0.19) \times 10^{14}\,\mathrm{cm}^{-2} \quad . \tag{4.2}$$

Not all P atoms shown in the SIMS profile are activated and contribute to the conductance of a δ-layer *e.g* those located in the oxide layer. SIMS can not measure the activated dopant density in δ-layers, instead, the effective P dopant density after post anneal incorporation can be deduced from the carrier concentration extracted from Hall magneto-transport measurments. Depending on the anneal temperature, carrier densities for saturation-dosed δ-layers have been published as $n_{\mathrm{sat,L}} = 0.3 - 2.4 \times 10^{14}\,\mathrm{cm}^{-2}$ corresponding to a P coverage of $0.05 - 0.37\,\mathrm{ML}$ [33]. For a incorporation anneal temperature between $450 - 550\,°\mathrm{C}$, a decrease in carrier density of $\sim 17\%$ to $2.0 \times 10^{14}\,\mathrm{cm}^{-2}$ has been reported, compared to samples of anneal temperatures ranging between $250 - 450\,°\mathrm{C}$. The decrease in dopant density is attributed to a partial PH_3 desorption at these temperatures due to an activated minor PH_2 and H recombination process [33] (also see section A.1.3 in the appendix). Note that we do not measure this expected slight increase in dopant density for the sample that was annealed at 350 °C. The value for our saturation density obtained from the SIMS profile is consistent with those found in literature, although the background PH_3 pressure of $(0.450 \pm 0.004)\,\mathrm{L}$ is much lower than the minimum dose for saturation of those found by Goh *et al.* of $\sim 1.25\,\mathrm{L}$. The probable reason is that we have a PH_3 capillary gas inlet inside

our VT-STM chamber, that extends to within a few cm of the sample. Thus the dose is more efficiently directed to the sample than is the case for gas inlets positioned at the VT chamber wall.

To determine the density of activated P dopants we perform transport measurement on δ-layer Hall bars of varying dopant density. Results are presented in section 5.3.4.

4.4.3 Silicon encapsulation

In the previous section, we pointed out that the incorporation anneal temperature determines the number of incorporated P dopants in the patterned δ-layer. To obtain high carrier concentrations in the patterned δ-layer, the crystallinity of the surrounding silicon is another key parameter. The crystallinity of overgrown silicon is mainly determined by the encapsulation temperature and the quality of the starting growth surface, especially for thin overgrown layers [33, 133]. We follow the conventional recipe that has been established for the fabrication of a single P δ-layer and/or δ-doped nanostructure devices comprising a $\sim 350\,^{\circ}$C incorporation anneal to maintain a good electrical activation and encapsulate at a sample temperature of $\sim 250\,^{\circ}$C which provides both a low donor surface segregation and a relatively smooth Si crystal growth [33,34]. For 3D devices we use a different recipe using so called 'Locking layers', as will be discussed in section 6.8.4.

Following the application of the conventional recipe described above, the donor patterned nanostructures are subsequently encapsulated with 15nm of silicon, grown by molecular beam epitaxy from a sublimation Si source (SUSI). At this depth the δ-layer structure is considered not being affected by surface roughness scattering or other surface effects [38,134,135].

4.4.4 Thickness calibration

We have carried out a silicon thickness calibration to obtain the growth rate on the clean Si(100)-2$\times$1 surface when heated to $250\,^{\circ}$C by direct current heating and to obtain insights about the crystallinity of the overgrown silicon at $250\,^{\circ}$C. We use a SUSI-63 Si sublimation source operating at 45 mA filament current which heats up the silicon arch to a constant $\sim 980\,^{\circ}$C during Si encapsulation. The deposition rate is a function of filament current and sample-source separation distance. The amount of deposited silicon is controlled by varying the sublimation time at a constant deposition rate via opening and closing the shutter in front of the SUSI rod shielding. In Figure 4.17, filled state STM topography images are presented obtained for different silicon deposition times. The images confirm the well

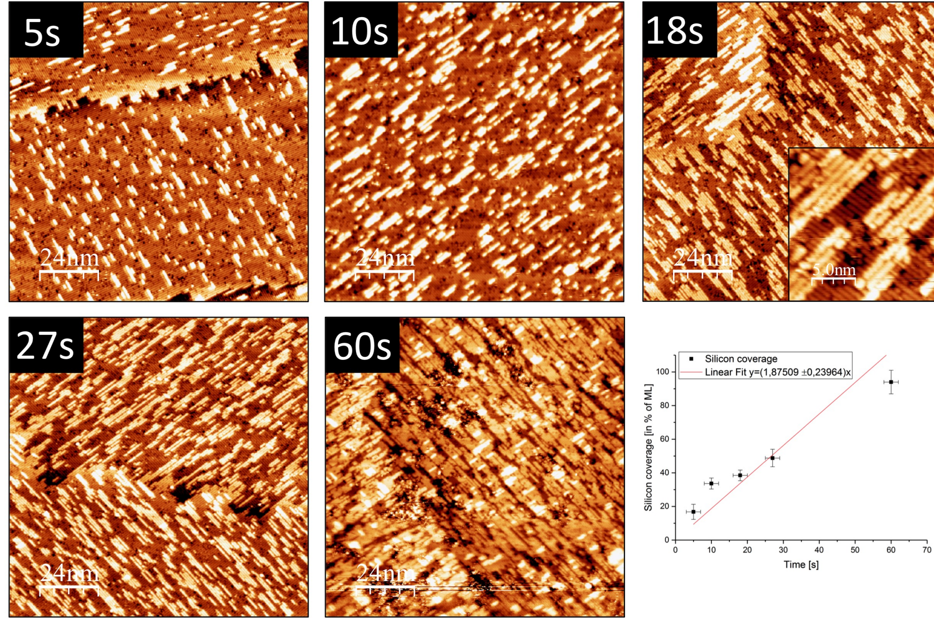


Figure 4.17: STM filled state topography images obtained for different silicon sublimation times. The linear fit yields $y = (1.875 \pm 0.240)\,\%$ of $\mathrm{ML/s}$.

established growth mechanism of sublimated silicon on clean Si(100)-2×1 reconstructed silicon at 250 °C [33, 34]. At low coverage the sublimated silicon form clusters of small islands on the surface, perpendicularly aligned to the underlying silicon dimer rows of the surface. Adatom diffusion on the surface is limited by the low sample temperature, prohibiting the formation of larger islands and the establishment of a growth front emerging from the terrace edges. At an intermediate coverage of $\sim 0.5\,\mathrm{ML}$ (at 27 s sublimation time), second layer growth starts before completion of the first silicon ML. With increasing sublimation time, the island growth on the first layer continues as observed for a sublimation time of 60 s in Figure 4.17. We have used a flooding tool in WSxM to determine the silicon coverage as a function of sublimation time. For each sublimation time, the coverage is obtained from two different areas on the sample surface and two different area detection thresholds are averaged. The silicon coverage in % of a ML as a function of sublimation time is shown in Figure 4.17. From a linear fit we obtain a sublimation rate yielding

$$y = (1.875 \pm 0.240)\,\%\ \text{of}\ \mathrm{ML/s}. \tag{4.3}$$

With $1\mathrm{ML} = 0.136\,\mathrm{nm}$, we estimate a silicon sublimation time for a 15 nm ($\sim 110\,\mathrm{ML}$) silicon capping layer thickness of $t_{15nm} = 1\,\mathrm{h}$ and $(38 \pm 12.5)\,\mathrm{min}$, which corresponds to a silicon growth rate of $(1.125 \pm 0.143)\,\mathrm{ML/min}$. In contrast, a P layer depth of

(14.45 ± 0.01) nm is obtained from SIMS measurements on a P δ-layer encapsulated for 57 min, which corresponds to a silicon growth rate of $\sim 1.86\,\mathrm{ML/min}$. The different effective growth rates demonstrate the limitation using the described procedure to determine the growth rate of sublimated silicon on clean silicon surfaces for several nm thicknesses. The extrapolation of the growth rate obtained from sub-ML coverages results in an underestimation of the actual capping layer thickness. The different growth rate might be caused by a different quality of the starting growth surface on clean silicon to those on P deposited δ-layers due to the presence of H and PH_x species, which leads to increased surface roughness. Although TEM studies confirm that the silicon growth on δ-doped surfaces is still epitaxial [25, 133, 136] for an encapsulation temperature of 250 °C, we detect an altered surface morphology for silicon sublimated on P doped and H-depassivated surfaces from SMM measurement, see section 6.5 which might be resulting from inherently different growth properties.

4.4.5 Oxide growth

Once the sample is removed from UHV environment, a native Si oxide starts to form at ambient condition, converting the upper ~ 1 nm of silicon to SiO_2 [137]. It was previously found that for high dopant concentration beneath the SiO_2, the oxide formation influences the segregation of the dopant concentration at the Si/SiO_2 interface by absorbing the dopants from the converted silicon material [138]. In addition, silicon growth on highly doped silicon regions exhibit an increased oxide growth rate [139]. The increased oxide growth rate results in a selectively different growth velocity between substrate an highly δ-doped nanostructures. Especially when performing the HF dip directly before Al deposition in section 4.5.6 this effect has to be considered, since more silicon has been oxidised and more material will be removed in the etch process. This could cause serious modification of the δ-layer pads in direct contact with the etched vias. Thus, the existence of a native oxide film degrades the controllability of the quality of device fabrication processing and the performance and reliability of semiconductor devices themselves [137].

4.5 4. Contacting buried nanostructures

We have demonstrated how we use a fiducial marker system to perform precise in-plane donor placement on reconstructed Si(100)-2$\times$1:H at a well defined position on the sample using STM hydrogen lithography. The subsequent silicon encapsulation prevents the ox-

idation of the patterned dopant structure but makes contacting to the buried dopant layer more challenging. In addition to achieving good alignment between the buried nanostructure and surface contacts, the contacting strategy also needs to provide a way to penetrate the capping layer to reach the buried nano structure. Contacting strategies that involve the macroscopic alignment of aluminium (Al) contacts on the surface to buried nanostructures have been reported. In these strategies the formation of ohmic contacts to the buried pattern is facilitated by subsequent annealing to 350 °C which results in Al diffusion from the surface down to the buried structure [88, 140]. In this thesis, we use a contacting strategy proposed by Fuhrer *et al.* that facilitates the fabrication of Al vias, drilled into the buried donor layer to form ohmic contacts of low resistance [96]. Following this contacting strategy, the sample was removed from the UHV environment and an array of holes, defined by electron beam lithography (EBL), were etched down to the buried nanostructures. A subsequent deposition of ~ 150 nm of aluminium (Al) onto the surface (see 4. in Figure 4.2a) led to the formation of Al vias and macroscopic contacts on the surface. The flow of the crucial contacting steps is schematically shown in Figure 4.18.

The use of EBL allows the alignment of the surface and buried contact pads a), while a good ohmic contact between them was ensured through the fabrication of an array of etched vias b-d), using RIE dry etching, which maximises the surface area in contact with the phosphorous layer. An alternative hydrofluoric acid dip removes the native oxide directly before Al deposition e). After removal of the resist, the sample was then mounted on a printed circuit board (PCB) chip carrier and wire bonded, ready for electrical measurement g).
We will demonstrate the subsequent contacting steps on a sample that will be subject of measurements presented in the outlook. The sample consisted of a dilute 2D phosphorus (P) dopant δ-layer of density of $(3 \pm 1) \times 10^{11}\,\mathrm{cm}^{-2}$, after exposing to $(1 \pm 0.5) \times 10^{-5}$ Langmuirs of PH_3, buried 15 nm below the surface. To enable electrical contact to be made to the dilute δ-layer, additional 2D saturation dosed P δ-layer contact pads (density $\sim 2.8 \times 10^{14}\,\mathrm{cm}^{-2}$, dimensions 4.5 μm $\times$ 4.5 μm) (from now on labelled 2D pads) were patterned in the same layer within the active 100 μm $\times$ 100 μm write field region, shown in Figure 4.19b). The EBL alignment accuracy necessary for contacting the 2D pads is comparably low, in contrast to the accuracy needed to contact the 1 μm $\times$ 10 μm patterned wire with 2 μm $\times$ 3 μm squared contact pads on each side of the wire (Fabrication is highlighted in section 7.3.1). Subsequently each contacting step is presented using the dilute 2D

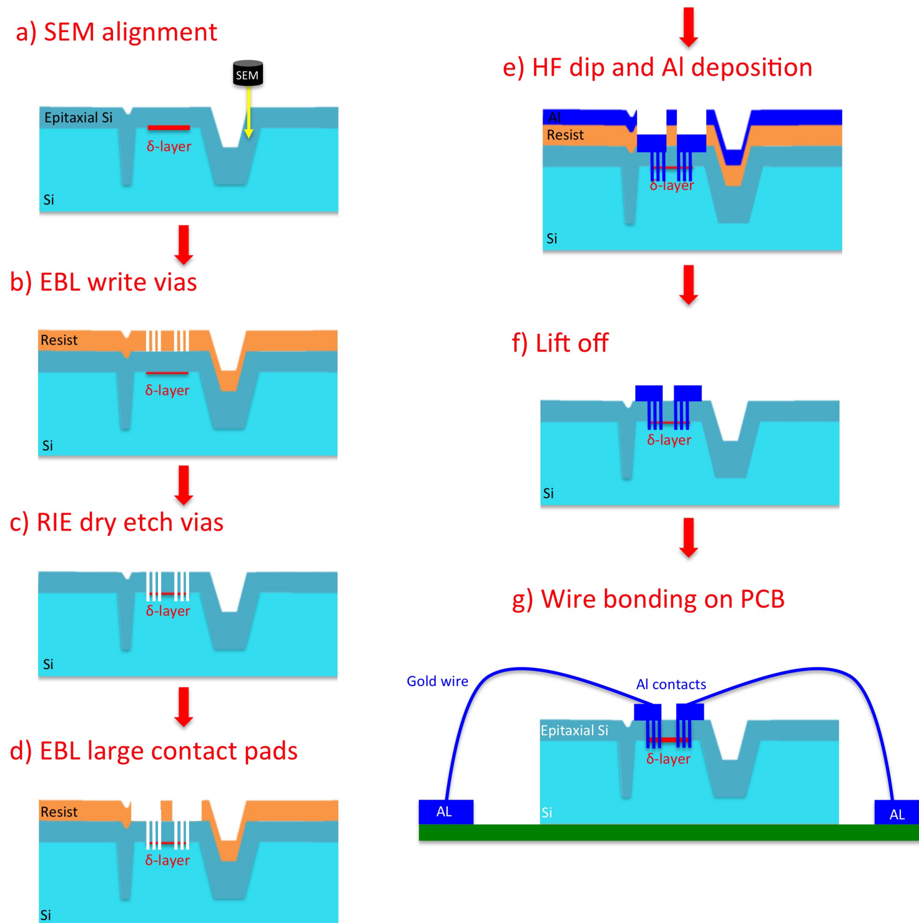


Figure 4.18: Flow of contacting steps for the fabrication of macroscopic Al contact pads on the surface with the help of deep etched vias.

phosphorus sample.

4.5.1 Electron beam lithography mask alignment

The aim of the first alignment step is to determine the exact location of the 2D P pads (which were defined using hydrogen lithography) within the active region on the sample and transfer their exact position into the EBL mask. In this fabrication strategy, the contacting process relies on the visibility of the 2D pads when imaged with a scanning electron microscope (SEM). The procedure to map the position of the buried features to the EBL mask will be described in detail because it was found to be a very crucial step in the contacting strategy that defines the accuracy needed and alignment accuracy achievable by scanning the set of small EBL alignment cross markers. Further, the position of the 2D pads have to be determined before performing EBL lithography steps, because once spin coated in resist, the EBL beam will cause a direct exposure of the scanned regions, making

the determination of the exact 2D pad position impossible. The patterned 2D pads in the active area of the large middle cross are resolvable in a SEM and optical microscope, as can be seen in a micrograph in Figure 4.19b) obtained directly after removing the sample from UHV environment. In addition to the 4.5 μm $\times$ 4.5 μm 2D pads, features from test pattering to determine optimal STM H-lithography parameters of varying dimensions have been lithography defined in the vicinity of the top left and top right pad. The centre of the sample exhibits a deep etched marker that originates from an old contacting strategy and is not of further interest, as well as line scans used for the automated alignment procedure to position the square in the centre. The following procedure was found to be most successful

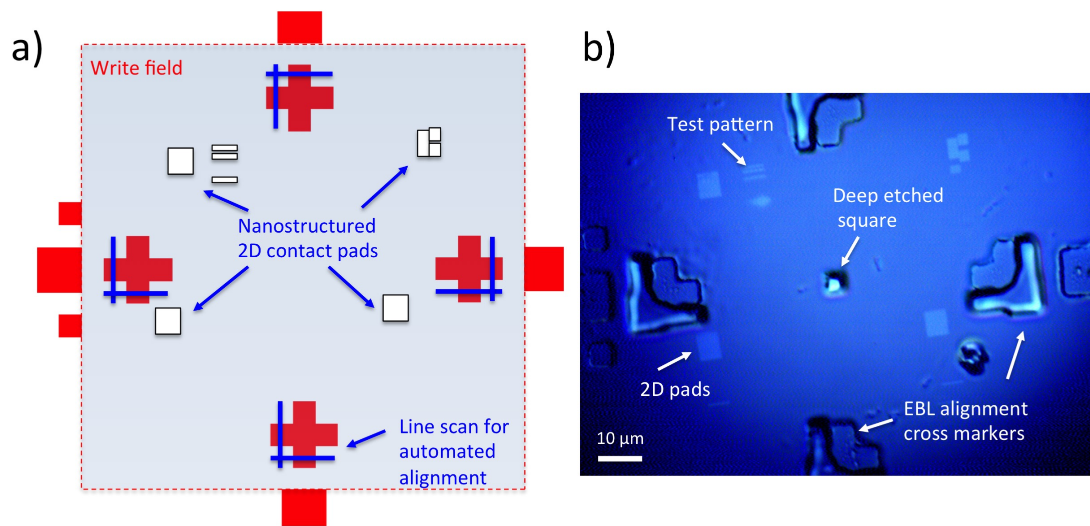


Figure 4.19: a) Schematic of the EBL mask showing the active area of the device. The location of the nanostructured contact pads in the mask is obtained via SEM alignment of the mask and markers on the sample. b) An optical micrograph displaying the patterned 2D saturation-dosed P δ-layer contact pads in the active area of the device region.

for precise alignment using a Raith-150-two EBL system:

1. SEM is used to scan the large marker system of crosses (depicted in Figure 4.3b)) on the sample and align the position of the large marker to those in the EBL mask by using a three point adjustment procedure. Once the sample and marker system are globally aligned, the electron beam is navigated to the active area of the sample.

2. The small EBL alignment cross markers in the active $100\mu m \times 100\mu m$ write field area in Figure 4.19 are scanned by using a manual or automatic alignment procedure (dependent on the quality of the marker). Thus, the precise position of the beam in respect to the active area in the mask can be determined.

3. After saving the new position list of the mask, the buried nanostructure can be scanned in a separate scan image.

4. Next, the array of holes in the EBL mask design can be overlaid with the previously acquired scan image and the position in the mask can be adjusted such that the array of holes is aligned over the patterned nanostructure pads on the sample.

5. Repeating steps 1-4 allows us to make an estimate of the alignment accuracy obtained by using the EBL cross markers. This way, the optimal position for positioning the array of vias in the mask design can be determined.

Note, that this alignment procedure is highly dependent on the quality of the small EBL cross alignment markers. In addition to an imperfect pre-UHV fiducial marker fabrication, the high temperature anneal steps in UHV results in a diffusion and a uniform blurring of the marker structure. While the uniform blurring out of the cross edges does not significantly affect the alignment accuracy, an insufficient etch depth and non uniform cross shape limits the applicability of the automatic alignment procedure. For contacting the 2D pads of the dilute 2D phosphorus sample, a large array of holes was aligned over the 2D pad area, see Figure 4.21b) in section 4.5.4, to circumvent the requirement for high precision alignment. Hence, a manual three point alignment to the EBL cross marker was used to position the hole array in the EBL mask over the location of the 2D pads.

4.5.2 Electron beam lithography process

In electron beam lithography a tightly focused and precisely controlled electron beam is used to transfer a pattern into a thin resist on the surface, which serves as a mask. The mask is directly defined by scanning the electron beam to only expose coordinates held in the mask scan file. The energy delivered to the resist in these regions chemically alters it. Half of the inelastic collisions of the incident electrons produce electrons with kinetic energy greater than the lowest electron binding energy in the resist. These secondary electrons are capable of breaking bonds at some distance away from the original collision. Hence, the feature resolution limit is not determined by the beam size, which can routinely go down to a few nanometers, but by forward scattering (or effective beam broadening) in the resist, while the pitch resolution limit is determined by secondary electron travel in the resist [141, 142]. As a consequence, thinning the resist can improve the resolution of the patterned features [143]. For contacting the buried nanostructured regions, we used a Raith

150-two EBL system with 20 nm resolution. A clamp system on the sample holder allows us to fix and load small 2.6×10 mm samples. In analogue to photolithography, samples were spin coated with a positive polymethyl methacrylate (PMMA) 950 resist for 45 s at 4000 rpm to produce a homogenous thickness of ~ 200 nm. The thickness of the resist not only determines the achievable feature resolution but also the maximal thickness of the Al deposition layer. An Al thickness of 150nm was found to cause clean and complete lift-off and a solid substrate for wire bonding.

4.5.3 Lithographically defined vias and test exposure

Before vias can be aligned and etched down to the 2D contact pads, optimal dose parameters for the desired array size and for the microscopic contact pads on the surface need to be established. The aim is to create small holes (vias), ~ 70 nm in radius and 60 nm in depth in the silicon, which traverse the 2D pads buried below the surface. For this, test patterns with different exposure parameters and length scales must be carried out on a test sample of the same substrate beforehand such that the current beam parameters of the machine are accounted for, as shown in Figure 4.20d). The required dose depends on the number of incoming electrons needed to fully expose the resist (i.e. exposure time $\times$ electron beam intensity) and varies relative to the thickness, shape or area of the resist to be exposed. The optimal dose for the resist used is $d_{beam} = 110\,\mu\text{A/cm}^2$, resulting in a beam current of $I_{Vias} \sim 0.2nA$ ($t_{Vias} \sim 0.005ms$) and $I_{Pads} \sim 3.2\,\text{nA}$ ($t_{Pads} \sim 0.01\,\text{ms}$) for vias and contact pads respectively. The test dose is critical for the success of the microscopic contact pads but especially for the via fabrication. In the worst case overexposure can lead to a broadening of the hole diameter and a subsequent etch results in a homogenous etching of the whole patterned region (see Figure 4.20d) and f)). For test exposure, the active area of the $100\,\mu\text{m} \times 100\,\mu\text{m}$ write field of the sample is patterned with an array of vias of varying dose factors ranging from $1.0 - 3.1$ and varying hole radius of $40 - 80$ nm, using a beam power of 10 kV and $30\,\mu$m aperture size (see Figure 4.20a)). The holes have a pitch of 250 nm.
The optimal exposer parameters for the large contact pads are determined by only varying the dose factor of area dosed features from $0.5 - 2.5$ in a write field of $1000\,\mu\text{m} \times 1000\,\mu\text{m}$ and a higher power of 30 kV with a $120\,\mu$m aperture (see Figure 4.21a)). A higher beam power and aperture will reduce the resolution but decrease the writing time. The insides of the circles in the pattern on the resist are then removed during the development stage by developing the resist for 30 s in Methylisobutylketone (MIBK) : IPA (1:3) developer solu-

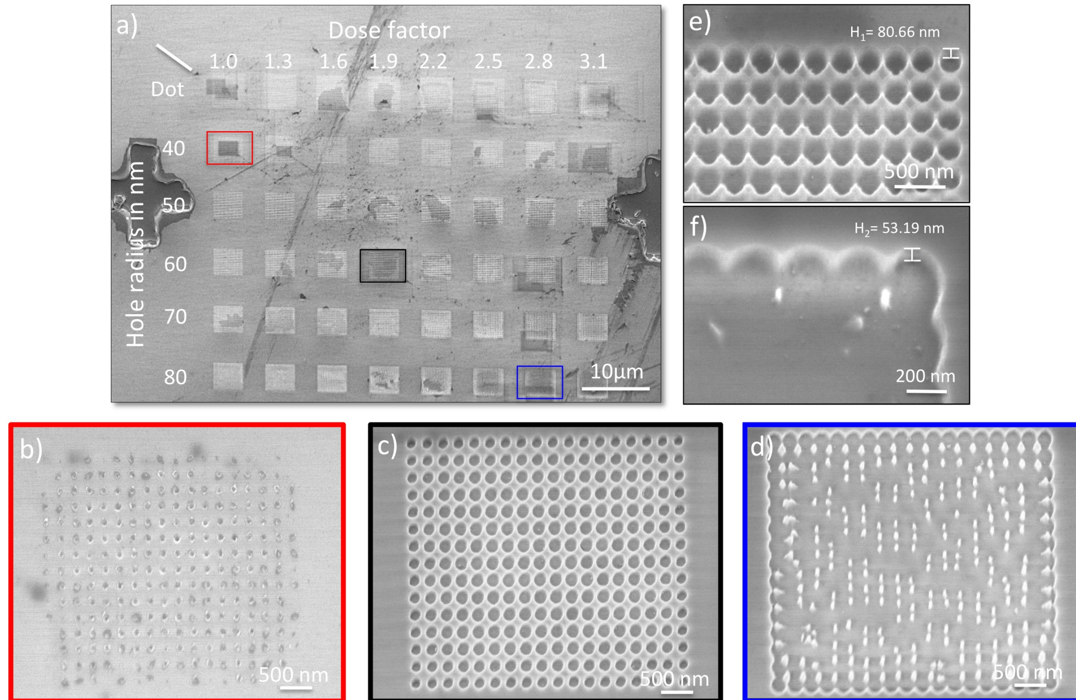


Figure 4.20: Test patterning for the fabrication of deep etched vias. a) SEM image of deep etched vias after exposing to different EBL exposure parameters (dose) and length scales (radius) to determine optimal exposure and etch parameter. Examples for underexposed b), optimal c) and overexposed d) array of holes. The effective etch depth is probed by tilting the sample stage of a focused ion beam setup by 45°, giving an estimated etch depth of 80 nm for an etch time of 2.30 min e) and $\sim$ 50 nm for 1.30 min f).

tion, followed by an IPA dip that stops the developing process. The resist-covered regions remain protected during further processing (until its removal).

4.5.4 Reactive ion etching of deep etched vias

After developing, the test sample is introduced into the RIE, and the patterns are transferred into the substrate by removing silicon in the exposed regions using the same recipe presented in section 4.2.3 but with a reduced etch time. After removing the resist with acetone and IPA, the etched array of vias on the test sample is scanned with SEM to determine the optimal exposure parameter from the shape and depth of the holes. In this test dose we determined for area holes of $50-70$ nm in radius an optimal dose of $d_{Vias} = 2.2\,d_{Beam}$. The effective via etch depth can be probed by tilting the sample stage of a focused ion beam setup by 45°, which gives an estimate of the via etch depth. We obtained $70-85$ nm for an etch time of 2.30 min and $40-60$ nm for an etch time of 1.30 min (see Figure 4.20e) and f) respectively.) The dilute δ-layer sample is covered in resist and loaded into the EBL, once the optimal exposure parameters have been determined from the test sample. Figure 4.21b)

displays the active area of the dilute δ-layer sample after deep etching of the vias.

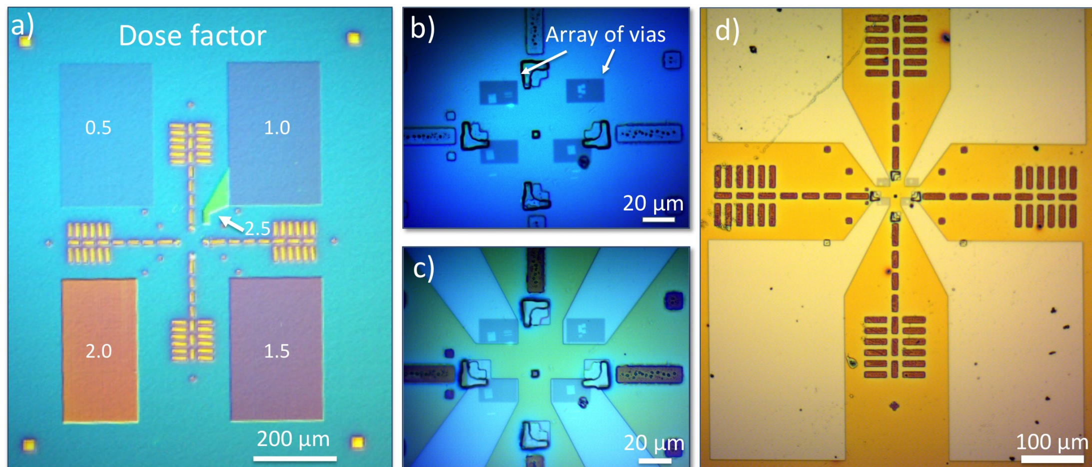


Figure 4.21: Optical micrograph of samples at various steps of the device fabrication. a) Test exposure for macroscopic Al contacts after resist developing. b) Active area of the nanostructured sample with 2D contact pads after aligning and deep etching an array of holes and c)+d) after alignment and developing macroscopic contact pads prior Al deposition.

4.5.5 Electron beam lithography of large contact pads

In analogy to the array of vias, a test exposure is used to determine optimal exposure parameters for the microscopic Al contact pads on the sample. Microscopic contacts pads of varying dose factors ranging from $0.5 - 2.5\,d_{beam}$ are shown in Figure 4.21a) directly after resist developing. The profiler can be used to probe the depth of the microscopic contact pads after developing to determine optimal exposer parameters for the large contact pads (Here $d_{Pads} = 1.5\,d_{Beam}$). Next, the dilute δ-layer sample is covered in resist again and macroscopic contact pads are exposed on the resist, aligned to the deep etched array of holes, as shown in Figure 4.21b). After the resist has been developed, a O_2 plasma cleaning for $1 - 2$ min in a Diener Plasma Asher removes remaining residues of photoresist in the developed regions of both samples.

4.5.6 HF dip and Al deposition

We used a Lesker PVD 75 system to sputter 150 nm of aluminium from an Al target in high vacuum $P < 2 \times 10^{-7}$ mbar onto the sample surface (500 W, DC, 12 min) (see Figure 4.22)a)). Directly before introducing the sample to high vacuum for aluminium deposition, an alternative HF dip removes the native oxide in the developed regions. Although it is well known that the removal of the native oxide reduces the contact barrier between Al and saturation dosed P pad, transport measurements of Hall bar samples without undergoing a

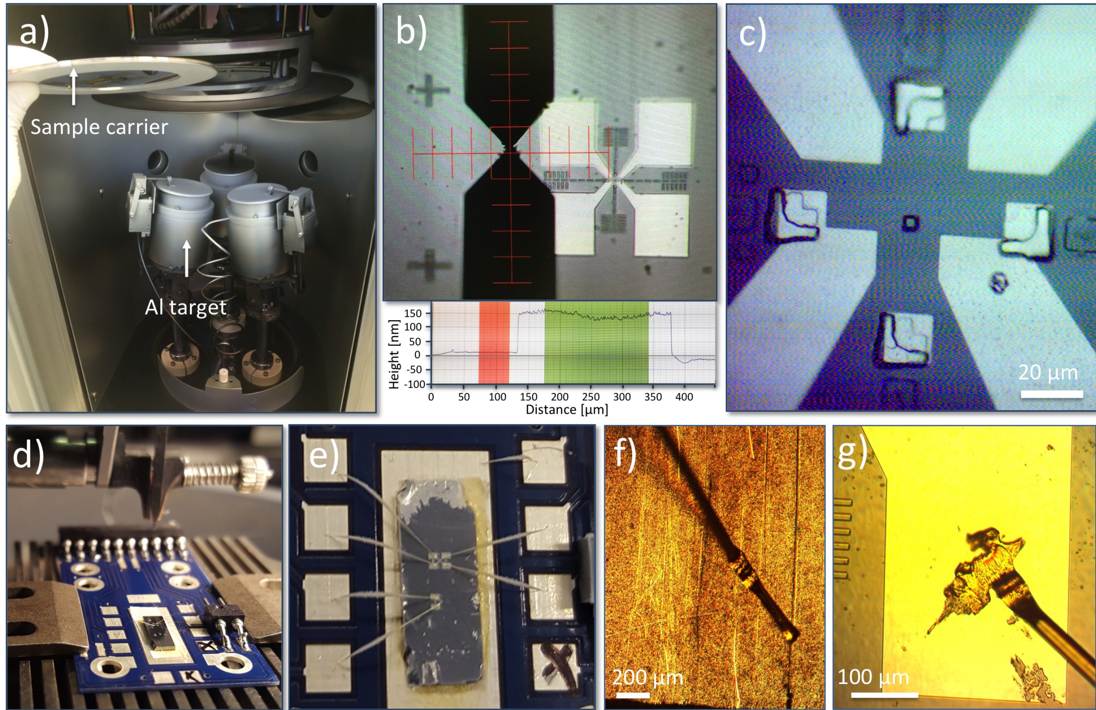


Figure 4.22: Aluminium deposition process. a) Lesker PVD 75 UHV system sputters aluminium from an Al target onto the sample. b) Profiler probes the Al thickness of 150 nm after deposition.c) Optical micrograph of the active device area after Al deposition displaying no shorting between contacts. d) Wedge wire bonder next to the sample mounted on PCB chip carrier. e) Sample architecture after wire bonding.f) The first wire bond on the PCB contact pad and g) second bond to the Al contact pad on the sample, deformed into a flat elongated shape of a wedge without the presence of a wire tail

HF dip before Al deposition displayed ohmic contact behaviour and no significant reduction in device performance (see section 5.3.4). In contrast, we found that HF etching on high P doped silicon regions result in an increased inhomogeneous oxide etch rate compared to native silicon. As pointed out in section 4.4.5, the oxide thickness is increased for highly doped P regions and thus, HF etching adds an additional variable to the fabrication process.

4.5.7 Lift-off and wire bonding

The sample was gently sonicated in acetone which dissolves the PMMA resist and lifts off all Al except those covering regions of the defined large contact pads (see Figure 4.22b)+c)). In the final step, the dilute δ-layer was mounted on a PCB by using UHV compatible silver paste and wire bonded using a wedge wire bonder with a gold wire diameter of $25\mu m$ (see Figure 4.22d)+e)). The design of the PCB carrier varies between a 10 pin connector for measurements in a stick cryostat or 20 pin connector for the dilution refrigerator. During the wire bonding process, the PCB is heated up to $\sim 90\,^{\circ}$C and ultrasonic energy and pressure is

utilised to create a bond between the wire and the bond pad. By carefully adjusting power, time and force, the first bond is made to the PCB contact pad (see Figure 4.23f)). When making the second bond to the Al contact pad on the sample, the wire is deformed into a flat elongated shape of a wedge (see Figure 4.23g)) without the presence of a wire tail, which reduces the risk of shorting the device in the densely packed region at the contact pads. After wire bonding, the resistance of the final device is measured at RT to confirm a successful contacting of the device. A schematic of the wire bonded final dilute δ-layer device on the PCB is shown in Figure 4.23, displaying the active device region. Measurements from this device are discussed in the outlook.

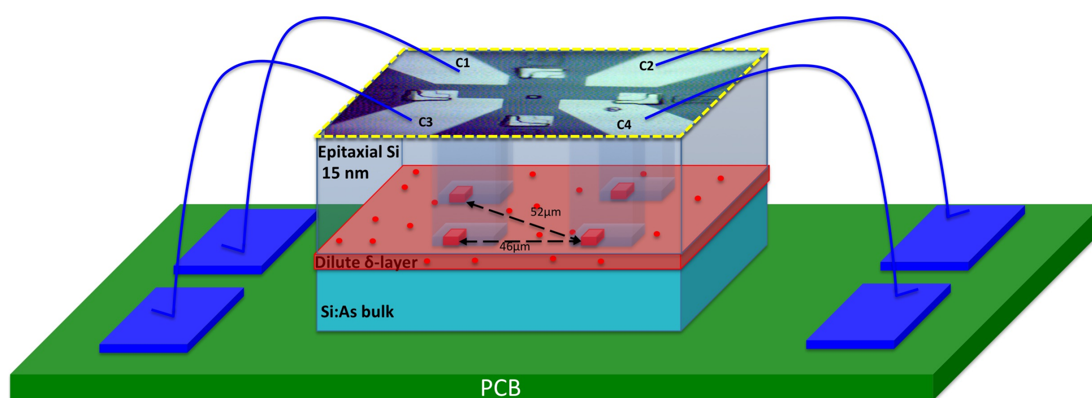


Figure 4.23: Schematic of the wire bonded final dilute δ-layer device on the PCB showing a close-up of the active device region. Note that dimensions are not drawn to scale.

4.6 Discussion and summary

In this chapter, we have presented the development of our STM hydrogen lithography device fabrication strategy and demonstrated how we use a fiducial marker system to perform precise in-plane P donor placement at a well defined position on the sample using STM hydrogen lithography. A detailed description of the methods and fabrication parameters required for fiducial marker fabrication have been presented, highlighting the limitations and advantages of the mask design for the fabrication strategy. We have demonstrated that by only using a native oxide in conjunction with RIE etching for the fiducial marker fabrication, the contamination level on the sample is not significantly higher, compared to those samples employing a protective thermal oxide. Consequently, unreliable TMAH wet etching can be circumvented, making the marker fabrication more time efficient, flexible, and less complex. In UHV we demonstrated that clean and atomically flat reconstructed silicon is an essential starting substrate to achieve a high quality hydrogen terminated surface. Fur-

ther we reported control of STM lithography in both atomic precision and field emission desorption modes and established high resolution phosphorus placement, employing PH_3 as precursor gas. Dose calibrations in low and high coverage regimes enabled us to control the effective dopant density in patterned P nanostructures. Microscopic surface contact pads were fabricated with the help of deep etched holes, defined by electron beam lithography (EBL) and a subsequent deposition of ~ 150 nm of aluminium (Al) onto the surface. This detailed description of the whole fabrication strategy is the basis for future device fabrication activities at LCN.

After the development and implementation of this fabrication strategy some remarks about improving elements of the procedure can be made. For increasing alignment accuracy the size of the active area of the STM device can be reduced to allow a precise pattern placement by aligning the STM tip to the centre of the write field. Ideally the edges of all EBL alignment markers should be detectable in one large STM scan field, which dimension is limited by $18\,\mu\text{m} \times 18\,\mu\text{m}$. To account for heavily contaminated samples, an additional cleaning cycle could be facilitated directly before introducing the diced samples to UHV. Ward *et al.* [87] add an oxygen plasma clean at 100 W of power for 20 minutes which removes most of the remaining hydrocarbon debris from the surface. In addition, the samples could be exposed to atomic hydrogen in UHV which removes the remaining trace carbon on the surface [144]. In general, the use of ion implantation for marker fabrication is an interesting alternative, providing a reliable way of contacting devices with high sample yield through the reduction of STM writing times and eliminating the need for EBL in the post-STM contacting steps [87, 89].

A limiting factor for a higher device output is the sample size, which is dependent on the Omicron VT sample holder design. For simplifying cleanroom processing and a larger device number per sample, a larger sample size would be beneficial. A modified sample holder specifically designed for STM device fabrications, which includes electrical contacting of ion implanted regions on the surface, within UHV, is highly desirable. Implementing a sample anneal capability directly in the VT stage of the STM would reduce the time for the re-approaching and relocating procedures required to find the active device region. More control over the temperature reading in the $200-400\,^{\circ}$C range would produce devices of more uniform electrical characteristics. Implementing a crystal growth monitor for silicon growth calibration would give rise to a more precise determination of the encapsulation

thickness.

Permanent monitoring of feedback signals like current and topography while performing STM hydrogen lithography in AP but also in FE mode, could be implemented in lithography software protocols that stop the lithography process after the signature of a tip modification is detected. This could help minimising the risk of contaminating already patterned areas after tip modifications and thus, increase the device fabrication yield. Sudden tip changes need to be accounted for, especially for complex 3D device fabrication procedures. In the following chapters the viability of the device fabrication strategy will be demonstrated.

Chapter 5

Magneto-transport measurements of the phosphorus δ-layer

5.1 Introduction

The building blocks for nanoscale STM hydrogen device fabrication are high-quality epitaxially overgrown silicon [34, 145, 146], maximised confinement and the electrical activation of the phosphorus dopants [33], as highlighted in the sample fabrication chapter 4. To reproducibly realise successful devices we need the ability to characterise our growth accurately and efficiently. As a consequence, characterisation methods allowing the determination of δ-layer properties as a function of fabrication parameters are highly desirable. Secondary ion mass spectroscopy (SIMS) and atom probe tomography (APT) [135, 147] are capable of probing the dopant profile of a δ-layer with varying spatial resolution but have the drawback of being destructive. In addition, the spatial resolution of SIMS is limited due to *e.g.* an insufficient decay length ($\sim$ 1 nm per decade of dopant density), surface roughness and sputter mixing [25, 148, 149]. Hall resistance and longitudinal magneto-conductance (MC) measurements at cryogenic temperatures are conventional ways to extract valuable physical parameters such as mobility, mean free path and phase coherence length from a two-dimensional (2D) system [150]. The method has been successfully applied to δ-layers [26, 151, 152] and has become a standard characterisation tool for 2D device fabrication.

Another important parameter is the δ-layer thickness. Sullivan *et al.* showed how to extract the vertical spread of a δ-layer [151] using in- and out-of-plane MC measurements by employing a theoretical model developed for metal-oxide-semiconductor field effect-transistors (MOSFETs) [153]. This method is sensitive to the vertical spread of charge

carriers in the δ-layer. This is facilitated by detecting changes in conductance in a magnetic field parallel and perpendicular to the δ-layer plane arising from weak localisation (WL) of the conduction electrons (an introduction to WL is given in section 5.4.1). In contrast to SIMS and APT, only active P dopants contribute to the magneto-transport (MT) signal, which provides information about the 'electrical width' of the δ-layer during transport, in comparison to the 'physical width' of the dopant profile. The thickness determination of a δ-layer using WL was reported to improve the spatial resolution of SIMS by approximately an order of magnitude [25, 151].

The disadvantage of the MT method lies in the processing into macroscopic Hall bar mesa structures, which is time consuming and requires the fabrication of extra samples. More importantly, this fabrication of an additional sample makes the comparison between macroscopic Hall bar and small-scale STM H-lithography-defined devices challenging. Although multi-terminal contacting of patterned nano-wires [26,28] and quantum dots [31] as well as their low-temperature transport characteristics have been demonstrated (as summarised in the introduction), pursuing a contacting process for every fabricated STM device, however, especially for complex 3D device geometries, is very time consuming, often with a low sample yield. Hence a non-destructive characterisation tool that allows local extraction of electrical parameters of patterned δ-layers in and outside UHV is missing but highly desirable. The development and applicability of such a characterisation tool will be presented in chapters 6 and 7. This chapter serves to point out the limitations but also advantages of transport measurements for the characterisation of contacted δ-layer devices.

In this chapter we use MT techniques to assess the quality and performance of the devices which were fabricated as described in chapter 4. We start with a short introduction about transport and its important length scales. Next we confirm the controlled placement of P atoms in δ-layer sheets at different doping densities and investigate their electrical properties. First, the contact and sheet resistance for a saturation-dosed δ-layer were determined from multi-terminal IV measurements. Then a set of five δ-layer samples of different dopant densities were fabricated in Hall bar mesa structures. We used Hall measurements to obtain mobilities and compared the findings to published values. In the last part of the chapter we used a vector magnet to take in- and out-of-plane MC conductance measurements, as well as a full-field angle-dependent MT measurement between $22\,\mathrm{mk} - 30\,\mathrm{K}$ for a dense saturation δ-layer ($n_d = 2.8 \times 10^{14}\,\mathrm{cm}^{-2}$). We demonstrate the validity of WL theory in quasi-2D by

including the finite thickness of the buried δ-layer. Finally, the extracted 'electrical width' of the δ layer is compared to its dopant distribution obtained from a SIMS profile.

This study was carried out as part of the COMPASSS collaboration. Sample fabrication, part of the measurements, modelling and analysis were carried out by the author. Large parts of measuring, modelling and analysing were done by various people in the COMPASSS project, mainly Guy Matmon, Juerong Li, Andrew J. Fisher and Eran Ginossar. The results of the work appear in [1].

5.2 Transport

The macroscopic conductivity of a 2D conductor is given as $G = \frac{w}{l}\sigma$, where w is the width, l the length and σ the conductance. Conducting electrons near the Fermi energy drift diffusively through the crystal and scatter inelastically or elastically with impurities, phonons, defects or other electrons. The scattering effects are manifest in the Drude equation

$$\sigma = en\mu_n = \frac{e^2 n\tau}{m^*}, \tag{5.1}$$

where μ_n is the electron mobility, e is the electron charge, n the carrier concentration, τ the elastic scattering time and m^* the effective mass of the electron.

At low temperatures the conductance deviates from the classical Drude expression because interactions beyond simple classical scattering events become important. Transport properties are determined by three length scales: i) the elastic mean free path of electrons L which determines the mobility, ii) the phase coherence length L_ϕ, defined as the distance over which electrons maintain phase coherence and iii) the Fermi wave length $\lambda_F = \frac{2\pi}{k_F}$ of the conduction electrons (k_F is the Fermi wave vector). At low temperature the inelastic scattering time $\tau_\phi = \frac{L_\phi^2}{D}$, where D is the diffusion constant, is significantly larger than the elastic scattering time $\tau = \frac{L}{v_d}$ (where v_d is the drift velocity). Thus, coherent transport is retained over many elastic scattering events. This gives rise to WL, a phase coherence effect of the electron wave function, which results in an increased resistance of the conductor. The phase coherence length is strongly temperature dependent.

In addition to the WL the conductance in a disordered 2D system is affected by Coulomb repulsion dominated by electron-electron interactions (EEI) between conduction electrons which lead to a decrease of σ. The dominating quantum correction to the conductivity in

2D at low temperatures can be expressed as

$$\Delta\sigma = \Delta\sigma_{WL} + \Delta\sigma_{EEI}\,. \tag{5.2}$$

Both $\Delta\sigma_{WL}$ and $\Delta\sigma_{EEI}$ scale as ln(T) [154–156]. At even lower temperatures, when the electron Fermi wave length λ_F is comparable to the mean free path L ($\lambda_F \sim L$ or $k_F L \sim 1$), or when the localisation length ζ, the envelope of the electron wave function, becomes comparable to L_ϕ, Anderson suggested that an electron eventually becomes trapped in local potential variations due to strong disorder [157]. This leads to strong localisation effects (also called Anderson localisation). The occurrence of strong localisation is also expected for low dopant densities, when inter-impurity spacing ($\sim 3\,$nm for a dopant density of $d \sim 1 \times 10^{13}\,\mathrm{cm}^{-2}$) becomes comparable to the Bohr radius a_B of an isolated P donor ($\sim 2.5\,$nm [42]). Here, the electron localisation causes a metal-insulator transition (MIT) of the system due to strong on-site Coulomb interaction compared to $k_B T$ as described by Mott [158]. The description of the transition between conducting and insulating systems can be improved by considering onsite coulomb repulsion of localised electrons which is described by the Hubbard model [159].

5.3 Density-dependent transport in a δ-layer

The dopant density in the δ-layer channel can be controlled by varying the PH_3 dosage during fabrication, allowing us to investigate its effect on the electronic transport. The extracted transport parameters allow confirmation of control over dopant density, and assist in assessing the δ-layer growth quality.

5.3.1 Mobility

When we compare our δ-layers to other 2D system and it should be noted that carrier densities exceed those found for graphene, 2D GaAs [160] and in Si MOSFETs by more than two orders of magnitude (see also table 5.2). At low temperature, transport in the δ-doped layers is dominated by coulomb impurity scattering [71] from ionised donors, which significantly limits the mobility $\mu_n = \frac{e\tau}{m}$ of the free carrier. Typical measured mobilities of $\mu \sim 30 - 120\,\mathrm{cm}^2/\mathrm{Vs}$ for P doping levels of $n_d \sim 10^{14}\,\mathrm{cm}^{-2}$ in δ-layer at 4 K have been pubilished [25, 26, 33, 161, 162], with a mean free path of the order of tens of nm and corresponding scattering times in the femtosecond range [26, 71]. In modulation-doped

GaAs systems or 2D Si MOSFETs the carrier density is rather independent of the impurity density, while the carrier density in a δ-layer is approximately equal to the dopant impurity density and density dependence shows qualitatively different behaviour there [71].

For P-dosed δ-layers Goh *et al.* observed that the mobility decreases monotonically with increasing densities [26], which is in line with other 2D systems *e.g.* graphene [163] or δ-doped Si:Sb and Si:B [164]. A depth-dependent resistivity has been reported for P δ-layers suggesting that oxide charge and surface roughness scattering play a significant role in the electron transport of shallow δ-layers buried within the first 5 nm under the surface [135]. Calculations employing Boltzmann transport theory, where surface-roughness scattering and localisation effects in the P δ-layers were neglected, suggest a monotonic mobility increase with increasing dopant density in the high coverage regime [71] in contrast to a monotonic decrease as found by [26].

Another reported observation is a characteristic minimum doping density of $n_C \sim 10^{13}\,\mathrm{cm}^{-2}$, leading to non-Ohmic conduction [26, 165]. Similar behaviour for densities around n_C is observed in other δ-doped samples such as Si:Sb and Si:B [164]. Theoretical calculations suggesting that a transition to Anderson localisation for Si:P δ-doped layers occurs around $n \sim 10^{13}\,\mathrm{cm}^{-2}$ ($k_F L \sim 4$), with a crossover from strong-screening to weak-screening behaviour in the system [71]. Only a few experimental studies have been reported that explored the effect of doping density on electronic transport in δ-doped layers [26, 165–167].

To test transport properties at high 2D carrier densities, we fabricated δ-layer samples of various dopant densities in a Hall bar mesa structure, shown in Figure 5.1. The free-carrier density is obtained through the determination of the classical Hall coefficient R_H via the measured Hall resistance

$$R_{xy} = R_H \cdot B = -\frac{B}{n_{Hall} e}, \tag{5.3}$$

where B is the applied magnetic field. By measuring the Hall resistance the carrier density n_{Hall} of a 2D system can be extracted from the slope of the curve. For a discussion of the Hall effect see e.g. [53]. At low temperatures only one type of charge carrier (electrons) contributes to the current flow in the δ-layer and hence the resistance is a direct measure of the free electron density and dopant density in the δ-layer.

5.3.2 Fabrication and experimental set-up

Our test devices were grown using a slightly modified δ-layer fabrication recipe (to the conventional recipe stated in chapter 4.4.3) by PH_3 dosing on a Si(100) flat surface, annealing for 1 minute at $\sim 470-480\,^\circ$C, then overgrowing 15 nm of silicon at 250 °C without the use of a locking layer [25, 69], as described in chapter 4. By controlling the surface dosage as described in section 4.4 five samples of different doses (0.45 L, 0.003 L, 0.0015 L, 0.0003 L, 0.00002 L) with an estimated sheet densities of $n_1 = (2.43 \pm 0.24) \times 10^{14}\,\mathrm{cm}^{-2}$, $n_2 = (0.26 \pm 0.04) \times 10^{14}\,\mathrm{cm}^{-2}$, $n_3 = (0.13 \pm 0.02) \times 10^{14}\,\mathrm{cm}^{-2}$, $n_4 = (2.64 \pm 0.67) \times 10^{12}\,\mathrm{cm}^{-2}$ and $n_5 = (2.20 \pm 1.32) \times 10^{11}\,\mathrm{cm}^{-2}$ were fabricated. The finished δ-layers were processed into a Hall bar geometry with mesa dimensions of $\sim 100\,\mu\mathrm{m} \times 20\,\mu\mathrm{m}$ using photolithography and subsequent reactive ion etching. For contacting, an array of vias was formed with electron beam lithography (EBL) alignment followed by an HF dip and an evaporation of ~ 150 nm of aluminium to create macroscopic contacts on the surface. An optical image and cross section of the sample appear in Figure 5.1.

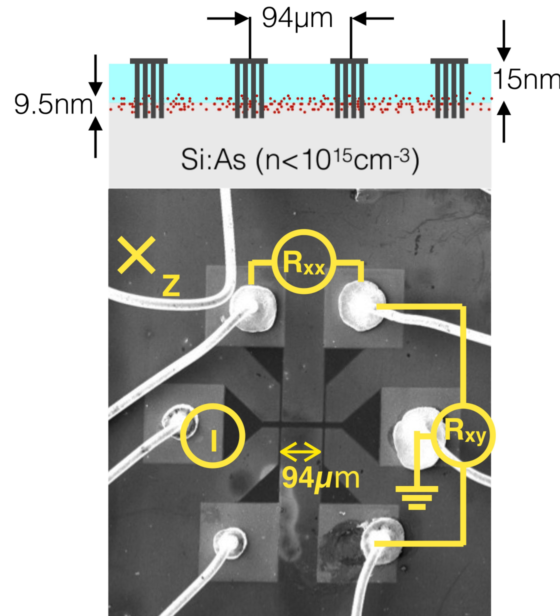


Figure 5.1: The Hall bar and the principal directions. a) A schematic of the device cross section showing the arsenic-doped substrate (light gray), the deposited phosphorus δ-layer (red), the overgrown silicon (cyan) and the aluminium contacts.b) Scanning electron microscope image of a wire bonded δ-layer Hall bar with mesa dimensions of $\sim 100\,\mu\mathrm{m} \times 20\,\mu\mathrm{m}$.

The devices were mounted in a pumped-helium cryostat with a magnet capable of out-of-plane (Z) and in-plane (X and Y) field magnitude of 7 T. The base temperature was

$\sim 4\,\mathrm{K}$ and a stable measurement temperatures of 1.8 K could be achieved by pumping on the helium bath. Transverse and longitudinal resistances were measured for linear field sweeps, with the magnetic field out-of-plane and in-plane.

5.3.3 Contact and sheet resistance

A multi-terminal (T) measurement is used to extract the sheet resistance of the δ-layers as well as the lead and contact resistance of the measurement set-up at 1.8 K, shown in Figure 5.2. By separating voltage and current electrodes in a 2T, 3T and 4T set up, selective contributions from individual elements in the electric circuit can be identified. This is shown schematically in Figure 5.2a). The resistance R of the 2T measurement is the sum of twice

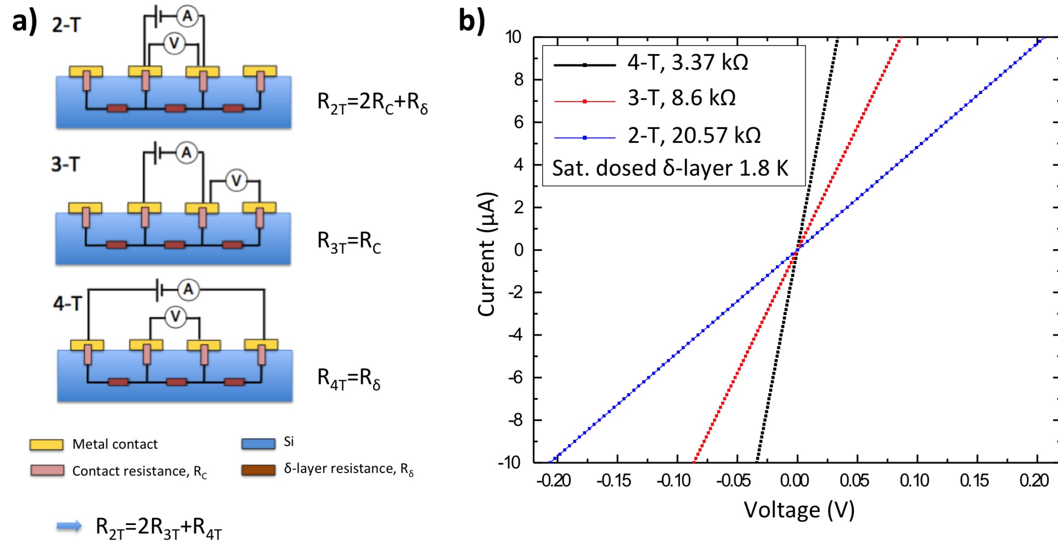


Figure 5.2: Multi-terminal measurements on δ-doped sheets. a) Schematic of a 2T, 3T and 4T equivalent circuit diagram and b) IV-characteristics and determined resistances for multi-terminal measurements at 1.8 K. Measurements performed by Juerong Li.

the contact resistance (for each contact) obtained from the 3T measurement and the δ-layer resistance measured with the 4T set-up. This matches the measured 2T resistance of $R_{2T} = 20.6\,\mathrm{k}\Omega$, see Figure 5.2b). From simple IV measurements the contact resistance at 1.8 K is determined as $R_C = 8.6\,\mathrm{k}\Omega$ and the saturation-dosed δ-layer resistance to be $R_\delta = 3.37\,\mathrm{k}\Omega$.

$$R_{2T} = 2R_{3T} + R_{4T} = 2 \times 8.6\mathrm{k}\Omega + 3.37\,\mathrm{k}\Omega = 20.57\,\mathrm{k}\Omega \tag{5.4}$$

The sheet resistance of the δ-layer is determined as

$$\rho_{xx} = R_\delta \frac{w}{l} = 674\,\Omega/\text{square}\,, \tag{5.5}$$

where $w = 20\,\mu$m the width and $l = 100\,\mu$m is the length of the Hall bar.

5.3.4 Hall measurements

Figure 5.3a)+b) display a typical Hall resistance R_{xy} curve as well as a magneto-resistance (MR) ρ_{xx} curve as a function of in-plane (black) and out-of-plane (red) magnetic field. Using the carrier sheet density from equation 5.3 the mobility

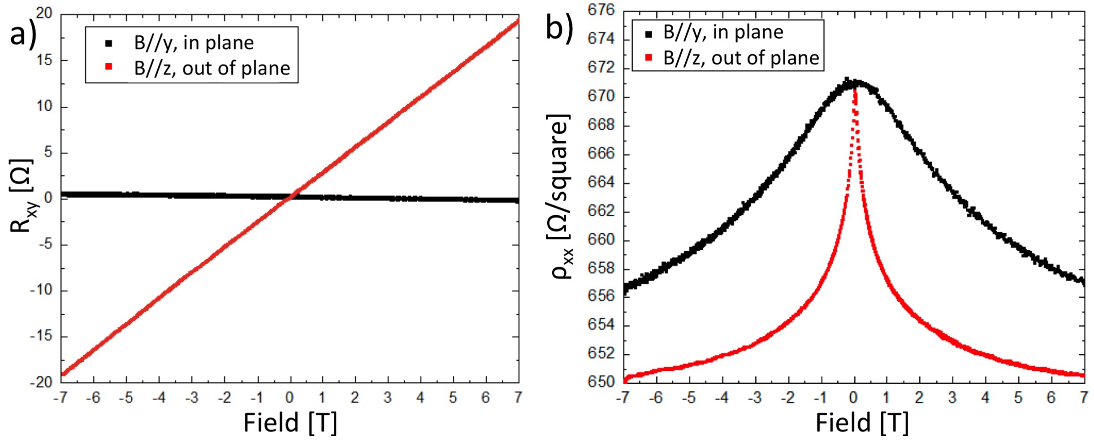


Figure 5.3: a) Hall resistance R_{xy} curves and b) magneto resistance ρ_{xx} curves at 1.8K on a saturation-dosed δ-layer as a function of in-plane and out-of-plane magnetic field. Measurements performed by Juerong Li.

$$\mu_n = \frac{1}{n_{Hall} e \rho_{xx}(0)} = \frac{R_H}{\rho_{xx}(0)}\,, \tag{5.6}$$

was calculated from the Hall coefficient R_H and $\rho_{xx}(0)$, the longitudinal sheet resistance at $B = 0$. We can then obtain the scattering time $\tau = \frac{\mu_n m^*}{e}$, where $m^* = 0.315 m_e$ is the effective mass for electrons [168]. The mean free path L is related to the mobility and carrier density by

$$L = \frac{\hbar \mu_n \sqrt{2\pi n_{Hall}}}{e}\,. \tag{5.7}$$

Table 5.1 summarises parameters obtained from Hall bar measurements for all samples. Sample 4 ($n_4 = (2.64 \pm 0.67) \times 10^{12}\,\text{cm}^{-2}$) and sample 5 ($n_5 = (2.20 \pm 1.32) \times 10^{11}\,\text{cm}^{-2}$) were not ohmic enough for Hall measurements.

		sample 1	sample 2	sample 3
PH_3 Dose	[L]	0.450 ± 0.004	0.0030 ± 0.0002	0.0015 ± 0.0001
P density	$[10^{14}\,\mathrm{cm}^{-2}]$	2.43 ± 0.24	0.26 ± 0.04	0.13 ± 0.02
n_{Hall}	$[10^{14}\,\mathrm{cm}^{-2}]$	2.279 ± 0.001	0.6217 ± 0.0002	0.1597 ± 0.0004
R_H	$[\Omega]$	2.748 ± 0.001	10.039 ± 0.003	39.07 ± 0.11
$\rho_{xx}(0)$	$[\Omega/\mathrm{square}]$	670 ± 1	1438 ± 2	4266 ± 12
μ_n	$[cm^2/\mathrm{Vs}]$	40.88 ± 0.02	69.84 ± 0.02	91.59 ± 0.26
L	[nm]	10.183 ± 0.004	9.085 ± 0.003	6.040 ± 0.02
τ	[fs]	7.32 ± 0.03	12.510 ± 0.004	16.40 ± 0.05

Table 5.1: Parameters obtained from Hall bar measurements on three Hall-bar-processed δ-layer samples of varying dopant density at 1.8 K. Sample 4 ($n_4 = (2.64 \pm 0.67) \times 10^{12}\,\mathrm{cm}^{-2}$ and $n_5 = (2.20 \pm 1.32) \times 10^{11}\,\mathrm{cm}^{-2}$) did not give Ohmic results and were omitted. Note, for τ the effective mass used is $m^* = 0.315 m_e$ [168]. Measurements performed by Juerong Li.

5.3.5 Discussion and summary

From the extracted carrier density $n_{Hall} = 2.28 \times 10^{14}\,\mathrm{cm}^{-2}$ for sample 1, the density of activated P dopants can be deduced by comparing the detected P concentration extracted from an integrated SIMS dopant profile, shown in Figure 4.16. The ratio of dopants/carrier density implies a $(94 \pm 10)\%$ dopant activation within the δ-doped sheet. Dopant deactivation has been reported for dopants located inside the oxide region and in close proximity to the surface as a result of surface depletion. This is mainly caused by defect states that trap charge carrier at the Si/SiO_2 interface and as a result of the dielectric mismatch between doped region and native oxide and/or vacuum which leads to an increase of the ionisation energy of the dopants [36, 37, 134, 135]. By assuming 100% dopant activation for the growth parameters used in the fabrication process, as supported by references [33, 34, 132], the depth where dopants become activated can be determined. The depth for which the value of the integrating SIMS profile exactly matches the extracted carrier density can be considered as the dopant activation depth. We determine a deactivation depth of (2.06 ± 4.18) nm for a $\pm 10\%$ SIMS carrier concentration uncertainty interval.

Our measured values for all Hall bar samples generally agree with published values [26]. We observe a large deviation between estimated dopant density and measured Hall carrier density for sample 2. The difference can be attributed to the change of the linear relation between dose and P coverage due to the limited PH_3 surface dissociation process in the high-coverage regime (see section 4.4.2 and section A.1.3 in the appendix). As a consequence, for high dopant densities (*e.g.* $(0.26 \pm 0.04) \times 10^{14}\,\mathrm{cm}^{-2}$) the dopant density

calibration curve obtained from STM measurements in the low coverage regime becomes incorrect. Results for all Hall bar samples as a function of dopant density appear in Figure 5.4. The extracted mobility of $40.9\,\mathrm{cm^2/Vs}$ fits well to published values of $38\,\mathrm{cm^2/Vs}$

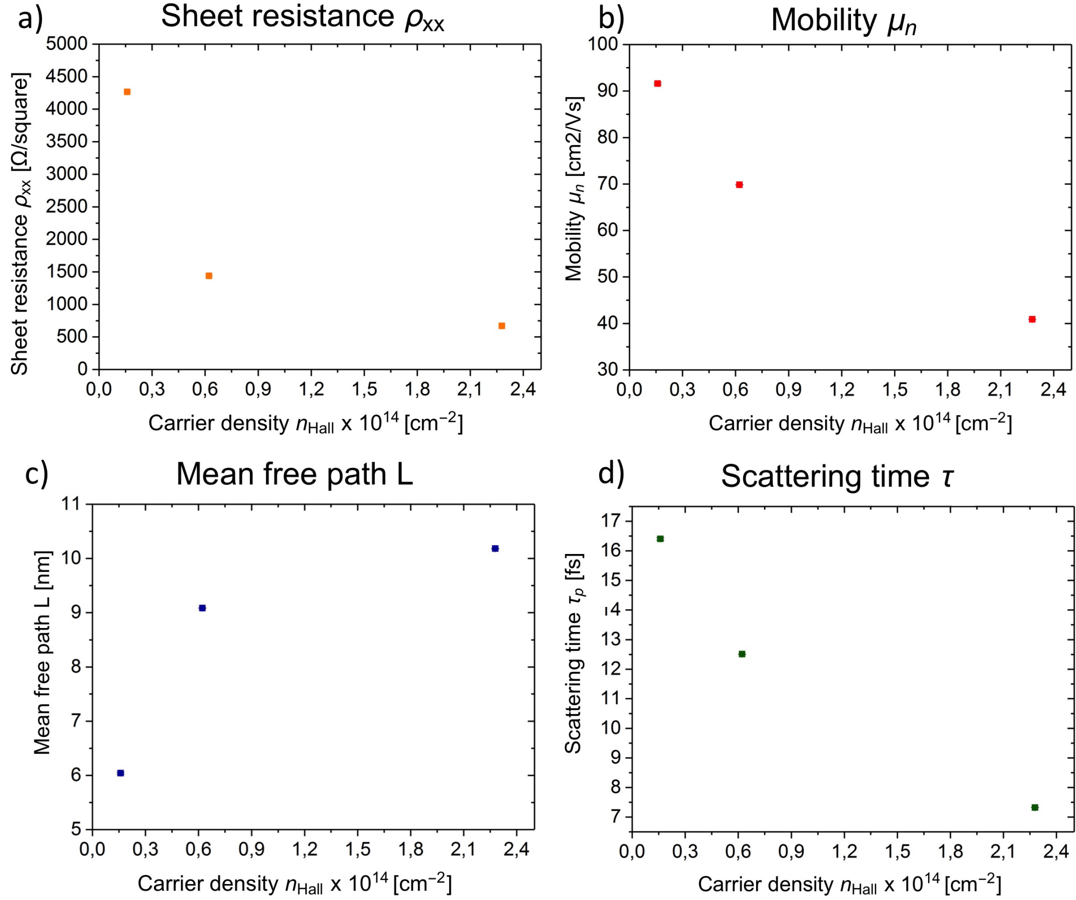


Figure 5.4: Hall measurement results of the δ-layers at 1.8K as a function of dopant density. a) Sheet resistance $\rho_{xx}(0)$, b) Mobility μ_n, c) mean free path L and d) scattering time τ.

for the sample of highest mobility in [166] and $\sim 36\,\mathrm{cm^2/Vs}$ for saturation dosed samples in [26] at 4K. High mobility of $(120 \pm 10)\,\mathrm{cm^2/Vs}$ as obtained in [34] has not been observed, however. In this section we focus on the dopant-density-dependent mobility of the δ-layer.

The low thermal energy ($k_B T = 155\,\mu\mathrm{eV}$) means that the dominant transport mechanism is carrier drift while the mobility is dominated by impurity scattering from ionised donors as noted earlier. In contrast to [166] and theoretical calculations from [71], we see a decrease in mobility as the doping density increases, similar to findings from Goh *et al.* [26, 165] and [164,167]. This can be seen in Figure 5.4b). These results are consistent with the classical Drude picture where a higher dopant density causes an increased impurity scattering rate

which in turn results in reduced scattering time and mobility, see Figure5.4b)+d). Electrons drift in an electric field E with an averaged velocity $v_d = -\frac{\mu}{E}$ due to scattering processes occurring at the characteristic time-scale τ, which is related to the mobility by $\mu_n = \frac{e\tau}{m^*}$. Hence for increasing dopant densities and corresponding decreasing sheet resistance ρ_{xx}, the scattering time τ decreases monotonically.

Although the mobility decreases with n_{Hall}, the mean free path L is observed to increase (seen in Figure 5.4c)). Due to an increasing number of ion impurity centres with higher P densities, we would expect L to decrease. Because $L = v_d \cdot \tau \propto \mu_n \sqrt{n_{Hall}}$, the larger increase in dopant density overcompensates the decrease in mobility. This implies that the increased carriers density dominates the electronic transport despite a corresponding increase in the number of ionised dopant scattering centres, also suggested in [26].

Our results for sample 4 and sample 5 show that no ohmic conduction is observed for critical densities between $n_C \approx 0.26 - 1.30 \times 10^{13}\,\mathrm{cm}^{-2}$, which is in line with experimental findings from [26]. One possible explanation could be the following: when the dopant density decreases, the electrical confinement of the electrons in the 2DEG well is reduced, which leads to a rise of the impurity band energies such that fewer sub-bands are occupied under the Fermi level to maintain charge neutrality [38]. Theoretical calculations point out the strong dependance of sub-band energy on relatively small changes in dopant density in the channel. With decreasing donor density from $2 \times 10^{14}\,\mathrm{cm}^{-2}$ to $1 \times 10^{14}\,\mathrm{cm}^{-2}$, the subband energy increases *e.g.* for $E_{1\Gamma}$ from $-400\,\mathrm{meV}$ to $-200\,\mathrm{meV}$ [38] as pointed out in the Methods and Scientific Background section 2.3.1. With decreasing dopant density the Fermi-level shifts closer to the donor band minimum, resulting in a completely depleted heavy Δ-valley at a doping density of 0.0156 ML ($< 10^{13}\,\mathrm{cm}^{-2}$), calculated for a δ-layer nanowire with a channel width of 1.5 nm [67].

The absence of occupied subbands (modes) for inter-sub-band conduction therefore suggests to limit ohmic conduction significantly at already relatively high dopant densities $\sim 1 \times 10^{13}\,\mathrm{cm}^{-2}$, corresponding to $\sim 3 \times 10^{19}\,\mathrm{cm}^{-3}$, which is significantly higher than the 3D metal-insulator-transition (MIT) density at $n_{\mathrm{MIT}} \sim 3 \times 10^{18}\,\mathrm{cm}^{-3}$ for bulk doped silicon [54].

To conclude, transport measurements confirm the viability of our fabrication strategy for δ-doped layers and the control over P doping at varying densities. Due to a limited ohmic conduction at already relatively high doping densities, control over doping could only be

confirmed for densities $d > 1.3 \times 10^{13}\,\text{cm}^{-2}$. The mobility value for the saturation-dosed sample agrees with those found in literature. The sensitivity of the δ-layer conduction to small changes in dopant densities is supported by a critical dopant density for ohmic conduction between $n_C \approx 0.26 - 1.30 \times 10^{13}\,\text{cm}^{-2}$, which implies strong dependance of sub-band energy on relatively small changes in dopant density in the channel.

5.4 Vector-field characterisation of magneto-conductance in a saturation δ-layer

5.4.1 Weak localisation and vector-field dependence

We now turn our attention to the MT properties of single saturation-dosed δ-layer Hall bar, namely WL. WL is a result of interfering electron waves that form closed localised trajectories [169]. Time-reversal symmetry requires that the probability of an electron forming a closed trajectory through a series of elastic scattering events be equal to forming the same trajectory in the opposite direction. As the same area is enclosed either way then as long as the trajectory is within the inelastic scattering length the paths constructively interfere at the origin, leading to a localisation of charge and thus a reduction in conductance. Any inelastic process that adds a phase difference between the interfering waves leads to random interference, which results in a reduced backscattering probability, as described in weak localisation theory *e.g.* by Altshuler *et al.* [155]. The flux from a perpendicular magnetic field introduces an Aharonov-Bohm phase difference Φ between oppositely directed and closed electron paths

$$\Phi = \frac{2S}{l_m^2} \tag{5.8}$$

where S is the area enclosed by the trajectory and $l_m = \sqrt{\frac{\hbar}{eB}}$ is the magnetic length. Since the area of the different trajectories lies on a distribution then the phase differences acquired by the different trajectories goes from exactly zero at zero field to a broad distribution as the field is increased, thus destroying the localisation effect. The phase coherence length is the mean distance over which the wave function loses phase coherence, and hence determines the maximum size and number of coherent backscattering loops that can be formed at $B = 0$ (where the maximum loop area is $S = \frac{L_\phi^2}{4\pi}$). The MC contribution to a 2D system in a perpendicular field is reflected in the shape of the MC curve whose height and width is controlled by L_ϕ (at a given mean free path L). The longer the coherence length, the larger

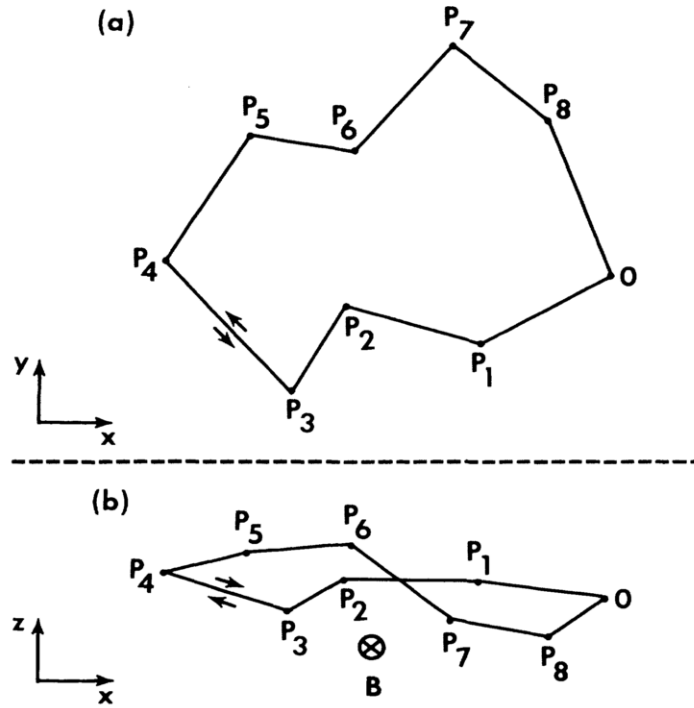


Figure 5.5: Weak localisation effect in a thin 2D film with finite thickness: a) A possible path of an electron propagation along a closed loop, which contributes to the weak-localization correction to the conductivity, projected on the xy-plane. A perpendicular magnetic field $B_\perp$ introduces a phase shift between interfering oppositely-directed electron waves and suppresses the weak localisation contribution. b) The same path projected on the xz-plane but now perpendicular to the parallel magnetic field $B_\parallel$. Due to a spread in mean electron position, a possible path for electron propagation is created along a closed loop, perpendicular to the 2D plane (from [153])

the number and size of loops and the more pronounced is the MC zero B peak (see Figure 5.7b)). The correction to the conductivity from weak localisation in a 2D sheet (at B=0) is given by [150] as

$$\Delta\sigma_{WL} = -\sigma_n ln\left(\frac{\tau_\phi}{\tau}\right). \tag{5.9}$$

where $\sigma_n = \frac{e^2}{2\pi^2\hbar}$. A perpendicular magnetic field can turn off the WL contribution and the expected conductance correction originating from 2D weak localisation is given by the Hikami-Larkin-Nagaoka equation [150] by

$$\Delta\sigma(B_\perp) = \left(\frac{e^2}{2\pi^2\hbar}\right)\left[\Psi\left(\frac{1}{2}+\frac{\hbar}{4DeB_\perp\tau_\phi}\right)-\Psi\left(\frac{1}{2}+\frac{\hbar}{4DeB_\perp\tau}\right)+ln\left(\frac{\tau_\phi}{\tau}\right)\right], \tag{5.10}$$

where Ψ is the digamma function. When fitting the formula to the magnetoresistance curve with magnetic field out-of-plane, the phase coherence length L_ϕ and mean free path L can

be determined by fitting both as free fitting parameters. Equation 5.10 is valid for the highly diffusive 2D regime, below a critical field of $B_0 = \frac{\hbar}{2eL^2}$ and in the limit of zero thickness. The formula depends only on the perpendicular magnetic field component. The weak localisation contribution to the conductance arising from a parallel field for thin films was predicted by Altshuler *et al.* [170]. Mensz *et al.* [153] showed from MC measurements of an inversion MOSFET layer that an additional parallel field $B_{\|}$ induces a phase-breaking rate $\frac{1}{\tau_B}$ which decreases the device resistance. The total phase-breaking rate is given by the addition of two independent rates resulting in an effective phase-breaking rate τ_{eff}

$$\frac{1}{\tau_\phi} \rightarrow \frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_\phi} + \frac{1}{\tau_B} \tag{5.11}$$

By including this into Equation 5.9, an expression for the change in conductance in parallel field is obtained as

$$\Delta\sigma(B_{\|}) = \sigma_n ln\left(1 + \frac{\tau_\phi}{\tau_B}\right), \tag{5.12}$$

Mensz *et al.* found an expression for the additional phase breaking rate $\frac{1}{\tau_B}$ in the 'dirty' limit ($d >> L$, where d is the film thickness), given as

$$\frac{1}{\tau_B} = \frac{4D\overline{\delta z_{av}^2}}{l_m^4} = \alpha B_{\|}^2, \tag{5.13}$$

where $\overline{\delta z_{av}^2}$ is the standard deviation of the electron position across the film. They interpreted the observed reduction in resistance to fluctuations of the mean electron position z during the motion along the interface in xy-plane. The potential fluctuations are attributed to the Si/SiO_2 interface roughness. The spread in mean electron position creates a possible path for electron propagation along a closed loop, perpendicular to the 2D plane, as schematically shown in Figure 5.5b). By fitting $\frac{1}{t_B}$ against $B_{\|}^2$ they could extract α, which in turn allowed them to determine the root-mean-square height value of the interface to be $\Delta < 0.210 \pm 0.015$ nm. Anderson *et al.* [171] used the method to measure the Si/SiO_2 interface roughness of a clean and intentionally textured MOSFET. Good agreement was demonstrated between roughness measured via WL and atomic force micrcoscopy (AFM) ($\Delta = 0.12 - 0.13$ nm and $\Delta = 0.55$ nm, for a clean and intentionally textured MOSFET, respectively). Later, Mathur and Baranger provided a relationship between the interface roughness parameters and the measured MC [172]. In addition to the RMS height fluctuations Δ they introduced the

correlation length L_c, the distance over which the fluctuations are correlated, as a roughness parameter to the expression of the phase breaking rate $\frac{1}{\tau_B}$. They showed that when the roughness is correlated over a very short length scale ($L_c < L$) the effect of the parallel field decreases the dephasing length and homogeneously broadens the MC curve of the perpendicular field. The MC contribution for parallel field is then determined as

$$\Delta\sigma(B_{\parallel}) = \sigma_n ln\left(1 + \frac{\tau_\phi}{\tau_B}\right) = \sigma_n ln\left(1 + \sqrt{4\pi}\frac{e^2}{\hbar^2}\frac{L_c}{L}L_\phi^2\Delta^2 B_{\parallel}^2\right), \tag{5.14}$$

where Δ is the root-mean-square height fluctuations or d, the averaged 2D film thickness. There is no independent measurement to determine L_c. Following [151] the correlation length is approximated by the mean donor spacing, $L_c = \frac{1}{\sqrt{n_d}}$, estimated to be $\sim 1\,\text{nm}$. Sullivan *et al.* [151] applied the 'WL technique' to δ-layers and showed that the RMS surface roughness of the model can provide an estimate of the δ-layer width for different annealing temperatures. Hagmann *et al.* [25] investigated how the spreading of the donor distribution is reflected in the WL contribution to the conductance. They achieved high in-plane dopant confinement by depositing 15 ML of Si at room temperature prior to encapsulation, a so called 'Locking layer' (LL). They found that the LL suppresses the phase-breaking rate $1/\tau_B$ compared to a saturation-dosed δ-layer without a LL. This is caused by a higher in-plane confinement of the P atoms which is supported by SIMS analysis (WL width of 24.2 nm and 0.85 nm without/with a LL, respectively). The drawback of using a LL for δ-layer sample growth is a reduced mobility and possibly L_ϕ due to scattering at interfacial impurities. A pronounced interface contrast near the δ-layer for the LL sample is observed in transmission electron microscope (TEM) images,

	2D system	L	L_ϕ	$n_s \times 10^{14}$	$n_s \times 10^{21}$	d	T
		[nm]	[nm]	[cm^{-2}]	[cm^{-3}]	[nm]	[K]
[152]	Ge:P δ-layer	5	184	0.63	0.42	1.49	5
[35]	Si MOSFET	48	252	0.07	0.007	10	1
[173]	Graphene	50	900	0.005	~ 0.005	~ 1	0.015
	Current work	15	320	2.8	0.30	9.44	0.022
[25]	sat. P δ-layer	16	150	1.9	0.08	24	2
[25]	sat. P δ-layer LL	4.3	53	0.72	0.85	0.85	2
[151]	sat. P δ-layer	30	101	1.4	0.1	14	0.2

Table 5.2: Typical parameters for 2D systems. L and L_ϕ are the mean free path and the phase coherence length, respectively. n_s(2D) and n_s(3D) are 2D sheet density and corresponding 3D carrier densities, respectively, by considering the thickness d of the layer.

which results in an increased defects density at this interface and in a reduced carrier density and activation of donors.

We applied the WL method as described by Sullivan *et al.* to a saturation-dosed δ-layer to obtain an estimate of the width of δ-layer. Typical parameters for some 2D systems appear in Table 5.2 and it is apparent that the δ-layer technique produces the densest 2D systems, while retaining the coherence characteristics at low temperatures.

5.4.2 Sample and vector magnet setup

The saturation-dosed Hall bar (sample 1) was mounted in a dilution refrigerator with a 3D vector magnet capable of a field magnitude of 2T in all directions, depicted in Figure 5.6a). The PCB carrier with mounted temperature sensor and wire bonded samples appears in Figure 5.6b). The base temperature was $\sim$ 13 mK and 22 mK with sweeping fields. Transverse

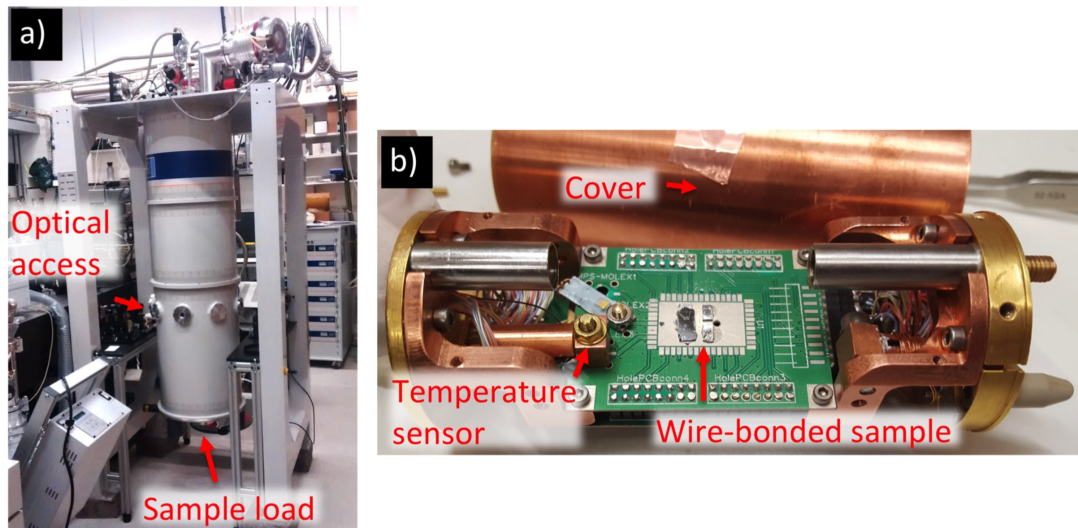


Figure 5.6: a) Dilution refrigerator with a 3D vector magnet capable of a field magnitude of 2T in all directions. The base temperature was 13 mK. b) PCB carrier with mounted temperature sensor and wire bonded samples.

and longitudinal resistances were measured for linear field sweeps, with the magnetic field out of plane (Z), in plane (X and Y), and for angular sweeps at a field magnitude of 2T in all three planes. The temperature was varied from 22 mK to 30 K. Additionally, angular sweeps were performed at 22 mK with different field magnitudes, from 2T to 0.1T. The current was fixed to a constant 114 nA in all magneto-resistance (MR) measurements. The current modulation frequency in all measurements was 7.6 Hz. The main axes of the magnetic field were finely adjusted by applying a maximum in-plane field in the X and Y directions and minimising the Hall effect.

5.4.3 Magneto-transport results

Typical Hall resistance and magneto-resistance curves obtained at 22 mK are shown in Figure 5.7. The Hall measurement yields a mean free path of 15 nm and a sheet carrier

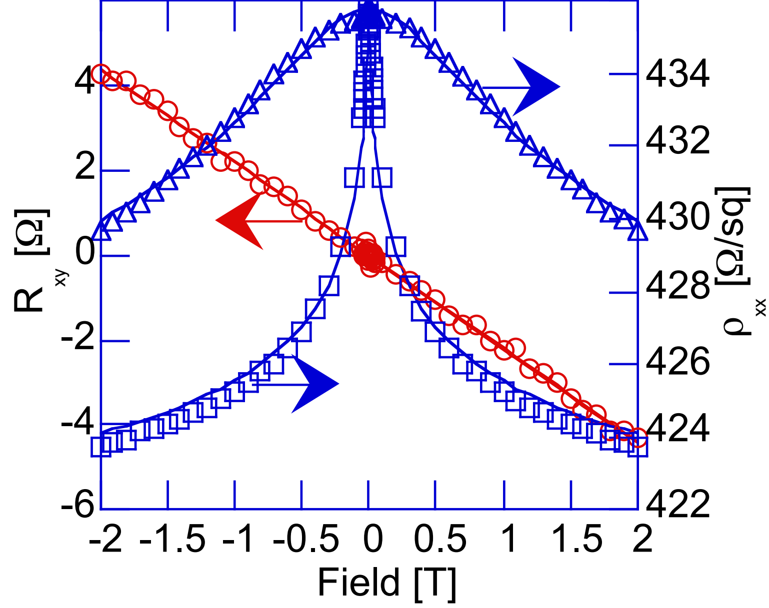


Figure 5.7: Typical Hall and magneto-resistance curves obtained at 22 mK. Magnetoresistance curves with magnetic field out-of-plane (blue squares) and in-plane (blue triangles) were fit to Equation 5.10 and 5.12. The Hall resistance curve with magnetic field out-of-plane (red circles) is fit to Equation 5.3. Measurements performed by Guy Matmon.

density of $n_{Hall} = (2.87 \pm 0.03) \times 10^{14}\,\mathrm{cm}^{-2}$, which displays a 26% larger value of carrier density and slightly increased electron mobility of $\sim 52\,\mathrm{cm}^2/\mathrm{Vs}$ compared to the same saturation-dosed Hall bar in the previous measurement in section 5.3.4. Equations 5.10 and 5.12 were fit to the MC curves in perpendicular and in-plane field respectively, revealing a coherence length of 320 nm at 22 mK and a δ-layer thickness of $d = 9.44 \pm 0.47$ nm, with a negligible temperature dependence. For a good comparison with reference [151] and [25] we estimated the correlation length as $L_c = 0.59$ nm by using the determined n_{Hall} from our Hall measurements. Note that the correlation length is actually dependent on the δ-layer thickness and thus not independent of Δ. Fitting α in Equation 5.13 by using Δ and L_c as free fitting parameter would take this dependancy into account. The temperature dependences of L_ϕ, L and the conductivity at zero field $\sigma(0)$ as derived from the fits are plotted in Figure 5.8a). For the mean free path a weak temperature dependence is observed, in contrast to the coherence length, which increases with decreasing temperature until it saturates at around ~ 300 mk. With increasing temperature L_ϕ tends towards L, as temperature-induced

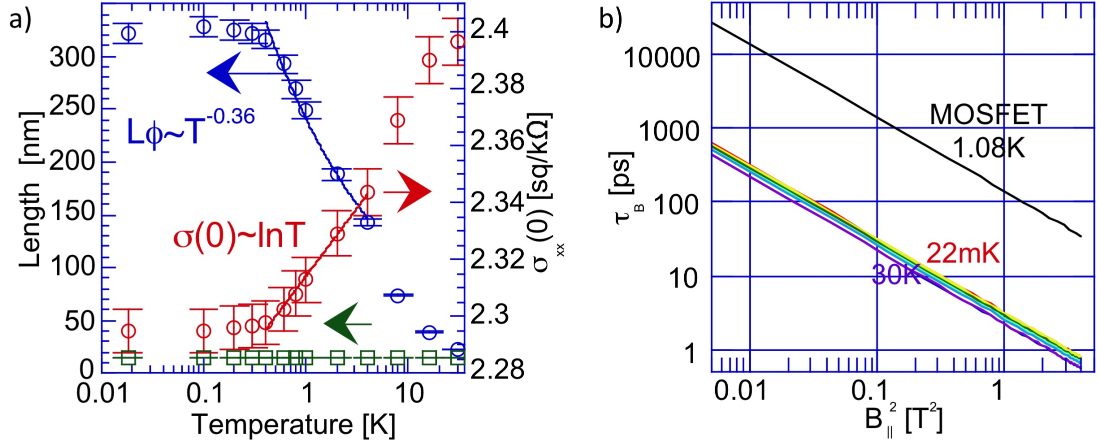


Figure 5.8: (a) Temperature dependence of L_ϕ (blue circles), L (green squares) and the conductivity at zero fields (red circles) as derived from the fits. The error bars are 95% confidence intervals. L_ϕ displays a $T^{-0.36}$ dependance while the conductivity scales with $\sim ln(T)$ between 3 K and 300 mK. The mean free path is $\sim$ 15 nm and temperature independent in this temperature range. b) The extracted phase-breaking time τ_B from Equation 5.13 is plotted against $B_{||}^2$ for different temperatures together with the MOSFET data from [153] (black line). Measurements performed by Guy Matmon

dephasing increases. Above 4K MT in 2D is dominated by electron-phonon interaction [174]. From fitting L_ϕ between 3K and $\sim$ 300 mK we extract a power law dependance of $L_\phi \sim T^{-0.36}$. The zero field conductivity $\sigma(0)$ scales with $ln(T)$ in the same temperature range, before saturating as well at low temperatures, $T < 300$ mK . The extracted phase-breaking time τ_B is derived from fitting equation 5.13 and is plotted against $B_{||}^2$, together with MOSFET data from [153].

A full angular dependent MC measurement was carried out as a function of temperature and magnetic-field strength and results are shown in Figure 5.9. In Figure 5.9a) the longitudinal MC $\Delta\sigma_{xx}$ (blue line) is plotted as a function of the tilted magnetic field angle at 22 mK for a constant field magnitude of 2 T. The green points show the sum of perpendicular and parallel MC traces at field strengths corresponding to the angular 2T measurement. Beside matching at angles of $0°, 90°, 180°$ and $270°$, where one field component is zero, the traces for detected MC in tilted fields does not converge with the sum of perpendicular and parallel MC traces. We found a power-mean (p-mean) relation that links the MC due to the perpendicular and parallel fields, to the MC caused by their constituent vector field:

$$\Delta\sigma^p = \Delta\sigma_{||}^p + \Delta\sigma_{\perp}^p. \tag{5.15}$$

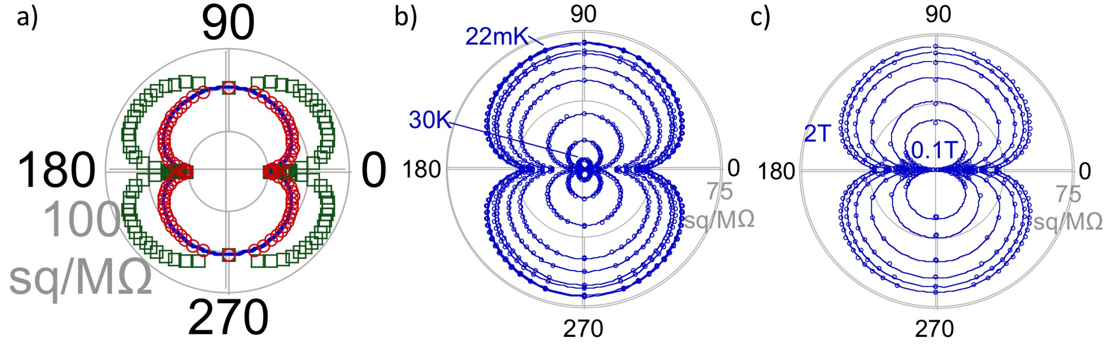


Figure 5.9: Angular MC. a) The longitudinal MC $\Delta\sigma_{xx}$ (blue line) as a function of the tilted magnetic field angle at 22 mK and constant field magnitude of 2 T. Sum of $\Delta\sigma_{||}$ and $\Delta\sigma_{\perp}$ at field strengths corresponding to the angular 2T measurement (green circles). A p-mean fit of in-plane and out-of-plane MC yields $p = 4.18 \pm 0.10$ (red points).b) Longitudinal MC and p-mean fits at 22 mK − 30 K (2 T) and c) for 0.1 T to 2.0 T (22 mK). Measurements performed by Guy Matmon.

Fitting the perpendicular and parallel field MC with Equation 5.15 yielded a p value of 4.18 ± 0.10 (red points). This p-mean relation holds over temperature, shown in Figure 5.9b) for a temperature range of 22 mK − 30 K, and fields from 0.1 T to 2.0 T, shown in Figure 5.9c). This remarkably simple form characterises all data except those with B nearly parallel to the planes. In brief, p represents a generalised, anisotropic power-law dependence of the quasi-2D MC on the magnetic field, analogous to the power law derived by Kawabata *et al.* [175]. The discussion about the p-mean relation is beyond the scope of this thesis; for details see [1]. In the discussion we will focus on the following: the coherence length, its dephasing mechanism, and the layer thickness which can provide insights about active P distribution of the δ-layer.

5.4.4 Discussion and summary

A very high Hall carrier density of $n_{Hall} = (2.87 \pm 0.03) \times 10^{14}\,\mathrm{cm}^{-2}$ is obtained which is higher than expected from previous measurements. Furthermore, the increase in carrier density of 26% compared to previous measurements in section 5.3.4 indicates a large deviations of this quantity for a sample, subsequently measured in two different setups. We could not find a reasonable explanation for this large deviation.

The phase breaking time τ_B is found to scale with $B_{||}^2$ as expected from Equation 5.13. The lower proportionality coefficient of 1.5 orders of magnitude compared to previous MOSFET results [176] suggests that the in-plane field in our work has a larger phase-breaking effect. This is supported by the large thickness.

Measuring the WL contributions to the MC in parallel fields does not probe the ion core den-

sity of P atoms like SIMS, but measures the electron spread in z during electrical transport. This provides an indirect method to detect the width of the Coulomb potential of activated P dopants which confine the charge carriers in the δ-layer. To put this value in relation to the dopant distribution of the δ-layer we compare the extracted thickness to a SIMS profile obtained on a saturation δ-layer that was fabricated under the same experimental conditions (for further details see section 6.7). To identify the P density range that could potentially contribute to the MC, the 3D MIT-transition density ($n_{\mathrm{MIT}} \sim 3 \times 10^{18}\,\mathrm{cm}^{-3}$, blue line) and the critical dopant density $n_C \sim 1 \times 10^{13}\,\mathrm{cm}^{-2}$ (gray line) found for δ-layers, that possibly marks the 2D weak-to-strong-localisation-transition, are indicated in the SIMS profile in Figure 5.10. The corresponding 3D density of n_C is $\sim 1 \times 10^{19}\,\mathrm{cm}^{-3}$, assuming a δ-layer thickness of $d = 10\,\mathrm{nm}$.

From dopant activation calculations in section 5.3.5 and the decay of the oxide concentration (grey points) of approximately two orders of magnitude, we estimate P dopant activation for a sub-surface depth below 2 nm. The region which is 9.44 nm around the peak of highest P density at $d_\delta = 14.5$ nm (highlighted in yellow in Figure 5.10) comprises a total number of $n_d = (2.08 \pm 0.21) \times 10^{14}\,\mathrm{cm}^{-2}$ active P dopants which is $(91.2 \pm 0.9)\%$ of the whole dopant profile. The MC measurement of the carrier density suggests that this region confines 2.87×10^{14} electrons per cm^2 during electrical transport.

That would result in a 27.5% difference between the measured Hall carrier density and n_δ obtained from SIMS. If we assume that during electronic transport in δ-layers electrons are spatially confined to regions of maximal dopant density, the increased carrier density would imply enhanced occupation of sub-bands which would result in an effective charging of the δ-layer sheet. Further, from the detected $9.44\,\mathrm{nm}$ width of the δ-layer we conclude that electron occupation of impurity bands during transport does not occur in region $< 6\,\mathrm{nm}$ close to the surface. Electron transport directly under the surface seems to be prohibited, although a fraction of dopants in this region should be activated and their concentration lies above the critical dopant densities N_C for ohmic conduction.

This observation is supported by WL thickness measurement of a δ-layer by Hagmann *et al.* [25], where WL determined a thickness of 24 nm and SIMS a δ-layer profile of 30 nm, indicating that MC in the first 6 nm was not observed. They assume that the conduction contribution originates from layers with densities higher than the 3D MIT concentration. As discussed in section 5.3.5, Ohmic conduction in δ-layer is only observed for densities

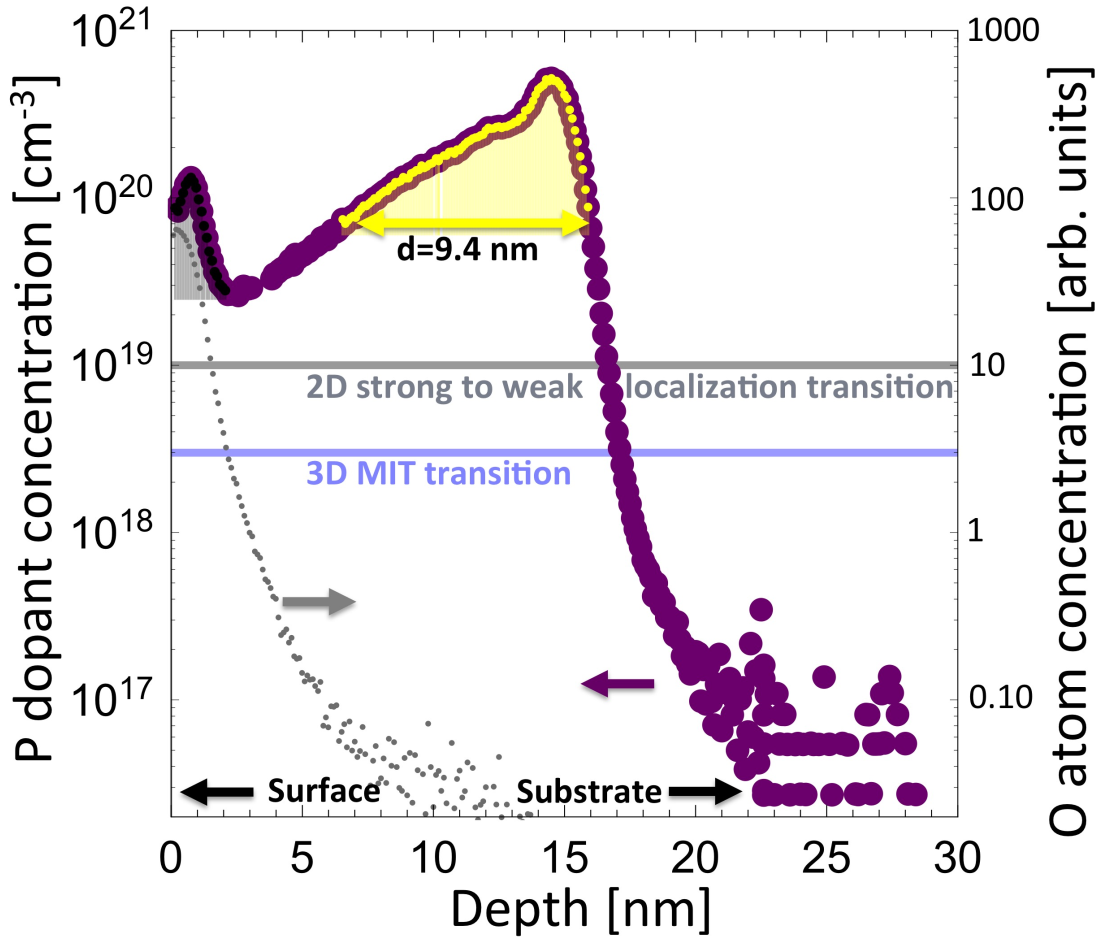


Figure 5.10: SIMS dopant profile of P (purple) and O (gray) atoms for a saturation-dosed δ-layer. The horizontal lines indicates the value for a 3D metal-insulator-transition density of $n_{\mathrm{MIT}} = 3 \times 10^{18}\,\mathrm{cm}^{-3}$ (blue line) and the 2D weak-to-strong-localisation transition density of $n_{\mathrm{C}} \sim 1 \times 10^{13}\,\mathrm{cm}^{-2}$ (grey line) found for the δ-layer, corresponding to $n_{\mathrm{MIT}} \sim 1 \times 10^{19}\,\mathrm{cm}^{-3}$ by assuming a δ-layer thickness of $d = 10\,\mathrm{nm}$.

higher than N_C, from which we can conclude that the assumption that only regions above 3D MIT transition level contribute to charge conduction was not strong enough.

The large width of the δ-layer is the reason for an increased phase breaking time τ_B compared to the measured 0.2 nm and 0.13 nm Si/SiO_2 interface roughness for MOSEFTs [171, 176]. In contrast to the MOSFETs where electrons are confined to the oxide interface layer by an applied gate bias, the Coulomb potential of the δ-layer restricts the electron position to the P dopant distribution. Thus, the WL methods applied to δ-layers is not sensitive to the surface roughness via induced potential fluctuations and resulting change in mean electron position z_{av} as described by Mensz *et al.* [176]. Instead, the finite thickness of the δ-layer is caused by P segregation, and possible paths for electron propagation along

a closed loop are created by a large spread in mean electron position perpendicular to the 2D plane. Because $L_\phi >> d$, the maximum size of backscattering loops in the xz- and yz-plane is determined via S $\propto L_\phi \cdot d$. This means that the z contributions to the overall intersection path length is small and thus the effective phase-breaking rate $\frac{1}{\tau_{\text{eff}}}$ displays only a weak dependance on the parallel field component. The use of a locking layer in a δ-layer was demonstrated to increase the dopant confinement by suppressing P segregation during sample growth, especially the pronounced dopant tail from the peak towards the surface in the SIMS profile. The LL minimises segregation and thus decreases the phase-breaking time τ_B. In turn, the increased scattering of interfacial impurities was found to result in a decreased mobility and L_ϕ.

We now focus on the coherence length. The measured coherence length of 320 nm at 22 mK is among the longest reported in literature (Longest reported value is 450 nm in [162]), indicating strongly coherent transport in the δ-layer and a reduced number of dephasing sources. The dominant dephasing mechanism at low temperatures in a disordered quasi-2D system has been found to be electron-electron interactions (EEI). Conduction electrons scatter with a fluctuating electromagnetic field produced by other electrons in motion. This so-called Nyquist noise leads to dephasing and a $T^{-1/2}$ temperature dependance of L_ϕ [177]. This temperature dependance is commensurate with findings for the δ-layer in the same temperature range [162]. From fits between 3K and $\sim$ 300 mK we extract a power law dependence for L_ϕ of approximately $\sim T^{-0.36}$, which suggests a highly disordered conducting 2D system with slightly reduced EEI. L_ϕ saturates at around $\sim$ 300 mK which has been observed for other materials and systems [162, 178–182]. We attribute the saturation of L_ϕ to a real physical mechanism and not to a extrinsic measurement effect due to a possible saturation of the sample temperature, as demonstrated in [162]. We claim this because we see that the magnitude of the zero-field peak caused by the superconducting transition of the aluminium contacts ($T_c \sim 1.2$ K) is still temperature-dependent at these low temperatures [162, 183]. The physical effect that dominates the saturation at low temperatures is still under debate.

To conclude, the sensitivity of the WL contribution to conductance in parallel and perpendicular fields can be used to probe the 'electrical width' of electrons confined in a δ-layer donor potential while undergoing electrical conduction. The extracted thickness of $\sim$ 10 nm, together with the large phase-breaking rate $1/\tau_B$ point towards inactive dopants at the sur-

face region and/or an increased scattering rate close to the surface. This might be due to trapped charges in the Si/SiO_2 interface and/or in the native silicon oxide. Further, we conclude that transport is restricted to regions comprising dopant densities above N_C. From the comparison between the SIMS profile and the electrical δ-layer width extracted from WL it can be concluded, that electrons only undergo electrical transport below a subsurface depth of $\sim 6\,\text{nm}$. That implies that a fraction of δ-layer dopants does not actively contribute to MT, although they are assumed to be activated and their density lies above N_C. A possible reason might be an increased phase-breaking rate at this depth (*e.g.* due to trapped charges at the Si/SiO_2 interface) and the high sensitivity of the 'WL method' to phase-breaking sources. In contrast to SIMS and ATP, this method provides a way to probe sharp dopant profiles with high spatial resolution. The large phase coherence length confirms a high crystal quality of our samples with a low number of in-plane dephasing sources and a somewhat reduced EEI within the δ-layer.

Chapter 6

Scanning microwave microscope detection of buried phosphorus

6.1 Introduction

One of the several exciting proposals for a surface code quantum computer (SCQC) [21] by Hill *et al.* is schematically shown in Figure 6.1. In this architecture, single dopant

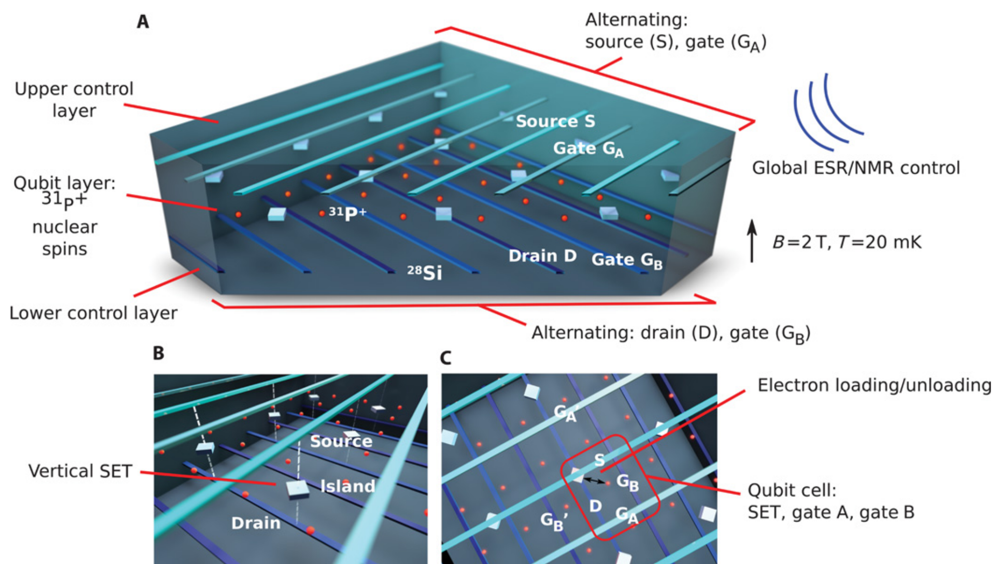


Figure 6.1: Physical layout of a donor-based surface code quantum computer. a) The system comprises three layers. The 2D donor qubit array is located in the middle layer while a perpendicular pattern of control gates (5 nm in width and 30 nm in pitch) reside in the top and bottom layer by forming a regular grid of cells. b) A vertically defined island forms a single electron transistor which is patterned by STM. c) A single P donor is located at the centre of each cell defined by the boundaries of G_A, G_B, source and drain lines (From [21]).

qubits are manipulated and read out using single-electron transistors (SETs) and a crossbar array of electrodes. Both the SETs and the array of electrodes are fabricated from pre-

cisely placed arrays of dopants, below the silicon surface, on three separate layers. However the fabrication of these buried nano wires in multiple separated layer in silicon is very challenging. Only one multi P layers in silicon device has been reported in literature. In this study [184], McKibbin *et al.* contacted a few nm wide δ-doped silicon phosphorus wire and demonstrated conductance modulation using another 45 nm vertically separated δ-doped silicon nanowire, perpendicularly aligned, as top-gate, as can be seen in the 3D schematic in Figure 6.2c) . There are several challenges for the fabrication of nanoscale

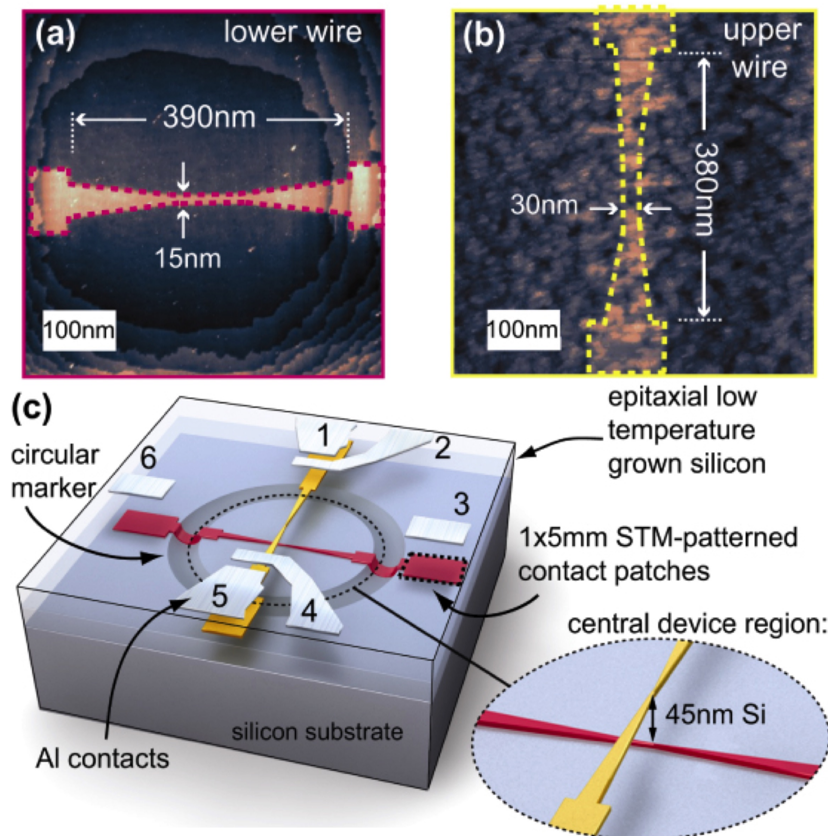


Figure 6.2: Epitaxial top-gated atomic-scale silicon wire in a three-dimensional architecture, forming independent contacts to vertically separated STM-patterned wires. (a) STM images after H depassivation show lower nanowire on flat Si(001)-2×1 and (b) the upper tapered nanowire on the overgrown silicon surface. (c) Schematic showing two STM-patterned wires with 45 nm of epitaxial Si vertically separating them. The Al contacts (silver layer), evaporated ex situ, are aligned to the buried STM-patterned wires allowing $I-V$ measurements (From [184]).

three-dimensional (3D) epitaxially doped circuits. One is precisely aligning vertically separated STM-patterned structures to each other and making independent contact to each layer. Once the first structure has been annealed and encapsulated with silicon the resulting overgrown silicon surface is rough (increased surface roughness of $\Delta R_{\mathrm{RMS}} = 0.32$ nm after over-

growth of 5 ML of Si on a flat silicon surface at $T = 110\,^{\circ}\mathrm{C}$ [185]). No contrast in STM topography images between the previously patterned and doped area and the surface of the overgrown silicon prohibits a precise alignment of the second nanostructure. In addition, to minimise surface roughening of the second layer for re-patterning, the incorporation and encapsulation process needs to be optimised for a successful H passivation and subsequent STM H-lithography. To achieve maximum dopant activation whilst minimising dopant diffusion for the first and second layer the thermal budget needs to be carefully tuned. These challenges/difficulties can be overcome by developing a growth and process recipe that includes the use of a locking layer as will be described in section 6.8.2. Another issue is the capability of imaging buried dopant nanostructures and characterising their quantitive properties such as sheet resistance at various points of the fabrication process, for example, after the first silicon encapsulation step or at the end of the STM device fabrication before contacting. Acquiring information of the quality of buried nanostructure at an early stage of the device fabrication process and hence understanding variations between devices as they relate to their performance, could tremendously speed up the field of device fabrication.
So far, fabricated devices are electrically characterised by transport measurements *i.e.* by performing laborious Hall and magneto-resistance measurements. Before the work described here, no non-destructive techniques existed that could quantitatively image dopants in 3D and especially access intrinsic electrical properties of patterned δ-layers. STM itself offers only limited subsurface sensitivity for imaging [185]. In Figure 6.3 shallow buried P nanostructures in Si are spectroscopically probed in situ with current imaging tunnelling spectroscopy (CITS). CITS is able to probe the local density of states (LDOS) and is less affected by surface roughness than topographic STM imaging because variations in the tunnelling current translate into topographic height changes only by a weak logarithmic dependence [185,186]. However, even after encapsulationg with just 5 ML of silicon at $110\,^{\circ}\mathrm{C}$ and applying a RTA at $500\,^{\circ}\mathrm{C}$ for 5 s, only a very low contrast originating from P electrical properties could be detected. Using this technique it is doubtful that deeper buried nano structures display enough contrast to locate their position. Once exposed to air the native oxide growth further limits the applicability of STM to image buried dopant structures of final devices. SPM techniques that probe the local impedance based on applying alternating electric fields are more sensitive to subsurface features because the field penetrates further in the crystal. Electrostatic force microscopy (EFM) and scanning capacitance microscopy

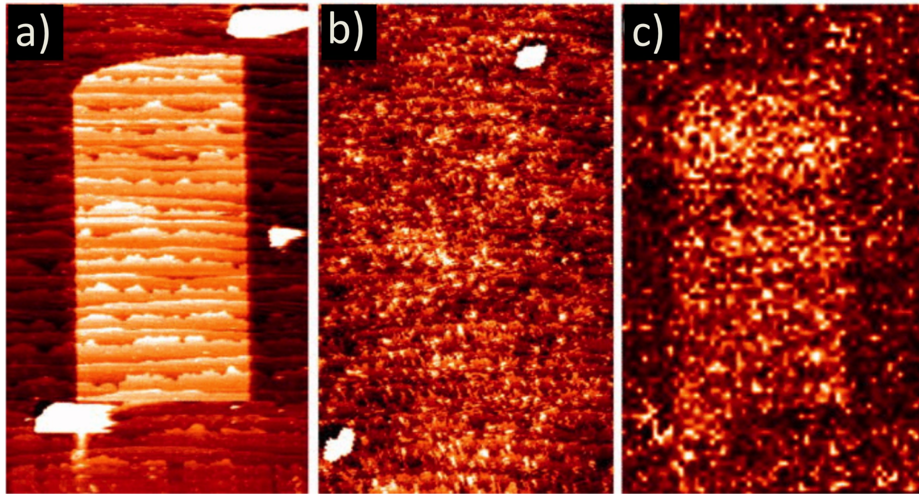


Figure 6.3: Changed labelling in Figure Patterning and imaging of P nano structures with STM: a) A topographic STM image (260 nm × 530 nm) of patterned hydrogen resist layer ($V_s = -2.0$ V, $I = 0.15$ nA), written using $V_s = +6.0$ V and $I = 1.5$ nA. b) A topographic STM image of the same area after P doping, 5 ML Si growth at room temperature and a 550°C anneal ($V_s = -1.3$ V, $I = 0.15$ nA). (f) CITS image obtained at +1.0 V, taken simultaneously with c), showing the 2D buried P nanostructure, as defined by the lithography in (d) (From [185]).

(SCM) are established techniques that measure the differential capacitances $\partial C/\partial V$ at kHz and mHz frequencies, are capable of imaging subsurface features [187–189]. However, the data depicted in Figure 6.4 only provides qualitative image contrast by measuring only the imaginary (capacitive) part of the complex sample impedance. The relatively low mea-

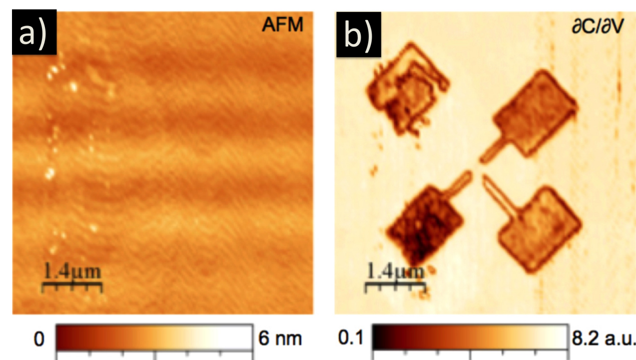


Figure 6.4: Changed labelling in Figure AFM and SCM images of a buried single electron transistor (SET) donor structure. a) Contact mode AFM image over the donor region showing the flat topography (1 nm roughness). b) SCM amplitude ($\partial C/\partial V$) over the donor structure. Contrast is due to variations in the dopant density (From [189]).

surement frequency limits overall signal strength such that no material information can be obtained [190, 191]. In addition, SCM neither provides electrical characteristics nor enables the extraction of the sub-surface depth.

In this chapter we use a scanning microwave microscope (SMM) developed by Keysight Technologies and others to image and electronically characterise 3D phosphorus nanostructures fabricated via hydrogen resist lithography. We show that SMM, which operates at higher frequencies ($1-20\,\mathrm{GHz}$) can measure the complex impedance of the buried nanostructures which gives access to both dielectric [192–194] and conductivity [191, 195, 196] properties, in particular of buried dopants [193, 195, 197, 198]. SMM-experiments can be performed with virtually no sample modification unlike other destructive imaging methods such as focused ion beam milling [199], secondary ion mass spectrometry (SIMS) [200] and/or transmission electron microscopy (TEM) [201]. By simply using a standard atomic force microscope (AFM) [202] or STM [203], combined with a vector network analyser (VNA) [204], a resonating network probes the minute electrical changes coming from the SMM probe.

For the development of an experimental method with the capability of extracting useful parameters such as depth, conductivity and capacitance there are strict qualitative requirements for the sample fabrication. The fabrication of these characterisation samples is one key result of this thesis. By using optimised growth parameters the layers are densely packed ($1.4\,\mathrm{atoms/nm^2}$) and can be confined to widths of a few nm, with near 100% carrier activation, within the confined region [34]. The capabilities demonstrated here are transformative for non-invasive diagnostics of atomic scale electric components that will form the next generation of 'classical' and quantum devices.

First, the basic concept for a SMM is explained and the experimental setup used is briefly sketched. The calibration procedure that allows extraction of quantitive parameters is explained. For this study two key samples have been fabricated and their growth process is highlighted. Subsequently results of SMM measurements obtained from these two samples are reported. First, on sample 1 we demonstrate how SMM combined with calibration and modelling allows depth and conductivity extraction of buried P nano structures. Then, the developed method is applied to an advanced 3D P rectangular 'multi-bar' structure (sample 2). For the fabrication of the complex 3D sample an advanced growth recipe has been developed. From fine patterns written on sample 1 we then estimate the lateral resolution and sensitivity of the SMM technique. Finally, in the discussion we compare sheet dopant density and silicon capping layer thickness extracted from δ-layer Hall bar samples from chapter 5 and secondary ion mass spectrometry (SIMS) measurements to results extracted

with SMM. SIMS and Hall bar measurements provide additional information about dopant distribution and activation of the δ-layer.

This study was carried out as part of a collaboration, where sample fabrication, measurement and part of the analysis was carried out by the author. Measuring, modelling and analysing of the obtained data has been done by George Gramse. The results of the collaboration have been published here [2].

6.2 Scanning microwave microscope setup

The basic SMM setup is conceptually straightforward and is shown together with the calibration and workflow for dopant depth extraction in Figure 6.5. A VNA is connected to a

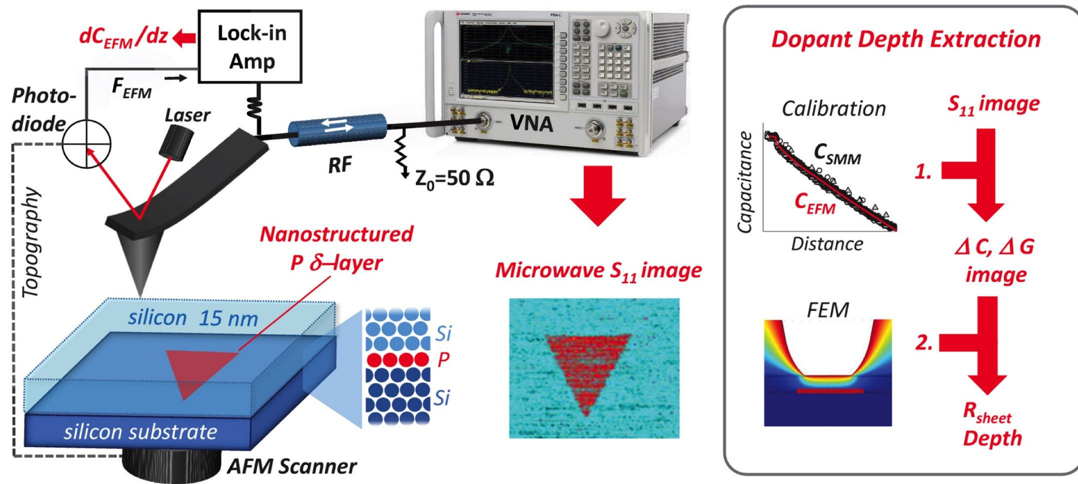


Figure 6.5: SMM experimental setup and workflow for calibrated impedance measurements and dopant depth extraction of buried 2D phosphorus layers. Vector network analyser (VNA) measures the local S_{11} reflection coefficient (amplitude and phase). For calibration dC_{EFM}/dz signal is detected by Lock-in amplifier. (Right) The workflow for dopant depth extraction consist of: 1) SMM S_{11} images/curves calibration [205] to obtain quantitative, complex admittance data, $Y = G + i\omega C$ with C being capacitance, G conductance, ω the angular frequency and $i^2 = -1$. 2) Finite element modelling (FEM) is used to extract sheet resistance and depth from the admittance signal.

conducting atomic force microscope (AFM) probe and transmits an electromagnetic wave to the tip. The VNA measures the reflected wave and the ratio of the incident and the reflected signal power (S_{11}-reflection parameter) gives information on the local sample properties below the probe. By operating the SMM at $f \approx 20$ GHz (see Figure A.4 in the appendix), high sensitivity to variations in the sheet resistivity of P dopant layers is obtained which increases the sensitivity to variations in impedance of the device under test (DUT) [206]. For quantitative dopant depth extraction, the measured S_{11}-reflection parameter is first converted into

conductance (G) and capacitance (C) parameters of the P layer by a suitable calibration processes [205] which will be explained in the next section. Combining the calibration process with robust finite element modelling (FEM) in the illustrated two-step procedure, shown in Figure 6.5, allows the extraction of the depth of the buried nano structure. A commercial transmission line SMM consisting of a standard 5600 AFM interfaced with a 20 GHz VNA was used (both from Keysight Technologies, Santa Rosa, CA, USA). In order to reduce the contact force and to maintain a sharp tip, soft ($k = 0.3\,\mathrm{N/m}$) solid platinum AFM tips (RMN, Salt Lake City, USA) were chosen. The AFM tip is employed as a nanoscale imaging and microwave probe, enabling simultaneous topographic and electromagnetic characterisation of the sample. We used contact mode for the xy-scans. Measurements were performed at frequencies between $4-20\,\mathrm{GHz}$. In order to transform the high impedance of the tip-sample contact to the sensitive $50\,\Omega$ of the VNA, a half-wavelength coaxial resonator in conjunction with a $50\,\Omega$ shunt resistor is used [206]. While the shunt resistor in parallel to the measured high resistive signal at the tip ensures a sensitive input resistance around $50\,\Omega$ at the VNA, the half wavelength resonator (15 cm cable length) at 1 GHz (30 cm wavelength) provides periodic notches with high signal-to-noise ratio (SNR).

6.3 Complex impedance calibration procedure

The task of this calibration is to map the refection coefficient $S_{11,\mathrm{m}}$ measured at the VNA to the complex impedance at the tip Z_{in} ($Z = \frac{1}{Y}, Y = G + i\omega C$, Y being the admittance and $i^2 = -1$) of the SMM for each scan point. We applied the calibration procedure recently proposed by Gramse *et al.* [205] shown in Figure 6.6, that allows us to calibrate the system directly on the sample. The transfer function is mapping the measured $S_{11,\mathrm{m}}$ for a given frequency at the VNA into the impedance calibration plane located directly before the cantilever which is of the form

$$S_{11,\mathrm{m}} = e_{00} + e_{01}\frac{S_{11,\mathrm{a}}}{1 - e_{11}S_{11}} \tag{6.1}$$

$$S_{11,\mathrm{a}} = \frac{Z_{\mathrm{in}} - Z_{\mathrm{ref}}}{Z_{\mathrm{in}} + Z_{\mathrm{ref}}} \tag{6.2}$$

where $Z_{\mathrm{ref}} = 50\,\Omega$ is the characteristic impedance of the VNA, $S_{11,\mathrm{a}}$ is the raw refection coefficient and e_{00}, e_{01}, and e_{11} are three complex error parameters [205]. The measured $S_{11,\mathrm{m}}$ was converted into the complex impedance Z_{in} using the one-port black-box calibration al-

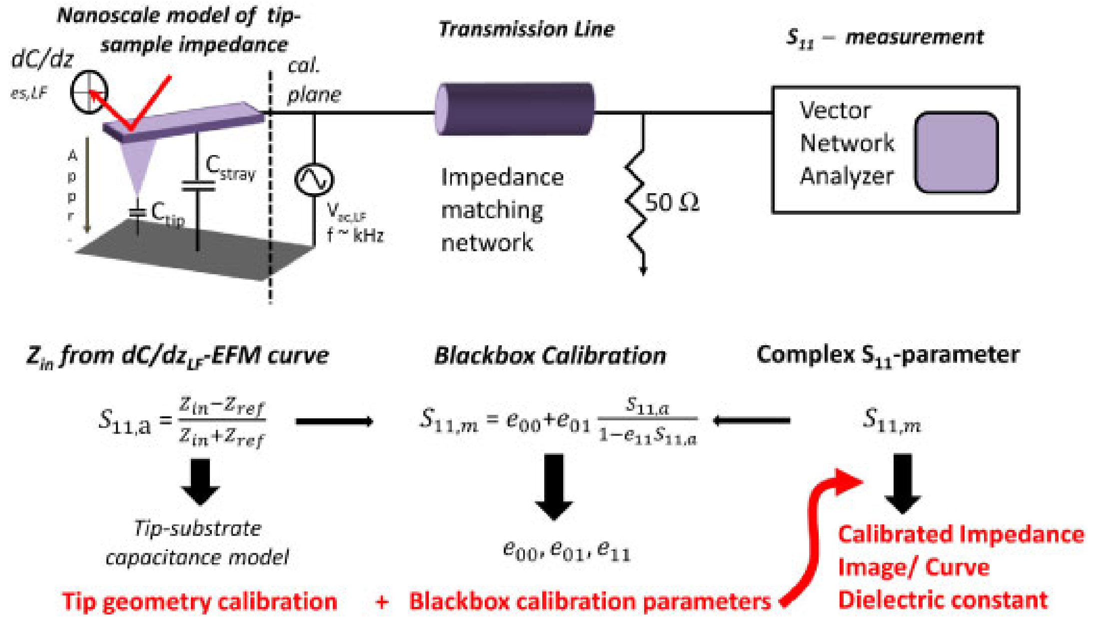


Figure 6.6: Schematics of the experimental setup, the calibration plane, and the calibration procedure. The conductive AFM-tip is connected to a vector network analyser by a transmission line and impedance matching network (50 Ω shunt). The black box calibration procedure compares measured S_{11} values with capacitance values measured at low frequencies by EFM during an approach curve in order to define the calibration error parameters e_{00}, e_{01}, and e_{11}. From the approach curve also the tip geometry is extracted (From [205]).

gorithm, which theory comes from the field of VNA calibration where VNA and the SMM are assumed to be a linear microwave network. The one-port blackbox calibration is an established method to calibrate the VNA and connection cables up to the DUT [206, 207]. This transfer function is determined by three complex error parameters e_{00}, e_{01}, and e_{11} that were calculated from simultaneously acquiring EFM and $S_{11,\mathrm{m}}$ approach curves (see 'dopant depth extraction' part in Figure 6.5). The calibration takes advantage of the fact, that the change in impedance for a metallic or dielectric non-lossy material is only capacitive and thus, can be measured simultaneously at a low frequency by EFM [205]. For this, the tip is approached to the surface until it made contact, and both the dC_{EFM}/dz and the $S_{11,m}$ signals were recorded. Integrating over the voltage normalised force $dC/dz = 2F_{es,2\omega}/V_0^2$ provides the desired tip-sample capacitance C(z) and the simultaneously acquired $S_{11,m}$ gives the impedance $Z_{in}(z)^{-1} = Y(z) = i2\pi f C(z)$. Using Z_{in} and $S_{11,m}$ as input data, finally, an optimisation algorithm is applied to calculate the complex parameters e_{00}, e_{01}, and e_{11} from equations 6.1 and 6.2. This calibration procedure works in situ on the sample, requires no additional calibration sample such that no external capacitance calibration sample is re-

quired.

6.4 Fabrication of a characterisation sample

As concluded from the introduction, there are currently very limited diagnostics to characterise buried nano structures in silicon. To demonstrate sample characterisation capabilities with SMM, multiple test pattern such as squares, rectangles and triangles, defined by STM H-lithography, have been written onto the clean silicon substrate (as detailed in section 4.3.2). After being exposed to a high background pressure of PH_3 these patterns consisting of a single phosphorus layer serve as an ideal testbed for the characterisation of SMM imaging and diagnostic capabilities. A schematic of the sample is shown in Figure 6.7.

To obtain high resolution SMM images, the correct sample fabrication procedure for atomically precise STM hydrogen lithography is crucial. A $9\,\text{mm} \times 2\,\text{mm}$ sized sample diced from an n-type, arsenic doped, Si(100) wafer with a sheet resistivity of $15\,\Omega\text{cm}$ was loaded into the STM with a base pressure of less than 2×10^{-10} mbar. Sample cleaning preparation and

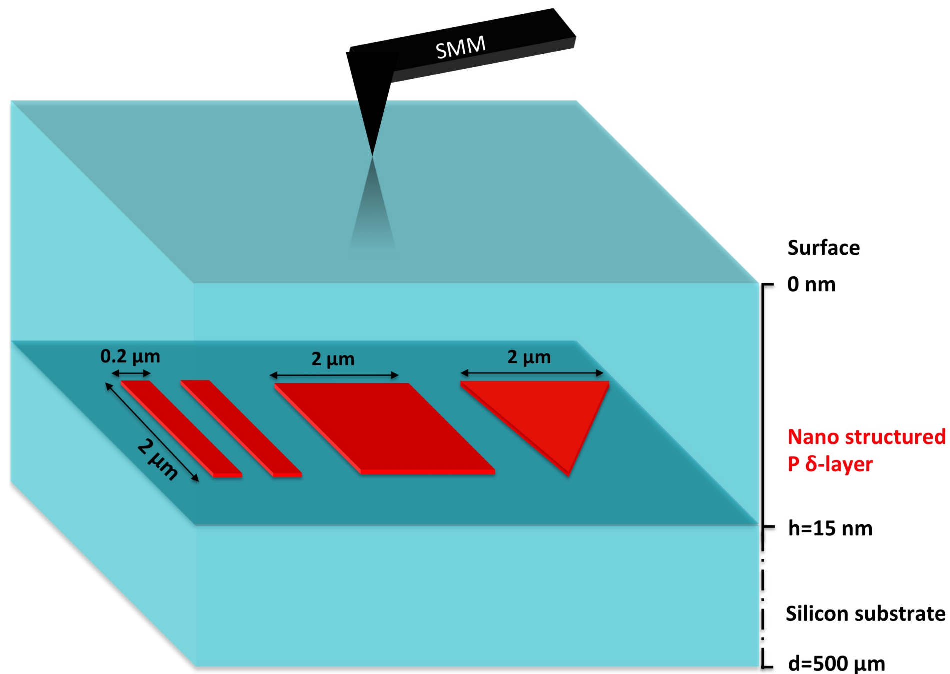


Figure 6.7: Schematic of a SMM characterisation sample. Squares, rectangles and triangles of different sizes defined by STM hydrogen lithography, were written to expose regions of a clean silicon substrate. Subsequently the sample was exposed to a high dosage of PH_3 and annealed to 350 °C to incorperate the P atoms into the surface layer. Finally the nano structures were encapsulated with 15nm of silicon.

termination procedures were performed as explained in section 4.3.1. Test patterns were

written by de-passivating the Si(100)-2 $\times$ 1:H surface [76] using the electron beam from an STM tip at relatively high tip-sample bias of $6-7.5\,$V, a tunnel current of 2.5 nA and writing speed of 50 nm/s, as described in section 4.3.2. The shape of two triangles, a square, five sets of two rectangles with varying separation and an LCN logo were written on sample1 using STM H-lithography, displayed in Figure 6.8 and Figure 6.21 respectively (LCN logo in Figure A.6 in the appendix). A PH_3 dose of 0.09 L, a 2 min anneal at 350 °C and a sample temperature of $\approx$ 250 °C during Si sublimation were used as fabrication parameter. We would like to investigate the SMM contrast originating from STM H-lithography

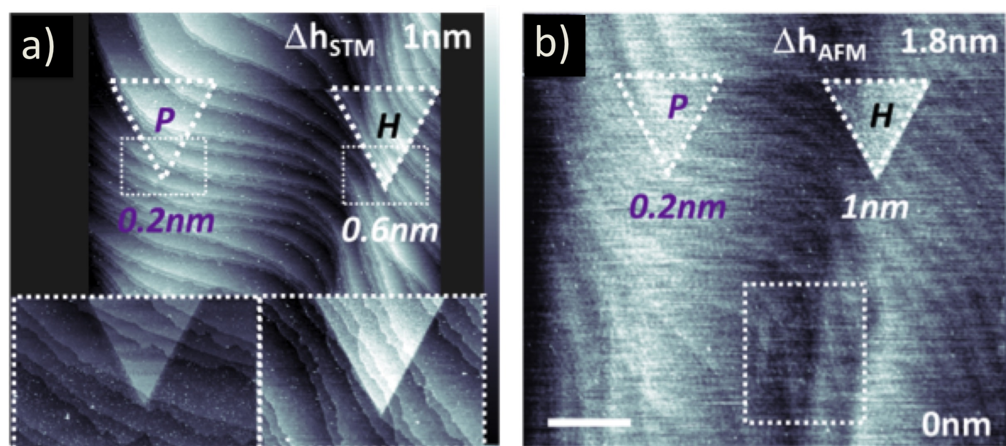


Figure 6.8: Two triangular patches and a square are written using STM H-lithography (U_{litho} = 7.5 V, I = 2.5 nA). a) STM filled state topography images (I = 0.02 nA, U = -2.6 V) after second depassivation of two triangular patches. Only the first triangular patch (purple) was exposed to a saturation background pressure of PH_3. The inset displays the bottom edge of each triangular patch, highlighting the difference in topography contrast between exposed and only depassivated patch region. Topography contrast scale bar is $0-1$ nm. b) AFM topography image after silicon overgrowth.Topography contrast scale bar is $0-1.8$ nm, scale bar is 1.4 μm.

defined patterns that were exposed to PH_3 and those that were only H depassivated. The second right triangle patch (white) in Figure 6.8a) has been written after dosing with PH_3 and therefore should not contain any phosphorus. The sample was then exposed to ambient atmosphere, shipped to Linz and mounted on the SMM sample stage.

6.5 Imaging of patterned phosphorus δ-layers

In Figure 6.9a) the AFM contact mode topography image acquired from the abovementioned sample shows a hardly visible height difference of $\sim$ 0.2 nm for the square of incorporated phosphorus. The height difference can be attributed to a increased surface roughness within the nanostructured area. Single silicon terraces (height difference of

$\sim 0.136\,\text{nm}$) are still visible in the topography image. A clearly visible, positive contrast of

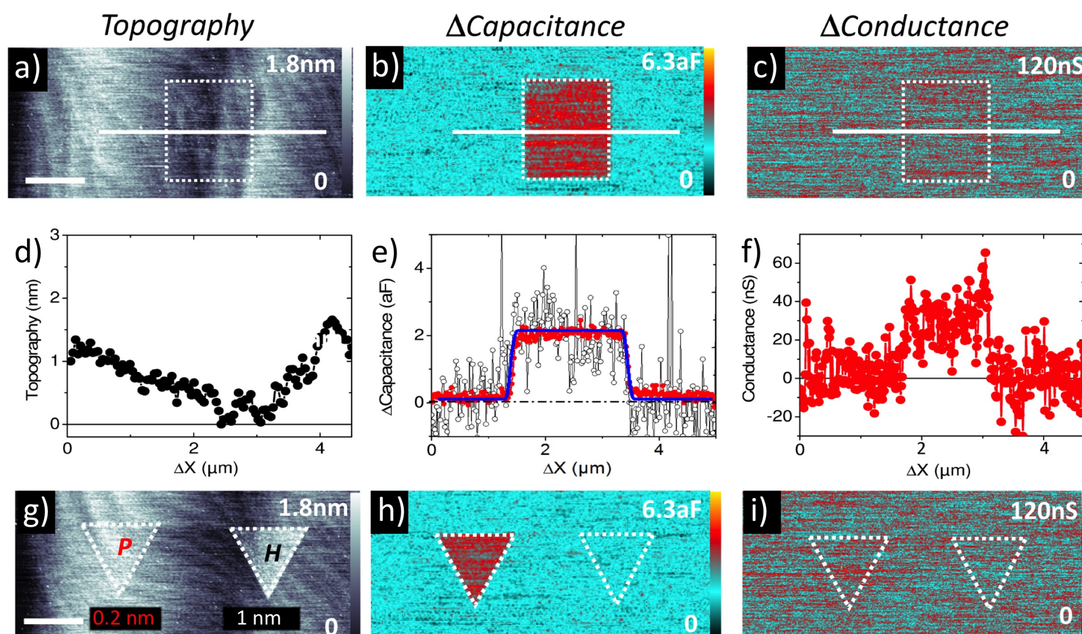


Figure 6.9: SMM imaging of buried patterned phosphorus δ-layers. a) AFM topography image after coverage with 15 nm of Si. b) SMM capacitance image showing clear contrast for the phosphorus pattern. c) SMM conductance image. Corresponding line profiles shown in d), e) and f), respectively. Line profile across the square pattern (black=single line, *red* = 10 lines average, blue = fit with logistic function). g) AFM topography image of patterned phosphorus (P) layer and depassivated hydrogen h) layer. Corresponding h) capacitance and i) conductance images. Scale bars are $1.4\,\mu$m, VNA power 1 dBm, $f = 19.81\,\text{GHz}$, scan speed 0.4 lines/s (512 points).

$\Delta C = 2.1 \pm 0.1\,\text{aF}$ for the nano structured phosphorus square with respect to the surrounding substrate is measured in the calibrated SMM capacitance image shown in Figure 6.9b) . A profile is shown in Figure 6.9e) and several profile lines can be averaged to further reduce the noise. The feature height is close to the SMM noise floor of $C_{noise} \sim 0.1\,\text{aF}/\sqrt{\text{Hz}}$ corresponding to $C_{noise} \sim 1\,\text{aF}$ at the chosen scan speed of 0.4 lines/s. We also observe a very small contrast in the conductance channel, which is hard to see in the image (Figure 6.9c)) because the signal is in the same range as the noise floor, $\Delta G_{noise} \sim 100\,\text{nS}$. After averaging individual line profiles taken across the entire square, as shown in Figure 6.9f), the contrast of $\Delta G = 25 \pm 15\,\text{nS}$ could be estimated. The measured AFM topography contrast (see Figure 6.9 g)) for the depassivated triangle after encapsulating with 15nm of silicon is $\sim 1\,\text{nm}$, in contrast to only $\sim 0.2\,\text{nm}$ for the phosphorus-incorporated triangle. 0.8 nm of relative height difference corresponds to approximately 6 layers of Si and suggests an inherent change in Si growth on the P and H patterned regions. The rate of homo epitaxial growth of Si is known

to be sensitive to small coverages of surface hydrogen [33] and a low coverage of residual H is likely to remain in the patterned region. The hydrogen depassivated triangle in Figure 6.9h) displays no measurable capacitance contrast in the image, confirming the absence of phosphorus. Furthermore, we note that the 1 nm roughness increase of the desorbed triangle is not detected in the SMM capacitance channel and thus conclude that cross-talk between capacitance and surface roughness is negligible.

6.6 Phosphorus depth and conductivity extraction

The contrast in the SMM is significantly stronger in the capacitance channel than compared to the conductance channel, which is a result of the buried dopant nano structures forming local conducting planes below the surface. A capacitance, $C = \varepsilon A/d$, is built up between the buried plane and the conducting probe-apex, where A is the physical contact area between the probe tip and the substrate surface, d is the depth, and ε is the Si dielectric constant. The measured substrate capacitance must be lower, since it is governed by the width of the depletion layer, which is much larger than the P-layer depth [53] (see also Figure A.10 in the appendix). To extract the exact depth and the conductivity of the phosphorus layer, a quantitative interpretation is required. We refine the simple picture by taking into account the dopants in the substrate and the precise geometry of the system. We have used finite element modelling (FEM) to calculate the theoretical admittance of the model shown in Figure 6.10a). The FEM simulations were performed by Dr. Georg Gramse at Johannes Kepler University. The phosphorus layer is modelled as a thin layer (0.2 nm) with a conductivity, σ_P,which is embedded at a depth, h, in the depletion layer of the low-doped As silicon substrate. The basis for the assumed δ-layer thickness is justified by the data in Figure 6.11 and associated text in the next section. The voltage distribution for this model is shown in Figure 6.10b) with (left) and without (right) the highly conductive layer present. From the voltage profile along the symmetry axis in Figure 6.10c) it can be seen that essentially the entire potential drops off in the $h = 15$ nm between tip and the buried phosphorus nanostructure which validates the initial assumption. Where no phosphorus is present the potential decays much more slowly within the substrate which is leading to a lower capacitance. The tip geometry and contact area between conducting tip and sample are essential properties for a quantitative extraction of the dopant layer depth. They need to be established experimentally by fitting simulated capacitances to a capacitance versus distance curve on the bare Si substrate obtained directly after imaging the nanostructure (Figure A.5 in the

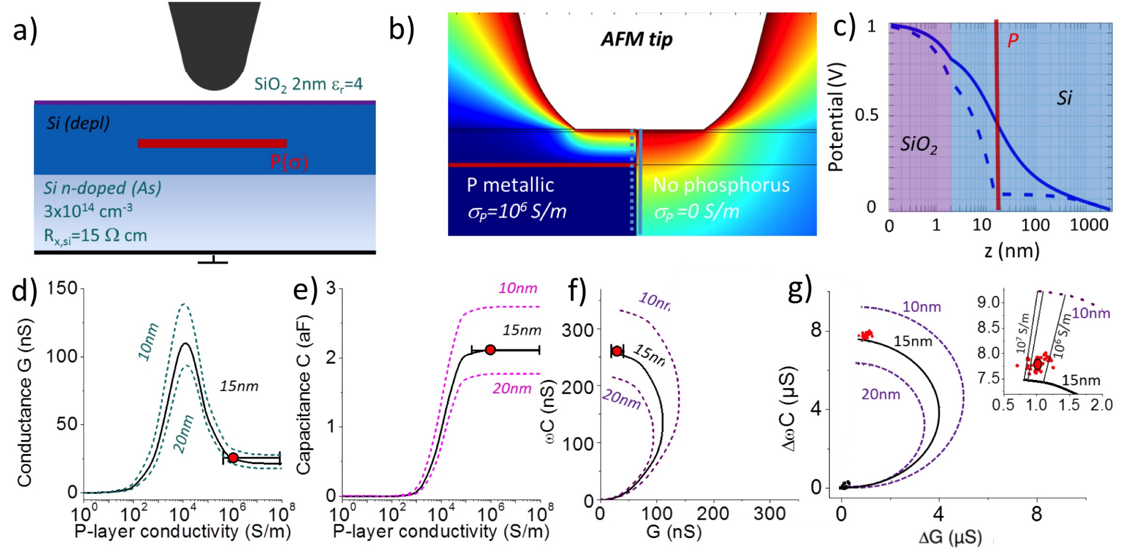


Figure 6.10: P δ-layer depth and conductivity extraction. a) Sketch of axi-symmetric finite element model used to calculate theoretical SMM admittance. b) Potential distribution for simulated model: tip in contact with bare Si substrate (right side) and P δ-layer present 15 nm below the surface (left side). c) Corresponding voltage profiles in z-direction parallel to tip symmetry axis for a 20 nm tip for the substrate (solid) and the phosphorus layer (dashed line). d)+e) Modelled capacitance (ΔC) and conductance (ΔG) dependence on phosphorus layer conductivity calculated for a dopant depth of $h = 15$ nm (solid line) and $h = (15 \pm 5)$ nm (dotted and colored line) for tip $r_a = 20$ nm. Experimental value (red dot) is shown in the graphs for extraction of dopant depth and P-sheet conductivity. f) Representation of ΔC and ΔG in complex plane. g) Measurement with larger probe ($r_a = 290 \pm 1$ nm) - representation of $\Delta\omega C$ and ΔG in complex plane.

appendix and inset Figure 6.5). The apex radius, cone angle and contact radius of the circular contact area are free parameters in this fitting procedure which are determined to be $r_a = 20 \pm 5$ nm, $\theta = 8 \pm 1°$ and $r_c = 11 \pm 2$ nm, respectively. While the first two parameters can be extracted from the out-of-contact region of the approach curve, the contact radius is determined from the region where the tip is already in contact with the substrate. The extracted values for r_c and r_a are within the nominal $10-30$ nm range of values provided by the tip manufacturer [208]. The precise determination of the tip geometry at different times of the experiment is of great importance. A measurement performed with a blunter tip for example (shown in Figure A.5) gives a clearly larger capacitance signal. After all geometrical parameters in the model have been defined, the conductivity of the P dopant layer and its depth can be extracted by comparing the simulated values with the experimental conductance and capacitance obtained from images in Figure 6.9. The simulated capacitance and conductance differences are shown in Figure 6.10d) and 6.10e) as a function of the phosphorus layer conductivity for a dopant depths of $h = 15$ nm (solid line) and $h = (15 \pm 5)$ nm,

respectively (dotted lines), where the red dots represent the experimentally obtained values. The best match between simulated and experimental values is obtained for a dopant layer depth of $h = 15 \pm 1$ nm and a conductivity of $\sigma_1 = 1.2 \times 10^6$ S/m. The decreasing sensitivity in the metallic regime at $> 10^5$ S/m (Figure 6.10d)+e) leads to a large confidence intervals of $(10^5$ to $10^8)$ S/m. By using a larger tip radii (see Figure A.5 in appendix and Figure 6.10g)) the confidence interval could be reduced to $(2 \times 10^6$ and $5 \times 10^6)$ S/m such that a depth of $h = 14 \pm 1$ nm and $\sigma_2 = 3 \times 10^6$ S/m could be extracted as best match. By equalising the simulated and measured complex admittance data two constraints have to be met such that phosphorus conductivity and dopant depth can be extracted clearly and without ambiguity. This becomes more obvious when simulated and measured complex admittance values are plotted in the complex plane (for a small (Figure 6.10f)) and large tip (Figure 6.10g)).

6.7 Secondary ion mass spectroscopy on single δ-layer sample

To validate the extracted depth value from SMM, we carried out SIMS on non-patterned P δ-layers fabricated under nearly the same experimental conditions as the patterned ones (phosphorous incorporation annealing temperature 480 °C). This SIMS profile is the same as shown in a logarithmic scale in section Figure 5.10 and Figure 4.16b). The concentration of phosphorus and oxygen as a function of depth below the surface is depicted in Figure 6.11a). A sharp P peak at a concentration of $(0.58 \pm 0.06) \times 10^{21}$ cm^{-3} is located at $h = (14.45 \pm 0.01)$ nm with a width of $d_{\mathrm{FWHM}} = 2$ nm. Symmetric spreading of the peak

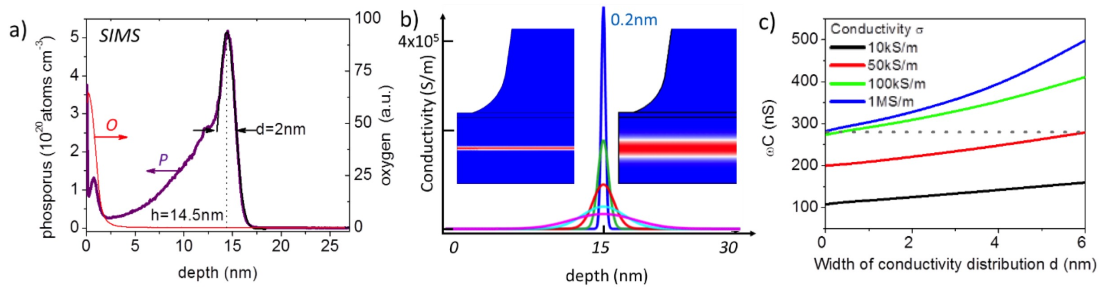


Figure 6.11: Finite width of P-layer distribution. a) SIMS of phosphorus and oxygen in sample. Phosphorus peak is located at $h = 14.45$ nm with a width of $d = 2$ nm (as extracted from gauss fit). b) Simulated Gaussian conductivity distribution for width of $d = 0.2, 1, 2, 4$ and 6 nm. Insets show 2D distribution for $d = 1$ nm and $d = 4$ nm. c) Calculated capacitance as function of conductivity distribution for 4 total contributions (dotted line represents experiment)

is the result of thermally induced P diffusion, occurring during incorporation anneal and

subsequent overgrowth. As mentioned earlier SIMS itself contributes to the vertical spread due to effects such as sputter-based broadening [209]. The measured depth h is in good agreement with the value extracted by SMM in this work. Studies of the 'electrical' and physical widths of such δ-layers can provide support for our assertion concerning the narrow widths. For example, Oberbeck, *et al.* [68] measured a segregation length of ~ 0.6 nm for a δ-layer overgrown at 250 °C. That the segregation tail extending towards the surface plays a minimal role is a result of not only the relatively smaller concentration when compared with the peak height, but also due to the electrical inactivity of the donors near the surface. From previous studies, it is established that the carrier density drops significantly within 8 nm of the surface, most likely due to carriers being localised in carrier traps at the Si/SiO_2 interface [134]. This means the capacitance contribution from dopant atoms closer to the surface drops significantly which is also suggested from the extraction of the 'electrical width' in the previous chapter. Especially P accumulation at the surface oxide interface (the P peak prominent in the surface region) is known to be non-conductive [210], and is thus not expected to contribute to the SMM signal, as the SMM data confirms. In addition, Polley *et al.* used in situ UHV four point probe to demonstrate a sharply increased resistivity for δ-layer encapsulation depths below 5 nm and that δ-layers become completely inactive buried shallower than 0.5 nm [135]. They attribute the increasing inactivity of the layers to enhanced surface scattering.

This allows us to reduce the number of parameters in our finite element modelling to essentially two: the depth and the sheet resistance and we approximate the P-layer as a true δ-layer (shielding boundary, width 0.2 nm). Indeed a wider distribution, as shown in Figure 6.11b)+c), would increase the simulated capacitance difference which would not agree as well with our results as the current picture does. Our calculations for shallower δ-layer depths (e.g. 10 nm in Figure 6.10d)-g)) tells us that the detected absolute signal best matches a modelled δ-layer width of 0.2 nm at 15 nm depth. Were the δ-layer, in fact, shallower, the signal should be significantly higher. By including simulations of SMM response to different δ-layer distributions along the z-axis, we find that a larger δ-layer width has only a small effect on the S_{11} signal (see Figure 6.11b)+c)). The dominant effect on the S_{11} signal therefore depends on the absolute conductivity value of the buried δ-layer and location of the peak dopant density. This justifies our treatment of the δ-layer as an essentially 2D embedded layer.

6.8 Application to three-dimensional phosphorus δ-layer structure

6.8.1 Design

To ultimately test imaging and characterisation capabilities of SMM a more advanced δ-layer structure is proposed to examine SMM contrast as function of depth, dose, and number of layers. A schematic of the complex 3D sample is displayed in Figure 6.12. This complex

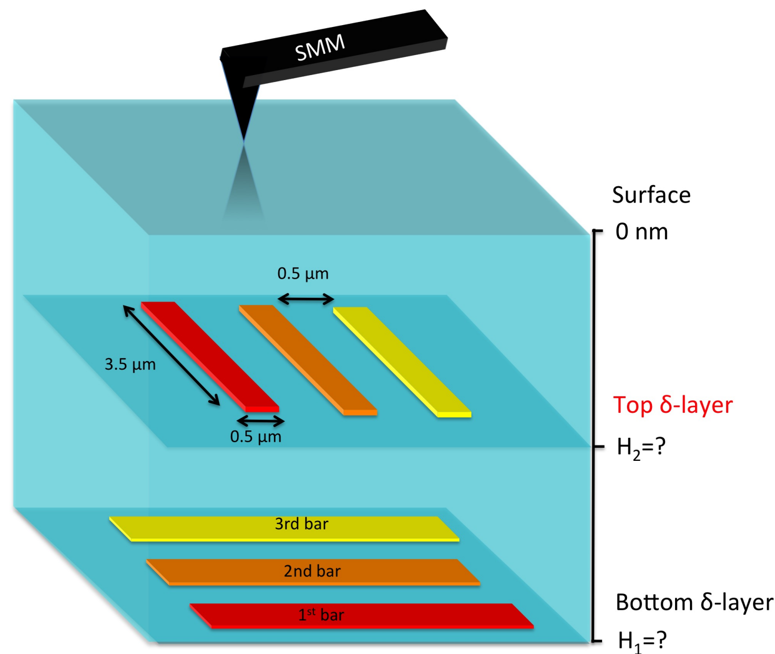


Figure 6.12: Schematic of a proposed 3D P δ-layer structure design comprising of six bars in two different depth and increased PH_3 dosages (coded by same colours for both layers).

structure consists of two overlaid perpendicular sets of three phosphorus-doped bars and besides the dimensions it meets the fabrication requirements in close approximation of the proposed criss cross gate structure for the surface quantum computer proposal by Hill *et al.* [21]. For each set of parallel bars, three different PH_3 dosages were used, one for each bar, leading to three different doping densities as indicated in colour coding at depths H_1 and H_2. The size of the bars should a) be large enough to be easily detectable by SMM and b) overlay in a criss cross structure that enables us to study crossing points of overlaying bars. The detection sensitivity for isolated P with SMM has been determined to be $Res^2\rho\ P \sim 4200$ atoms buried at $h = 15\,\mathrm{nm}$ (see section 6.9). This result has been estimated for a sample using a conventional fabrication recipe. For the fabrication of a complex 3D sample as

depicted in Figure 6.12 an advanced growth recipe could alter the dielectric properties of the epitaxial silicon and P δ-layer. Therefore, bar dimension of $3.5\,\mu\text{m} \times 0.5\,\mu\text{m}$ with a pitch of $0.5\,\mu\text{m}$ have been chosen to fulfil these requirements. However, as already mentioned in the introduction there are several challenges for the fabrication of such a complex 3D P patterned δ-layer structure.

6.8.2 Challenges for sample fabrication

At first, STM topography images obtained on areas that were previously patterned and encapsulated with silicon show no contrast that would allow the detection of buried STM lithography defined features. Using CITS as described in reference [185] is a time consuming method to detect buried nanostructures for small encapsulation thicknesses. It is not sufficient for locating nano structures buried under tens of nm, especially for large scan areas ($\approx \mu m$). Hence, since high precision in vertical alignment of the two sets of bars is crucial, a fiducial marker system on the sample is necessary to locate the patterned area after overgrowth and encapsulation. Second, STM H-lithography requires a flat H passivated silicon surface to work. The surface roughness of overgrown silicon depends on the sample growth temperature, more precisely on the thermal budget (temperature and duration) of the silicon atoms on the surface during growth [34, 102]. With increasing thermal budget silicon atoms diffusion is enhanced which increases the mass transport in and on the surface layer and causes the growth of large silicon islands and terraces [33, 69]. This results in a trade off between achieving good confinement to prevent dopant segregation (low thermal budget) and achieving a flat 2D regrowth surface which typically requires higher temperatures [33, 211]. Therefore, as mentioned in section 4.4.3 δ-layers are conventionally fabricated by exposing to a PH_3 saturation background pressure followed by an incorporation anneal of 350 °C for 1-2 minutes, encapsulated with silicon at an optimal temperature of 250 °C [34]. This way, maximum active carrier density of $2.4 \times 10^{14}\,\text{cm}^{-2}$ (sheet resistivity $210\,\Omega$ per square) has been archived with such a single dose strategy. An even higher active carrier density and lower resistivity can be achieved [212] by using two saturation doses, the first followed by a 550 °C incorporation anneal, and the subsequent dose followed by a 350 °C anneal. However, by applying this method the hydrogen mask is desorbed (hydrogen desorption temperature is ≈ 415 °C [213]) after the first incorporation anneal step, which is making the method incompatible with STM H-lithography patterning of nano structures. In order to achieve maximum carrier density and dopant confinement

in a 2D P δ-layer, the segregation of P donors and the subsequent formation of electrically inactive P-P dimers [212, 214] should be minimised.

A good dopant confinement in 2D can be achieved by encapsulating at low temperatures followed by a rapid thermal anneal which flattens the surface for re-patterning and repairs vacancy and interstitial defects in the overgrown silicon [215]. However, the induced thermal budget needs to be carefully tuned since dopants tend to diffuse during anneal and will spatially broaden the layer in which they were originally confined [69]. Dopant segregation is a strictly surface phenomenon [185] where P dopants from the δ-layer segregate to the growth front during silicon growth [214]. This process is thermally induced and hence, segregation can be minimised by encapsulating at low temperatures [185]. Further, P segregation can lead to accumulation of P right under the silicon surface as a result of annealing. This is clearly visible in SIMS measurements in Figure 6.11a) and later in Figure 6.17b) which can be a limiting factor for device fabrication [212] (see also section 4.4.5). Keizer *et al.* developed a growth strategy where a high carrier density is maintained whilst suppressing dopant segregation, results are shown in Figure 6.13. By growing > 9 ML of silicon

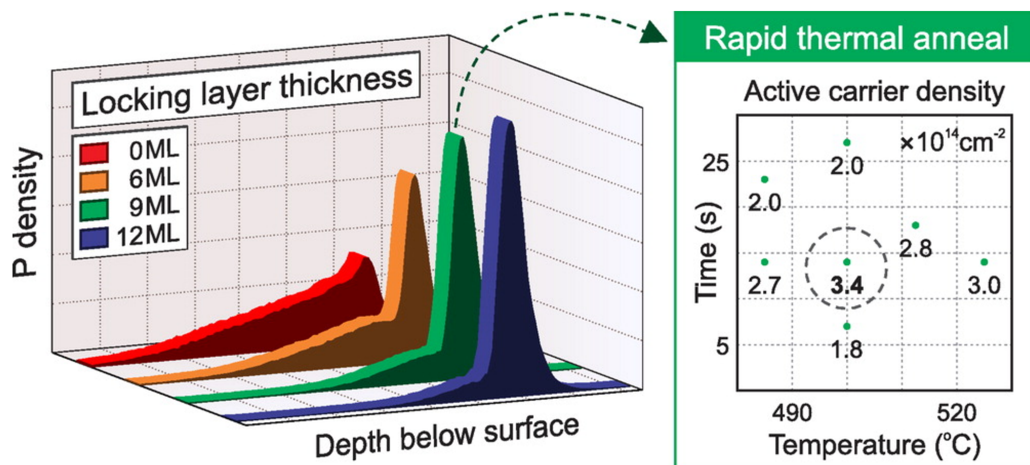


Figure 6.13: Left: SIMS measurement on double dosed P delta layer samples grown at different locking layer thicknesses. Best confinement of the delta layer whilst maximising dopant activation is achieved for 9 ML locking layer thickness. Right: Active carrier density of delta layer samples versus rapid thermal anneal parameters, time and temperature. A final RTA at 500 °C for 15 s can restore the active carrier density to $3.4 \times 10^{14}\,\mathrm{cm}^{-2}$ while maintaining ultra sharp dopant profiles (From [69]).

at ambient temperatures a so called 'locking layer' effectively suppresses P segregation. A rapid thermal anneal (RTA) for 15 s at 500 °C right after locking layer growth was found to fully restores the active carrier density in the δ-layer and further provides an epitaxial silicon growth [69]. However, Keizer *et al.* have developed their growth method for unpat-

terned single δ-layer samples using a double dose strategy. This leads us to two important questions:

1. Can we experimentally confine two δ-layers at different depth and
2. Can we hydrogen re-passivate and pattern on overgrown silicon ?

6.8.3 Test measurements for the sample fabrication

To investigate if an encapsulated nano structure can be re-passivated and patterned using STM hydrogen lithography, a fabrication growth recipe has been developed based on findings from Keizer *et al.* [69]. To flatten the overgrown surface after silicon encapsulation an additional second RTA is included in the recipe. The developed fabrication growth recipe for the first layer is shown as timeline in Figure 6.14. In addition, the developed recipe can be used for the fabrication of patterned multi-layer devices. The timeline for the growth

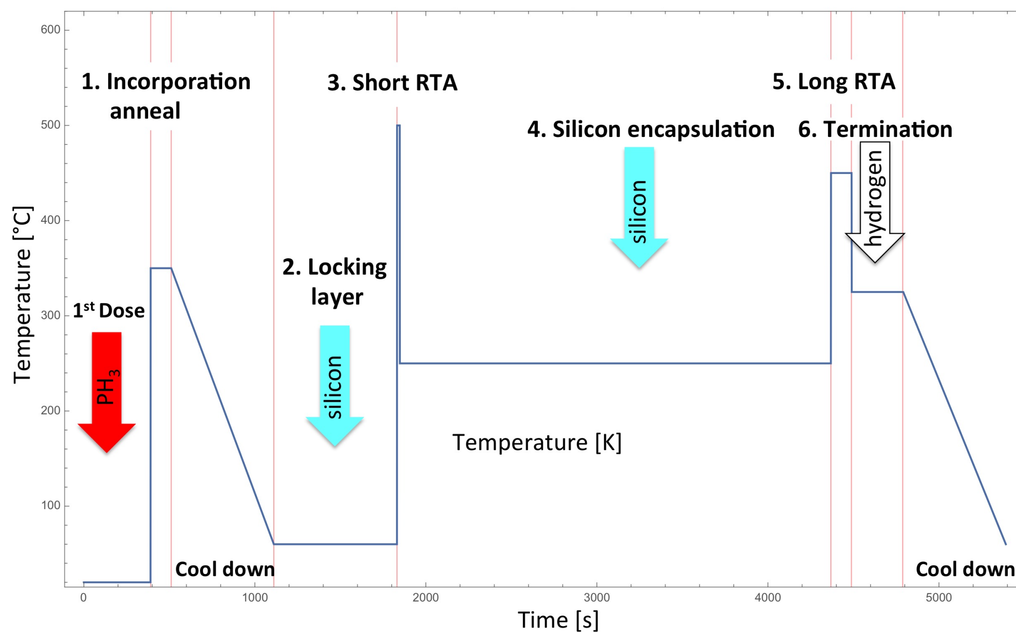


Figure 6.14: Timeline of recipe for the fabrication of a patterned multi layer sample. Shown are the steps for the growth of the first layer. After an incorporation anneal (1), a locking layer of $\approx$ 10 ML of silicon is grown at RT (2) which suppresses the segregation of P to the surface. A short RTA (3) activates the P and ensures a epitaxial silicon growth for the following silicon layer. After the growth of approximately 5 nm of epitaxial silicon (4), a second longer RTA (5) smoothens the rough surface necessary for a successful re-passivation (6) and patterning of the surface. For growing the next layer the steps are repeated and for the final layer the steps are repeated with exclusion of the anneal and termination step.

starts right after dosing the first patterned nanostructure. After an incorporation anneal for 2 min at 350 °C (1), the direct current heating is switched off and the sample is allowed

to slowly cool down to ambient temperatures. The temperature sensor in the manipulator is still reading 60 °C 5 min after turning the sample heating off. Silicon is then sublimated onto the sample from a silicon sublimation cell, such that a 10 ML thick locking layer (2) is grown in order to suppress P segregation. Radiation from the sublimation cell slightly heats the sample up to $\approx 100\,^{\circ}$C during the evaporation (as read by a temperature sensor in the manipulator). According to Eaglesham [211], growing 10 ML of silicon grown at a rate of $\approx \frac{1ML}{min}$ at 60 °C is still in the limited thickness epitaxy (LIE) regime, where crystalline silicon growth occurs up to a certain thickness, called the 'epitaxial thickness'. After the LIE regime a transition to amorphous deposition is observed.

A filled state topography image presented in Figure 6.15a) obtained after encapsulation with 10 ML of silicon (2) reveals that due to the low growth temperature the surface roughness measured as root-mean-square roughness, R_{RMS}, increased from $R_{RMS} = (0.05 \pm 0.01)$ nm to $R_{RMS} = (0.32 \pm 0.03)$ nm, compared to a clean flat prepared silicon surface. The first RTA (3) for 15 s at 500 °C repairs the vacancy and interstitial defects [215] in the overgrown silicon and gradually flattens the surface ($R_{RMS} = (0.06 \pm 0.01)$ nm) for subsequent epitaxial silicon growth. Figure 6.15b) displays the hydrogen terminated silicon surface after applying a first RTA step, which flattens the surface by forming silicon cluster. A square shaped area of the surface (dashed line) has successfully depassivated by STM H-Lithography. After encapsulating with 5 nm of silicon (4) with a growth rate of $\approx 1\,\frac{\mathrm{ML}}{\mathrm{min}}$ the STM topography image in Figure 6.15c) reveals a rough surface of $R_{RMS} = (0.42 \pm 0.04)$ nm. A longer second RTA (5) of 2 min at 450 °C flattens the silicon surfaces for re-passsivation (6) and patterning. The resulting silicon surface in Figure 6.15d) (here already terminated) is characterised by an decreased silicon island size and increased surface roughness of $R_{RMS} = (0.09 \pm 0.02)$ nm compared to the silicon surface right after first RTA in Figure 6.15b). We also observe an increased vacancy density in the silicon islands (indicated by a white edged line) pointing towards a low mass transport in and on the surface induced by the second RTA.

However, the surface is suitable for termination and subsequent depassivation as demonstrated in Figure 6.16a) where a large area of three bars ($0.5\,\mu$m $\times\, 3.5\,\mu$m each) has successfully been depassivated. To investigate if we are able to confine two δ-layers in different depths, separated by 5 nm of silicon by using the developed growth recipe, a test sample comprising of two unpatterned δ-layers at different depths has been fabricated without applying STM H-lithography. The test sample is schematically shown in Figure 6.17a). SIMS

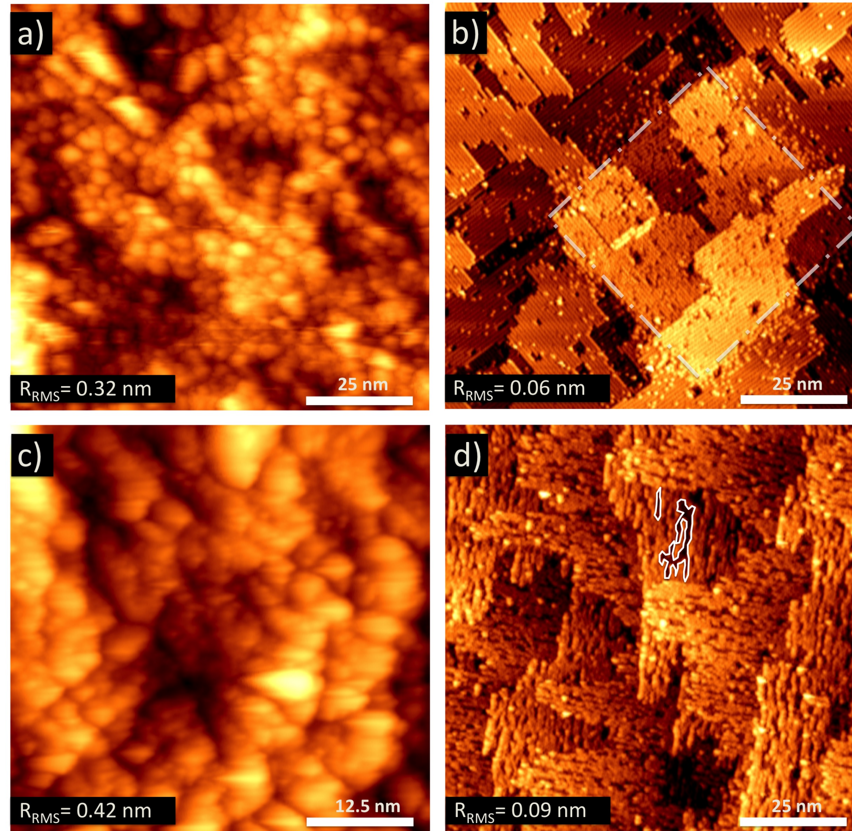


Figure 6.15: STM filled state topography images ($U = -2\,\mathrm{V}$ and $U = -2.5\,\mathrm{V}$, $I = 0.02\,\mathrm{nA}$) at various points of the developed growth recipe. a) Silicon surface after encapsulation with $\approx 10\,\mathrm{ML}$ of silicon (step 2) grown at low temperatures resulting in an increased surface roughness. b) Surface after applying a first RTA (step 3) on a) and subsequently terminating with hydrogen. The surface flattens by forming large silicon islands. A STM H-Lithography defined square (white dashed line) has successfully depassivated (Depassivation parameter: $U_{lith} = 7.5\,\mathrm{V}$, $I = 2\,\mathrm{nA}$, $100\frac{nm}{s}$)). c) After subsequent encapsulation with $\approx 5\,\mathrm{nm}$ of silicon (step 4) grown at $250\,°\mathrm{C}$ and d) after applying a second and longer RTA (step 5) for 2 min at $450\,°\mathrm{C}$ and subsequently terminating with hydrogen. The silicon surface shows silicon island formation with an increased density of vacancies (indicated by white edged line).

has been performed on the stacked unpatterned δ-layer test sample (Figure 6.17b)). We find a good confinement of the P layers when separated by 5 nm by making use of our developed growth recipe, that includes locking layer. The SIMS results display the effectiveness of the locking layer in suppressing the P segregation. For both layers 94% of the deposited phosphorus is confined in a layer with a full width at half-maximum thickness of 1.0 nm. The peak concentration of $(1.25 \pm 0.13) \times 10^{21}\,\mathrm{cm}^{-3}$ of the top δ-layer at 3.8 nm below the surface is 32% higher than the one of the bottom layer ($(0.95 \pm 0.10) \times 10^{21}\,\mathrm{cm}^{-3}$) at 8.9 nm below the surface which might result from P donor diffusion from the bottom layer towards the surface during the first anneal and further segregation during growth to the surface of

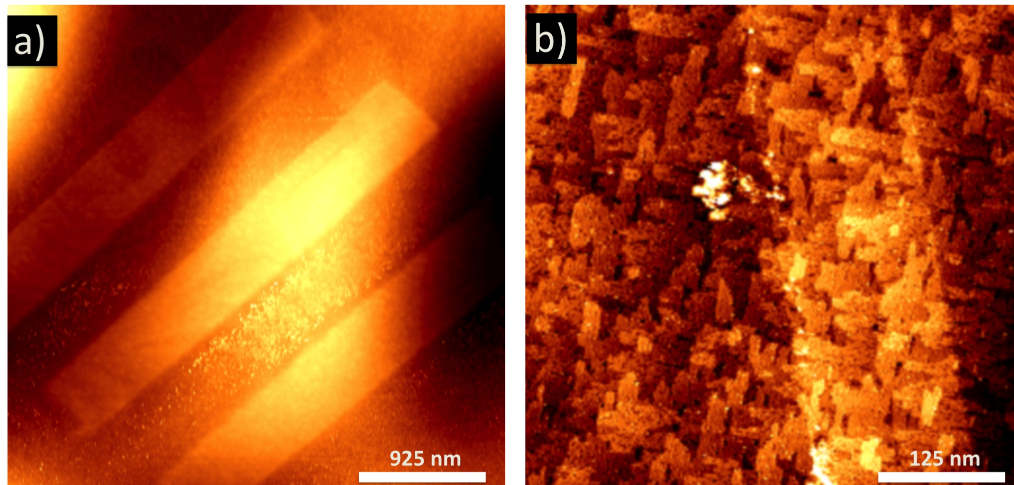


Figure 6.16: a) STM filled state topography images ($I = 0.02\,\text{nA}$, $U = -2.6\,\text{V}$) after applying the developed fabrication growth procedure. The overgrown silicon surface has been successfully passivated and an area of three bars ($0.5 \times 3.5\,\mu\text{m}$ each) has been written onto the surface (Depassivation parameter: $U_{lith} = 7\,\text{V}$, $I = 3\,\text{nA}$, $50\frac{nm}{s}$). b) Close up of a smaller depassivated bar displays silicon island formation and confirms complete depassivation in the patterned bar region.

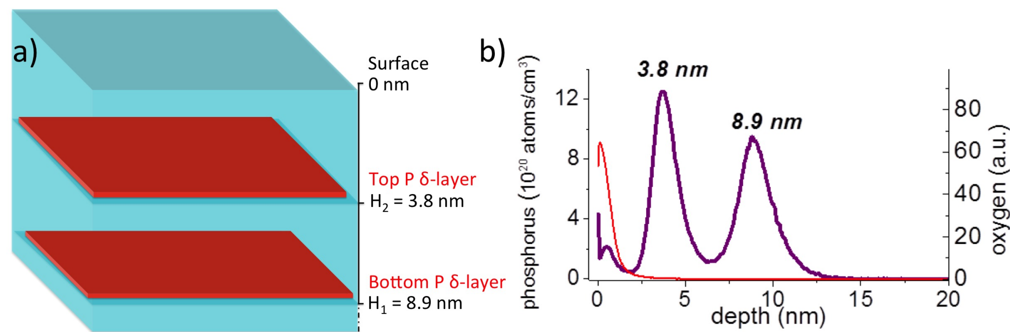


Figure 6.17: Test sample consisting of two unpatterned δ-layer at different depth separated by 5 nm of silicon by using the same growth recipe we have developed. Left: Schematic of the test sample and performed SIMS measurements on the sample (Right). Phosphorus peaks are located at $h_1 = 8.9\,\text{nm}$ and $h_2 = 3.8\,\text{nm}$ with full width at half maximum of $d_1 = 1.7\,\text{nm}$ and $d_2 = 2.1\,\text{nm}$ (as extracted from Gaussian fits), respectively.

the top layer. Compared to SIMS data in Figure 6.11a) of an unpatterened single saturation δ-layer fabricated using a conventional growth recipe, both δ-layers display a higher peak density (compared to $(0.58 \pm 0.06)) \times 10^{21}\,\text{cm}^{-3}$) and a less pronounced segregation tail towards the surface (FWHM of 1.7 nm and 2 nm for top and bottom layer respectively) pointing towards a better P confinement of the P atoms in the δ-layer plane. These results are very much in line with the SIMS data from [69]. The FWHM thickness of the oxide on the sample, determined to be 1.3 nm (absolute thickness $\sim 2\,\text{nm}$), is comparatively thick for native SiO_2 oxide (normally the absolute thickness of $\approx 1\,\text{nm}$ for degenerately doped n-

type silicon [137]) and indicates an increased oxide growth rate on high saturation δ-layer samples. A high number of dopants in the SiO_2 loosens the material and reduces its density, which enables a better oxidant diffusion through the SiO_2 to the interface [138] (see also section 4.4.5). The separation and absolute depth of the two layers in the complex 3D sample are dependent on the SMM imaging resolution. From the characterisation of the first sample, sample 1, it was found that SMM offers a good resolution down to 15 nm. For the complex 3D sample, it was thought that the advanced growth strategy might result in a reduced SMM imaging contrast. Consequently, the bottom layer was buried at ≈ 10 nm instead of the 15 nm value used for the first sample. A minimum depth for the top layer was chosen to be 4 nm because it has been shown that the room temperature resistivity of the δ-layer increases significantly for an encapsulation depth of < 4 nm [135] due to interactions with the silicon surface such as incomplete ionisation [37, 216], surface charge transfer [36, 217] and interface roughness scattering [218].

6.8.4 Fabrication

Before writing the first bottom bar a clean Si sample was prepared and passivated as described in section 4.3.1. After aligning the tip to an orientation marker, a test desorption routine was carried out to determine the ideal desorption parameters for complete desorption (see section 4.3.5 for details). Depassivating large areas ($\approx \mu$m) for long duration ($\approx$ hours) at high positive voltages ($6-9$ V) and high setpoint current ($\approx$ nA) increases the risk of tip modifications during the desorption process. This leads to modified desorption parameters of the tip and could alter or stop the depassivation process, as can be seen in the depassivated LCN logo in Figure A.6 in the appendix. In the worst case, tip modification could result in contaminations that drop from the tip onto the patterned area. Hence, a stable tip whilst desorbing but also during imaging is crucial for the success of a complex sample fabrication consisting of multiple scan and desorption steps. So far there is no procedure incorporated in the hydrogen lithography software that monitors the current and tip parameter during desorption. The fabrication procedure for a 3D P δ-layer structure sample comprising of six bars in two different depth and three different PH_3 dosages using a developed fabrication growth recipe as explained above is summarised in Figure 6.18.

The fabrication starts by depassivating an area of $3.5\,\mu\text{m} \times 0.5\,\mu\text{m}$ for the first bar B1 at the first bottom layer. On a micron scale the silicon surface displays local height minima and maxima due to islands formation of multiple stacked silicon terraces during growth,

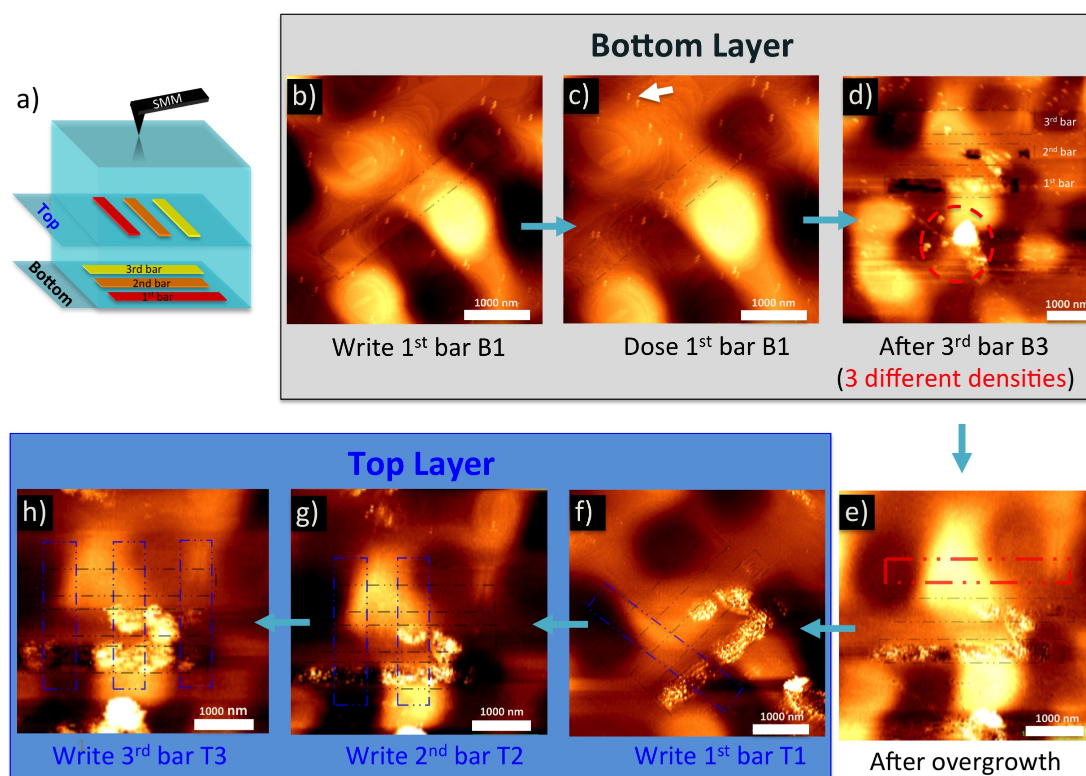


Figure 6.18: Fabrication guide of 3D P δ-layer structure design comprising of six bars in two different depth and different PH_3 dosages. a) Schematic of the sample design. b)-h) STM topography filled state images ($U = -2.6\,\text{V}$, $I = 0.02\,\text{nA}$. Depassivation parameter: $U_{lith} = 7\,\text{V}$, $I = 3\,\text{nA}$, $50\frac{nm}{s}$). b)-c) The surface topography after depassivating an area of $3.5 \times 0.5\,\mu\text{m}$ for the first bar B1 at the first bottom δ-layer. d) Overview of the active writing area after the depassivation of the first three bottom bars. A pronounced change in surface contrast partially for bar B2 and bar B1 is visible, accompanied by a large agglomeration of material at the bottom of the active area marked by a red dashed circle. e) Surface tomography after encapsulation with 5 nm of silicon with the use of locking layer. The buried bar B3 (red dashed area) displays no surface contrast in the STM topography image. h)-f) Three bars in the top layer were written and dosed with the same parameters as those in the bottom layer but rotated by 90°.

which makes it difficult to identify the contrast in height of only 0.136 nm originating from dangling bonds in depassivated areas. By tilting the scan image by 45° the contrast of the depassivated area can be slightly increased as can be seen in Figure 6.18b). For the first saturation dose the tip is retracted 50 steps ($> 70\mu m$) from the surface to avoid screening of the depassivated area by the presence of the tip and subsequently the surface is exposed to a PH_3 saturation dosage of 0.09 L. An STM image obtained immediately after dosing confirms the adsorption of PH_3 molecules exclusively within the depassivated bar shaped region indicated by a contrast change due to the altered structural surface morphology (see dashed lined area in Figure 6.18c). After the first depassivation and dosing white protru-

sions as indicated by a white arrow in Figure6.18c) are present on the sample surface. The features' appearance can be attributed to a tip artefact, possibly originating from a double tip, because their shape looks the same for all features and is mostly doubled. Scanning large areas of $4\,\mu\mathrm{m} \times 4\,\mu\mathrm{m}$ at a tip scan speed of $1000\,\frac{\mathrm{nm}}{\mathrm{s}}$ a 256/256 pixel image takes about $\approx 20\,\mathrm{min}$. Stable scanning and desorption parameters are very important for a successful fabrication, therefore all sorts of processes that could potentially modify the tip-sample properties should be minimised. Increasing the scan speed to minimise the tip sample interaction could result in undesired tip crashing because the feedback control needs enough time to regulate the tip height to changes in topography. Thus, only overview images were taken with minimum resolution that enable us a) to confirm successful depassivation or/and PH_3 adsorption after dosing and b) allows for realignment of the tip to already written structures after approaching for subsequent depassivation. The procedure of depassivating, dosing and realigning is subsequently repeated for the 2nd (0.00305L) and 3rd (0.00196L) bottom bar but with varying PH_3 dosages. From dose calibrations presented in Figure 4.16 we estimate a P dopant density from the low P coverage regime of $(2.62 \pm 0.42) \times 10^{13}\,\mathrm{cm}^{-2}$ and $(1.69 \pm 0.27) \times 10^{13}\,\mathrm{cm}^{-2}$ for B2 and B3 respectively.

An overview topography image is presented in Figure 6.18d). A pronounced change in surface roughness is seen in part for bar B2 and bar B1, accompanied by a large agglomeration of material at the bottom of the active area marked by a red dashed circle. One explanation for the agglomerations could be contamination from the tip caused by a tip crash after re-approaching the surface after dosing. We have observed an increased probability for tip crashes right after dosing with PH_3, indicating that PH_3 molecules that adsorb on the tungsten tip during the dose and especially at the apex of the tip, in the tip sample tunnel junction region, could drastically perturb the approach process. The tip is triggered to approach until a certain setpoint tunnel current is detected. The PH_3 molecules in the junction could behave as effective insulator and stop the flow of electrons from the sample to the tip. Hence the tip continues approaching until the tip makes unintended contact to the surface. To minimise the effect of an unintended tip crash the tip's resting position during dose and the tips landing location when re-approching has been assigned to be at the bottom of the scan image. The location matches with the position of the large agglomerations in the red dashed circle, pointing towards an unintended tip crash. One explanation for the observed pronounced change in surface contrast at bar B1 and B2 could be due to strong interactions

of the depassivated region with the crashed tip. Scanning across the depassivated regions of bar B1 and B2 with a modified tip directly after crashing could lead to the observed pronounced change in surface contrast by depositing loose material from the apex of the tip onto the surface. But a detailed explanation of a mechanisms that could lead to such a change in roughness remains unclear.

For the next step, the sample has been transferred to the preparation chamber, annealed for 2 min at 350 °C and encapsulated with 5 nm of silicon. For the first 10 ML the sample temperature was kept at low temperatures (around 60 °C) to suppress P segregation as described above, followed by a rapid thermal anneal at 500 °C for 15 s and a lower silicon encapsulation temperature of 250 °C with a rate of 1 ML/min. After reaching the estimated final encapsulation thickness of 5 nm, a 2 min anneal to 450 °C leads to a low surface roughness ensuring a high quality H-passivation for the second δ-layer patterning. The sample is transferred into the VT chamber, loaded onto the VT stage and with the help of alignment markers the location of the previous patterned region is located.

As mentioned in the introduction, after overgrowth of 5 nm of silicon the patterned bottom bar B3 of the bottom layer displays no surface contrast in STM topography images as can be seen in the red dashed area in Figure 6.18e). In contrast to bar B3, bar B1 and B2 have been affected by unintended tip interactions and reveal a clear height contrast over the patterned region. The bars in the top layer depicted in Figure 6.18h)-f) have been written and dosed with same parameters as those in the bottom layer but are rotated by 90° and encapsulated under 5 nm of silicon with the use of locking layer. The whole fabrication process of this complex 3D sample involved over 30 subsequent process steps as well as obtaining multiple large scan STM topography images. Even though sample contamination from the tip was likely to limit the quality of the final device, the time consuming nature of the fabrication steps described above warranted processing of the sample to completion. The measurement described in the rest of the chapter reveal the effectiveness of the fabrication process.

6.8.5 Depth and conductivity extraction

We have applied the SMM imaging and characterisation capabilities to the advanced 3D δ-layer structure as shown in Figure 6.19a). For the SMM capacitance image in Figure 6.19b) we obtain remarkably good contrast between the top and bottom levels, whereas the topography image is completely uncorrelated with the capacitance except on bar B1. Here the measurement has been hindered by surface modification during the lithography

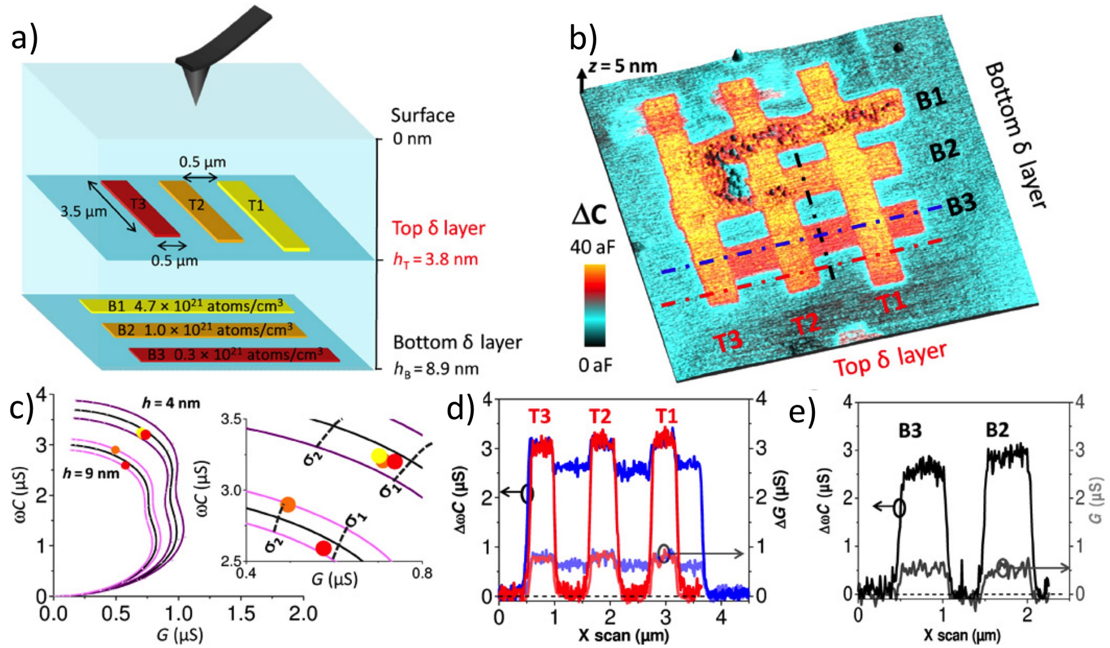


Figure 6.19: 3D P δ-layer structure depth and conductivity extraction. a) Schematic of a 3D structure comprising three bars with increased dosing (coded by same colours for both layers) at two different heights as indicated and verified by SIMS. b) AFM 3D topography image with SMM capacitance signal as colour overlay (image size $5.4\,\mu\text{m} \times 5.4\,\mu\text{m} \times 5\,\text{nm}$). c)+d) $\Delta\omega C$ and ΔG line profiles, allowing contributions from different device layers to be identified, extracted from positions indicated in b).e) Modelled admittance (capacitance ΔC and conductance ΔG) as a function of phosphorus layer conductivity σ for dopant depth $h = 4\,\text{nm}$ and $h = 9\,\text{nm}$ (solid black lines) and for $\pm 1\,\text{nm}$ of these values (purple lines). Experimental values (red, orange and yellow dots) extracted from d)+c) are shown in the graphs for extraction of dopant depth and P-sheet conductivity. Inset shows zoom for extraction of depth and phosphorus layer conductivity from simulations (dashed lines mark layer conductivities of $\sigma_1 = 0.6 \times 10^6\,\text{S/m}$ and $\sigma_2 = 1 \times 10^6\,\text{S/m}$). (Measurement frequency $f = 19.83\,\text{GHz}$, power 0 dBm, tip radius $r_a = 173\,\text{nm}$.

process, as can be seen in Figure 6.20b). Good in plane confinement of the dopants in the bar nano structured regions confirms a successful fabrication and growth strategy of the device. The measurement also confirms that SMM is sensitive to variations in depth, as can be seen in the line profiles obtained across the top layer (red line) and bottom layer (blue line) in the cross-sectional profile in Figure 6.19d). In addition, SMM is capable of detecting different dopant densities in the same layer, as can be seen in the bottom bar B3, which shows a clear decrease in capacitance contrast, see Figure 6.19c). By comparing theory with experimental admittance values we can extract the depth of the top and the bottom layer bars in analogy to sample 1 in section 6.6, but with a full 3D model (Figure 6.19a). Experimental admittance data extracted from Figure 6.19c)+d) is plotted in Figure 6.19e) together with the simulated values in the complex admittance plane where bar B1was

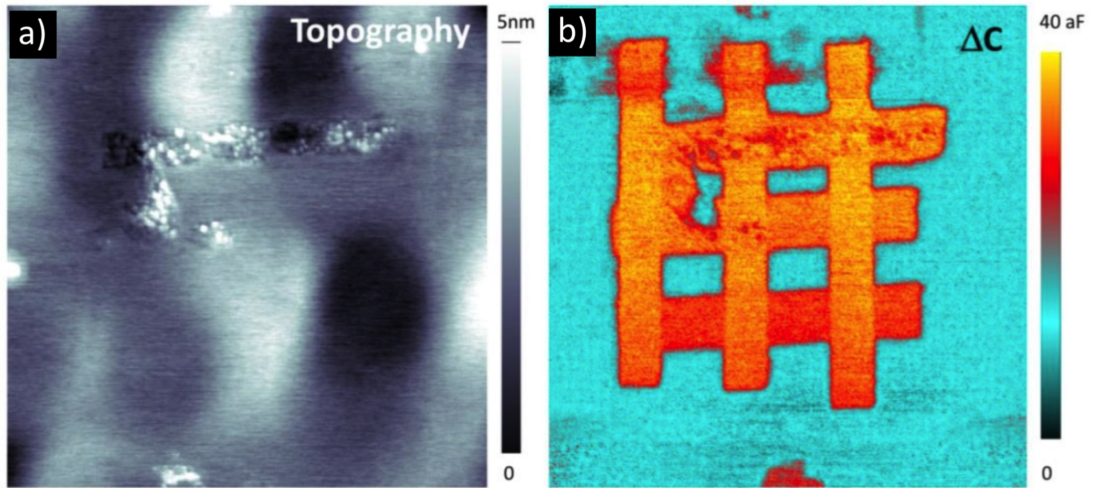


Figure 6.20: AFM Topography and SMM capacitance image of 3D sample. Same data as shown in Figure 6.19b) but with the 3D topography image a) and capacitance texture b) shown separately, as opposed to the overlaid version shown in Figure 6.19b). As can be seen, the underlying topography of the surface shows virtually no correlation with the capacitance image, except where the surface has undergone tip modification during lithography (primarily in the region of the top horizontal rectangle).

excluded in this analysis due to the surface modification. The bars in the top level agree well with a depth of $h_{T1} = 4.3 \pm 0.5\,\text{nm}$, $h_{T2} = 4.5 \pm 0.5\,\text{nm}$ and $h_{T3} = 4.2 \pm 0.5\,\text{nm}$ and also the depth of bottom bars of $h_{B2} = 8.2 \pm 0.7\,\text{nm}$ and $h_{B3} = 9.6 \pm 0.7\,\text{nm}$ can be still extracted, however, with lower accuracy. These values are in very good agreement with the depth position determined via SIMS measurements of the calibration double δ-layer sample ($h_B = 8.9\,\text{nm}$ and $h_T = 3.8\,\text{nm}$). For the P layer conductivities we extract $\sigma_{B2} = (1 \pm 0.2)10^6\,\text{S/m}$, $\sigma_{B3} = (0.7 \pm 0.1)10^6\,\text{S/m}$ and for the top levels $\sigma_{T1} = (0.7 \pm 0.1)10^6\,\text{S/m}$, $\sigma_{T2} = (0.65 \pm 0.1)10^6\,\text{S/m}$, $\sigma_{T3} = (0.62 \pm 0.1)10^6\,\text{S/m}$. The values scale nicely with the phosphorus doses applied during sample preparation.

6.9 Lateral resolution and sensitivity

Finally, we make a quantitative estimate of the feature size that can be resolved with SMM as well as the sensitivity to buried and isolated P atoms. The capability to laterally resolve fine P patterns is a key feature of the technique. We can derive the lateral resolution from the capacitance profile line in Figure 6.9e). By fitting the profile with a difference of two logistic functions

$$f_{logis}(x) = A(1+e^{-(x-x_0)/\delta})^{-1} - A(1+e^{-(x-x_1)/\delta})^{-1} \tag{6.3}$$

where A, δ, x_0, x_1 are the fitting parameters and δ defines the sharpness of the step, the width of the step from Si to P has been estimated to be $\mathrm{Res}_{50-88,C} = 2\delta = 55 \pm 4\,\mathrm{nm}$. Applied to the shallower 3D structures in Figure 6.19 $\delta_B = 47 \pm 3\,\mathrm{nm}$ for the bottom layer and $\delta_T = 37 \pm 1\,\mathrm{nm}$ even displayed an improved lateral resolution. Note that a bigger tip radius was used in this measurement to increase the accuracy of the extracted R_{sheet}. From measurements on fine patterns such as a LCN logo patterned in phosphorus (see Figure A.6 in the appendix) isolated features in the STM topography image prior Si coverage as small as 10 nm could still be detected. These features then buried at 15 nm appear broadened in the capacitance image ($\sim 60\,\mathrm{nm}$). Thus, five pairs of stripes with increasing pitch have been patterned (200 nm, 150 nm, 100 nm, 70 nm, 30 nm) and buried below 15 nm of Si for a quantitative estimate of the feature size that can be resolved in more complex and dense circuits. Stripes separated by 70 nm could still be resolved as shown in the SMM capacitance image in Figure 6.21a) and the corresponding line profile Figure 6.21b), whereas at 30 nm separation the SMM could not distinguish the individual stripes anymore. Simulated capacitance curves from a 3D finite element model (red curves in Figure 6.21b)) agree well with the experiment. Only at low separations ($L = 30 - 70\,\mathrm{nm}$) a minor difference between experiment and simulation is observed. The deviation can be explained by investigating the effect of the depth of the dopant layer, h, and the apex radius, r_a, on the lateral resolution. For this, simulated capacitance profiles are plotted for a varying depth and apex radius shown in Figures. 6.21c)+d), and 6.21e)+f), respectively. The depth of a two stripes separated by 100 nm was varied from $h = 5\,\mathrm{nm}$ to $h = 100\,\mathrm{nm}$ displaying an increase in contrast for a lower Si encapsulation depth shown in Figure 6.21c). From this data the maximum resolvable feature separation, L, has been calculated as a function of the depth by assuming an SMM capacitance sensitivity of 0.5 aF (bandwidth 25 Hz) As can be seen in Figure 6.21d) separations of $d = 40\,\mathrm{nm}$ are well resolved by SMM for a dopant depth of $h = 5\,\mathrm{nm}$, while for deeper buried features at $h = 40\,\mathrm{nm}$ only sub-μm lateral resolution is expected Interestingly, the lateral resolution does not increase monotonically with decreasing tip radius as can be seen from simulations with varying tip radius in Figure 6.21e)+f). In fact, there is an optimum contact radius in the range of $30 - 40\,\mathrm{nm}$ (see Figure 6.21f)). The contrast is inverted for a tip radii above 100 nm and individual stripes are not resolved anymore. To understand the obtained simulation results not only the tip apex has to be taking into account, but also the less local cone that is contributing to the capacitance signal (for details

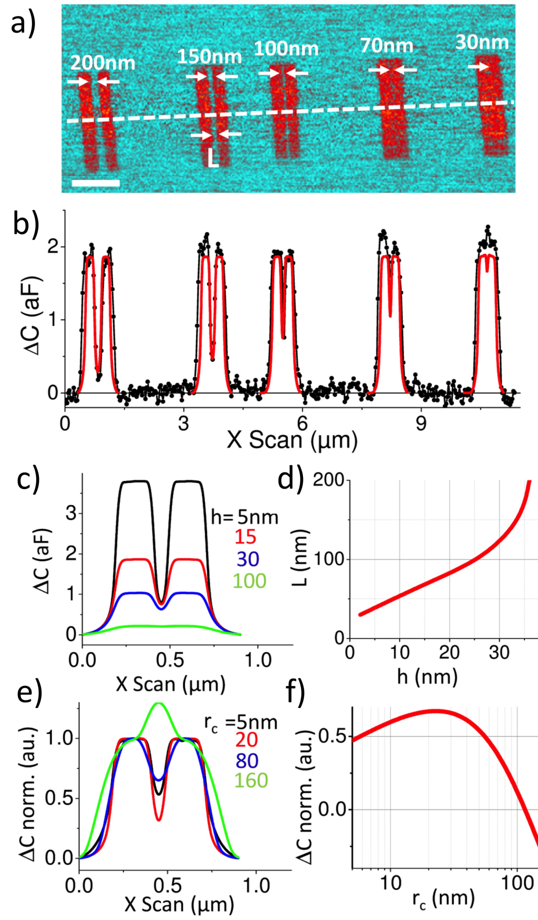


Figure 6.21: SMM capacitance sub-surface lateral resolution. a) SMM capacitance image of stripes and b) corresponding capacitance line profile (black dots, ten lines averaged) including simulated capacitance for corresponding phosphorus stripes assuming $h = 15\,\text{nm}$ depth below surface, apex radius $r_a = 20\,\text{nm}$ and contact radius $r_c = 12\,\text{nm}$ (VNA power 1 dBm, $f = 19.05\,\text{GHz}$). c) Simulated capacitance profile for phosphorus structure at $h = 5, 15, 30$, and 100 nm depth (separation $L = 100\,\text{nm}$). d) Resolvable P feature separations as a function of the layer depth (for a SMM sensitivity of 0.5 aF). e) Normalized simulated capacitance profiles of P stripes in dependency of contact radius ($L = 100\,\text{nm}$). f) Normalized capacitance contrast from e) as a function of contact radius r_c (Note $r_c = r_a$ are set to be identical to reduce number of parameters).

see Figure A.3 in the appendix). The tip apex contributes less than the cone to the capacitance signal for tip radii less than 30 nm. This is leading to a decrease in lateral resolution. For the observed lateral resolution for isolated P atoms we have estimated that for a density $\rho_P = 1.4\,\text{atoms/nm}^2$ [92, 102] of P atoms in the subsurface layer as few as $Res^2\rho_P \sim 4200$ atoms can be detected (at the bandwidth of 10 Hz). Finite element simulations are supporting this estimation by suggesting that 4600 P atoms at $h = 15\,\text{nm}$ are enough for a sensitive SMM detection (see Figure A.6 in appendix). This number is even reduced to 1500 atoms at h= 5 nm.

6.10 Discussion and summary

We have demonstrated SMM to be an excellent tool for locating, imaging and investigating of buried electronic features. This novel technique enables the location of features in 3D with high-resolution, is non-invasive and determines their quantitative electrical characteristics. In particular, patterned δ-layers of phosphorus fabricated using STM hydrogen lithography buried below 15 nm of silicon were easily resolvable and SMM was successfully employed to provide their electrical characteristics. Using STM hydrogen lithography a characterisation sample consisting of a buried P nano structure has been fabricated by following a conventionally established growth recipe (sample 1) which served as a ideal test bed for SMM characterisation capabilities. We found that due to thermal enhanced segregation during growth the vertical δ-layer spread has no significant effect on the SMM detection mechanism. We have applied the developed characterisation method to a complex 3D P bar structure. For the fabrication of the 3D sample an advanced growth recipe has been developed that suppresses P segregation whilst RTA steps flatten the overgrown surface enabling subsequent re-passivation and hydrogen lithography. This growth recipe enables precise P nano structure patterning for future 3D device fabrication using STM hydrogen lithography.

For the single patterned P nano structure of sample 1 a depth of 14 ± 1 nm and sheet resistance of $R_{sheet} = 1.7\,\mathrm{k\Omega/sq}$ (the confidence interval is 1 to $2.5\,\mathrm{k\Omega/sq}$) was determined by applying the developed depth and conductivity method. These values compare favourably with similar values measured for P δ-layer samples that were fabricated in an identical way but without the STM hydrogen lithographic step. While SIMS measurements revealed a depth of (14.45 ± 0.01) nm, Hall bar measurements of a saturation δ-layer Hall bar determined a sheet resistance of $(0.67 \pm 0.001)\,\mathrm{k\Omega/sq}$ (as presented in section 5.3.4). The increased measured resistivity in SMM might result from contribution of trapped charges in the silicon interface layer to the resistivity which are not detected via Hall measurements.

We have applied SMM to more complex 3D structures. The technique distinguishes different doping concentrations and depths of the δ-layers and can be of practical use to assess the quality of patterned structures in terms of their electrical conductivity. The extracted depth of both layers $h_B = 8 - 10$ nm and $h_T = 4$ nm is in good agreement to those obtained from SIMS measurements on a test sample of $h_1 = 8.9$ nm and $h_2 = 3.8$ nm (see Figure 6.17b). We have observed a significantly higher sheet resistance of $R_{sheet}(3D) = 5 - 8\,\mathrm{k\Omega/sq}$ for

the 3D sample compared to the single layer sample $R_{sheet}(\text{sample}\,1) = 1.7\,\mathrm{k}\Omega/\mathrm{sq}$ buried below 14 nm of Si. One possible explanation for this quantitative difference in R_{sheet} might be from a reduced P activation and/or Si homogeneity due to the more complex preparation procedure which includes the use of locking layers [69, 136]. Our results would also support the findings of Clarke *et al.* [134] that suggest a 40 % lower carrier density from carriers located at dopants closer to the surface (4 nm) compared to those at 9 nm. This also would explain why the bottom layers display a lower R_{sheet} and a stronger dependence on the applied P-doses than the top layers. Again, a comparison to the sheet resistance obtained from Hall bar measurements is only partially possible since all Hall bar measurements have been carried out on unpatterened δ-layer samples of different dosages encapsulated with 15 nm of silicon.

Our results suggest that the SMM technique is capable of detecting a region of patterned P with as few as 1900 or 4200 densely packed atoms, when buried 4 or 15 nm below the silicon surface, respectively. The sample does not have to be destroyed to achieve the measurement, as is the case for TEM or atom probe tomography. Indeed, other techniques such as SIMS cannot be used at all to measure the properties of these buried nanostructures, since SIMS needs a $\sim 100\mu$m sized area for accumulative dopant profiling. The scanning DC or low frequency capacitance microscopy technique can potentially image the same number of dopants, however, it cannot provide the depth and electrical information of SMM. The current interest in non-invasive imaging is highlighted by a very recent paper which describes the use of a near-field THz imaging technique to image a printed circuit board on the underside of a 115 μm-thick silicon wafer [219]. However the technique only has a lateral resolution of $\sim 100\,\mu$m, over three orders of magnitude coarser than the SMM.

By providing a measurement capability that is not possible with any other technique this results presented here open up exciting opportunities for dopant nanostructure fabrication. SMM can be implemented within the same scanning probe instrument that is used to pattern the devices, which allows in-situ and iterative control during the entire lithography/MBE process for atom-scale deterministic doping. This ability is expected to be especially useful to speed up the current development of 3D patterned device structures [220] and significantly aid in the interpretation of their electrical transport behaviour. One of several exciting applications that could emerge from our research is the use of SMM as a diagnostic for the development of a surface code quantum computer [21–23].

Chapter 7

Spectroscopy of buried nanostructures and characterisation of a powered buried nanowire

7.1 Introduction

To guarantee reliable device performance, especially by including newly emerging materials such as δ-layers, nanowire, graphene and spintronics in the device fabrication processes, non-destructive detection of physical relevant device properties, such as carrier concentration, capacitance and conductivity are highly desirable. In situ characterisation of structural and electronic properties at the operating frequency of devices over large distances are essential requirements for future device metrology methods. As demonstrated in the previous chapter, scanning microwave microscopy (SMM) has been successfully employed to probe relevant physical quantities such as resistivity and depth of patterned δ-layers with nanoscale spatial resolution. [2, 194, 197]. Capacitance and conduction signal show good agreement with standard MOS diode theory [197, 221] and/or FEM modelling in conjunction with a lumped element model.

For more advanced characterisation using the SMM setup, electrical properties of semiconductors can be tuned by the field effect of a DC bias, applied in addition to the low RF signal to the tip. By detecting the S_{11} and dS_{11}/dV signal simultaneously, further information about the electrical properties of the sample, such as dopant density, can be extracted [197]. A piece of additional SMM hardware called the 'dopant profile measurement module' (DPMM) is used for dS_{11}/dV measurements and is attached to a standard AFM and VNA unit in conjunction with a lock-in amplifier. The components of a typical SMM sys-

tem with DPMM module are schematically illustrated in a simple block diagram in Figure 7.1 (From [222]). The VNA generates a microwave signal that is split at the DPMM module

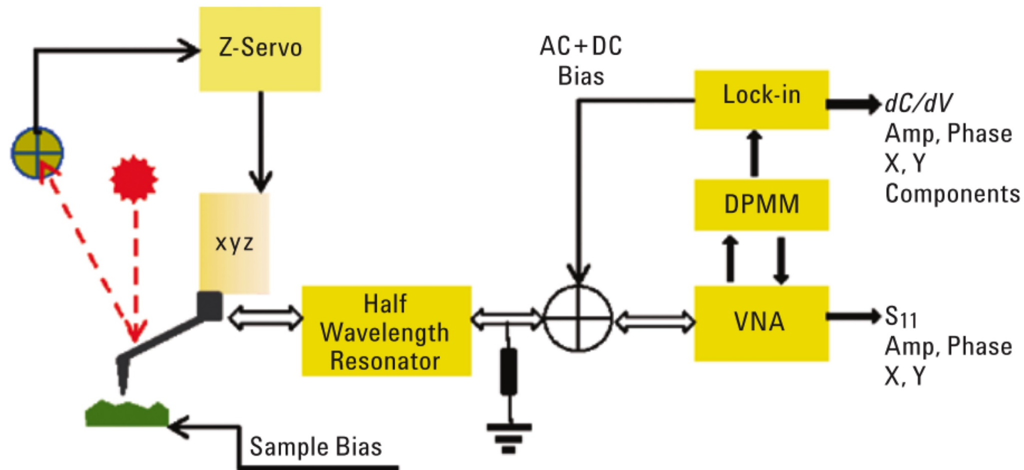


Figure 7.1: A simple block diagram of the SMM configuration for capacitance measurements and dopant profiling. The measuring microwave signal is split at the DPMM module into two parts, one part is used as the local oscillator signal (LO) for the dC/dV mixer, while the other part is guided to the conductive AFM probe tip. After calibration, S_{11} and dS_{11}/dV can be converted into capacitance, conductance and dC/dV and dG/dV signal, respectively (From [222]).

into two parts, one part is used as the local oscillator signal (LO) for the dC/dV mixer while the other part is guided to the conductive AFM probe tip. A DC bias is modulated with a low RF (kHz) AC from a function generator and applied between tip and sample [222]. While the DC bias remains at a constant bias, the AC bias modulates the carriers in the device under test (DUT) and thus, the change in capacitance and conductance is picked up by the reflected measured microwave (MW) signal. The reflected MW signal is then divided into two parts as well. One part is directed to the DPMM internal mixer, where after mixing with the LO of the AC signal and lock-in demodulation, dS_{11}/dV amplitude and phase signal can be extracted. The second part is delivered to the VNA receiver, used to measure the amplitude and phase of the S_{11} [222]. Using the described impedance calibration procedure in section 6.3 [205] the detected S_{11} and dS_{11}/dV can be converted into capacitance, conductance, dC/dV and dG/dV, respectively. Depending on the applied DC bias, mobile charge carriers in the doped regions of semiconductor devices can either accumulate or deplete in the vicinity of a contact electrode. Modulating with a varying AC voltage V_{AC} around a fixed DC working potential V_{DC} causes a change in capacitance/conductance in response to V_{AC}, which is illustrated in Figure 7.2 for the capacitance. Consider an AFM tip in contact

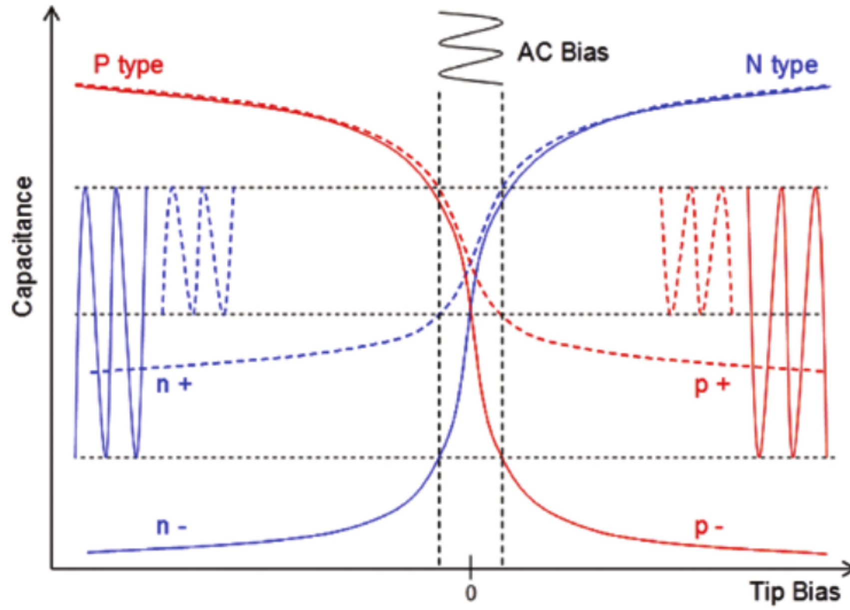


Figure 7.2: Capacitance vs voltage plot for n-doped (blue) and p-doped (red) semiconductors. For the same AC modulation signal applied, the change in capacitance is larger for lower doping density (solid line) and smaller for higher doping density (dashed line). For p and n-doped samples they are identical in amplitude, but opposite in sign (From [222]).

with the silicon wafer consisting of silicon oxide on a doped substrate which forms a MOS structure. The total capacitance C_{total} is a series combination of the insulator capacitance C_{ox} and the depletion capacitance C_D, given as

$$C_{total} = (1/C_{ox} + 1/C_D)^{-1} = \frac{C_{ox}C_D}{C_{ox} + C_D}. \tag{7.1}$$

The serial capacitance of each element is determined by the parallel plate capacitor formula,

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d} \tag{7.2}$$

where A is the tip radius in contact with the sample surface, ε_r the relative dielectric constant of the corresponding material ($\varepsilon_{SiO_2} = 3.9$ and $\varepsilon_{Si} = 11.9$) and d is the thickness of the corresponding layer (d_{ox}, $d_{ep.Si}$). For a given insulator thickness d_{ox}, the value of C_{ox} is constant and corresponds to the maximum capacitance of the system. When all carriers are accumulated at the Si/SiO_2 interface, the total capacitance is independent of the depletion capacitance and hence, close to the oxide capacitance of the system. With decreasing bias the depletion region expands because the ionised donors build up charge to compensate for the applied electrostatic field. The depletion depth d_{depl} is strongly dependent on

the doping density. While heavily doped silicon displays only a small depletion depth, in low-doped silicon donors need to be ionised down to much deeper layers to build up the same amount of charge. Because $C_D \propto 1/d_{depl}$ a small depletion depth results in a higher capacitance value. But due to the serial relation to the oxide capacitance, C_{total} is governed by the smallest capacitance element (see Equation A.6). This means that a higher change in C (dC/dV) value corresponds to low carrier concentrations, while a lower change in C (dC/dV) value corresponds to higher carrier concentrations. The dS_{11}/dV magnitude is the same for n and p-type dopants but of opposite sign and hence, it can be used to characterise the structure and type of dopant in semiconductor devices [222].

For imaging, maximum sensitivity is achieved when adjusting V_{AC} at that point where the capacitance-voltage (CV) curve has its largest slope which is around the flat band voltage (here at $U = 0\,\text{V}$) [222]. The reader is referred to section A.3.2 in the appendix for a more detailed explanation where MOS diode theory was applied to a simplified tip-sample model. Until now, differential dS_{11}/dV was mainly used to image metal-oxide-semiconductor (MOS) structures, such as a gold contact directly placed on p-type silicon, and MOS capacitors of varying oxide thicknesses for dopant profiling [223]. Calculated MOS capacitance, labeled C_t, as well as the obtained spectroscopy dC/dV amplitude curves versus DC tip bias on differently n-type doped silicon region are shown in Figure 7.3. The maximum change in capacitance C_t in Figure 7.3a) and the maximum dC/dV amplitude peak value in Figure 7.3b) is highest for the lowest n-doped region. The CV and dC/dV curves

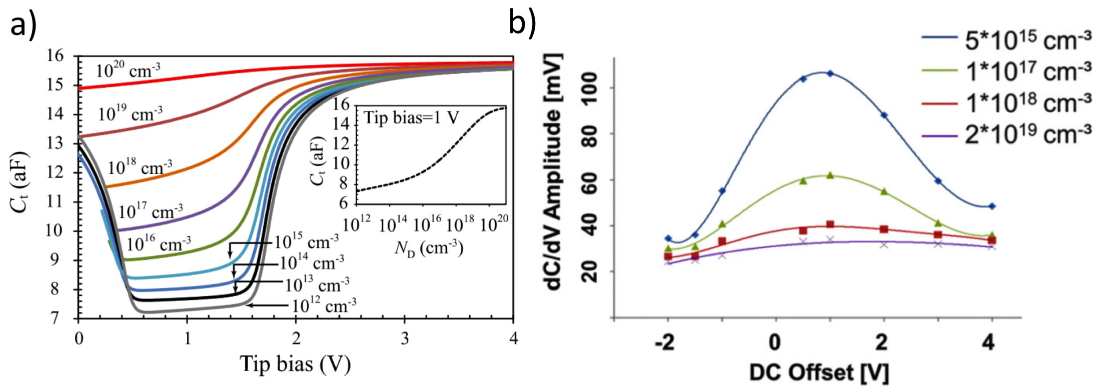


Figure 7.3: Left: Typical calculated MOS capacitance C_t voltage curves for a spherical tip of $R = 50\,\text{nm}$ in the n-type carrier range of $10^{12} - 10^{20}\,\text{cm}^{-3}$.The rise in capacitance at $V < 0.5\,\text{V}$ only occurs due to strong inversion for low frequencies (see section A.3.1). The inset indicates the carrier concentration dependence of the capacitance obtained at the applied DC bias of 1V contact (From [224]). Right: Spectroscopy curves showing dC/dV amplitude versus DC tip bias on differently doped regions of a n-type semiconductor (From [225]).

are shifted in positive bias direction caused by a varying flat band voltages of the differently doped MOS regions (see section A.3.1). Besides using differential capacitance dC/dV spectroscopy for spatially resolved dopant profiling on calibration samples, only a few studies have been reported on real devices such as a hetero-bipolar SRAM sample [225] and sub-surface semiconductor wafer devices [194]. The obvious reason is the need of a calibration sample to calibrate the measured dC/dV signal into dopant density or in quantitative values (e.g. aF/V).

A major disadvantage of SMM is the fact that is measuring in contact mode. By applying a DC bias between tip and sample, charges and contamination in and on the surface at ambient temperatures tend to modify the tip sample contact, resulting in unstable scanning conditions. Especially SMM CV imaging is very sensitive to surface contamination, while the dC/dV signal is more robust [191]. One possible solution to circumvent the problem is by combining SMM with a non-contact dC/dV method such as the scanning capacitance force microscope (SCFM). Figure 7.4 displays the calculated capacitance gradient dC/dV for a 50 nm tip at 10 nm separation above a silicon surface for different doping concentrations. To

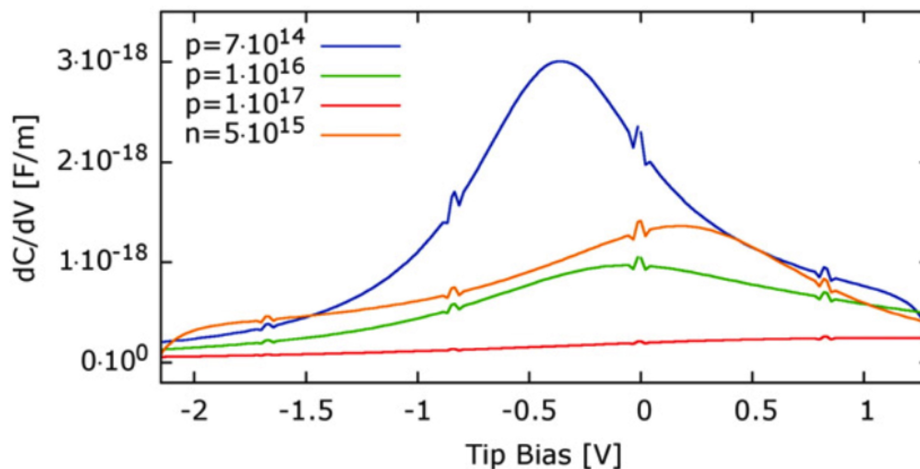


Figure 7.4: Calculated capacitance gradient dC/dV for a 50 nm tip at 10 nm separation above a silicon surface for different doping concentrations. The biggest gradient is observed for the smallest dopant density. The small ripples on the gradient curves are caused by numerical artefacts (From [226]).

study electrical properties of low dimension material *e.g.* two dimensional electron gases (2DEGs) with SMM or SCFM at room-temperature (RT), it is an advantage to decouple their electrical properties from those of the substrate. Thus, most of the studied 2D material such as MoS_2, WSe_2 [227], nanotubes [190] and/or graphene [228] were placed on top of a thick thermal oxide. SMM can be used to probe capacitance and conductance contribu-

tions that arise from the finite local density of states (LDOS) of low-dimensional materials, the so called 'quantum capacitance '. Classical capacitors are solely determined by their geometric dimensions and the electron charge distribution in the capacitor to minimise the electrostatic energy [229]. In addition to the classical geometric capacitance C_{geo} of the 2DEG, the LDOS at extra energies add additional contributions to the capacitance defined as $C_q = \frac{\partial Q}{\partial V_a}$, where Q is the voltage-dependent two-dimensional charge density and V_a is the local electrostatic potential. A detailed expression for C_q for a 2D system can be found in references [230] and [231]. C_q adds in series to the C_{geo} which reduces the total capacitance of the 2DEG, yielding the capacitance of the 2DEG as

$$C_{\mathrm{2DEG}} = (1/C_{\mathrm{geo}} + 1/C_q)^{-1}. \tag{7.3}$$

C_q contributions to the total capacitance have been reported for prepared 2D systems using $\mathrm{dS_{11}/dV}$ spectroscopy. Berweger *et al.* performed SMM imaging and $\mathrm{dS_{11}/dV}$ spectroscopy on transition metal dichalcogenides (TMDs), more explicitly, on a single layer of MoS_2 and n- and p-doped WSe_2 located on a 260 nm thick thermally grown oxide on p^{+2}-doped Si, results are shown in Figure 7.5. They use the integrated density of states at the band edged to find a relationship between charge carrier density and applied voltage. By comparing simulated to measured $\mathrm{dS_{11}/dV}$-voltage curves, they determine the quantum capacitance to be $C_q = 100\,\mathrm{nF/cm^2}$ which is significantly smaller than typical values for 2D materials of $1-10\,\mu\mathrm{F/cm^2}$ [228, 232].

So far, buried 2D materials exhibiting 2DEG properties in silicon have not been characterised quantitatively with $\mathrm{dS_{11}/dV}$ imaging or spectroscopy. Especially investigations of buried patterned δ-layer nanostructures at RT are lacking. Buried patterned P nanostructures are components for future surface code quantum computing proposals [21] and their characterisation with differential $\mathrm{dS_{11}/dV}$ setup can aid the improvement and speed up of nanoscale P device fabrication. In addition, studies reporting the characterisation of active devices are rare as is the use of a combination of multiple scanning probe techniques to detect different properties of the same sample characteristics.

In this chapter we exploit the full range of scanning probe capabilities of a SMM setup to i) perform calibrated $\mathrm{dS_{11}/dV}$ imaging and spectroscopy on buried nanostructures and ii) to characterise a buried nano-patterned P wire (hereafter referred to as P-wire) in working condition, meaning while applying an in-plane bias. We first apply a tip sample bias to sample 1

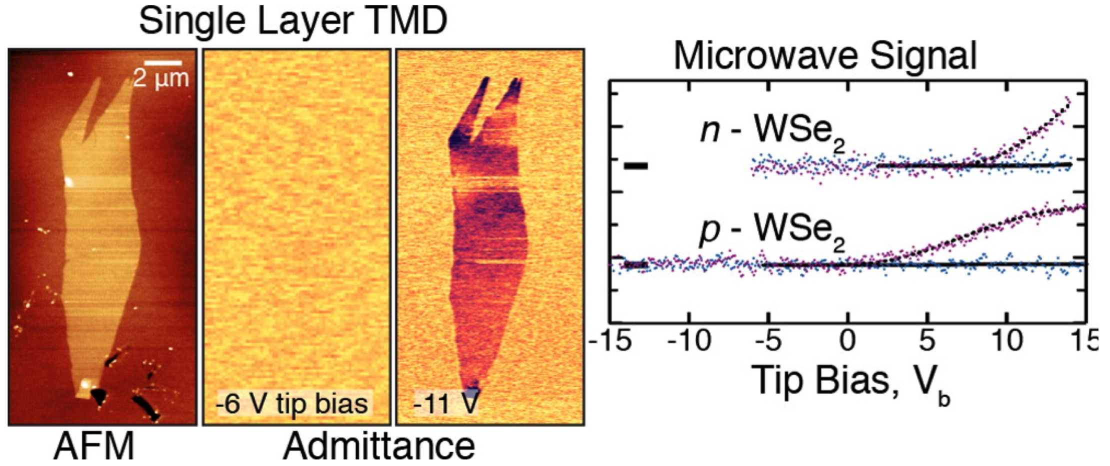


Figure 7.5: SMM on transition metal dichalcogenides (TMDs). Left: AFM topography and dY_{11}/dV images of the resistive component of a single layer MoS_2 with tip-sample bias V_b as indicated. Right: Resistive (purple) and capacitance (blue) components of dY_{11}/dV voltage sweeps obtained from a few layer n and p-WSe_2. Dashed lines in Re$[dY_{11}/dV]$ are fits to a modelled Re$[dY_{11}/dV]$. Solid line in Im$[dY_{11}/dV]$ fits to a modelled Im$[dY_{11}/dV]$ by considering a quantum capacitance (From [191])

while the reflected S_{11} Ghz-signal is modulated with a low frequency ($30-75$ kHz) AC bias ($\approx 3V$) to measure the dS_{11}/dV response with respect to the applied bias. We demonstrate how dS_{11}/dV spectroscopy in conjunction with FEM-modelling can be employed to identify contributions to the admittance that originate from the substrate, the patterned δ-layer region and the 2D nature of the 2DEG. By obtaining dS_{11}/dV spectroscopy curves from this pure and unperturbed sample setup, quantified parameter such as capacitance derivative dC/dV and conductance derivative dG/dV can be extracted.

In the second part of the chapter we make use of the broad range of characterisation tools available with a modified SMM setup to characterise a buried P-wire. The fabrication and contacting process of the P-wire is briefly outlined. The versatile setup allows us to easily switch between different scanning probe microscopy (SPM) operation modes, such as kelvin probe force microscope (KPFM), SCFM and SMM. For the first time, a buried P-wire is characterised at RT and quantitative parameters such as contact potential and carrier density are extracted.

This study was carried out in a collaborative work, where sample fabrication, measurement and parts of the analysis were carried out by the author. Part of measuring, modelling and analysing of the obtained data has been done by George Gramse. A manuscript is in preparation for publication, with the author leading this publication.

7.2 dS_{11}/dV spectroscopy and imaging of buried nanostructures

We now present dS_{11}/dV imaging and point dS_{11}/dV spectroscopy data obtained on patterned P regions of sample 1. The same commercial transmission line SMM was employed as described in section 6.2, consisting of standard 5600 atomic force microscope (AFM) interfaced with a 20 GHz vector network analyser (VNA) in conjunction with a DPMM module with lock-in amplifier for dC/dV measurement.

For a good comparison to the results of the previous chapter 6, we measured the same sample region, comprising an incorporated square and triangle of phosphorus accompanied by a depassivated triangle region. For clarity, first, the characteristics of dS_{11}/dV imaging and spectroscopy will be pointed out. We then focus in detail on the obtained dC/dV and dG/dV gradient curves and discuss the underlaying physical principles supported by finite element modelling of the system.

7.2.1 dS_{11}/dV imaging

The dC/dV image in Figure7.6a) has been acquired with the same tip (apex radius $\approx 20nm$) as in Figure 6.9, giving a strong differential capacitance signal of the STM-patterned phosphorus layers at zero DC bias and a locally highly resolved image. Obtaining S_{11} and

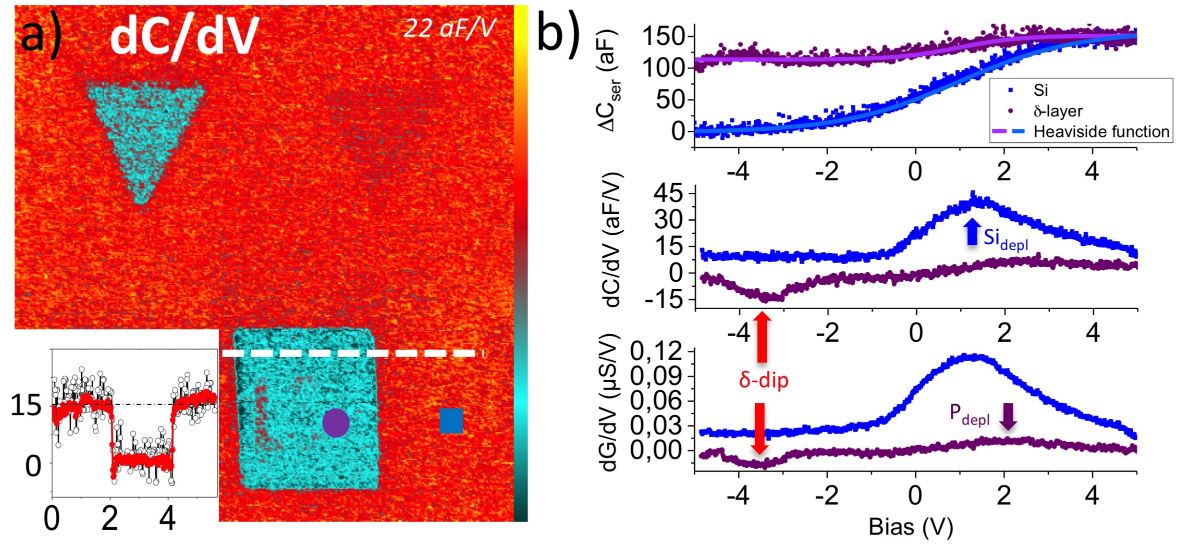


Figure 7.6: dS_{11}/dV imaging under changing bias conditions. a) dC/dV image acquired at $f = 19.36\,\text{GHz}$, $f_{LF} = 32\,\text{kHz}$, $V_{AC} = 3\,\text{V}$, $V_{DC} = 0\,\text{V}$ acquired with a small tip (apex radius $\approx 20nm$). b) Serial capacitance (ΔC_{ser}), capacitance dC/dV and conductance gradient dG/dV curves as function of tip bias. Curves on Si substrate (blue) and P-layer (purple) with a bigger tip (apex radius $r \approx 330\,\text{nm}$). As guide for the eyes blue/magenta solid lines represent fitting of a Heaviside function to the data.

dS_{11}/dV images at a fixed finite applied DC bias in contact with the sample often leads to

undesired charging effects and tip modifications during scanning. To avoid sample contamination by tip interaction with material on the surface at ambient temperature, we can circumvent these effects by setting the DC bias to zero and applying a low frequency (here 32 kHz) AC signal, which modulates S_{11}. Even on the right hand side triangle, patterned by only depassivated hydrogen, a very slight contrast can be observed, pointing to a possible difference in interfacial structure or overlayer morphology. The effective low carrier modulation of nanostructured phosphorus regions with respect to the surrounding substrate under changing bias gives rise to an increased contrast of $\sim 15\,\mathrm{aF/V}$ compared to $(2.1 \pm 0.1)\,\mathrm{aF}$ obtained for the nanostructured phosphorus square from the calibrated SMM capacitance in Figure 6.9. In contrast to the low-doped substrate ($n_{\mathrm{substrate}} = 2.5 \times 10^{14}\,\mathrm{cm}^{-3}$) where the capacitance change is governed by the width of the depletion layer d_{depl}, the buried dopant nanostructures form local conducting planes below the surface, remaining largely unaffected by the applied AC bias modulation. Hence, the surrounding substrate is heavily modulated around the patterned features, as can be seen in the in Figure 7.6a), resulting in a negative contrast with respect to the surrounding silicon, compared to the positive contrast in calibrated SMM capacitance images which results from a increased serial capacitance with respect to the substrate.

7.2.2 Serial capacitance spectroscopy

The different sensitivity between substrate and P nanostructured regions under changing bias described above is also reflected in the serial capacitance ΔC_{ser} curves, seen in the top panel of Figure 7.6b), obtained with a larger tip ($\approx 330\,\mathrm{nm}$) on locations highlighted in the dC/dV image in Figure 7.6a). The advantage of using larger tips is to benefit from an overall stronger signal and sensitivity compared to tips with smaller radius of curvature, as demonstrated in serial capacitance (C_{ser}) and capacitance gradient curves obtained at the same location shown in Figure A.13 in the appendix.

The local sensitivity variation and resulting response in absolute serial capacitance as a function of DC bias can be exploited to improve the contrast between patterned phosphorus layer and silicon substrate for imaging. By simply working in the silicon depletion region (high negative bias) the serial capacitance difference between P and the substrate regions of $(29.08 \pm 1.17)\,\mathrm{aF}$ at zero bias increases to $(96.86 \pm 0.68)\,\mathrm{aF}$ at $U < -3.4\,\mathrm{V}$, making a total contrast increase of $(67.78 \pm 1.86)\,\mathrm{aF}$. At $U < -3.4V$, the capacitance signal approximately saturates for both, substrate and δ-layer, indicating that the detectable change in depletion

capacitance has reached its limit. As the bias becomes larger $U > 1.5V$, more electrons are accumulated at the Si/SiO_2 interface region and the serial capacitance approaches the constant serial capacitance of the SiO_2 [224]. By averaging the serial substrate capacitance between $4\,\mathrm{V} < U < 5\,\mathrm{V}$ we determine the constant serial capacitance of the SiO_2 as

$$\Delta C_{SiO_2} = (136.58 \pm 0.8)\,\mathrm{aF}. \tag{7.4}$$

As explained in the introduction, at this high positive bias the detected signal does not depend on the depletion width of the substrate, because all carrier are in accumulation directly under the Si/SiO_2 interface.

7.2.3 $\mathbf{dS_{11}/dV}$ spectroscopy

We now focus on the signature of capacitance dC/dV and conductance dG/dV gradient curves, displayed in the middle and bottom panel of Figure 7.6b). In contrast to the absolute serial capacitance measurement, only bias-dependent elements in the MOS structure are detected in the dS_{11}/dV signal, which gives rise to an increased sensitivity to the intrinsic electrical properties of the sample. That is because the total dielectric admittance $Y_{\mathrm{dielectric}}$ which is the series combination of oxide and the epitaxial silicon admittance (Y_{Si0_2} and $Y_{ep.Si}$, respectively) is estimated to be constant and thus, voltage independent,

$$\frac{d}{dV} Y_{\mathrm{dielectric}} = \frac{d}{dV}\left(\frac{Y_{Si0_2} \cdot Y_{ep.Si}}{Y_{Si0_2} + Y_{ep.Si}}\right) = 0\,. \tag{7.5}$$

Sensitive lock-in-detection of the gradient dS_{11}/dV signal at varying applied DC bias from $-5 < U < 5$ yields the complex dC/dV and dG/dV channels after applying the calibration procedure (middle and bottom panel in Figure7.6b) respectively). We take a closer look at the positions and heights of the observable peaks obtained on the substrate and the patterned δ-layer in Figure 7.6b).

First, the most apparent feature in the spectra is the Si peak arising at a positive bias position of $(1.39 \pm 0.01)\,\mathrm{V}$ and $(1.37 \pm 0.01)\,\mathrm{V}$ in the dC/dV and dG/dV curve, respectively (blue arrow). For the phosphorus doped regions only a hardly visible, much smaller and wider peak emerges at $(2.79 \pm 0.02)\,\mathrm{V}$ and $(2.25 \pm 0.02)\,\mathrm{V}$ in the corresponding channels (purple arrow). Second, besides the total shift of both peaks to positive bias, we observe a large relative voltage offset of $(1.40 \pm 0.03)\,\mathrm{V}$ and $(0.88 \pm 0.03)\,\mathrm{V}$ between the Si and P peak maxima in both channels.

The relative shift and relative height difference of $\sim 22\,\frac{\text{aF}}{\text{V}}$ ($\sim 0.06\,\frac{\mu\text{S}}{\text{V}}$) $\Delta dC/dV$ ($\Delta dG/dV$) between the peak maxima can be attributed to the dopant density dependent flat band position and difference in depletion layer depth between low-doped substrate and regions featuring densely packed patterned phosphorus. The peaks are further referred to as silicon depletion Si_{depl} and phosphorus depletion P_{depl} peaks.

In addition to a modulation of the depletion layer width, the tip-sample bias also affects the electronic properties of the phosphorus layer. A clear dip in the capacitance gradient dC/dV at $(-3.36 \pm 0.01)\,\text{V}$ accompanied by a dip in the conductance gradient dG/dV at $(-3.58 \pm 0.01)\,\frac{\mu\text{S}}{\text{V}}$ is observed only for the patterned δ-layer region (red arrow). Because the dip is not present for the substrate, we assign this dip to a signature of the P nanostructured region, further referred to as 'δ-dip'.

7.2.4 Finite element modelling of $\mathbf{dS_{11}/dV}$ spectroscopy curves

For a qualitative interpretation of the experimental data, the simple picture of the MOS model (see section A.3.2 in appendix) where the δ-layer is approximated by a bulk doped region of equal dopant density, has to be refined. The precise geometry of the system and the confinement of the dopants in the δ-layer is taken into account. We used finite element modelling (FEM) to calculate the theoretical admittance gradient as a function of applied voltage for the substrate and the patterned δ-layer similar to the δ-layer model used in chapter 6 (see Figure 6.10a).

First, we simulate the substrate response under changing bias. For this, the substrate admittance gradient, given as

$$\frac{d}{dV}Y_{\text{substrate}} = \frac{d}{dV}[\frac{1}{R_{depl}} + i\omega C_{depl}], \tag{7.6}$$

for a set of bulk dopant densities ($d = 10^{14} - 10^{20}\,\text{cm}^{-3}$) is computed and plotted as a function of applied DC bias, see Figure7.7a)+b). The simulated capacitance gradient displays a strong dopant density dependance, as expected and drops from $\sim 40\,\frac{\text{aF}}{\text{V}}$ to almost $\sim 0\,\frac{\text{aF}}{\text{V}}$ from $d = 10^{14}\,\text{cm}^{-3}$ to $10^{16}\,\text{cm}^{-3}$. In contrast, the conductance gradient dG/dV exhibits a non-monotonic dependance to variations in this dopant density range, similar to the modelled conductance dependence of a δ-layer in Figure 6.10d). The simulated dC/dV and dG/dV channel of a bulk-doped model display a good agreement with the obtained spectroscopy curves on the substrate for the position of the peaks and their heights, as shown

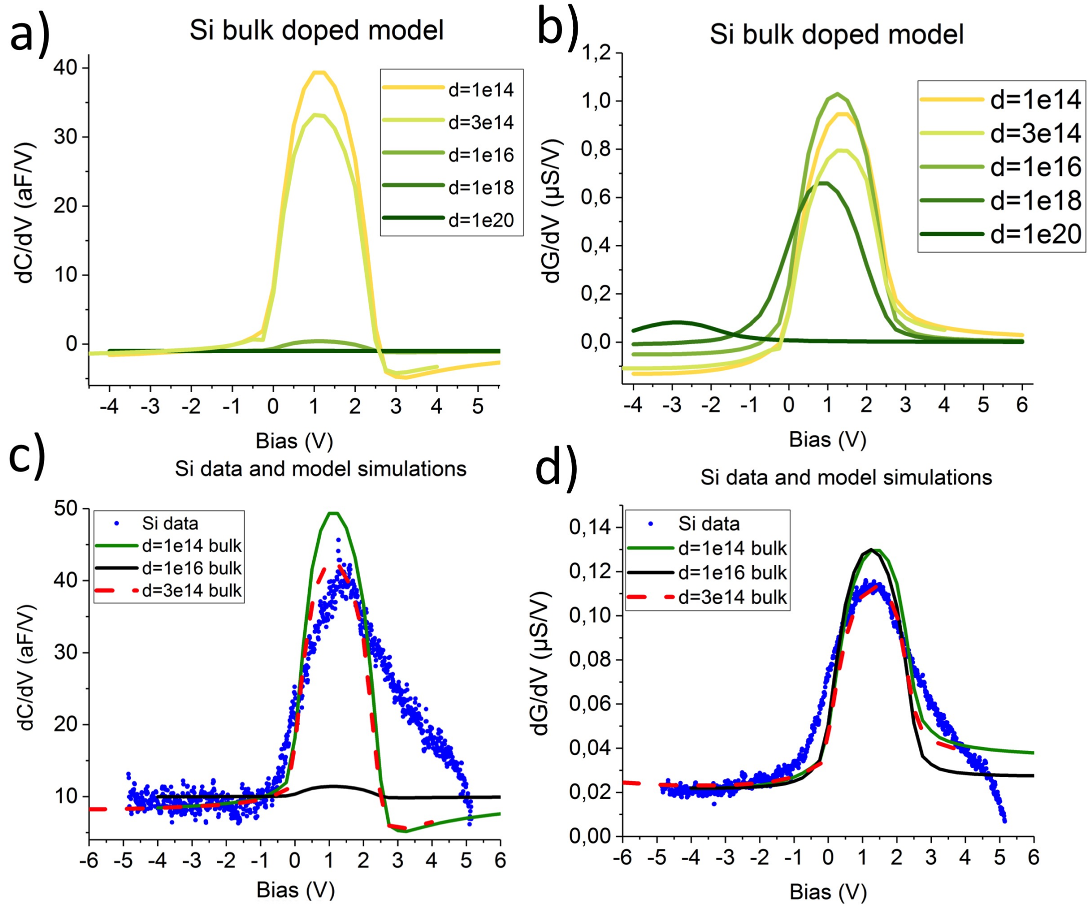


Figure 7.7: Finite element modelled admittance gradient for a set of bulk dopant densities ($d = 10^{14} - 10^{20}\,\mathrm{cm}^{-3}$) as a function of applied DC bias. a) Strong dopant density dependance of the capacitance gradient with varying bias .b) The conductance gradient dG/dV displays less sensitivity to a change in dopant density, but exhibits a peak shift to negative bias for very high dopant densities. c)+d) The simulated dC/dV and dG/dV signals display a good agreement with the obtained spectroscopy curves on the substrate.

in Figure 7.7c)+d). Parameters chosen for the model: oxide thickness $d = 2nm$, substrate density $n_d = 3 \times 10^{14}\,\mathrm{cm}^{-3}$, tip work function $W_{a,Pt} = 5.3\,\mathrm{eV}$, electron affinity of silicon $\chi_{Si} = 4.05\,\mathrm{eV}$ [233]. A pronounced deviation to the simulated curves is apparent in the experimentally obtained peak shapes, displaying a shoulder especially in the higher positive bias region (carrier accumulation) suggesting a tip effect and/or the presence of charges in interfacial traps. A smaller tip radius would result in a lower overall dS_{11}/dV signal and due to a locally more sensitive tip the width of the dC/dV and dG/dV peak is slightly reduced as demonstrated in Figure A.13 in the appendix. The effect of interface trapped charges at the Si/SiO_2 interface and in the silicon oxide on the shape of the CV curve is presented in section A.3.3 in the appendix. Especially charge traps located at the Si/SiO_2 interface

trap electrons such that a higher applied voltage is required to accomplish the same surface potential [53]. As a result the CV curve is stretched out in the voltage direction which is reflected in a broadening of the dC/dV peak in Figure 7.7c)+d). An asymmetric broadening indicates the presence of a majority of p-type traps of presumably trivalent Si atoms (silicon atoms just bound to only three other Si atoms) [37]. The agreement with the simulation confirms the conceptual viability of our model setup.

In order to simulate the spectroscopy curves with patterned δ-layer present we have chosen three different approaches to include the finite depth and confinement of the P dopants in the surrounding silicon substrate. The first model comprises a 15 nm surface doped region with an abrupt cut-off down to substrate density. This 'surface doped' approach is motivated by the acquired SIMS profile of a saturation dosed δ-layer in section 4.4.2, in the discussion 5.4.4 and section 6.7, displaying a dopant profile of high density ($d \sim 10^{20}\,\mathrm{cm}^{-3}$) within the 15 nm surface region due to dopant segregation. Second, the phosphorus is modelled as a thin layer (3 nm) with a dopant-dependent conductivity, σ_p, embedded at a depth of 15 nm in the depletion layer of the low-doped silicon substrate. In this 'δ-doped model' only the dopant density within the confined δ-region is varied. In the third approach, in addition to an embedded δ-layer of $d = 10^{21}\,\mathrm{cm}^{-3}$, a second high δ-doped region of $d = 3 \times 10^{20}\,\mathrm{cm}^{-3}$ positioned at 1 nm under the surface is added to the model to explore the effect of two separated dopant profiles on the responding spectroscopy curves. The detailed plots of the simulations can be found in Figure A.14 in the appendix. Instead, the simulated capacitance and conductance gradient curves from the different models are plotted as a function of applied voltage in Figure 7.8. Most agreement with the obtained P_{depl} peak in the dC/dV spectroscopy data provided the second δ-doped model using dopant densities of $d = 10^{18}\,\mathrm{cm}^{-3}$ (green), $d = 10^{20}\,\mathrm{cm}^{-3}$ (orange) and $d = 10^{21}\,\mathrm{cm}^{-3}$ (black) as well as the third double δ-layer approach (red). Using the surface or bulk-doped model, in contrast, did not result in a good fit to the obtained dC/dV curve. In the dG/dV channel the closest match between simulation and experiment is visible for the highly doped δ-layer model and the double δ-layer approach. Surface- or bulk-doped model as well as the double δ-layer model exhibit a peak at higher negative bias. None of the simulations could model the presence of the δ-dip at negative bias in both channels.

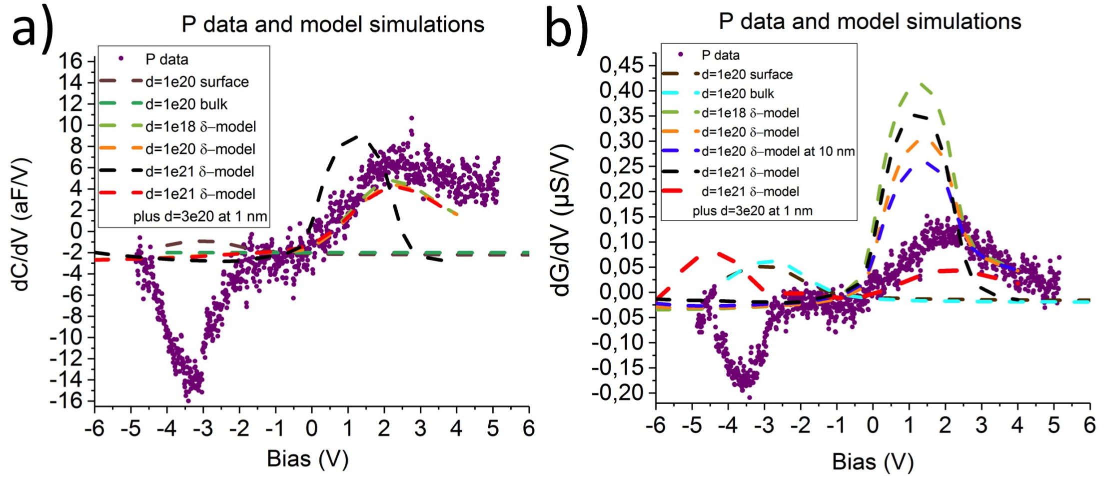


Figure 7.8: Finite element modelled capacitance and conductance gradient from different models are plotted as a function of applied voltage together with the obtained experimental values obtained for the patterned δ-layer.

7.2.5 Discussion

In the discussion, we focus on the presence of the P_{depl} peak and δ-dip.

The simulation of different dopant models suggest that the phosphorus depletion peak P_{depl} at positive bias can only be understood when using the δ-doped model where P dopants reside in a confined dopant profile embedded in the substrate 15 nm under the surface. The simulations give rise to a reduced dC/dV and dG/dV depletion peak signal and to a relative peak shift in positive bias direction compared to the Si substrate. The relative shift can be attributed to an increased contact potential difference between the metal tip and highly P doped regions. Although the relative shift of $(1.40 \pm 0.03)\,\mathrm{V}$ (dC/dV) and $(0.88 \pm 0.03)\,\mathrm{V}$ (dG/dV) between the Si and P depletion peak maxima is larger than the calculated $\Delta V_{CPD}(\delta/\mathrm{substrate}) = 0.335\,\mathrm{V}$ from the MOS model in section A.3.2 in the appendix, the more accurate description of the sample-tip geometry using FEM exhibits good agreement with the experimental P_{depl} peak position.

From the surface-doped model that aimed to reflect the measured SIMS dopant profile of the δ-layer in the modelling, we observe a higher sensitivity of the dC/dV signal at lower doping densities (compare Figure A.14a) and b) in the appendix) when the depletion width exceeds the 15 nm surface doped region. The confinement of a highly doped 15 nm surface region in turn does not lead to a P depletion peak at positive bias and thus can not explain the height and position of the P_{depl} (same for the bulk doped model). In fact, all models where a high P dopant density is in direct contact with the SiO_2 interface, exhibit no depletion peak

at positive bias but a small peak at high negative bias (between ~ -3 V to -4 V) in both channels. One possible explanation of that peak could be that the AC modulation bias can not cause any physical displacement modulation of the carrier when the depletion layer is located very close to the surface. Only when the depletion layer is moved deeper into the sample with increasing negative bias, away from the oxide, the effective carrier modulation increases which is reflected in a peak in capacitance and conductance derivative channel. This observation is supported by calculations of the depletion depth for degenerately doped bulk silicon using a simple MOS system, as presented in Figure A.10 the appendix. The depletion depth was determined as $4-10$ nm at $U = -5$ V which is very close to the surface and implies that for heavily doped silicon the depletion width will remain inside the doped surface region, not showing any depletion peak at positive bias.

In the δ-doped model, the depletion capacitance and conductance appear as a non-linear function of the dopant density which has been demonstrated earlier in Figure 6.10 for a smaller tip ($r \sim 20$ nm). And thus, the derivative capacitance and conductance value of P_{depl} do not monotonically decrease with increasing dopant density (see $d = 10^{21}\,\text{cm}^{-3}$ (black curve) in Figure 7.8a)).

Finally, in the double δ-layer model we explore the effect of an additional highly confined δ-doped region 1 nm under the surface, that shows up in the SIMS profile where the phosphorus in the oxide layer is considered to be inactive. In addition to a smaller depletion P_{depl} peak, the simulated dG/dV signal of the double δ-layer model displays an additional conductance peak at ~ -4.5 V. In the depletion picture, the low-doped substrate region between the δ-layers and the surface gives rise to the first depletion peak. With decreasing bias, the depletion width sinks deeper into the sample until it exceeds the depth of the deeper buried δ-layer. Thus, the additional peak at high negative bias can possibly be assigned to the sharp cut-off from the high density at the δ-layer to the low substrate density. None of the simulations could predict the presence of the δ-dip at $-3.36V$ and -3.58 (dC/dV and dG/dV) in both channels. In fact, the bulk, surface and double δ-layer model suggest an exact opposite response of the capacitance and conductance of the P system at high negative bias. The fact that the dip is observed only for the patterned δ-layer and not on the substrate suggests a selective effect for the P δ- layer region. The narrow FWHM of 1.4 V and 1.15 V of the dips indicates a sharp decrease in capacitance and conductance which points towards a turn on voltage of an energy state effect. When the applied bias at the tip is high enough to

overcome the oxide barrier, electrons of the tip can potentially tunnel into the empty states of the sample. For the case of a phosphorus δ-layer the 2DEG comprises two impurity bands, the Γ- and the Δ-band, located in the band gap of silicon. Tunnelling into these states would lead to a decrease in capacitance in the parallel plate MOS capacitor picture and reduced conductance. If this 'δ-dip' can be associated with the quantum capacitance of the 2DEG, as mentioned in the introduction, it needs further systematic investigation. So far, we did not include the effect of oxide charges and tunneling in the model. An improvement of the model needs further analysis of the system parameters.

7.2.6 Summary

We applied an AC modulation bias to perform dS_{11}/dV imaging under changing bias conditions on phosphorus nanostructures and demonstrated that the effective low carrier modulation of nanostructured phosphorus regions with respect to the surrounding substrate can be exploited to obtain locally high resolved dC/dV images with increased contrast of $\sim 15\,\mathrm{aF/V}$, in contrast to calibrated SMM capacitance images.

Even for the depassivated triangle region with no P in Figure 7.6a), a very slight contrast can be observed, pointing to a possible difference in interfacial structure or overlayer morphology. This highlights the increased sensitivity of voltage modulated imaging and the applicability of dS_{11}/dV for defect imaging and growth process characterisation of STM naostructured devices. Further, from obtained capacitance spectroscopy curves we demonstrate that due to the local sensitivity variation and resulting response in absolute serial capacitance with changing DC bias, the total imaging contrast can be increased by $(67.78 \pm 1.86)\,\mathrm{aF}$ ($\sim 230\%$) by simply working in the silicon depletion region ($U < -3.4\,\mathrm{V}$).

We performed sensitive lock-in-detection of the dS_{11}/dV signal at varying applied DC bias from $-5 < U < 5$ which yields the complex dC/dV and dG/dV channels after applied calibration procedure. We showed that dS_{11}/dV spectroscopy is sensitive to the small changes of electrical properties of a sample. Finite element modelling is employed to simulate dC/dV and dG/dV spectroscopy curves using a bulk doped model which displays a good agreement with the obtained spectroscopy curves on the substrate and confirms the conceptional viability of our model setup. For the obtained spectroscopy curves on patterned phosphorus regions, we find that position and height of the reduced depletion layer peak shows only agreement to a model where the phosphorus is simulated as a thin, confined layer (3 nm) of high dopant density ($d = 10^{18} - 10^{21}\,\mathrm{cm}^{-3}$) embedded at a depth of 15 nm

in the depletion layer of the low-doped silicon substrate. In addition to a modulation of depletion layer width, we find that the tip-sample bias also selectively modulates the electronic properties of the phosphorus layer region, exhibiting a clear 'δ-dip' at $-3.36\,\mathrm{V}$ and $-3.58\,\mathrm{V}$ (dCdV and dGdV) in both channels. The narrow FWHM of 1.4 V and 1.15 V of the dips indicate a sharp voltage onset of an energy state effect, possibly from the finite DOS of the phosphorus 2DEG. A detailed analysis of the physical origin of this 'δ-dip' is subject to ongoing research.

7.3 Scanning microwave microscopy of a buried nanowire

In the following section, we exploit the full range of scanning probe microscopy (SPM) capabilities of an advanced SMM setup to characterise a P-wire in working condition, meaning while applying an in-plane bias. The versatile setup allows us to easily switch between different operation modes such as kelvin probe force microscope (KPFM), scanning capacitance force microscope (SCFM) and scanning microwave microscope (SMM). At first, fabrication and contacting procedure of the P-wire is briefly presented and the SPM setup and methods used are introduced. We then qualitatively characterise the transport properties of the P-wire by detecting the contact potential, the capacitance derivative originating from carrier density as well as the capacitance and conductance derivative. KPFM and SCFM work in non-contact operation mode and have less physical interactions with the sample surface, while in SMM the tip is in contact with the sample surface. For SMM spectroscopy, we therefore use the more robust dS_{11}/dV signal and propose a new scan technique to minimise charging and tip modification effects induced by contamination of the surface.

7.3.1 Fabrication of a δ-layer wire for powered device characterisation

The fabrication process of the buried P-wire structure is summarised in Figure 7.9. Follow-

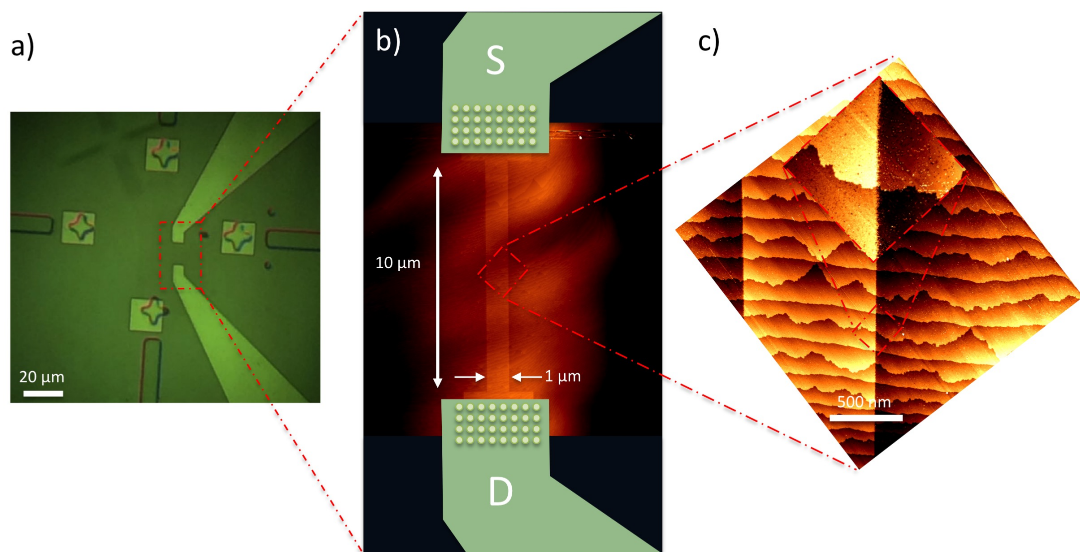


Figure 7.9: Sample design of the buried P nanowire. a) Micrograph of the active device area showing alignment marker and S and D leads. b) STM filled states topography image ($U = -2.0\,\mathrm{V}$, $I = 20\,\mathrm{pA}$) of the patterned wire structure after hydrogen depassivation (Depassivation parameter: $U_{lith} = 8\,\mathrm{V}$, $I = 2\,\mathrm{nA}$, $100\frac{nm}{s}$), overlaid with a schematic of source (S) and drain (D) Al contacts (green). C) STM filled state topography image of the middle wire region after depassivation displaying flat single terraces of silicon, confirming a complete H-desorption within the depassivated area.

ing the standard cleaning and H-lithography procedure, as described in section 4.3, a region of clean terminated silicon has been depassivated in the shape of a $1\,\mu\text{m} \times 10\,\mu\text{m}$ wire with $2\,\mu\text{m} \times 3\,\mu\text{m}$ contact pads at each side of the wire ends. Depassivation parameters used were $U_{lith} = 8\,\text{V}$, $I = 2\,\text{nA}$ at a tip speed of $100\frac{nm}{s}$. The depassivation process for such a large structure took $\approx 20\,\text{h}$. The wire dimensions were chosen such that a large AFM tip can be conveniently approached to the active wire region between the source (S) and drain (D) contacts. This way, cross-talk between Al contacts and tip is minimised when scanning under changing bias condition. This enables us to characterise the wire properties without perturbations arising from the Al contacts. STM filled states topography images in Figure 7.10a)+b) and c) show a successful complete depassivation over the whole length of the patterned region. After exposing to a saturation-dose of 0.03 L, a close-up of the edge in

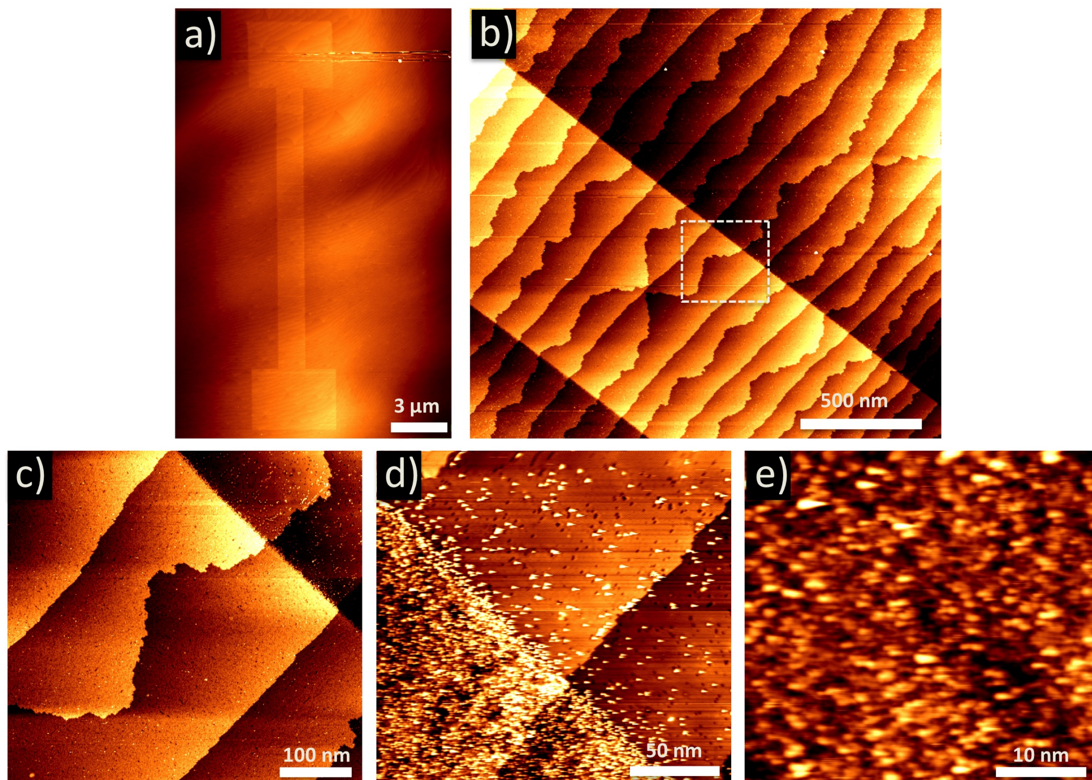


Figure 7.10: STM filled state topography images of the buried P nanowire structure after depassivating a region of clean terminated silicon a)-c) and confirming complete depassivation in the shape of a $1\,\mu\text{m} \times 10\,\mu\text{m}$ with $2\,\mu\text{m} \times 3\,\mu\text{m}$ contact pads at each side of the wire ends ($U = -2.0\,\text{V}$, $I = 0.02\,\text{nA}$, depassivation parameter: $U_{lith} = 8\,\text{V}$, $I = 2\,\text{pA}$, $100\frac{nm}{s}$). Surface after exposing to a saturation dose of 0.03 L reveal PH_3 adsorption exclusively in the depassivated region in d) and close-up in e).

the middle of the depassivated wire region (dashed white region in Figure 7.10b)) reveals PH_3 adsorption exclusively within the depassivated region, see Figure 7.10d) and close-up

in Figure 7.10e). Directly after exposing the surface to a background pressure of PH_3, STM imaging is challenging due to unstable tunnel conditions resulting from loosely attached PH_3 molecules in the tunnel junction. To minimise the risk of contaminating the patterned area with material from the tip, induced by PH_3 tip modifications, only a few low resolution images were aquired directly after dosing. In contrast to the standard fabrication procedure, the sample was annealed at $T \approx 350\,^{\circ}\mathrm{C}$ for $\approx 3\,\mathrm{min}$ radiatively. Switching to direct current heating on the sample was not possible, pointing towards an imperfect contact between sample and contact foil of the sample holder. The sample was encapsulated with $\approx 15\,\mathrm{nm}$ of silicon at an estimated sample growth temperature of $200-250\,^{\circ}\mathrm{C}$. An advantage in using resistive heating for the Si overgrowth is the absences of a temperature gradient across the sample, compared to direct current heating. However, the change in sample heating mode whilst Si sublimation might result in a modified growth process and sample characteristics of the epitaxial silicon. The sample was then taken out of UHV and the subsequent contacting process was performed as described in detail in section 4.5. The contacting process of the buried P-wire sample is briefly summarised in Figure 7.11. Electron beam lithography

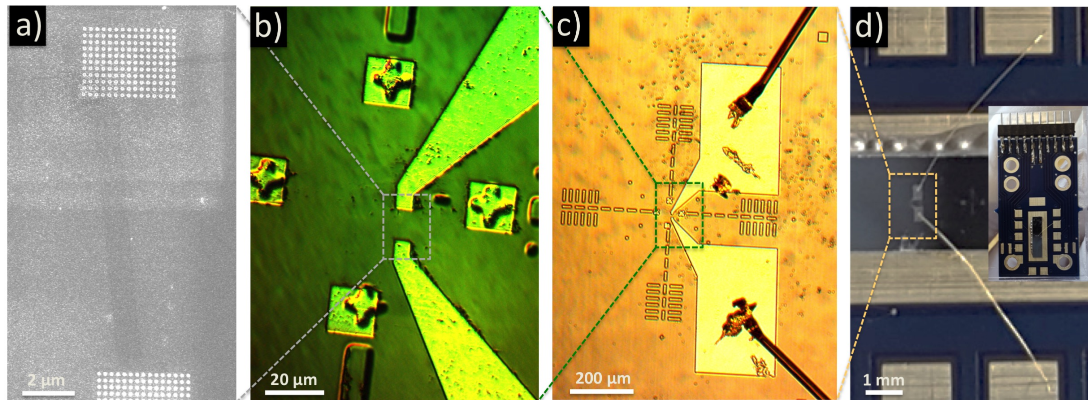


Figure 7.11: Contacting process of the buried P wire. a) EBL was used to align an array of deep etched vias over the region of the patterend P contact pads . b) and c) Al contact pads, defined by electron beam lithography (EBL), were fabricated by the deposition of 150 nm of alumnium (Al) onto the surface. The sample was mounted on a printed circuit board (PCB) d) and wire-bonded c) and d).

is used to align an array of deeply etched vias over the region of patterned P contact pads as shown in Figure 7.11a). Al contact pads, defined by EBL, were fabricated by the deposition of 150 nm of Al onto the surface (see Figure 7.11b)+c)). The sample was then mounted on a printed circuit board (PCB) and wire-bonded (see Figure 7.11 d)), ready for electrical measurement.

7.3.2 Scanning microwave microscope setup for a powered nanowire

In addition to the DPMM module in section 7.2, a DC source meter unit is used to apply an in-plane-bias to the buried wire offering both an accurate DC source as well as precise measurement channels for voltage and current. The AC modulation bias can be applied to the tip for sensitive charge carrier measurement in z-direction or on the S and D contacts in the transport (y) direction. In the latter configuration, the charge carrier between the SD contacts are modulated in the xy-plane and the measured signal in this setup is less affected by charge arising from the epitaxial layer and interfaces. The experimental setup is depicted in Figure 7.12. In analogy to the MOS model in section A.3.2 in the appendix,

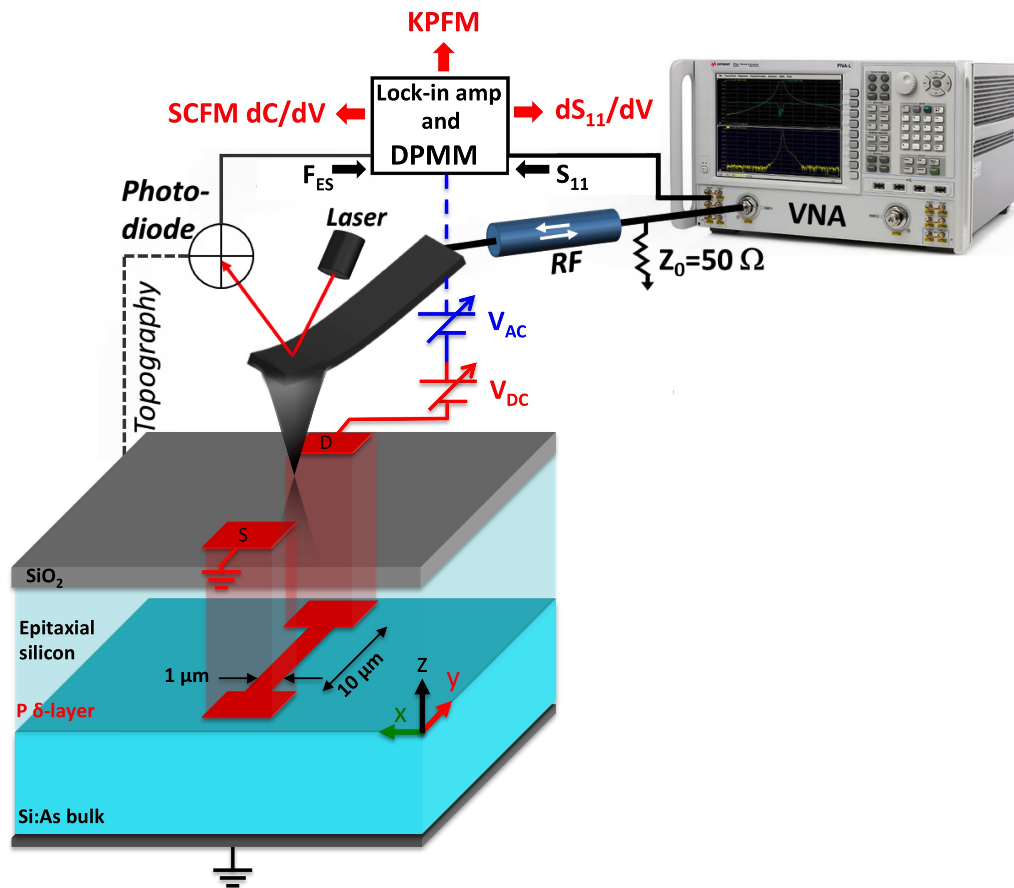


Figure 7.12: Scanning microwave microscope experimental setup for the characterisation of a buried nano-wire. A modulation AC plus a fixed DC bias is applied between S and D, resulting in a modulation of carrier in the region between the contacts. The change in charge carrier density is reflected in different physical properties which can be probed by lock-in detection of the electrostatic force signal F_{ES} by using kelvin probe force microscope (KPFM) for contact potential measurement, scanning capacitance force microscopy (SCFM), probing the change in carrier density $\partial C/\partial V$ and the scanning microwave microscope (SMM) to measure the local S_{11} and dS_{11}/dV reflection coefficient gradient by using the vector network analyser (VNA).

we estimate the detected admittance under the tip from a simple lumped element model shown schematically in Figure 7.13a)+b). Depending on the location of the tip between the S and D region, the local capacitance C_{local} is determined by the voltage dependent change of the local charge carrier density n_{local} in the substrate (C_{sub}) and the wire that adds in parallel. The $Si0_2$ plus epitaxial silicon dielectric capacitance adds in series with the voltage dependent local capacitance C_{local} yielding

$$C_{\mathrm{total}} = \left(\frac{1}{C_{\mathrm{SiO_2}}} + \frac{1}{C_{\mathrm{epi.Si}}} + \frac{1}{C_{\mathrm{local}}}\right)^{-1} \quad \text{where} \quad C_{\mathrm{local}} = C_{\mathrm{wire}} + C_{\mathrm{sub}} \tag{7.7}$$

Thus, due to the in-plane potential drop of the electrical field between the S and D contacts,

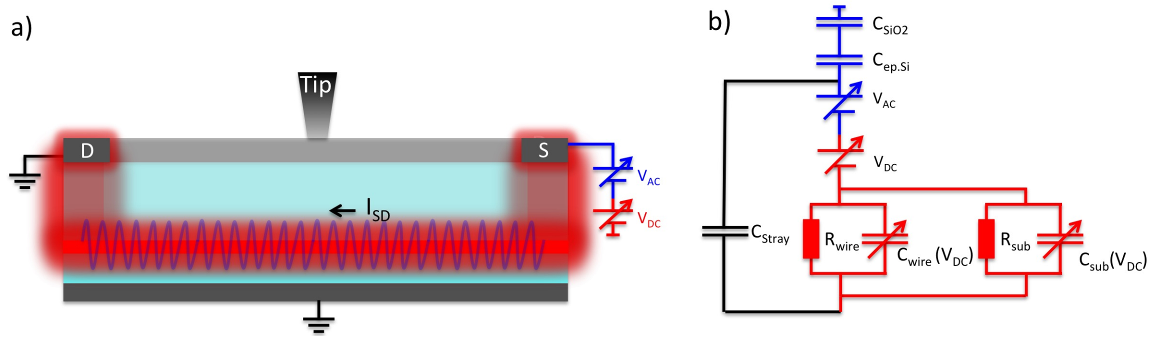


Figure 7.13: a) Cross sectional schematic of the sample composition under in-plane applied bias modulation. The AC bias applied in current direction is sensitive to variations of the charge carrier density of the substrate between SD contacts and inside the wire during transport. b) Lumped element model for the buried nano-wire. Capacitance contribution from SiO_2 and epitaxial silicon add in series to the local bias dependent capacitance C_{local} consisting of substrate and wire capacitance.

the tip only probes a fraction of applied bias at various locations between the contacts. In the parallel capacitance model, the local depletion width can be mapped for the silicon substrate and the saturation-doped wire. Applying a bias between S and D electrodes enables us to study the dynamic charge distribution of the system. The experiments are carried out at ambient temperatures in a dry atmosphere to account for an unintended oxide growth on the surface while applying a bias voltage.

This experimental setup is mainly establishing two novel things. First, instead of modulating the carriers in z-direction, an in-plane AC modulation bias applied between tip and sample directly affects the carriers inside the wire between the contacts. Thus, using this configuration, a direct in-plane change in carrier density of the working device can be detected. Second, applying versatile SPM operation modes enables us to to detect a broad

range of device properties which paves the way towards a comprehensive characterisation of nanoscale devices.

7.3.3 Introduction to electrostatic force microscopy techniques

The SMM setup is used in KPFM operation mode as depicted in Figure 7.12 to probe the local electrostatic force originating from the tip. The Kelvin probe force microscope, firstly introduced by Nonnenmacher *et al.* [234], is based on a non-contact variant AFM setup and detects the contact potential difference V_{CPD} between tip and the sample under test which is originating from their difference in work functions. Whilst scanning, a bias voltage equal to V_{CPD} is applied to compensate for the local electrostatic forces F_{ES}. In addition to the DC bias, an AC bias tuned at the resonance frequency of the AFM cantilever is added and applied between tip and sample, yielding

$$V = (V_{DC} - V_{CPD}) + V_{AC} sin(\omega t)\,. \tag{7.8}$$

The AC+DC voltage offset will cause the cantilever to vibrate and the lock-in amplifier is used to detect the changes of the cantilever oscillation around ω. The resulting vibration of the cantilever is detected using a diode laser and a four-quadrant detector, see Figure 7.12. The electrostatic force F_{ES} in a capacitor is found by differentiating the energy function with respect to the tip sample separation z, resulting in

$$F_{ES} = \frac{1}{2}\frac{dC}{dz}V^2\,, \tag{7.9}$$

where C is the capacitance and V is the voltage applied between tip and surface. By substituting the previous formula 7.8 for the applied voltage in Equation 7.9, the electrostatic force can be split up into three spectral component contributions [235]:

$$F = F_{DC} + F_{\omega} + F_{2\omega}\,. \tag{7.10}$$

The force acting on the cantilever can be split into a static F_{DC} contribution which contributes to the topographical signal, and dynamic contributions (F_{ω}, $F_{2\omega}$) given as

$$F_{DC} = \frac{1}{2}\frac{dC}{dz}[(V_{DC} - V_{CPD})^2 + \frac{1}{2}V_{AC}^2] \tag{7.11}$$

$$F_{\omega} = \frac{dC}{dz}[V_{DC} - V_{CPD}]V_{AC}sin(\omega t) \tag{7.12}$$

$$F_{2\omega} = \frac{1}{4}\frac{dC}{dz}V_{AC}^{2}cos(2\omega t) \tag{7.13}$$

For contact potential measurements F_{ω} is nullified by applying a DC potential at the tip that exactly compensates the V_{CPD}. A feedback loop is used to maintain $F_{\omega} = 0$ in conjunction with a lock-in amplifier that detects the cantilever oscillation at ω. V_{CPD} is acquired as an image and thus, the local work function difference of the surface is probed as an 'electronic potential map'. KPFM has been employed to image p-type dopant profiles [226] and individual P dopants [236–238] and clusters [239, 240] at the surface of a P-doped silicon-on-insulator-field-effect-transistor (SOI-FET) channel at low temperatures ($\approx 13\,\mathrm{K}$). We use the conventional KPFM operation mode at RT where the AC bias is applied between tip and sample and a DC bias is applied between S and D by only varying the potential on the top source electrode while drain is grounded. This way KPFM probes the local change in total potential Φ comprising of $V_{CPD} - V$ as stated earlier in Equation A.1 in the appendix. The $\partial C(V,z)/\partial z$ component in the $F_{2\omega}$ signal could be measured directly by a lock-in detection of the second harmonic oscillation but is not commonly used because it contains topographic artefacts [241]. The basic idea of scanning capacitance force microscopy (SCFM) is to detect an induced electrostatic force oscillating at the third harmonic frequency 3ω of the cantilever. $\partial C/\partial z$ depends on the applied bias voltage and hence $\partial C(V,z)/\partial z$ is composed of a DC and AC component as

$$\frac{\partial C(V,z)}{\partial z} \simeq \frac{\partial C(V_{DC},z)}{\partial z} + \frac{\partial C(V_{DC},z)}{\partial V \partial z}V_{AC}cos(\omega t)\,. \tag{7.14}$$

Accordingly, F_{ES} contains a force component that oscillates at 3ω of the cantilever, given as

$$F_{3\omega} \simeq \frac{1}{8}\frac{\partial^{2} C(V_{DC},z)}{\partial V \partial z}V_{AC}^{3}cos(3\omega t)\,. \tag{7.15}$$

Hence, the detected amplitude $A_{3\omega}$ of the third harmonic oscillation is related to the voltage derivative of the force gradient by $A_{3\omega} \propto \frac{\partial^{2} C(V_{DC},z)}{\partial V \partial z}V_{AC}^{3}cos(3\omega t)$. SCFM is much more sensitive to topographic artefacts than KPFM and has originally been developed for dopant profiling on semiconducting samples [226, 241]. It has been demonstrated, that the change of the capacitance originating from the depletion capacitance $C_D = \frac{dQ_D}{dV}$ for doped Si gave the largest contribution to the overall $A_{3\omega}$ amplitude [226].

7.3.4 Kelvin probe force microscope on powered buried P nanowire

First, we have a closer look on the sample topography and electrical potential of the contacts, then we move over to the wire region. A 3D AFM topography image in Figure 7.14a) displays two prominent features on the surface region between the Al contacts ($h_{Al} \sim 160$ nm from the top line scan). Areas with a depression (white dashed line in Figure 7.14b)) of

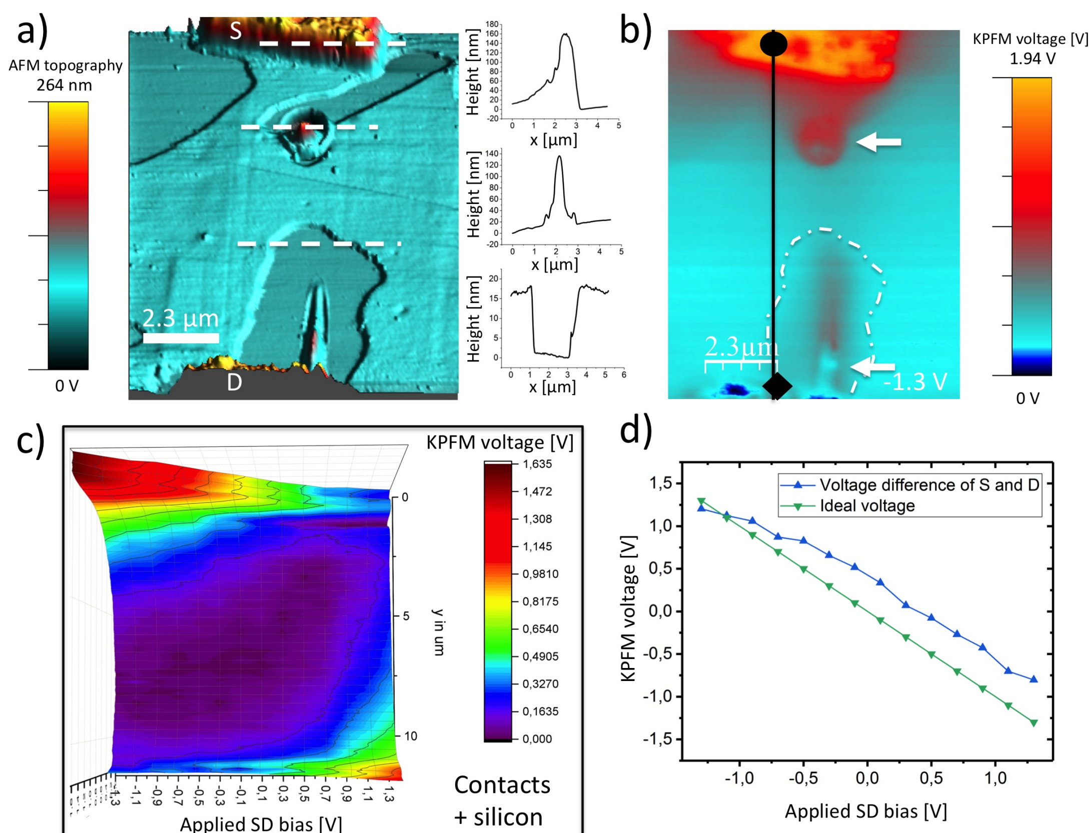


Figure 7.14: a) AFM topography image of the buried P-wire region plus S and D Al contacts and line scans of prominent surface features. b) KPFM surface potential image obtained at $-1.3V$. The vertical line indicates the location of an obtained surface potential slide as a function of applied bias plotted as 3D graph in c). The black square and circle mark the points plotted in d) as a function of applied bias.

$d_{\text{hole}} \sim 15$ nm compared to the surrounded Si are located at the bottom D and top S contact and appeared while performing the experiment. The depth of the valleys (bottom line scan) are matching the exact thickness of the epitaxial overgrown silicon layer and thus are refereed to as 'epitaxial holes'. The second feature is protrusions (white arrows in Figure 7.14b)) of $h_{\text{con}} \sim 130$ nm, that occurred during the experiments and can be assigned to unintended tip contamination (middle line scan). Their potential response to changes in S and D bias is similar to those of the Al contacts, as can bee seen in the potential increase of the

protrusions at negative bias ($-1.3\,$V) in Figure 7.14b) and later in Figure 7.16. Hence, we attribute these peaks to metallic contamination.

A set of 14 KPFM potential images were obtained for applied SD-bias from $-1.3\,$V to $1.3\,$V (depicted in FigureA.15 in the appendix,) which build the data base for a 3D potential map. A surface potential slide of this potential map obtained $\sim 2\,\mu$m apart from the buried wire along the line (indicated in Figure 7.14b)) as a function of SD bias reveal a large electronic potential increase on the top S contact and the silicon in close proximation to the contacts, especially for large negative bias (shown in Figure 7.14c)). While blue contrast indicates a relative lower electronic potential, associated with the presence of positive charges (holes), red contrast displays a high electronic potential caused by the accumulation of negative charges (electrons) [238], as can be seen for the top S electrode at high negative bias of $-1.3\,$V in Figure 7.14b). The bottom drain contact is grounded, hence most of the absolute potential variations occur at the top S contact. With increasing negative bias, the Fermi level of the Al is raised up, as illustrated in Figure A.7 and the increase in total potential between Pt tip and Al contact is probed by KPFM. The detected surface potential difference between S (black circle) and D (black dot) (as indicated in Figure 7.14b) is plotted against the actual applied voltage in Figure 7.14d) which reveals that the detected surface potential difference (blue) approximately follows the ideal ohmic voltage curve (green). The V_{CPD} of Pt/Al can be determined from the flatband voltage at V=0 and/or the average offset between both curves as $V_{CPD}(Pt/Al) = (0.36 \pm 0.03)\,$V.

In the analysis of the P-wire region we focus on two locations: i) the unperturbed wire region at the central wire channel (referred to as 'P-wire') and ii) the exposed wire region in the epitaxial hole (referred to as 'P-wire (epitaxial hole)'). For both locations, KPFM surface potential point and line spectroscopy data is presented in Figure 7.15. The potential landscape at the central P-wire region (purple) displays a significantly different appearance as a function of SD bias compared to the wire region in the epitaxial hole. The potential for the central P-wire region remains constant almost across the whole bias range with an average potential depth of $\Phi(wire) = (20 \pm 0.2)\,$meV as can be seen in Figure 7.15b)+c). Because the surface potential is constant in this bias range we approximate the contact potential between Pt tip and P-wire as $\Phi(wire) = V_{CPD}(Pt/wire)$. Only for large negative bias $U_{SD} > -1\,$V a slight increase in surface potential up to $96\,$mV is detected.

For the wire region in the uncovered epitaxial hole (red), the valley depth of $\Phi(\text{wire hole}) =$

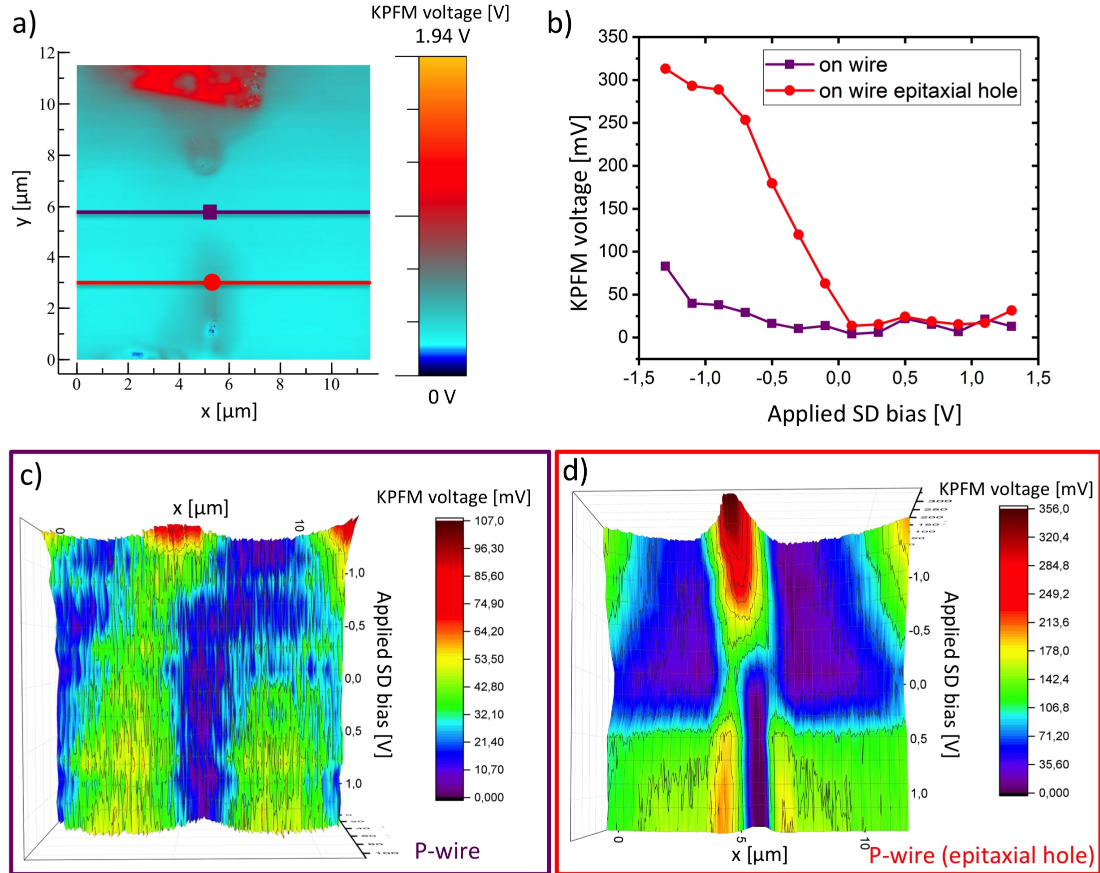


Figure 7.15: KPFM surface potential plotted as a function of applied bias for the wire region. Point b) and line spectroscopy c)+d) for the central P-wire and epitaxial hole region as indicated in a). The voltage modulation of the wire is stronger for the uncovered region.

$V_{CPD}(\text{wire hole}) = (23 \pm 0.1)\,\text{meV}$ is similar compared to the covered central wire channel but only for a positive bias range between $1.3V > U > 0.1V$ (see Figure7.15b)+d)). With decreasing bias, the electrical potential in the wire region rises up to 320 mV at $U_{SD} = -1.3V$, displaying a much higher sensitivity on SD bias changes compared to the central P-wire region. In addition, the silicon substrate inside and outside the epitaxial hole region is also strongly affected by a change in SD bias. For $U_{SD} > 0.4V$, a sharp increase in potential is observed only for the substrate outside of the epitaxial hole region, suggesting a stronger modulation of the silicon in close proximity to the bottom D contact than in the centre. The potential of the silicon inside the epitaxial hole region is rising up to 180 mV at $U = 1V$, indicating an electron charge built up at the Si/wire interface due to the relative positive potential of the wire.

This suggests that the presence of the epitaxial silicon layer on top of the P-wire significantly affects the detection of the surface potential as a function of SD bias. This observation will

be further evaluated in the following sections using SCFM and SMM.

7.3.5 Discussion and summary of KPFM results

The topography image of the region between the Al contacts reveals two prominent features, metallic contamination and epitaxial Si holes that appeared while performing the experiment, more precisely while performing dC/dV measurements in contact mode. The metallic contamination most likely occurred due to a strong interaction between tip and sample while applying a high DC bias. The epitaxial Si hole and the weakly attached epitaxial silicon layer might have been induced by the formation of stress around the Al contacts due to a large lattice mismatch of both materials. Another reason could be the imperfect epitaxial Si growth due to resistive heating during Si evaporation and multiple heating and cooling processes of the sample to low temperatures ($\approx 2K$) in previous experiments. However, the presence of the contaminations and epitaxial holes does not hinder further characterisation of the sample properties. In fact, the partial lift-off of the epitaxial Si at the wire channel region allows us to gain additional information about the contrast mechanism.

The detected surface potential difference approximately follows the ideal ohmic voltage curve for the applied source-drain bias. From this, we can conclude that the actual applied bias voltage is dropped between the S and D contacts and not somewhere else in the device. We have detected a contact potential difference between the Al contact and the Pt tip of $V_{\mathrm{CPD}}(\mathrm{Pt/Al}) = (0.36 \pm 0.03)\,\mathrm{V}$. This is an important result since literature values have a large associated uncertainty due to the specific material properties of different samples e.g. $\mathrm{W}_{\mathrm{a,(Pt/Al)}} = 1.02\,\mathrm{V}$ [53] or $W_{\mathrm{a,(Pt/Al)}} = 0.18 - 0.63\,\mathrm{V}$ [242].

For the wire region, we detected an averaged potential depth of $V_{CPD}(\mathrm{Pt/wire}) = 20 \pm 0.2\,\mathrm{meV}$ at the central covered wire channel and of $V_{CPD}(\mathrm{Pt/wirehole}) = 23 \pm 0.1\,\mathrm{meV}$ for the epitaxial hole. By considering the patterned δ-layer region as degenerately-doped silicon we calculated for $V_{CPD}(Pt/wire) \sim 1.25\,\mathrm{V}$ (see Table A.1), mainly arising from the large difference in work function of Pt and wire. The large disagreement between measured and theoretical CPD for the wire could potentially result from a high density of surface defects. It was found that a high density of surface defects can lead to partial pinning of the Fermi level and subsequently, a reduced contact potential difference [226, 243]. In extreme cases, the Fermi level is pinned and the CPD would be independent of dopant concentration.

For the covered central wire channel, the surface potential is approximately uniform in a

bias range from $1.3V > U > -1.1V$ and no effective change in contact potential in the wire is observed. The buried wire in contact with the low-doped substrate forms a potential well due to the formation of a contact potential difference (calculated as $0.335V$ at 300 K) between the δ-layer and surrounding silicon substrate. In the arising 2DEG, all donors are expected to be thermally activated and spatially extended free electrons screen the dopant potentials in the wire [238]. When applying an in-plane bias between S and D, electrons start to flow by the conventional drift and diffusion mechanism along the lowest electronic potential path in the wire channel and silicon between the S and D contacts [238]. The conduction electrons screen the P donor in the wire region such that the carrier density remains constant. The low density of states per energy of the δ-layer 2D band structure [38] limits the ground state conduction via their two valleys (Γ and Δ). The main conduction path is via the CB of silicon with a much higher effective density of states of $N_C = 2.81 \times 10^{19}\,\text{cm}^{-3}$ at 300 K (for intrinsic silicon). At higher negative bias, the surface potential increases in the central wire region, induced by an increased electron density in the CB of silicon. The onset value for the increased electron injection via the CB is detected at $U \sim -1.1\,\text{V}$ in Figure 7.15. The presence of the epitaxial silicon layer on top of the P-wire appears to shift the electron injection onset to higher SD-bias voltages. For the exposed P-wire in the epitaxial hole, this onset occurs at $U \sim -0.7\,\text{V}$. The shift of $\Delta U \sim 0.4\,\text{V}$ in negative direction could be explained, by the presence of charges in the oxide and interfacial epitaxial Si layer, since they play a significant role in KPFM detection contrast [226]. The absence of these charges might be the reason for sharper contours of the wire in the epitaxial Si hole region as well as a more uniform change of the silicon surface potential landscape (see Figure 7.15d)).
Further sophisticated modelling and experiments with the use of a back gate or in-plane gate structure potentially at low temperatures to freeze out the bulk carriers would help to make more quantitative statements. To conclude, KPFM seems to be a valuable method to visualise the surface potential at different interfaces and to identify transport properties arising from charge transfer in the active device. The technique measures the overall potential variation in the substrate while small contributions from the δ-layer may be effectively shielded by the covering Si. SCFM probes variation of the differential capacitance of the sample originating from long range electrostatic forces. As a consequence, SCFM is more sensitive to small changes of the charge density on and inside the sample.

7.3.6 Scanning capacitance force microscopy on a powered buried P nanowire

The cantilevers used were platinum silicide cantilevers (PtSi) from NanoandMore with a nominal spring constant of 4.2 N/m. The first mechanical Eigenmode at 70 kHz was used to scan the topography, while the second Eigenmode at 420 kHz was used to detect the third harmonic oscillation 3ω which provided an improved signal-to-noise ratio. With SCFM we are able to probe the voltage-induced change in charge, arising from the local carrier density of electrons and positive charge from ionised donors in the silicon depletion region (holes). In contrast to KPFM, both DC and AC bias are applied between S and D inducing carrier modulation in transport direction. In this configuration, the charge carriers are accelerated by a constant electrical field of the DC bias voltage and an AC modulation voltage of 1.7 V detects voltage-dependent change in capacitance arising from of carrier density modulation in the y-direction. This way, the measurement is sensitive to carrier density changes between the SD contacts and is not only probing the local capacitance change between tip and buried P-wire.

Figure 7.16 shows a set of 19 SCFM $\partial C/\partial V$ amplitude images (12 μm $\times$ 9 μm) of the buried P wire region plus Al contact obtained for SD bias voltages from -1.8 V to 1.8 V. In contrast to KPFM potential images, the blue contrast now indicates a lower capacitance derivative in $\partial C/\partial V$ amplitude associated with the voltage-induced change of negative charge, while red contrast displays a high capacitance derivative $\partial C/\partial V$ amplitude, associated with the change of positive charge. The robust $\partial C/\partial V$ amplitude signal gives rise to a very detailed capacitance derivative map of the P-wire plus contact region. We begin the analysis of the data set with the observation that for an applied negative bias from -1.8 V to 0 V, the strongest change in capacitance can be observed in the silicon around the top source contact. At these voltages, the n-type substrate is in depletion around the negative top source contact and hence, the depletion width and resulting depletion capacitance between SD is highly voltage-dependant. The contacts display a small change in charge density and capacitance with varying voltage as expected for a metal. The contamination dot (white arrow in the image obtained at -1.6 V) also exhibits the same voltage dependance as the contacts which support the hypothesis of Pt contamination from the tip.

The voltage-dependent change in capacitance of the P-wire can be subdivided approximately in four voltage regions. (1) From -1.8 V to -1.2 V the P-wire and epitaxial hole

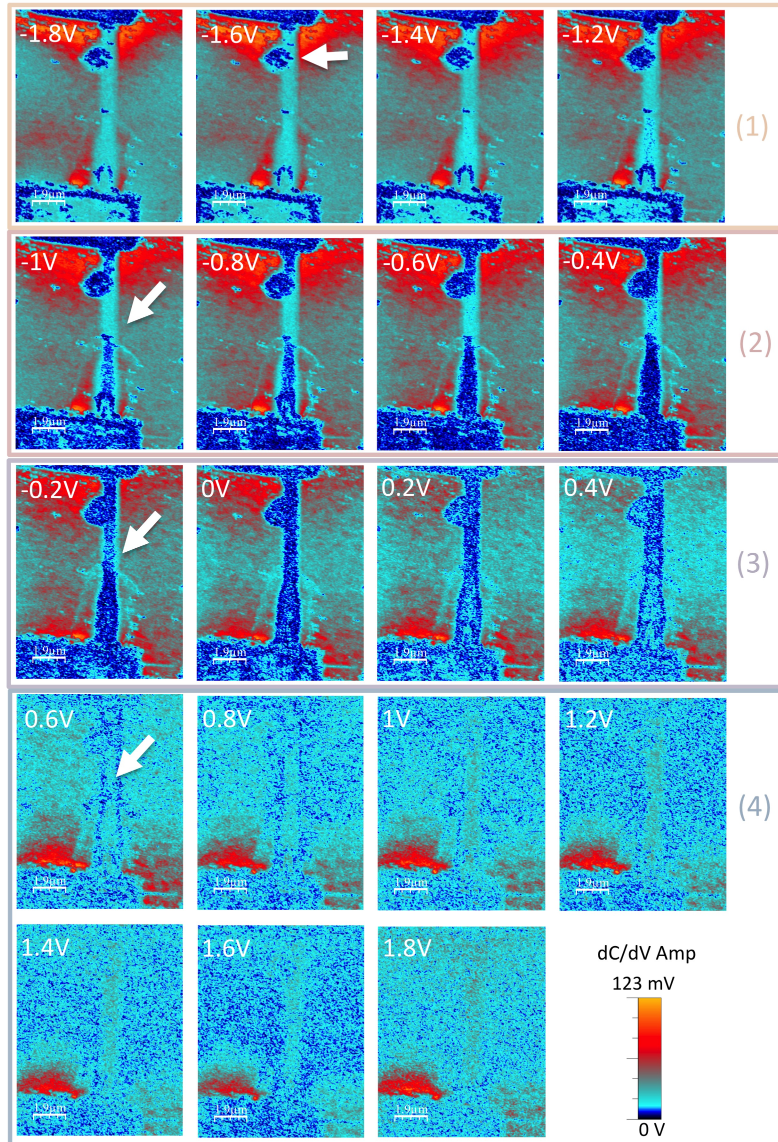


Figure 7.16: Set of 19 SCFM $\partial C/\partial V$ amplitude images ($12\,\mu$m $\times$ $9\,\mu$m) of the buried P wire region plus Al contact obtained for SD bias voltages from -1.8 V to 1.8 V. Applied AC voltage of 1.7 V at 15 kHz.

region both display a constant $\partial C/\partial V$ Amp of ~ 11 mV compared to the silicon substrate of ≈ 23 mV. (2) From -1 V to -0.4 V a change in capacitance only for the wire at the epitaxial Si hole region is observed (see white arrow in image -1 V). (3) At -0.2 V to $0.4V$ the $\partial C/\partial V$ amplitude signal of the central P-wire channel also reduces till the contrast of the P-wire across its whole length matches those of the metallic contacts (see white arrow in image -0.2 V). (4) Above 0.6 V the whole P-wire together with the contacts only display a small increased contrast in $\partial C/\partial V$ amplitude compared to the silicon background. The most dominating change in capacitance results from the silicon close to the bottom D con-

tact, associated with an increasing depletion of the adjacent silicon.

Furthermore, in the analysis we focus on the wire and substrate $\partial C/\partial V$ amplitude signal. Horizontal SCFM $\partial C/\partial V$ amplitude voltage line scans obtained on the central P-wire channel between the SD-contacts and from the epitaxial hole in Figure 7.17a) and b) respectively demonstrate the large voltage dependance of the silicon substrate in respect to changes in the wire region. For both wire regions, the capacitance derivative remains on a rather constant

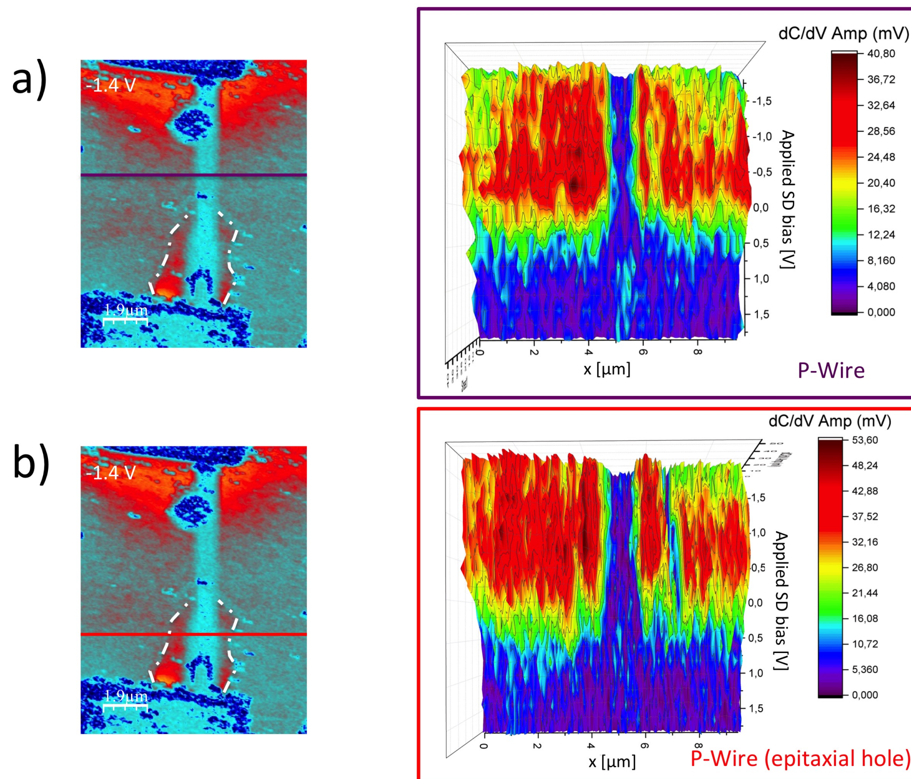


Figure 7.17: Horizontal SCFM $\partial C/\partial V$ amplitude voltage line scan obtained from covered a) and uncovered b) buried P wire channel region between the SD contacts for voltages from $-1.8\,\mathrm{V}$ to $1.8\,\mathrm{V}$. Applied AC voltage of 1.7 V at 15 kHz.

level, only at a bias voltage of $\sim 0.6V$ the capacitance in the central wire channel starts to be slightly more affected by a change in SD voltage. Figure 7.17b) reveals an overall stronger voltage dependance for silicon in close proximity to the wire in the epitaxial Si hole region, similar to the observation from KPFM. In order to increase the sensitivity for small changes of the $\partial C/\partial V$ amplitude in the wire region, point spectroscopy and vertical voltage line scans on the buried P-wire region and on the silicon substrate are separately depicted in Figure 7.18. The silicon between the SD contacts is strongly modulated by the SD bias and the strength of changing $\partial C/\partial V$ amplitude is dependent on the distance to the contacts (see

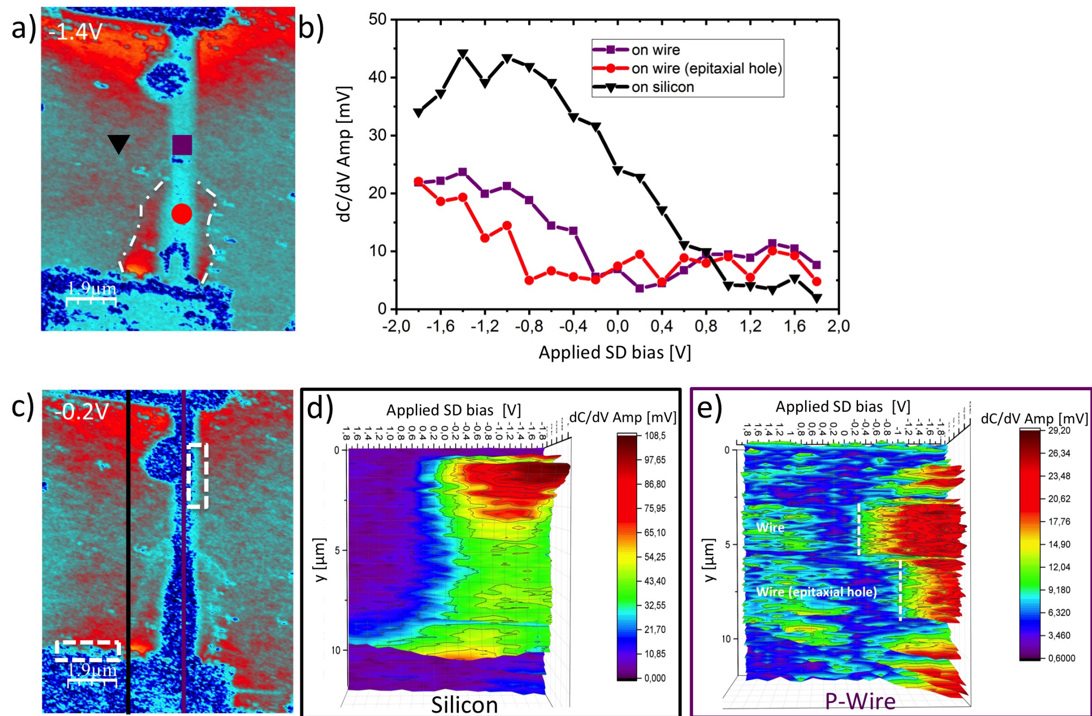


Figure 7.18: b) The SCFM $\partial C/\partial V$ amplitude of different points along the wire and on the silicon region as indicated in a) are plotted as a function of applied bias. d)+e) Vertical SCFM $\partial C/\partial V$ amplitude voltage line scan on the silicon substrate region and on the buried P wire region between the SD contacts for voltages from $-1.8\,\mathrm{V}$ to $1.8\,\mathrm{V}$ along lines as indicated in c). Dotted boxes show where the $\partial C/\partial V$ amplitude increases near the wire and contact edges. Applied AC voltage of $1.7\,\mathrm{V}$ at $15\,\mathrm{kHz}$.

Figure 7.18b)+d)). The region close to the top source contact (108 mV) displays a stronger voltage dependance than the silicon close to the grounded bottom drain contact.

From the sensitive horizontal voltage line scan in Figure 7.18e), it can be observed that the $\partial C/\partial V$ amplitude increases significantly at $-0.2\,\mathrm{V}$ for the central wire channel in contrast to $\sim -1\,\mathrm{V}$ for the wire in the epitaxial Si hole. Similar to KPFM measurements, in SCFM the presence of the epitaxial silicon layer increases the effective charge modulation on the P-wire region.

We have also observed an increase change of $\partial C/\partial V$ amplitude arising form the edges of contacts and as well at the wire, as indicated by the white dashed boxes in Figure 7.18c). This points to a well known effect in devices where the electrical field is strongest at the edges of a conductor and hence, increased carrier transport occurs at the edges. The dC/dV phase signal does not contribute additional information and therefore is not shown here.

7.3.7 IV characteristics of buried phosphorus δ-layer wire

With the precise measurement channels of the DC source meter unit, the current through the wire can be detected and Figure 7.19 shows the measured IV and conductance dI/dV characteristic of the P-wire as a function of SD bias from $-2V$ to $2V$. The buried δ-layer

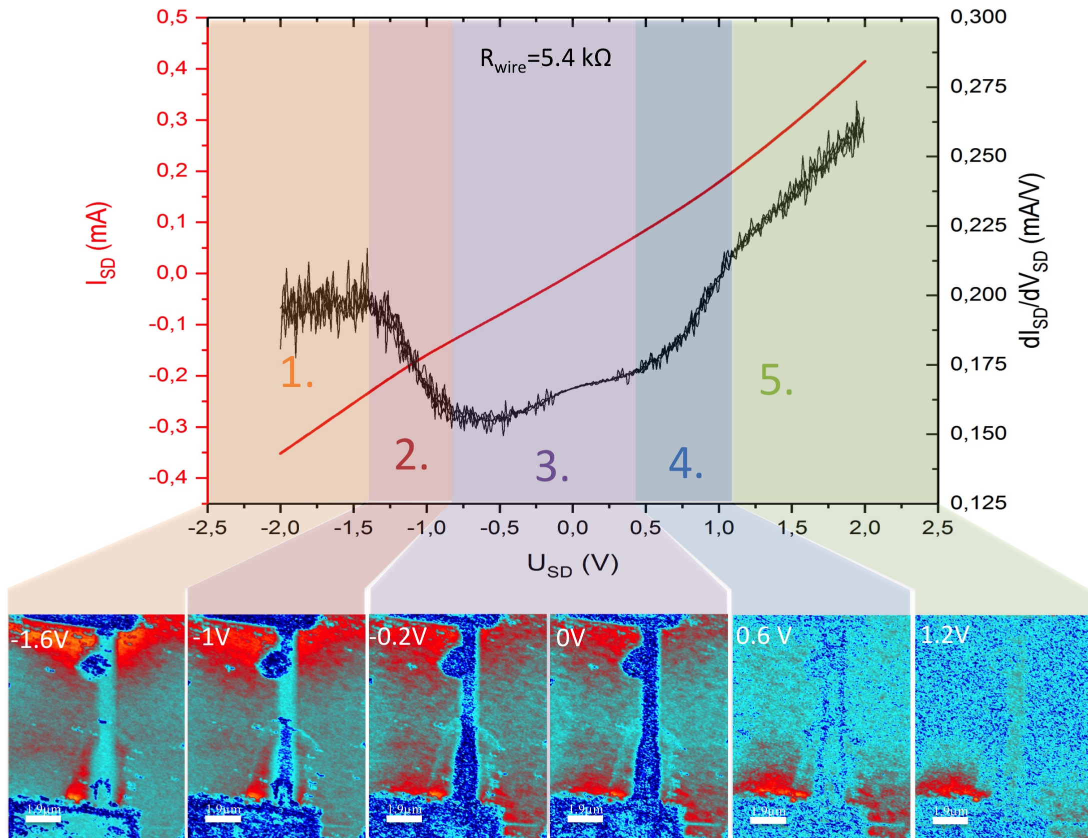


Figure 7.19: Measured IV and conductance dI/dV characteristic of the buried P wire by sweeping the bias of the SD from $-2V$ to $2V$. Comparing the dI/dV conductance curves to SCFM $\partial C/\partial V$ amplitude images, obtained at various bias voltages reveal the transport paths of the carriers between the SD contact.

wire displays an approximately ohmic IV curve for a 2-terminal measurement at RT with a resistance of $\approx 5.4\,\text{k}\Omega$, extracted from a linear fit between $-0.5\,\text{V}$ and $0.5\,\text{V}$. Comparing the dI/dV conductance curves to SCFM $\partial C/\partial V$ amplitude images obtained at various bias voltages reveals the transport paths of the carrier between the SD contacts. At high negative bias (1), the current contribution through the substrate via the CB of silicon dominates the current signal. The hole concentration is very low and hole transport through the valance band is negligible. As the applied bias increases (2), the conductance of the substrate decreases and the electron transport through the P-wire is via the impurity bands of the δ-layer. This is reflected in a constant SCFM $\partial C/\partial V$ amplitude on the wire in the

epitaxial hole region for bias voltages between $-1V > U < 0.4V$ and on the wire in the central channel region for bias voltages between $-0.2V > U < 0.4V$ (3). With increasing bias, the process repeats for the bottom D contact (4) only with an enhanced current-voltage response in forward direction originating from the Al/silicon Schottky diode characteristic (5).

7.3.8 Discussion and summary of SCFM results

The $\partial C/\partial V$ amplitude as a function of applied SD provides a very detailed capacitance derivative map of the P-wire and contact region. The change in capacitance can be attributed to a change in charge density arising from the majority carrier (electrons) and the ionised donors in the depletion region. By applying an AC bias modulation in wire direction, we are sensitive to small capacitive changes in the SD junction both in the wire and silicon substrate. The observations for the silicon substrate are consistent with those found by using KPFM, demonstrating a strong modulation of the substrate carriers with varying SD bias, especially in a negative bias range between $-1.8\,\mathrm{V} < U < 0.2\,\mathrm{V}$ at the top S contact. Around zero SD bias, a uniform low capacitance derivative is observed, remaining constant along the whole wire region. The change in carrier density is therefore comparable to those of the metallic Al contacts. A significant increase in $\partial C/\partial V$ amplitude for the central wire region at $U < -0.2\,\mathrm{V}$ compared to an onset of $-1V$ for the uncovered wire region in the epitaxial hole suggests that the presence of the epitaxial silicon layer increases the change in charge density. One possible explanation could be the presence of surface defects and/or charge traps in the region of the epitaxial Si plus SiO_2. The absence of a contrast difference between the covered and uncovered region at zero SD bias thus could be understandable because there would no bias to drive the occupation of the traps in the covered region. With increasing negative bias, traps are becoming charged leading to an increased $\partial C/\partial V$ amplitude at the covered wire region.

We have observed an increase change of $\partial C/\partial V$ amplitude arising from the edge of the Al contacts and the wire region, which can be attributed to the well known edge effect on devices [53].

Comparing the dI/dV conductance curves to SCFM $\partial C/\partial V$ amplitude images obtained at various bias voltages reveals the transport paths of the carriers between the SD contact. At high negative and positive bias, the current contribution through the substrate via the CB of silicon dominates the current signal. As the applied bias becomes less negative

the conductance of the substrate decreases and the electron transport through the P-wire is via the impurity bands of the δ-layer. Although SCFM gives good qualitative information on the local change of the capacitance, quantification is not straightforward and depends strongly on imaging parameters. To extract quantitive properties of the buried P-wire, we use SMM, particularly the more robust dC/dV signal.

7.3.9 dS_{11}/dV on buried wire sample

For dS_{11}/dV measurements, the tip is in contact to the sample such that the electric field of the GHz-signal can penetrate deep into the sample. For imaging, we set the DC bias to zero and only modulate the carriers between the SD contacts by applying an AC bias at the tip, similar as in section 7.2.1. Figure 7.20 shows an AFM topography image, an SMM dS_{11}/dV amplitude image and the AFM image overlaid with the SMM dS_{11}/dV amplitude texture (scale $9.4\,\mu\text{m} \times 6.6\,\mu\text{m}$). dS_{11}/dV imaging yields a highly resolved dC/dV ampli-

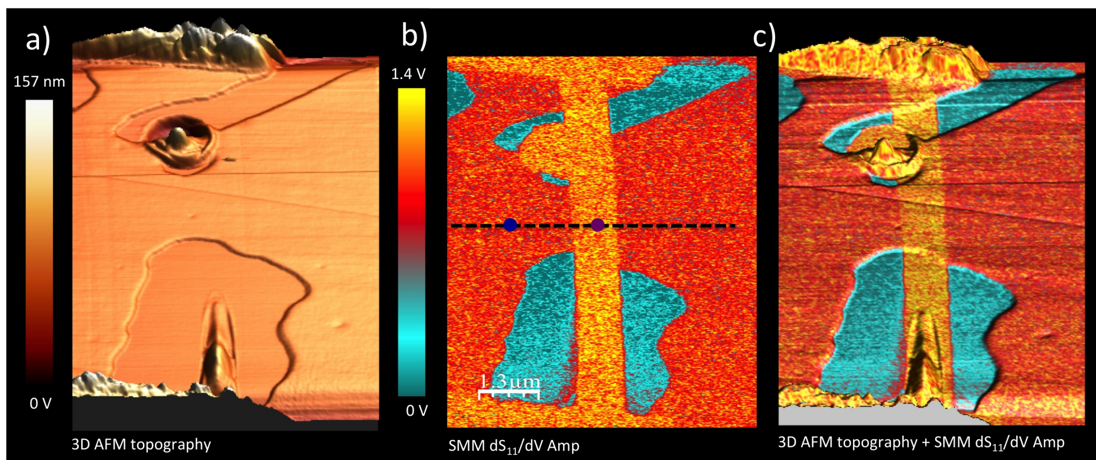


Figure 7.20: a) AFM topography image, b) SMM dS_{11}/dV amplitude image obtained at 8.31 GHz (scan line indicated for dynamic spectroscopy in Figure 7.21) and c) the AFM image overlaid with the SMM dS_{11}/dV amplitude texture. AC bias of 1.7 V. Image size is $9.4\,\mu\text{m} \times 6.6\,\mu\text{m}$.

tude image of the STM-patterned phosphorus wire between the contacts (see Figure 7.20b). The P-wire is clearly not visible in the topography image and displays a uniform dC/dV amplitude contrast at zero SD bias for the wire channel and the contacts. A pronounced difference to SCFM is observed for the silicon contrast inside and outside the epitaxial hole. The silicon in the epitaxial hole shows a reduced sensitivity to changes of AC bias modulation, pointing towards a reduced charge of the silicon inside the epitaxial hole and an increased charge density in the epitaxial silicon layer.

In order to obtain quantitive capacitance and conductance values for the buried nanowire

sample, we would like to measure the S_{11} and dS_{11}/dV for varying applied SD bias, similar to the KPFM and SCFM measurement and calibrate the obtained signal into C/G and dC/dV plus dG/dV. The main problem in dS_{11}/dV imaging is arising from the increased tip-sample interaction when scanning in contact mode at high applied DC bias. We attribute the sudden appearance of contaminations and the epitaxial Si lift-off in the hole to strong tip sample interactions occurring/induced during contact mode SMM dS_{11}/dV measurements. Therefore, we focus on the more robust dC/dV signal, that is less sensitive to tip sample modifications. In general, it is better to measure the derivative of a quantity to improve resolution. Secondly, instead of performing standard point spectroscopy, which leads to a build-up of charges in the DUT and increases the risk of contamination, we use a new approach where we obtain dynamic spectroscopy data by keeping the y-scan direction fixed and gradually sweeping the DC bias whilst scanning (indicated line scans in Figure 7.20b)). An average of several vertical lines in the obtained voltage line scan map provides information equivalent to those obtained from standard point spectroscopy. In this 'dynamic' spectroscopy mode, charging and tip modification effects of the surface are minimised.
The converted SMM dC/dV and dG/dV spectroscopy curves as a function of SD bias are shown in Figure 7.21 for an applied AC modulation bias in y-direction.

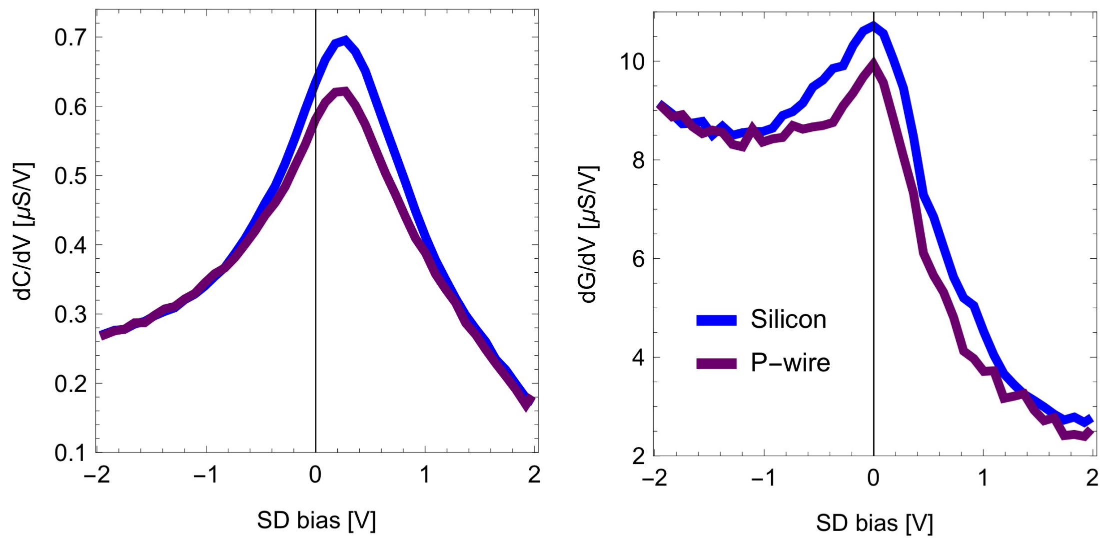


Figure 7.21: Calibrated dC/dV and dG/dV curves as a function of SD bias with AC modulation bias applied in y-direction obtained at the silicon substrate (blue) and central wire region (purple).

Compared to the substrate peak in Figure 7.7 obtained in AC z-modulation, the substrate peak of $\sim 0.7\,\mu\mathrm{S/V}$ in the dC/dV channel in the central region is sharper while shifted

$\sim 0.4\,\mathrm{V}$ in positive voltage direction (Figure 7.21b)). The dG/dV channel shows a conductance derivative peak of $\sim 10.5\,\mu\mathrm{S/V}$ at $\sim 0\,\mathrm{V}$ for the substrate. The central wire region displays a similar peak structure as the substrate in both channels but with slightly reduced peak height.

7.3.10 Discussion and summary of dS$_{11}$/dV

We obtain a highly resolved image of the STM-patterned phosphorus wire between the contacts, when setting the DC bias to zero and modulating the tip with an AC bias of $1.7\,\mathrm{V}$. Strong contrast is obtained especially compared to the silicon in the epitaxial hole which is very sensitive to changes in AC bias, pointing towards an increased variation of the charge carrier density in the epitaxial silicon layer.

We successfully obtain dynamic spectroscopy data by minimising charging and tip modification effects. In y-direction, the central wire region displays a similar peak structure as the substrate in both channels but with slightly reduced peak height. That indicates, that the change in capacitance and conductance at the wire is mainly governed by the charge carrier modulations in y-direction from the silicon substrate. The difference between the dC/dV and dG/dV curves obtained on the substrate and the wire is the change in carrier density originating from transport across the wire. This difference is largest between $-1\,\mathrm{V} > U < 1\,\mathrm{V}$ where the electron injection via the CB of silicon is reduced, mostly reflected in the capacitive dC/dV signal. Compared to the substrate peak in Figure 7.7 obtained in AC z-modulation, the peak obtained in both channels for the substrate is sharper in the y-direction which indicates that we are sensitive to changes in the in-plane depletion capacitance between the contacts and less sensitive to interactions with the surface charges at the interface and the oxide.

7.3.11 Discussion of frequency-dependent contrast

SMM and SCFM/KPFM are operating at different measurement frequencies (GHz and kHz, respectively) which should be taken into account when drawing conclusion about the origin of the observed local contrast difference on the sample between all operation modes. Dynamic effect such as a limited lifetime of minority carriers and charge traps as well as the penetration depth of the microwave can make critical contributions to the capacitance and conductance signal.

In the SMM spectroscopy curves in Figure 7.21 and especially in Figure 7.6 no inversion peak is observed at negative bias and no increased dC/dV derivative signal is detected in

imaging mode in the direct vicinity of the contacts (see also Figure 7.22). This suggests that the minority carrier (holes) can not follow the high GHz microwave frequency of the SMM. This is different for the SCFM mode as can be seen in Figure 7.22c) where a strong derivative signal indicates a high charge density around the contacts. The comparably low measurement frequency of the SCFM therefore captures the dynamics of the holes which have a 10 times lower mobility than electrons [221] and results in a strong modulation of the dS_{11}/dV signal from the substrate.

An other frequency-dependent parameter is the penetration skin-depth δ of the microwave signal, which is determined as

$$\delta = \sqrt{\frac{\rho_s}{\mu \pi f}}, \tag{7.16}$$

where ρ_s is the resistivity of the doped region of the sample, f is the frequency of measurement and μ is the mobility of the conducting plane [221]. The penetration depth of the microwave power signal is inversely dependent on the applied frequency f. Thus, it is possible to calculate the penetration depth of microwave investigation for each frequency, which allows the establishment of an in-depth cartography of buried nanostructures for metallic samples [244]. However, by calculating the skin depth for semiconductor samples, it was found, that the skin depth as function of frequency only effectively changes for a depth range between mm and μm, much deeper then the depletion layer depth of the substrate and the depth of our buried patterned δ-layer of $\sim 15\,\text{nm}$ [197]. We can conclude that the skin depth and related change in frequency does not play a significant role for our low doped substrate and patterned δ-layer.

The most plausible explanation for the contact potential and SCFM $\partial C/\partial V$ amplitude difference between the covered central P-wire and the uncovered wire in the epitaxial hole is a strong sensitivity of KPFM/SCFM to the presence of surface charges in the epitaxial layer. Interface trapped charges Q_{it} act as electron acceptors as their interface states move up and down with the applied modulation AC bias and become effectively charged when they cross the Fermi level [221]. This charging and discharging leads to a broadening of the dC/dV peak as mentioned earlier. Their associated lifetime is $\tau = C_{it}R_{it}$, where C_{it} and R_{it} are the capacitance and resistance of the interface charges and lies in the GHz range [53, 221]. Because their contribution to the total capacitance is proportional to $\propto \frac{C_{it}}{1+(\omega\tau_{it})}$, their contribution decreases with increasing frequency. This might be an explanation for the more homogenous contrast along the whole length of the wire in the SMM dS_{11}/dV amplitude

image in Figure 7.20.

7.3.12 Discussion of the epitaxial hole

The unintended lift-off of $\sim 15\,\text{nm}$ of material in the epitaxial hole region means that a large amount of the deposited phosphorus in the δ-layer of the wire should have been removed or become inactive by the formation of a new native oxide. Nevertheless, we still detect a strong signal in all three operation modes which indicates the presence of a large number of active phosphorus in the wire xy-plane of the epitaxial whole region. One possible explanation could be that the epitaxial silicon layer is actually thicker than the estimated 14.5 nm as obtained from a reference sample (see section 4.4.2). However, the slightly increased epitaxial silicon growth rate, potentially caused by a worn-out filament, would only result in a few extra nm of silicon. A systematic thickness calibration for each fabricated sample directly after overgrowth and a dopant density dependent study of the acquired signal would shine more light on the properties of the epitaxial hole and the amount of P in that region.

7.3.13 Conclusion

The versatile SMM setup allows us to locally characterise the transport properties of the buried P-wire with high spatial resolution. Non-contact operation modes such as KPFM and SCFM are sensitive to different electrostatic force components and thus allow us to extract characteristics originating from different depth location of the device. We demonstrated how KPFM can be employed to probe the surface potential at different interfaces and to identify transport properties arising from charge transfer in the active device. The pronounced contact potential difference between the covered central P-wire and the uncovered wire in the epitaxial hole suggest a strong sensitivity of KPFM to the presence of surface charges in the epitaxial layer.

SCFM was found to probe the change in charge density arising from the majority carriers (electrons) and the ionised donor in the depletion region with AC bias applied in the transport direction. The comparison between SCFM amplitude with the dI/dV conductance of wire allowed us to identify the dominating transport paths of the carriers between the SD contact as a function of SD bias. Finally, SMM dS_{11}/dV imaging in contact with the device yielded a highly resolved image of the buried wire, revealing an enhanced sensitivity of the silicon in the epitaxial hole region. The risk of sample modification while scanning with applied DC bias was minimised by using a new dynamic spectroscopy mode. Quantitative parameters such as dC/dV and dG/dV have been extracted. For comparison, images ac-

quired by using all operation modes are shown for the wire plus contact region in Figure 7.22. Although the device studied here displayed some imperfections such as contamination

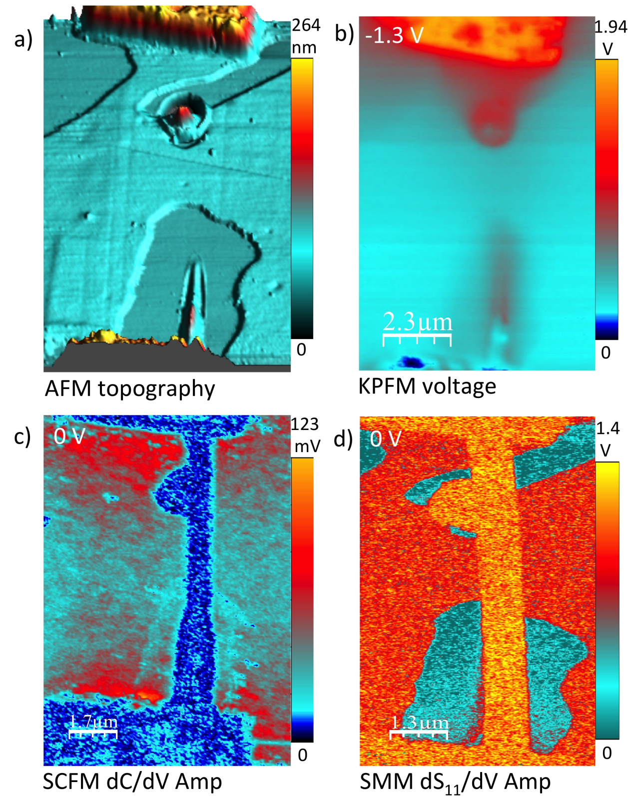


Figure 7.22: Comparison of images obtained from different operation modes of the SMM setup. a) AFM topography, b) KPFM surface potential, c) SCFM $\partial C/\partial V$ amplitude and d) SMM dS_{11}/dV amplitude image of the wire plus contact region.

and the partial absence of an epitaxial silicon layer between the SD contacts, all operation modes point towards a strong effect of charge modulation in the epitaxial layer.

We conclude that KPFM, SCFM and SMM are valuable complementary methods to investigate patterned P nanostructures and characterise active devices in working conditions. The ability to characterise nanostructured devices by using multiple detection mechanisms demonstrates the power and broad range of applicability of an SMM setup for device characterisation.

Chapter 8

Summary and Outlook

8.1 Device fabrication

A complete strategy for the fabrication and contacting of nanoscale devices using STM H-lithography has been developed at LCN and its viability in producing samples of high crystal quality and with good ohmic contacts has been demonstrated by conventional transport measurements. Dose calibrations in the low-coverage regime determined by STM and in the high-coverage regime from Hall measurements enabled us to control the effective dopant density in patterned P nanostructures. To gradually decrease the uncertainty of the calibration curve, more data points for the intermediate doping density range ($\sim 0.1 - 2.4 \times 10^{14}\,\mathrm{cm}^{-2}$) should be acquired systematically via Hall, SIMS and/or SMM measurements. The replacement of the slightly leaking valve between PH_3 capsule and VT-chamber together with the implementations of an additional dose option by *e.g* a PH_3 gas inlet that is not line-of-sight with the sample, would probably lead to more control over dopant placement in the low-coverage range. Note that after these implementation a completely new dose calibration is required.

Recently developed recipes for ion implantation markers (at NIST and Sandia Labs) could be employed to minimise STM writing times (e.g. for large contact pads) and the necessity for a high ex-situ EBL alignment accuracy which would potentially increase the sample fabrication yield. In addition, these conducting ion implanted regions can be facilitated as gates and electrodes, allowing in-situ electrical characterisation of patterned nanoscale devices in UHV. Performing electrical characterisation after each device fabrication step (*e.g.* incorporation anneal, silicon encapsulation and oxidisation) would potentially shine light on their contributions to device performance.

To conclude, this developed fabrication strategy can be employed for the fabrication of

2D P dopant nanostructures to investigate building blocks of the Si-based Kane quantum computer and for future realisations of the Stoneham-Fisher-Greenland (SFG) scheme.

8.2 Magneto-transport

Conventional transport measurements on δ-layers confirm control over dopant density in the growth and high crystal quality of the sample, comparable to samples fabricated following established fabrication strategies. Heavy δ-doped P layers have the advantage of being highly conductive at very low temperatures due to their very high carrier densities (*e.g.* compared to VLS-grown Si wires), even for strongly confined systems such as 1D wires (see introduction). The disadvantage lies in the low mobility compared to MOSFETs which results in slow switching rates of the conducting electrons in the device. In addition, Hall measurements indicate that the conductance is highly sensitive to small dopant density variations in the high-density limit. Supported by theoretical calculations from [38, 67, 71] our measurements suggest that occupation of impurity bands is already significantly limited at comparably high dopant densities between $n_C \approx 1.3 - 0.26 \times 10^{13}\,\mathrm{cm}^{-2}$. The mobility reduction with increasing dopant density in δ-layers needs further experimental evidence.

We have taken advantage of the weak localisation effect as a metrology tool to probe the vertical spread of electrons in a δ-layer while undergoing transport with high spatial resolution. The extracted δ-layer thickness of $d = 9.44 \pm 0.47\,\mathrm{nm}$ points towards deactivated donors at the surface region ($< 6\,\mathrm{nm}$) possibly induced by trapped charges in the Si/SiO_2 interface and/or in the native oxide region as well as the dielectric mismatch between doped regions and oxide/vacuum [36,37] . The role of interface trapped charges and the proximity of the surface on the conduction of δ-layer need to be further investigated *e.g* as a function of depth.

8.3 Scanning microwave microscopy

SMM was applied as novel characterisation technique for precise location of buried 3D nanosturctures and to extract important electronic properties such as conductivity and conductance. For this, a depth characterisation method has been developed and applied to a pattered P nanostructured sample. From imaging, we can demonstrate control over precise dopant placement and estimate a lateral resolution of SMM to be $\sim 50\,\mathrm{nm}$ for 15 nm deep buried pattern. The applicability of the technique to extract depth and conductivity was

demonstrated on a complex 3D sample. An advanced growth recipe has been developed for the 3D sample fabrication that suppresses P segregation while RTA steps flatten the overgrown surface enabling subsequent re-passivation and hydrogen lithography. We showed that higher imaging contrast can be obtained by using the field effect of a DC bias and detecting the S_{11}/dV signal.

To increase the number of applications even further, first measurements have been carried out on a powered buried δ-layer nanostructured device to investigate possible SMM applications for CMOS and future electronic devices. We use the full range of an advanced SMM set-up to characterise a P-wire with SMM and non-contact operation modes (KPFM and SCFM) while applying an in-plane DC bias. In addition to conducting wires, other nanoscale electrical components in operation mode could be studied with this technique such as in-plane tunnel junctions, capacitors or single electron transistors.

Appendix A

Appendix

A.1 Device fabrication strategy

A.1.1 HF and TMAH for fiducial marker etching

The optical lithography defined patterns are first transferred into the thermal silicon oxide by dipping the wafer for $> 120\,\mathrm{s}$ into buffered HF with an estimated constant silicon oxide etch rate of $\sim 60\,\mathrm{nm/min}$. Buffered HF selectively etches silicon oxide and the etch process is interrupted once all oxide has been removed in the exposed region of the resist. However, due to the isotropic SiO_2 etch of HF, the etch time is optimised to prevent undercutting of the resist, which results in significant increase in the designed pattern dimensions. The resist is removed by sonicating the wafer for 10 min in acetone followed by 5 min in isoprophanol (IPA). The thickness measurement directly after the HF dip reveals a profile depth of $(114.5 \pm 5.0)\,\mathrm{nm}$ which can be attributed to the silicon oxide thickness and is in line with the oxide thickness detected from ellipsometry. No difference in etch depth has been detected after 2 min or 3 min HF etch which indicates an etch rate faster than $120\,\mathrm{nm}$ per minute. No effective etching was observed for features with short exposure time ($2\,\mathrm{s}$), confirming exclusive etching of silicon oxide. We also tried to transfer the pattern into a wafer with only native oxide present on the surface, which did not succeed.
Subsequently, the fiducial marker patterns are transferred into silicon by using the thermally grown oxide as a mask and the anisotropic etching of silicon in TMAH, which prevents significant undercutting. The wet-chemical TMAH silicon etch rate is dependent on the solution temperature and we determined an effective silicon etch rate of $(71.1 \pm 7.3)\,\mathrm{nm/min}$ for an etch temperature of $T_{TMAH} = (51.4 \pm 0.1)\,^{\circ}\mathrm{C}$.

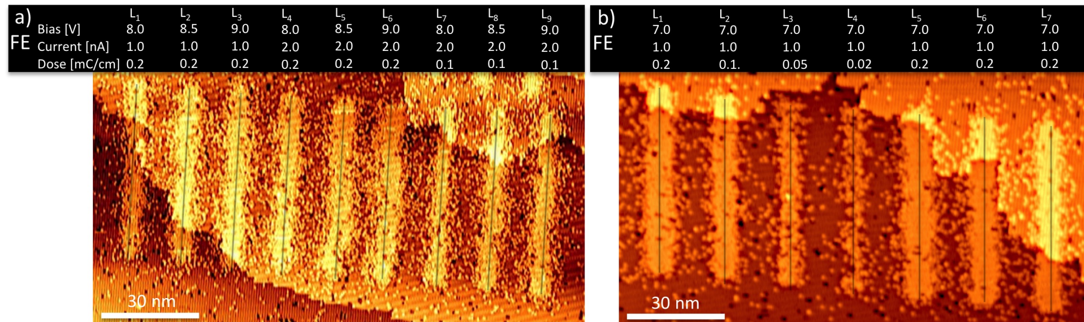


Figure A.1: Filled state topography images of the passivated Si(100)2×1:H silicon surface after depassivating a set of vertical scan lines in FE mode demonstrating a) bias, current and dose dependent and b) dose dependent width of the depassivated line region.

A.1.2 Depassivation parameter

The dose was found to mainly determine the desorption density within the line region, as can be seen from line 1 to line 4 in Figure A.1b). For complete depassivation the local electron flux underneath the tip needs to be higher than the desorption yield of $\sim 2.4 \times 10^{-6}$ H-atoms per electron. For a constant current and hence constant electron flux, the main parameter for FE depassiation is the tip speed during depassivation, more precisely the exposure time per Si-H bond at a constant electron flux.

A.1.3 High coverage calibration and incorporation anneal

The filled state STM topography image in Figure A.2a) are obtained directly after a PH_3 saturation dose of > 0.1 L where the coverage displays a disordered alloy of PH_2 + H and PH + 2 species [127]. For saturation dosages it was found that PH_3 molecules adsorb on one side of a dimer and dissociate to form PH_2 + H, leading to a full occupation of the dimer binding sites. This is evidenced by the significant number of PH_2+H features which order in local regions exhibiting a p(2×2) reconstruction with a local PH_2 coverage of 0.5 ML, see Figure A.2a). It was found that further dissociation steps are thermodynamically favoured, but will occur only if sufficient bare sites are available on neighbouring dimers [127]. A thermal anneal step incorporates P into the silicon lattice by ejecting a silicon adatom [51] The dissociation pathway for a high PH_3 coverage is schematically shown in Figure A.2f) derived by Wilson *et al.* from density functional theory (DFT) calculations (modified from [127]). They suggest that an activated dissociation process at low temperature ($185-335\,°$C) creates available dissociation sites causing partial PH_3 desorption. Regardless of the phosphorus coverage after room-temperature exposure this means that the effective P dopant density after post anneal incorporation would saturate for high coverages at 0.25 ML. Experimen-

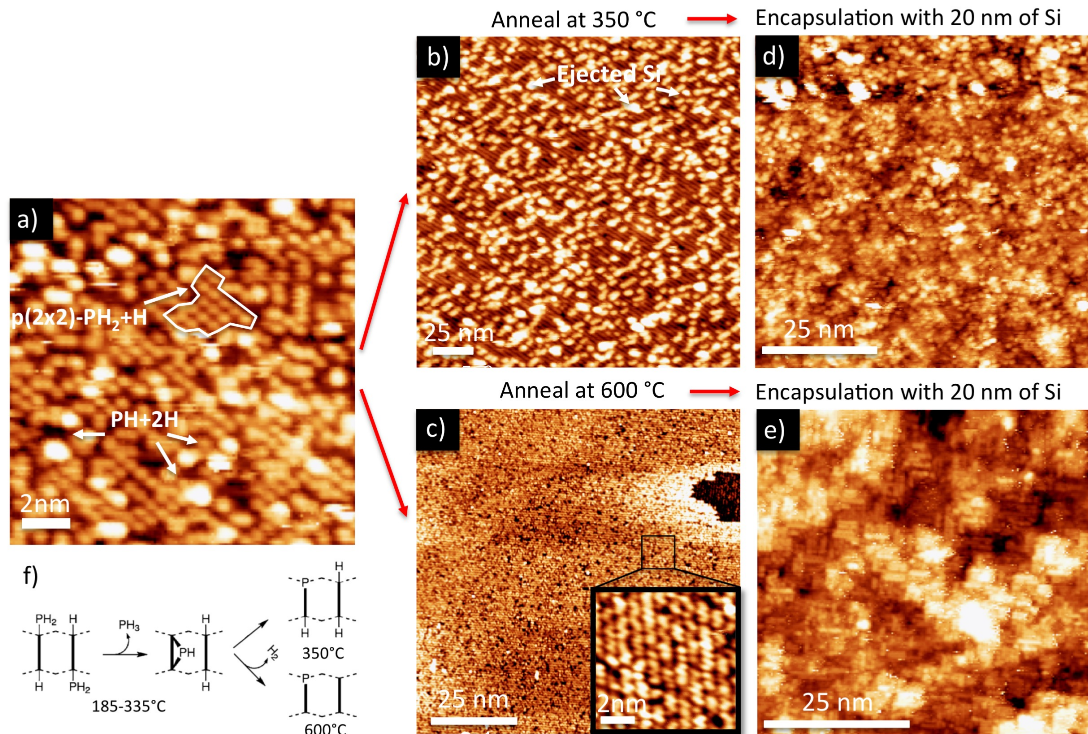


Figure A.2: Filled state STM topography images obtained after a PH_3 saturation dose of > 0.1 L. a) Surface coverage displaying a disordered alloy of PH_2 + H and PH + 2 species. b) Saturation dosed surface after a thermal anneal step at 350 °C for 2 min results in the incorporation of P into the silicon lattice by ejecting an Si adatom. A passivated Si:H reconstruction is present on the surface, in contrast to a thermal anneal step at 600 °C c) which results in H_2 desorption, leaving a silicon surface with bare silicon dimer sites. The regrowth surfaces of the δ-layers incorporated at 350 °C d) and 600 °C e) after encapsulating with 20 nm of silicon reveals a more crystalline Si growth on the high temperature annealed surface. f) Schematic of a dissociation pathway for a saturated PH_3 coverage, modified from [127].

tally, however, a saturation surface coverage of 0.37 ML of phosphorus has been measured via photoemission [245]. From Hall magneto-transport measurements it was found that a maximum carrier density of $n_{\text{sat}} = 2.4 \cdot 10^{14}\,\text{cm}^{-2}$ was achieved for annealing temperatures ranging from $250 - 400\,^\circ$C [33], corresponding to a coverage of ~ 0.37 ML. A small reduction of the carrier density ($\sim 17\%$) was obtained for annealing temperatures between $450 - 550\,^\circ$C which was attributed to an activated minor PH_2 and H recombination process above H_2 desorption temperature ($\sim 415\,^\circ$C [213]), resulting in partial PH_3 desorption from the surface. A second decrease in carrier density above 550 °C was assigned to P_2 desorption during the incorporation anneal.

In contrast to the annealed surface of 350 °C where hydrogen still occupies silicon dimer sides on the surface, as can be seen in Figure A.2b), a high temperature anneal at $\sim 600\,^\circ$C

activates the H_2 desorption processes, leaving a reactive silicon surface with bare silicon dimer sites, shown in Figure A.2c). At these high anneal temperatures, the formation of complete terraces is observed which indicates enough thermal energy for the ejected Si to migrate on the surface and attach to step edges, in line with findings from [33]. The silicon surface after a 600 °C anneal is atomically flat which is reported to provide a more ideal starting surface for the overgrowth of high quality, epitaxial silicon [33]. Even higher P coverages in the plane of a δ-doped layer can be achieved (~ 0.5 ML) when the incorporation anneal is conducted at temperatures above H_2 desorption temperature followed by a second PH_3 dose and anneal on the already dosed surface [212]. The high temperature annealing for a double dose strategy causes dopant diffusion and thus a less confined dopant profile as well as the formation of electrically inactive P-P dimers [212, 246]. Besides the presence of ejected silicon on the surface after an anneal, a signature of a successful P incorporation is the formation of a Si-P heterodimer [24, 102, 131], indicated by white circles in Figure 4.14 for a low dosed surface and in Figure A.2e) for a saturation-dosed surface after a 600 °C anneal step.

A.2 SMM detection of buried phosphorus

A.2.1 FEM for the extraction of conductivity and depth of dopant layer

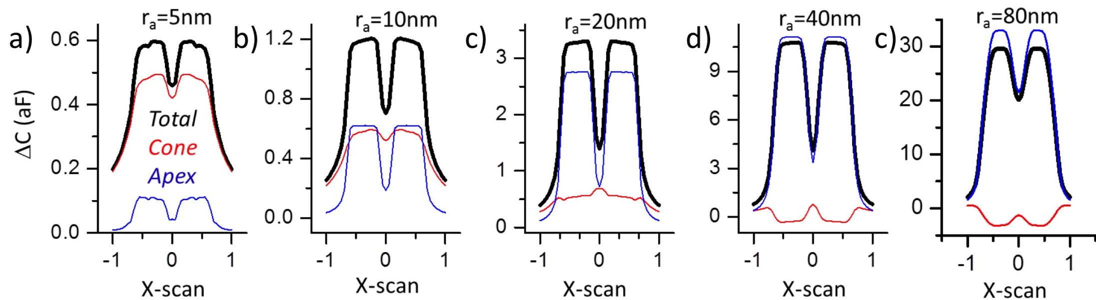


Figure A.3: Lateral SMM capacitance resolution for increasing tip radii. Total capacitance, cone and apex contribution are shown ($r_c = r_a$, $h = 15$ nm, $f = 19.83$ GHz).

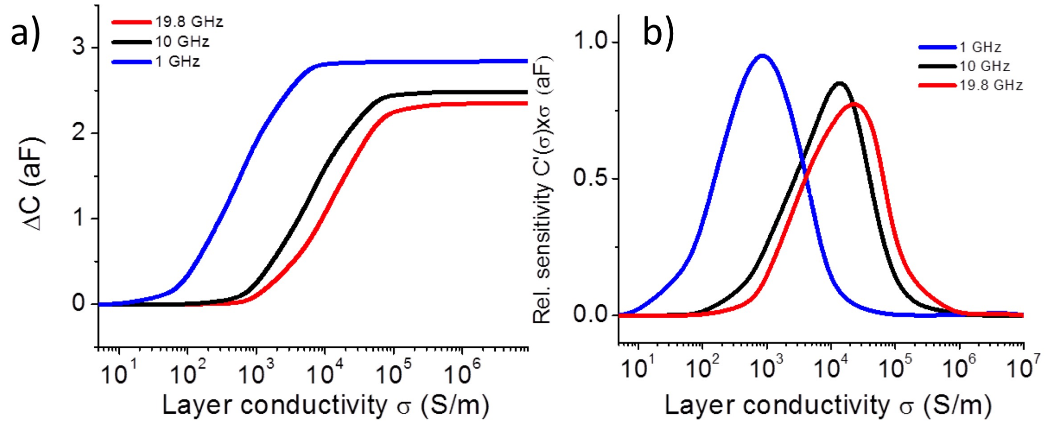


Figure A.4: Frequency sensitivity analysis. a) SMM capacitance contrast as function of layer conductivity for three measurement frequencies as indicated. b) Corresponding relative capacitance sensitivity. (Tip apex radius $r_a = 20\,\mathrm{nm}$, depth $h = 15\,\mathrm{nm}$). Selection of high measurement frequencies ($f \sim 20\,\mathrm{GHz}$) yields increased sensitivity to variations of σ for highly conductive layers ($\sigma > 10^4\,\mathrm{S/m}$).

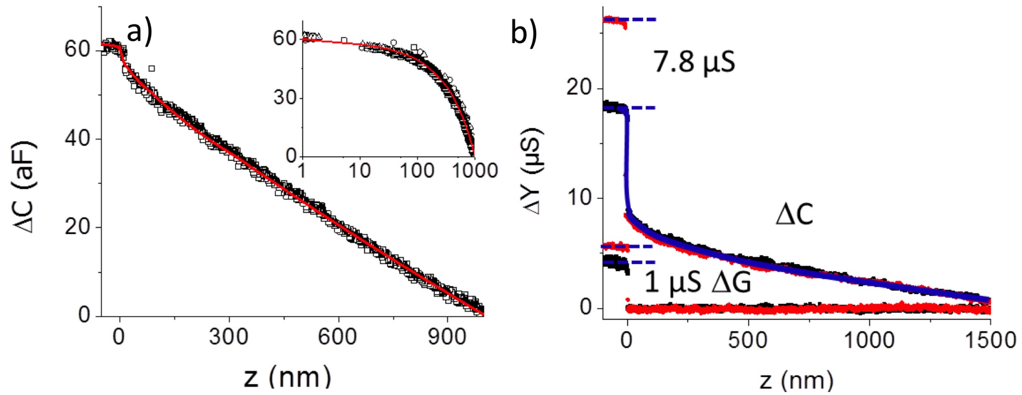


Figure A.5: SMM approach curve for electrical tip calibration. a) SMM capacitance approach curve on bare substrate for tip radius calibration of measurements in Figure 6.9 and quantification in Figure 6.10, d)-f) (inset in semi-log representation). Red solid line represents best fit for apex radius $r_a = 20\,\mathrm{nm}$ and cone angle $\theta = 8^\circ$ and contact radius $r_c = 8.7\,\mathrm{nm}$. b) SMM susceptance ($\Delta\omega C$) and conductance (ΔG) approach curve on bare substrate (black dots) and phosphorus layer (red dots) for tip calibration and for quantification of layer conductance and depth shown in Figure 6.10g). Blue solid line represents fitting for tip calibration with the extracted parameters $r_a = 290 \pm 1\,\mathrm{nm}$, $r_c = 28 \pm 2\,\mathrm{nm}, \theta = 8\,\mathrm{deg}$. Data in contact region is used for quantification of σ and h in Figure 6.10g). Interestingly, during the approach the black and red curve are almost completely overlapping and only a few nm before contact and in contact a clear signal difference can be observed. This underlines the advantage of SMM to probe the complex admittance directly in contact with the sample

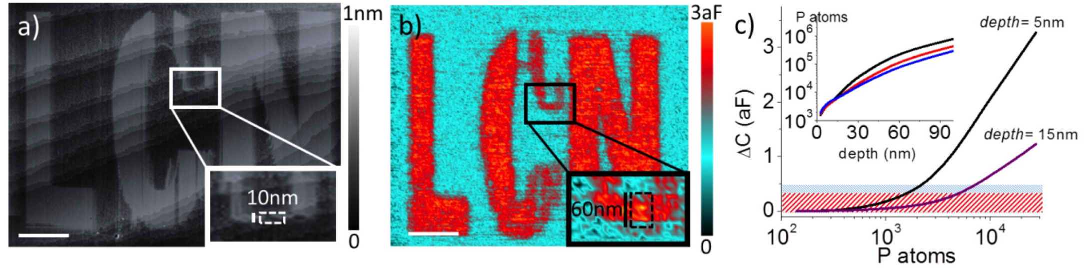


Figure A.6: Lateral resolution from STM and SMM capacitance. a) LCN logo patterned in phosphorus and imaged by STM prior to Si coverage (scale bar 400 nm). b) SMM capacitance image of subsurface LCN logo below $d \sim 15$ nm of Si (scale bar 400 nm). c) Simulated capacitance contrast as function of number of P atoms for 5 nm (black) and 15 nm (purple) dopant depth (by assuming a δ-layer width of 1.4 atoms per nm^2, $r_a = 20$ nm). Blue and red bars at 0.5 aF and 0.3 aF mark SMM sensitivity limit for bandwidth of 25 Hz and 10 Hz, respectively. Inset shows detectable P atoms as a function of depth for apex radius $r_a = 10$ nm (black), $r_a = 20$ nm (red) and $r_a = 30$ nm (blue) assuming 0.5 aF sensitivity.

A.3 Spectroscopy of buried nanostructures and characterisation of a powered buried nano wire

A.3.1 Metal-oxide-semiconductor theory

In the following section we summarise fundamental MOS theory from [53] for a basic understanding of the MOS structure, evident at our setup. In addition, characteristics of CV curves are introduced as well the effect of interfacial charge traps and oxide charges.

When a metal comes in contact to a semiconductor surface, the Fermi level of both materials align and charge will flow from the semiconductor to the metal and thermal equilibrium is established as a single system, see Frigure A.7b). The work function is the energy difference between the vacuum level and the Fermi level E_F. This quantity is denoted by $W_{a,m}$ for the metal and $W_{a,Si} = \chi + \phi_n$ for the semiconductor, where χ is the electron affinity measured from the bottom of the conduction band E_C to the vacuum level and ϕ_n is the energy difference between E_C and the E_F, see Figure A.7a). The contact potential difference V_{CPD} is defined as the difference between the Fermi energy of the metal and the semiconductor. By using the full depletion approximation, the total potential difference ϕ_{total} of the MOS, equals the contact potential difference V_{CPD} in thermal equilibrium minus the positive/negative applied voltage (see Figure A.7c)), which further reduces/increases the total potential, yielding

$$\phi_{total} = V_{CPD} - V\,. \tag{A.1}$$

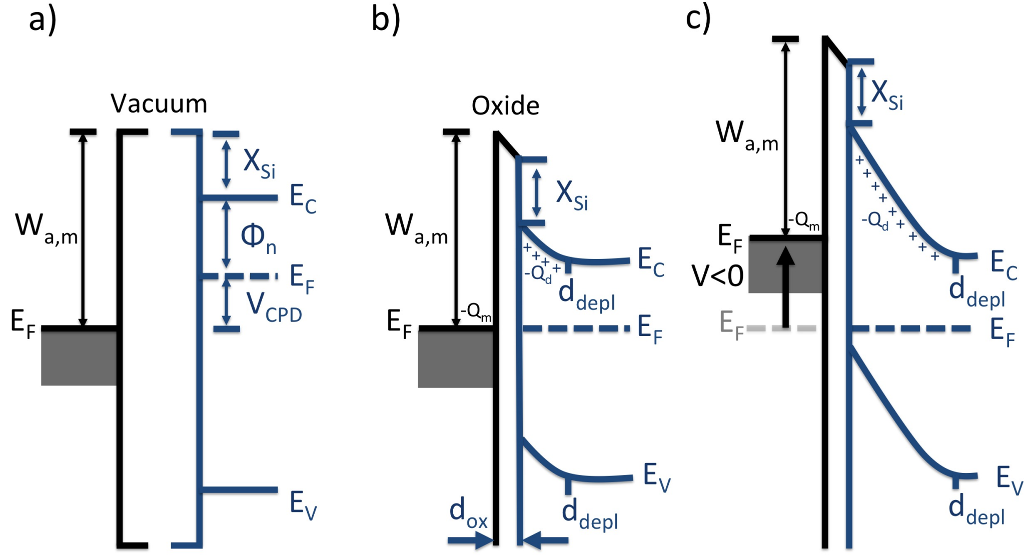


Figure A.7: Energy-band diagrams of metal-semiconductor contacts. Metal and semiconductor a) in separated systems, and b) connected into one system with an interfacial oxide layer. c) An applied negative bias at the metal raises the Fermi level and results in an increase in depletion width on the semiconductor side (Modified from [53]).

Between two metals, such as aluminium (Al) and platinum (Pt), the total contact potential difference is only determined by the work function difference of both material, $V_{CPD}(Pt-Al) = W_{Pt} - W_{Al} = 5.3\,\mathrm{V} - 4.28\,\mathrm{V} \approx 1\,\mathrm{V}$ [53]. For n-doped silicon in contact to a metal tip (e.g. Pt), the contact potential is determined as

$$V_{CPD} = \phi_M - \chi_{Si} - \frac{E_C - E_F}{q} = W_{a,Pt} - \chi_{Si} - kTLn\left[\frac{N_C}{n_0[T, E_a, N_d]}\right], \tag{A.2}$$

where e.g. $W_{a,Pt} = 5.3\,\mathrm{eV}$ is the work function of platinum, $\chi_{Si} = 4.05\,\mathrm{eV}$ is the electron affinity of silicon, N_C the temperature dependent effective density of states in the conduction band of silicon and k is the boltzman constant. $n_0[T, E_a, N_d]$ is the free electron density in CB of silicon, derived as

$$n_0[T, E_a, N_d] = -\frac{N^*}{2} + \sqrt{\frac{(N^*)^2}{4} + N^* N_d} \qquad \text{where} \qquad N^* = \frac{N_C}{2} e^{\frac{-E_a}{kT}}. \tag{A.3}$$

$E_a = E_d - E_C$ is the activation or ionisation energy for phosphorus $E_{a,P} = 45.6\,\mathrm{meV}$ and arsenic donors $E_{a,As} = 53.8\,\mathrm{meV}$ (From 1s(A_1) ground state) [247]. The depletion zone thickness d_{depl} resulting from the charge density of the ionised donor at the metal semicon-

ductor interface can be calculated according to the formula

$$d_{depl} = \sqrt{\frac{2\varepsilon_{Si}\phi_{total}}{qN_D}}, \tag{A.4}$$

where $q = 1.602 \cdot 10^{19}$ C is the elementary charge and N_D the number of donors due to doping [53,223]. The relation is valid for an abrupt approximation where the charge density $\rho = qN_D$, for $x < d_{depl}$ and $\rho = 0$ for $x > d_{depl}$. The negative electron charge at the metal side $-Q_m$ equals the positive charge of the ionised donors $Q_d = qN_D d_{depl}$ in the silicon depletion region in full depletion approximation.

A.3.2 Theoretical MOS-model for buried nanostructures

We apply standard MOS theory [53, 221] to a simple model of our sample setup to understand the physics of this MOS system under changing bias and its effect on the measured reflected microwave signal S_{11} and its derivative dS_{11}/dV. In a lumped element model for sample 1 is indicated how different elements of the MOS structure contribute to the measured sample admittance Y_S, when the tip is placed over the silicon substrate (blue circuit) or over the patterned δ-layer (red circuit). In this simplified picture, the patterned δ-layer

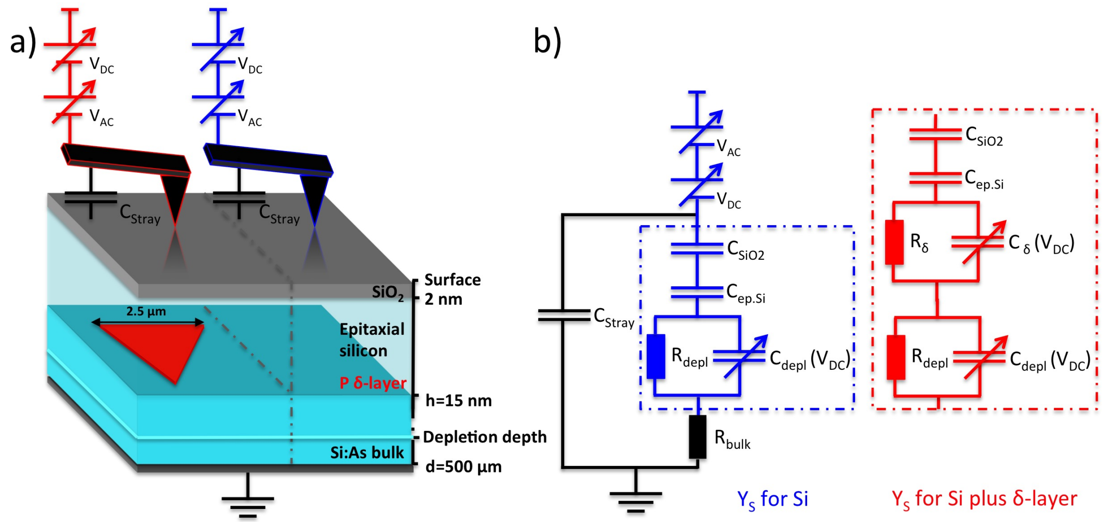


Figure A.8: Setup for quantifying dS_{11}/dV imaging. a) Schematic of sample design. b) Lumped element model for sample 1. Capacitance contribution of the silicon oxide SiO_2, the epitaxial silicon layer and bias dependent depletion layer in series. With patterned δ-layer present most of the potential drops between tip and δ-layer. The depletion layer resulting from the low doped As substrate adds in series to the overall capacitance C_{tot}.

is modelled as a high P doped silicon substrate with a P dopant density equal to the δ-layer

density, yielding a total capacitance of

$$C_{\text{tot.simple}}(\text{Pt}/\delta) = (\frac{1}{C_{Si0_2}} + \frac{1}{C_{ep.Si}} + \frac{1}{C_{depl.\delta}})^{-1}. \tag{A.5}$$

To estimate the dopant density of the δ-layer as 3D bulk doped equivalent, we estimate three different values: 1) a total 3D equivalent of $n_{SIMS} = 8.6 \cdot 10^{19}\,\text{cm}^{-3}$ from the SIMS profile in Figure 5.10 in the first 28.5 nm, which provides a lower limit for the 3D dopant density of the δ-layer. 2) From Hall measurements we extract a total carrier density of $n_{Hall} = 2.87 \cdot 10^{14}\,\text{cm}^{-2}$ for the first 28.5 nm, which equals to an estimated dopant density of $n_{Hall} = 1.1 \cdot 10^{20}\,\text{cm}^{-3}$. 3) From WL thickness measurements, where the carrier n_{Hall} are confined in a region of 9.44 nm in the δ-layer, which provides an upper dopant limit as $n_{WL} = 3 \cdot 10^{20}\,\text{cm}^{-3}$.

For the serial capacitance of each element we use the parallel plate capacitor formula,

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d} \tag{A.6}$$

where $A = \pi r^2$ and $r = 330\,\text{nm}$ is the tip radius of the tip used for the point spectroscopy measurement, ε_r the relative dielectric constant of the corresponding material ($\varepsilon_{SiO_2} = 3.9$ and $\varepsilon_{Si} = 11.9$) and d is the thickness of the corresponding layer (d_{ox}, $d_{ep.Si}$ and d_{depl}). As estimated from SIMS in section 5.3.5, the oxide thickness is estimated as $d_{Si0_2} = 2\,\text{nm}$ and the thickness of the epitaxial silicon layer is $d_{ep.Si} = 14.5\,\text{nm}$. The resulting constant oxide and epitaxial silicon capacitance is then calculated as

$$C_{Si0_2} = 5907\,\text{aF} \quad \text{and} \quad C_{ep.Si} = 2486\,\text{aF}. \tag{A.7}$$

Note that this is an ideal picture of the sample composition where the dopant density in the epitaxial oxide arising from dopant segregation is not considered.

We now can use Equation A.2 and Equation A.4 to calculate the voltage-independent V_{CPD} and the depletion depth of a Pt and Al tip in contact to the bulk substrate and a δ-layer equivalent bulk dopant density as a function of the applied bias for $T = 300\,\text{K}$ (see Figure A.9 and Figure A.10). The total capacitance of the MOS system is calculated according to Equation A.5, and plotted as a function of the applied bias in Figure A.11. The total capacitance for substrate and δ-layer in accumulation (positive bias) is dominated by the

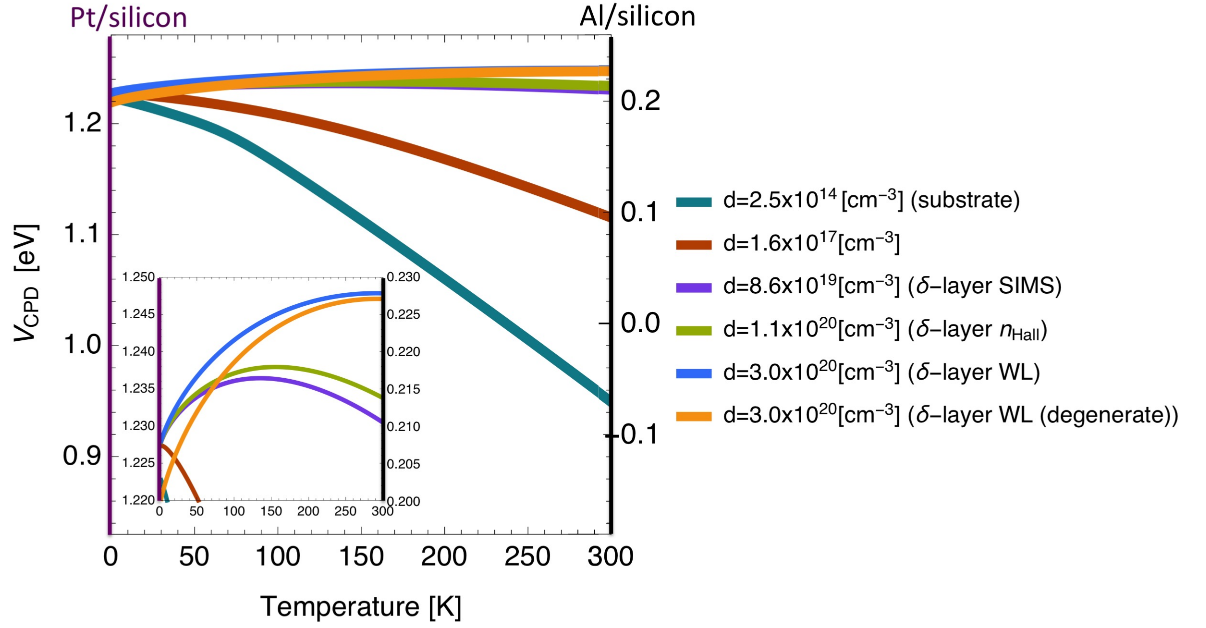


Figure A.9: Calculated built in contact potential difference V_{CPD} for Pt (left axis) and Al (right axis) in contact to doped silicon of different densities plotted as function of temperature. Inset shows a magnification of V_{CPD} between 0.2 V and 0.23 V.

smallest contributing element in the lumped element diagram model, which is the oxide in series with the epitaxial silicon layer $C_{Si0_2,ep.S} = (1/C_{Si0_2} + 1/C_{ep.Si})^{-1} = 1749.7\,\text{aF}$. In depletion (negative bias) the total capacitance for the metal in contact to the substrate is low and resides in the range of the depletion capacitance of the substrate ($C_{depl.sub} = 6.45\,\text{aF}$ for Pt at $V = -5\,\text{V}$). For the δ-layer density the change in total capacitance is less sensitive to a change in bias. The largest change is apparent for the lowest SIMS approximated density of $C_{\delta-SIMS} = 1186\,\text{aF}$ for Pt at -5V and the smallest change for the highest WL approximated density of $C_{\delta-WL} = 1412\,\text{aF}$ for Al at -5V. With increasing bias the total capacitance asymptotically increases till reaching the flat band voltage.

To conclude, in our simple model the depletion zone in the doped silicon substrate is responsible for variations in capacitance under changing DC bias voltage. Because of the serial circuit, the large serial capacitance of the δ-layer only has a small influence of the overall total MOS capacitance $C_{total} \propto 1/C_{depl.\delta}$. We therefore do not expect significant changes of the total MOS capacitance under changing DC bias for the δ-layer region but for the surrounding substrate region. We estimated a uniform thickness for all interfaces, no trapped charges and approximated the δ-layer as a highly infinite doped region of degenerately doped silicon for the simple model, which is of course, a considerable simplification

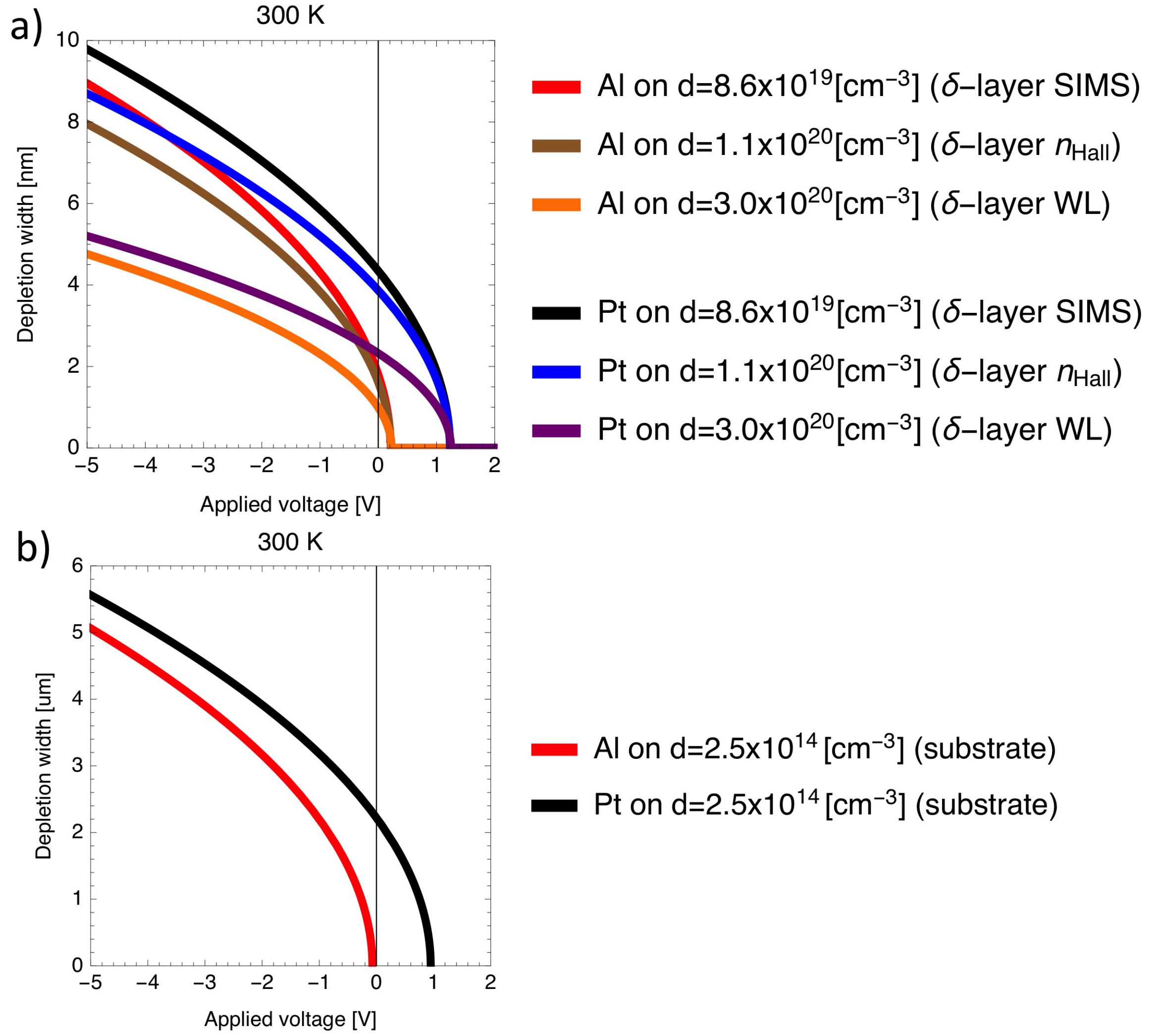


Figure A.10: Calculated depletion layer depth of a Al and Pt tip in contact to the a) bulk substrate and b) the δ-layer plot as a function of the applied bias.

of the real geometric and electrical properties of the sample.

A summary of V_{CPD}, d_{depl}, the resulting serial depletion capacitance C_{depl} and total capacitance C_{total} of the MOS structure at $V = 0$ and $T = 300K$ are summarised in Table A.1.

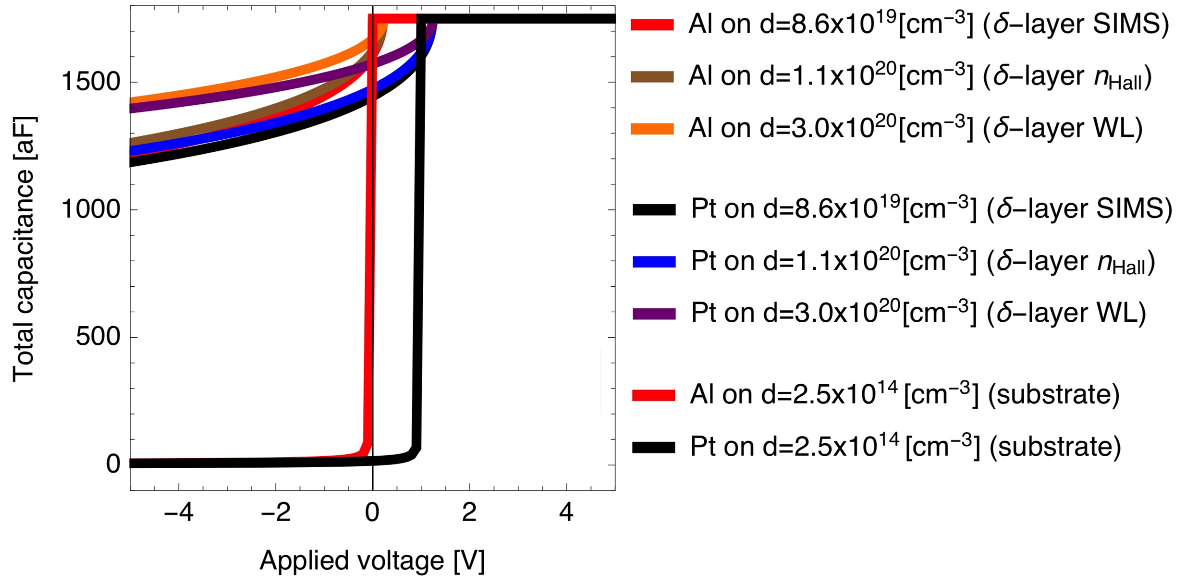


Figure A.11: Calculated total capacitance for a Pt and Al tip in contact with the low doped silicon substrate and doped silicon with a density equal to the δ-layer density. The smallest contribution comes from the oxide in series with the epitaxial silicon layer $C_{Si0_2,ep.Si} = 1749.7\,\text{aF}$.

		V_{CPD}	d_{depl}	C_{depl}	C_{tot}
a) Pt	units	V	nm	aF	aF
	substrate	0.950	2521	16.21	16.07
	δ-layer SIMS	1.230	4.3	8289	1445
	δ-layer n_{Hall}	1.234	4.3	9317	1473
	δ-layer WL	1.248	2.3	15504	1572
b) Al	units	V	nm	aF	aF
	substrate	−0.07	1025	–	1749
	δ-layer SIMS	0.210	1.8	20041	1609
	δ-layer n_{Hall}	0.214	4.3	22382	1622
	δ-layer WL	0.228	0.95	36283	1669

Table A.1: Table summarising the contact potential difference V_{CPD}, depletion layer depth d_{depl}, resulting depletion capacitance C_{depl} and total capacitance C_{total} of a MOS structure consisting of a Pt tip a) and Al b) in contacted to silicon bulk substrate and doped silicon with density of the δ-layer. All values for $V = 0\,\text{V}$ and $T = 300\,\text{K}$.

A.3.3 Interface and oxide trapped charges

Here we briefly introduce the affect of interface and oxide charges on the shape of the CV curve. A typical CV curve for n-type silicon is shown in Figure A.12a) (Modified

from [53]). At low frequencies where the recombination-generation rates can keep up with

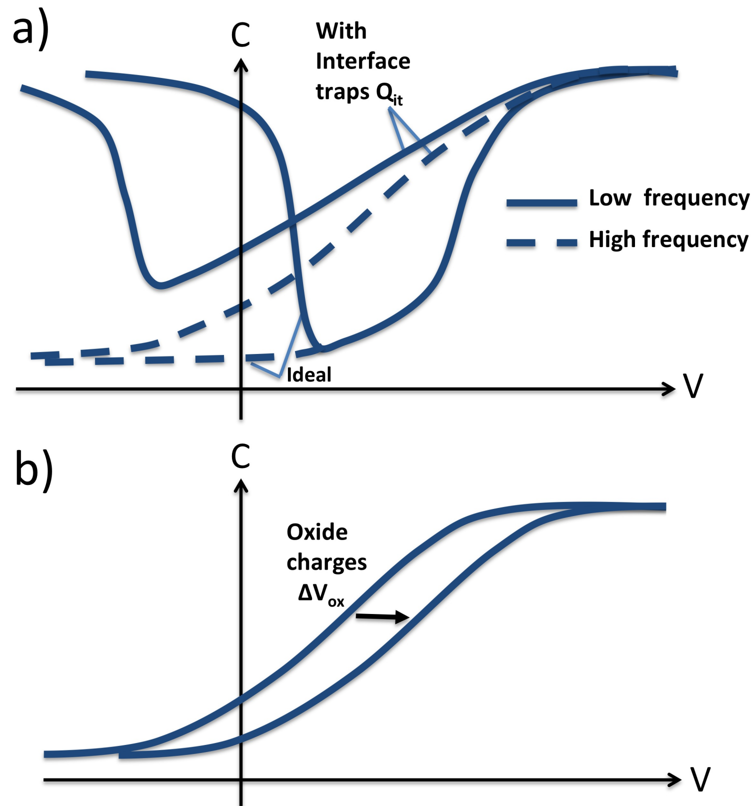


Figure A.12: a) Ideal CV curves of a MOS structure at high and low frequency and the affect of bias dependent interface charges for n-type silicon. The stretch out of C-V curves is due to a less effective modulation of surface potential by the applied voltage induced by interface trap charges. b) High-frequency CV curve shifted along the voltage axis due to positive oxide charges (Modified from [53]).

the small signal variations, an inversion layer of holes is formed directly under the silicon-SiO_2 interface which leads to an increased capacitance. At high frequencies the minority carrier concentration (in our example holes) can not follow the modulation rate of the AC bias. Experimentally it is found that for the metal-SiO_2-Si system the range in which the capacitance is most frequency-dependent is between 5 Hz and 1kHz [248]. As a consequence, MOS curves measured at higher frequencies do not show the increase of capacitance in strong inversion in Figure A.12 a) which is the case throughout all measurements in this thesis.

The quality of the oxide and Si/oxide interface is of particular importance for 2D materials located close to the surface while exhibiting a large surface-to-volume ratio [37]. Following the standardised terminology of Deal *et al.* [249], one commonly distinguishes between four types of charges: oxide-trapped charges (Q_{ot}), mobile ionic charge (Q_m) in the oxide, fixed

oxide charge (Q_f) at the Si/SiO$_2$ interface and most important interface trapped charges Q_{it}. Q_{ot}, Q_m and Q_f are fixed and independent of bias. They mainly change the electrostatics of the system which cause a parallel shift in the gate-bias direction, as indicated in Figure A.12 b), which modifies the V_{CPD} of the MOS to

$$V_{CPD}(ox) = V_{CPD} - \frac{Q_f + Q_m + Q_{ot}}{C_{ox}}\,. \tag{A.8}$$

Interface traps are located at the monolayer of SiO$_x$ that is incompletely oxidised (historically also called interface states, fast states, or surface states). They exist due to the interruption of the periodic lattice structure at the surface of a crystal [53]. The charge density, Q_{it}, of these traps can be very high $\sim 10^{15}\,\text{atoms/cm}^2$ [37,250]. Their density depends on the position of the Fermi level in Si and by exchanging charge with their surroundings they can trap or release charge carriers. For n-type silicon the Fermi level E_F resides below the silicon CB such that all traps below E_F are negatively charged. The trapped electron is withdrawn from the surrounding silicon causing silicon depletion to a certain depth. It was found that the physical origin of these traps are trivalent Si atoms, silicon atoms just bound to only three other Si atoms, simply forming a DB at the interface or a so called P_b resonance [37]. A very noticeable effect of the interface traps is that the curves are stretched out in the voltage direction [53]. This is due to the fact that extra charge has to fill the traps, so it takes more total charge or applied voltage to accomplish the same surface potential, as seen in Figure A.12 a). In the corresponding dC/dV curve the peak associated to the change in depletion is broadened compared to an ideal MOS CV curve.

A.3.4 Measured reflected microwave signal

In this section we briefly explain why it is a valid to approximate, that the measure reflected microwave signal S$_{11}$ is proportional to the detected sample admittance $-Y_S$ and the derivative of the parameter: $\frac{dS_{11}}{dV} \propto -\frac{dY_S}{dV}$. The measured reflected microwave signal S$_{11}$ is given by

$$S_{11} = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{Y_0 - Y_L}{Y_0 + Y_L} \tag{A.9}$$

with the $Z_0 = 50\Omega$, the reference load, and the measured load impedance Z_L, which is a sum of the stray capacitance from the cantilever and the sample impedance. First of all, as a result of the impedance matching network $Z_L \approx Z_0 = 50\Omega$. We only apply a voltage at the

tip, thus the reference impedance is voltage independent $dY_0/dV = 0$, which enables us to approximate [191].

$$S_{11} \approx -\frac{Y_L}{2Y_0} \propto -Y_L \quad \text{and} \quad \frac{dS_{11}}{dV} \approx -\frac{\frac{dY_L}{dV}}{2Y_0} \propto -\frac{dY_L}{dV} \tag{A.10}$$

The stray capacitance in parallel to the sample admittance Y_S has been excluded by moving the calibration plane right in front of the tip [194]. This yields a valid approximation of the measure deflected microwave signal

$$S_{11} \propto -Y_S \quad \textit{and} \quad \frac{S_{11}}{dV} \propto -\frac{dY_S}{dV} \tag{A.11}$$

A.3.5 dS$_{11}$/dV point spectroscopy for a small tip

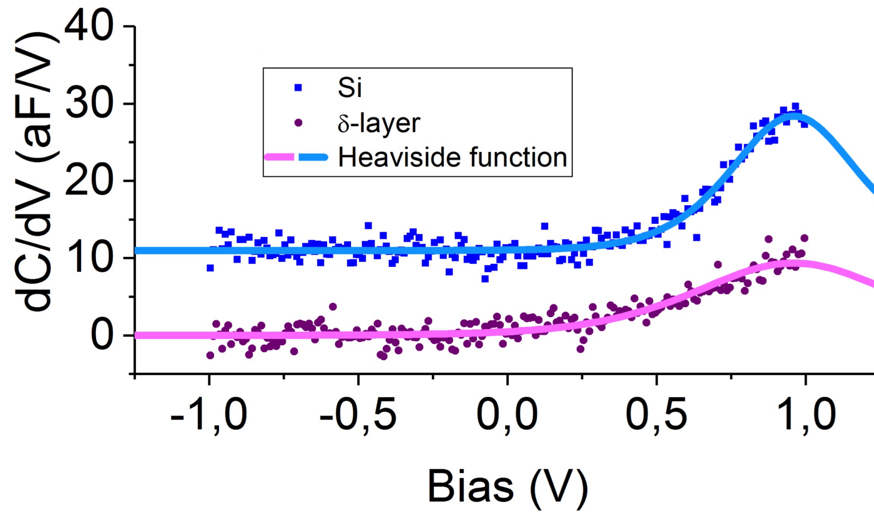


Figure A.13: dS$_{11}/dV$ point spectroscopy. Capacitance gradient dC/dV versus tip bias measurement on Si substrate (blue) and P-layer (purple) with small tip (apex radius ~ 20 nm). As guide for the eyes a pink/blue solid lines represent fitting of a Heaviside function and its derivative to the data. The spectra were obtained on locations highlighted in the dC/dV image 7.6. $f = 19.36$ GHz, $f_{LF} = 32$ kHz, $V_{AC} = 3$ V.

A.3.6 Finite element modelling of admittance gradient

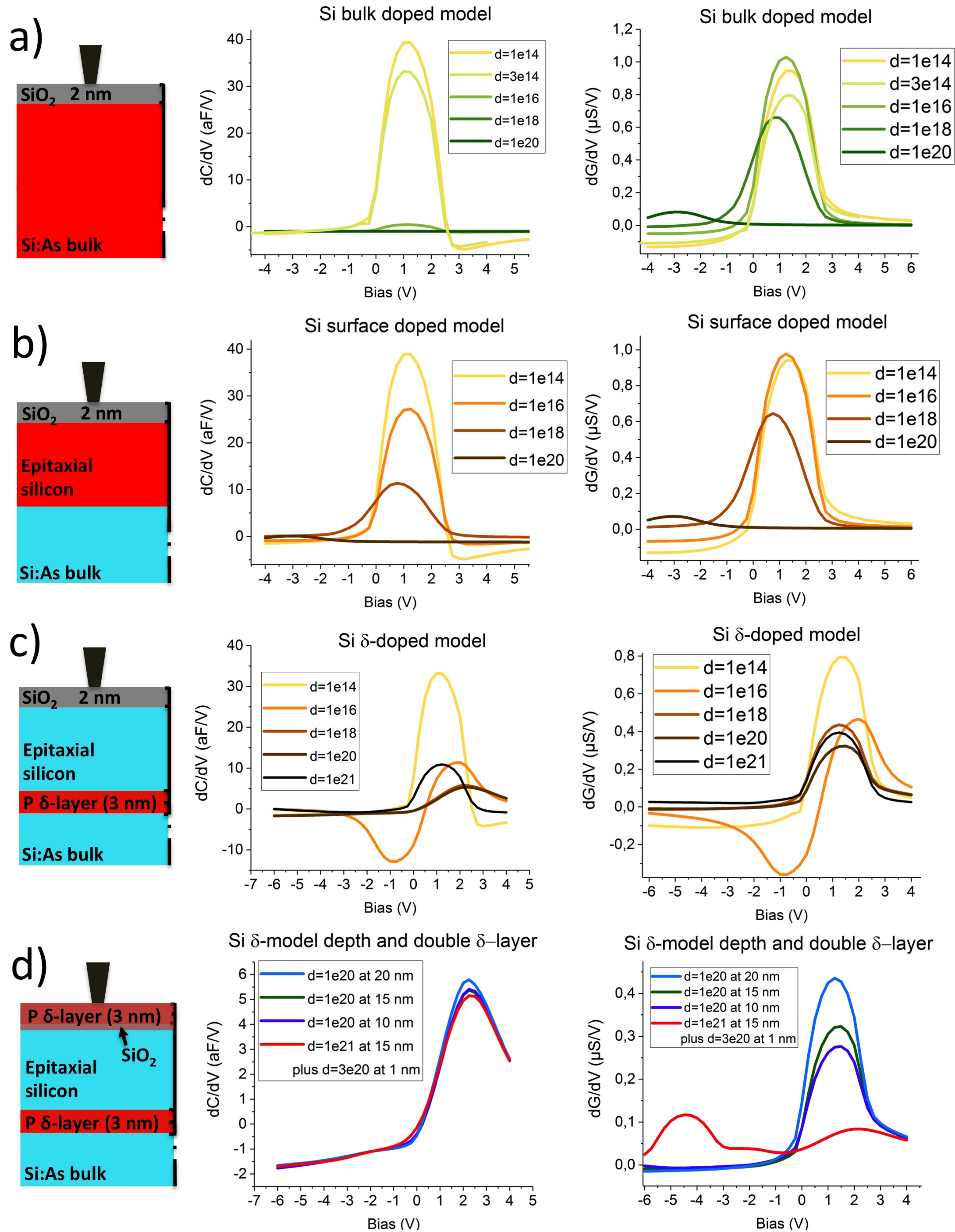


Figure A.14: Finite element modelled admittance gradient for a set of bulk dopant densities ($d = 10^{14} - 10^{20}\,\text{cm}^{-3}$) as a function of applied DC bias for a) bulk doped model, b) surface doped model, c) δ-doped model and d) embedded δ-layer dopant profile of $d = 10^{21}\,\text{cm}^{-3}$ plus a second high δ-doped region of $d = 3 \times 20\,\text{cm}^{-3}$ at 1 nm under the surface.

A.3.7 KPFM data set for 3D potential maps

Figure A.15 depicts a set of obtained KPFM electronic surface potential images of the buried P wire region plus Al contacts for a S and D bias voltage ranging from -1.3 V to 1.3 V. The

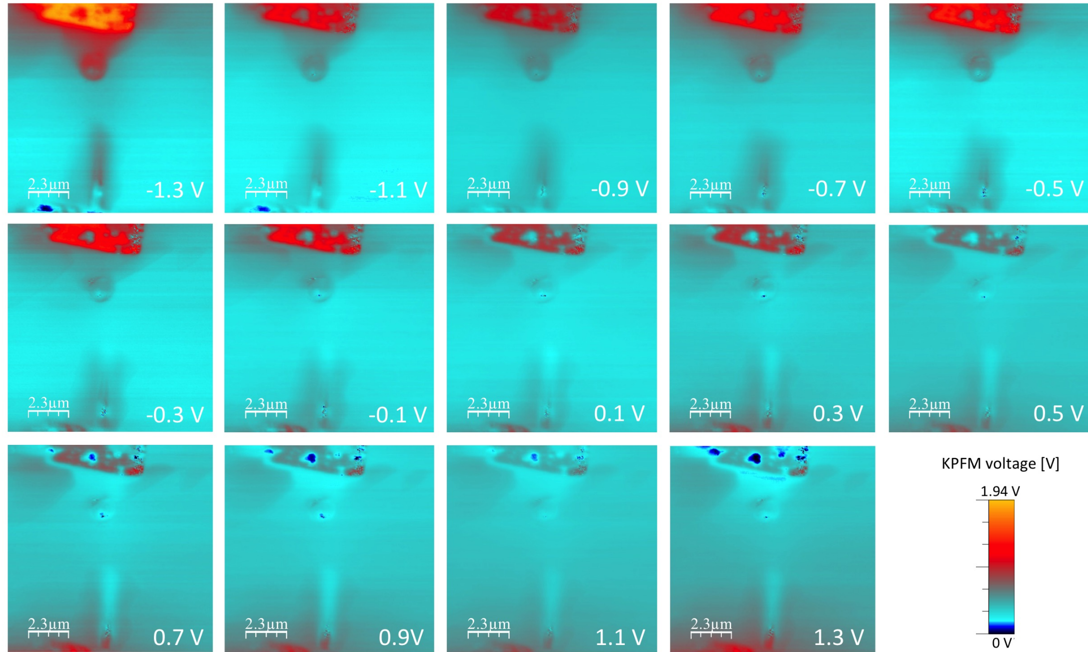


Figure A.15: KPFM electronic surface potential images of the buried P wire device plus Al contact for SD bias voltages between -1.3 V to 1.3 V. Scale $11.6\,\mu$m $\times$ $11.6\,\mu$m. The main contrast is arising from the regions of the SD Al contacts.

main contrast change in potential is arising from the regions of the SD Al contacts, in contrast to a rather uniform potential landscape of substrate and wire between the SD contact. The contrast for the KPFM images is specifically adjusted to visualise large signal contributions from the contacts. While blue contrast indicates a relative lower electronic potential, associated with the presence of positive charges (holes), red contrast displays a high electronic potential caused by the accumulation of negative charges (electrons) [238], as can be seen for the top S electrode at high negative bias of -1.3 V. The bottom drain contact is grounded, hence most of the absolute potential variations occur at the top S contact.

A.4 COMPASSS project devices

For the implementation of the SFG scheme, two major milestones need to be accomplished. The first is the controlled placement of a second group-5 donor species to selectively address control- and data-qubits which allows control over qubit exchange interactions. For this, we have investigated arsine, AsH_3, as precursor gas and its dissociation chemistry on

the clean silicon surface. It shows similar surface chemistry as phosphene and due to its full compatibility with STM H-lithography, AsH_3 can be employed to precisely deliver a second group-5 donor species onto the silicon surface. This ongoing work is a project lead by Taylor Stock at UCL and results of that study will be submitted for peer review [7].

The second major challenge is to demonstrate optical control of in-plane placed donor atoms. Group-5 donors in silicon recapture their electron at low temperatures and can be treated as hydrogen-alike Rydberg states, with smaller effective mass, where the loosely bound electron can be optically excited (Figure A.16a). When optically exicted by resonant Thz light, the extent of the wave function dramatically increases *e.g.* from $1s(A_1) \rightarrow 2p_0$ from $\sim 2.5\,nm$ to $\sim 10\,nm$, enclosing $\sim 10^4$ silicon atoms [43].

We have studied the simplest 2D donor structure, a disordered dilute δ-layer, comprising $(3 \pm 1) \times 10^{11}$ P atoms per cm^{-2} buried under 15 nm of silicon in a low-doped As substrate, as introduced in the fabrication strategy chapter in section 4.5. We characterised the sample by Fourier transform infrared spectroscopy (FTIR) to obtain a spectrum of absorption via electrical detection. At transition energies, increased conduction in the current signal originates from photo-thermal ionisation (PTI) [251], where electrons in the excited states are further excited into the silicon conduction band via energy transfer from thermal phonons.

In Figure A.16b) an electrically-detected spectrum obtained at 18 K of the dilute δ-layer is compared to a phosphorus bulk doped substrate of an equivalent dopant density of $\sim 3 \times 10^{16}\,cm^{-3}$ which serves as a reference sample. The Rydberg series (levels in meV) and identified optical transition frequencies (in cm^{-1}) from the $1s(A_1)$ ground state for an isolated phosphorus and arsenic donor in silicon appear in Figure A.16a) (slightly modified from [252], values from [253]). For the lowest excited Rydberg states of the δ-layer, $2p_0$ and $2p_\pm$ (purple), as also shown in the inset of Figure A.16b), an eminent peak shift of $\sim 3\,cm^{-1}$ to higher energies is observed while the As lines (red) of the substrate as well as P states of the P bulk doped reference sample remain unperturbed. We also observe a broadening of $2p_\pm$ excited-state peak in the dilute δ-layer and the absence of higher-lying transition lines (*e.g.* $4p_\pm$, $5p_\pm$) compared to the reference sample. By using the Kohn-Luttinger effective mass Hamiltonian [42] to calculate the excited state energies as a function of depth, we can show that the selective shift of the optical excited states is originating from the proximity to the surface. Results will be submitted for peer review [3]. The surface proximity affects the symmetry of the excited orbital, most critical for valleys extended in the z-direction. In

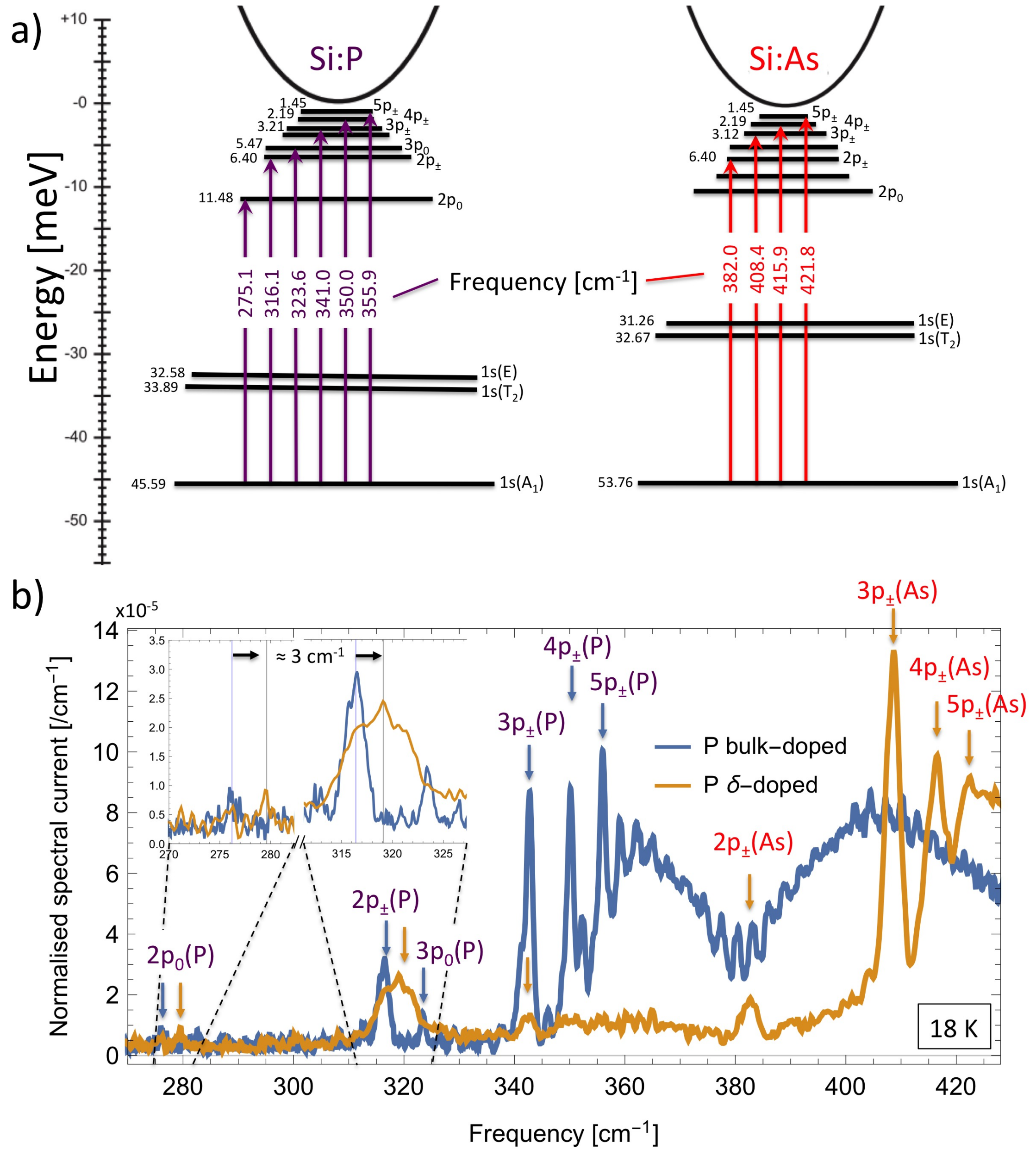


Figure A.16: a) Rydberg series (levels in meV) and identified optical transition frequencies (in cm^{-1}) from the $1s(A_1)$ ground state for an isolated phosphorus (left) and arsenic donor (right) in silicon (slightly modified from [252], values from [253]). b) Electrically-detected response of a dilute δ-layer compared to a phosphorus bulk doped substrate of an equivalent 3D dopant density of $\sim 3 \times 10^{16}\,\mathrm{cm}^{-3}$. An eminent peak shift of $\sim 3c\,\mathrm{m}^{-1}$ for $2p_0$ and $2p_\pm$ transitions (see inset of Figure A.16b)) is observed only for the δ-layer sample. Measurements performed at 18 K .

closing, it should be noted that the sensitivity of the excited state energy of these valleys on their subsurface depth can be facilitated to i) tune the selection frequency of the donor which would make the placement of a second donor species redundant and ii) provides a useful way to determine the depth of shallow buried dilute δ-layers.

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