A Non-Linear Feedback Current Driver With Automatic Phase Compensation for Bioimpedance Applications

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***Abstract*—In a conventional sinewave current driver for electrical impedance spectroscopy, as the frequency is increased the input/output phase delay of the current driver increases due to limited bandwidth. The required maximum phase delays of < 4° mean that operation is limited to about 1/12 of the driver bandwidth. A new phase compensation scheme is presented to reduce the phase delay at higher frequencies and can extend the useful operating frequency range of a current driver. The system is capable of reducing the phase error due to the current driver by an appreciable level so that it can operate much nearer the pole frequency of the driver. An integrated circuit was fabricated in a 0.35-μm CMOS process technology, which provides a phase error reduction from 22° to 3° at 3 MHz. Its core occupies a silicon area of 1.2 mm^2. It operates from a ±2.5 V power supply and can deliver output currents up to 1.8 mA$_{p\text{-}p}$ at 3 MHz.**

***Index Terms*—Current driver, electrical impedance spectroscopy, non-linear feedback, phase error.**

I. Introduction

ELECTRICAL impedance spectroscopy of biological tissue (or cells) can provide significant information regarding its physiology and pathology [1]. Biompedance measurements are generally performed by applying an alternating ac current through a pair of electrodes and measuring the subsequent induced voltage signal via another pair. The tissue impedance may be obtained via methods such as synchronous detection [2]. It is necessary to generate an accurate current amplitude independent of load variations with minimum phase delay throughout the operational bandwidth (which can be several MHz [3]) so that any measured voltage amplitude and phase is only attributed to the tissue under test [4].

Among various designs of current driver, the modified Howland circuit, has gained popularity for discrete implementations [5]. However, for integrated circuit realizations the very tight matching of resistors is impractical. The linear feedback current drivers in [6] and [7] present designs suitable for integration where the output current is defined by an input voltage and a sense resistor in a negative feedback configuration. The upper frequency of operation of these systems is limited by their phase delay.

This brief describes a method of canceling the phase delay at frequencies near the pole frequency of the conventional linear feedback current drivers. An integrated current driver with non-linear feedback is presented using the phase cancelation method. This brief is an extension of [8]. It includes measured results of a fabricated current driver chip and analysis on the limitations of the analog multiplier based on the square-law characteristics of MOS transistors in saturation. The system provides an accurate transconductance limited by the accuracy of two feedback on-chip (or off-chip) resistors. The rest of this brief is organized as follows. Section II describes the system architecture and operation. Section III identifies the limits of linearity of the analog multiplier and details the output current amplifier. The overall performance with chip measured results are presented in Section IV. Section V concludes this brief.

II. Non-Linear Feedback Current Driver With Phase Compensation

The proposed non-linear differential current driver block diagram (upper part) with phase compensation (lower part) is shown in Fig. 1 [8]. The top circuit controls the output current drive amplitude and the bottom circuit the phase delay compensation. The system has the advantage that unlike the linear circuit (e.g., [6]) in which the dominant pole must be adjusted for stability, the high frequency performance is independent of the dominant pole but has a slower transient response. The amplitude of the differential output current is set by the differential dc control voltages $\pm V_{\text{cont}}$ and the frequency of operation is dictated by the frequency of the differential sinωt and cosωt input signals of the analog multipliers M_{X2} and M_{X4} and the corresponding square waves at M_{X1} and M_{X3}. The differential voltage across the sense resistors R_S is converted to a dc voltage through the switch multipliers [8] M_{X1} and M_{X3} and four single-pole RC low-pass filters (LPFs) to extract the dc components. It results in an output voltage of $(2/\pi)V_p/2$ where V_p is the peak voltage of the ac signal across R_S. The dc voltages are compared to $\pm V_{\text{cont}}$ and amplified by A_1 in the current driver, and compared to zero in the phase compensation circuit and amplified by A_2. The signals are then modulated back to ac via analog multipliers M_{X2} and M_{X4} followed by current amplifiers AI_1 and AI_2. In the compensation part, the same circuit as the top current driver runs at the same frequency but with a 90° phase shift (cosωt) with respect to

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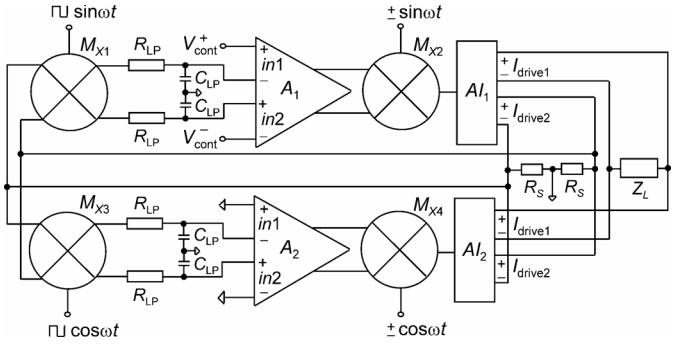

Fig. 1. Block diagram of the current driver with phase compensation. The upper part represents the current driver and the lower part with zero control voltages provides the compensation and cosωt input. A_1 and A_2 are differential difference amplifiers (DDAs).

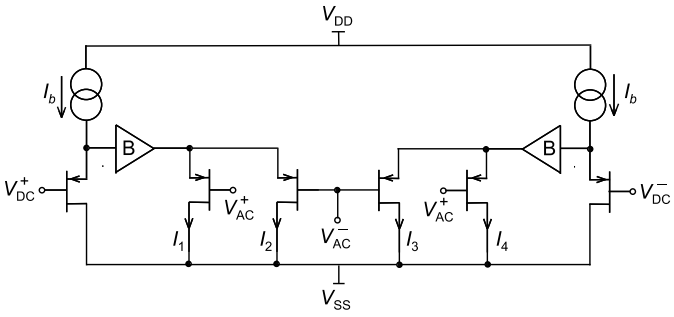

Fig. 2. Idealized four quadrant analog multiplier with ideal buffers. V_{DD} and V_{SS} are positive and negative power supplies. The common mode voltages at the inputs are zero.

the main driver (ω is the desired frequency of operation of the current driver [8]). Operating the same current driver by cosωt and with zero control voltages will automatically cancel out the phase error due to the bandwidth limitations of the multipliers and the stray capacitance across the sense resistors R_S. The detailed analysis of the phase compensation is provided in [9].

In this system configuration, there are two differential current outputs, I_{drive1} and I_{drive2}, from the current amplifiers AI_1 and AI_2; one drives the load Z_L and the other is used for feedback via the differential voltage across R_S. The output resistance is attained by using high swing cascodes. The loop gain of the current driver is analogous to the linear feedback system [8] with an additional $2/\pi$ factor as a result of ac-dc conversion at the LPFs.

If $A_V G R_S >> 1$ then

$$I_{\text{drive(peak)}} = \frac{\pi V_{\text{cont}}}{R_S} \tag{1}$$

where A_V is the voltage gain of amplifiers $A_{1,2}$ and, G is the transconductance gain of multipliers $M_{X2,4}$ and current amplifiers $AI_{1,2}$.

The LPFs have an on-chip 100 kΩ resistor R_{LP} and an off-chip 100 nF capacitor C_{LP} (providing a cutoff frequency of 16 Hz). The very low cutoff frequency is necessary to provide a dc component of the signal without ac noise. A_1 and A_2 are differential difference amplifiers (DDAs) [8]; their gain is 54 dB, phase margin is 74° and bandwidth 1.8 kHz.

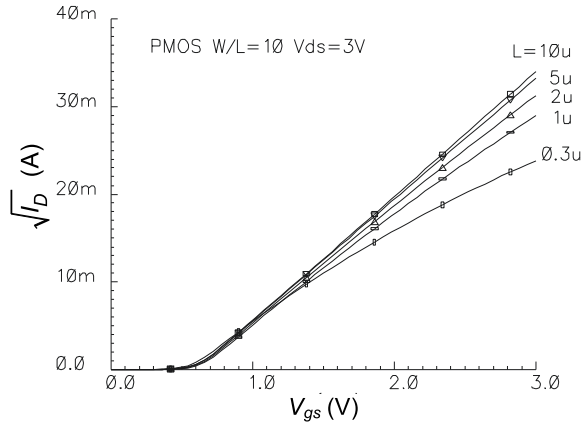

Fig. 3. Simulation of $\sqrt{I_D}$ vs. V_{gs} for different values of L.

III. Analog Multiplier Non-Idealities

The four quadrant analog multipliers M_{X2} and M_{X4} are based on the square-law characteristics of MOS transistors in saturation [8]. An idealized version is shown in Fig. 2. The harmonic distortion due to the divergence from the square characteristics in MOS transistors is a basic limitation in the linearity of the multiplier output.

The standard basic model for the square law-behavior of the MOS transistor in the saturation region is

$$I_D = K\big(V_{gs} - V_{\text{th}}\big)^2 \tag{2}$$

where I_D is the drain current, V_{gs} is the gate-to-source voltage, V_{th} is the threshold voltage, $K = \mu_o C_{\text{ox}} W/2L$; W, L are the channel width and length, μ_o is the carrier mobility, and C_{ox} is the gate oxide capacitance per unit area.

In Fig. 2 for a multiplier with differential signals $\pm V_{\text{AC}}$ and $\pm V_{\text{DC}}$, based on (2), the multiplier output current I_{out} is

$$I_{\text{out}} = (I_1 + I_3) - (I_2 + I_4) = 2K\big(V_{\text{AC}}^{+} - V_{\text{AC}}^{-}\big)\big(V_{\text{DC}}^{+} - V_{\text{DC}}^{-}\big). \tag{3}$$

A. Multipliers With Transistors Having Second Order Effects

The square characteristic of the saturated MOS transistor is modified by second order effects, primarily channel length modulation, velocity saturation and mobility reduction. The plot of $\sqrt{I_D}$ vs. V_{gs} in Fig. 3 demonstrates how the square-law deviates for decreasing values of L in a 0.35-μm CMOS technology. The slope is nearly constant for $L > 5$ μm (<0.5% variation for $\Delta V_{gs} = 1$ V).

1) Channel Length Modulation: For the channel length modulation effect λ, (2) is modified to

$$I_D = K\big(V_{gs} - V_{\text{th}}\big)^2(1 + \lambda V_{ds}) \tag{4}$$

and the multiplier output current $I_{\text{out}(\lambda)}$ due to λ is

$$I_{\text{out}(\lambda)} = 2K[1 + \lambda(V_{\text{SS}} + V_{\text{th}})]\big(V_{\text{AC}}^{+} - V_{\text{AC}}^{-}\big)\big(V_{\text{DC}}^{+} - V_{\text{DC}}^{-}\big). \tag{5}$$

Equation (5) shows that the output current is only a function of multiplication of the input voltages with an amplitude change of $[1 + \lambda(V_{\text{SS}} + V_{\text{th}})]$ compared with (3), with no harmonics.

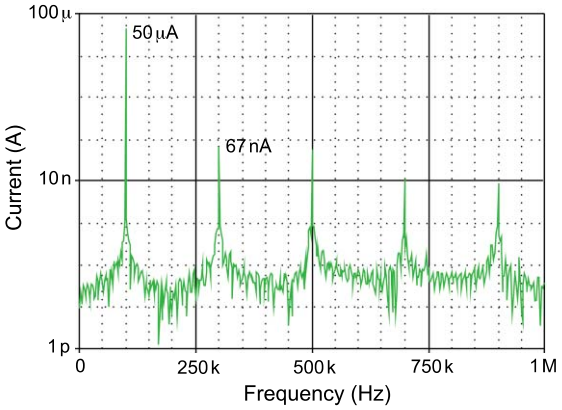

Fig. 4. FFT of the current output of the ideal multiplier in Fig. 2.

2) Velocity Saturation and Mobility Reduction: To account for velocity saturation and mobility reduction (2) is modified to [10]:

$$I_D = \frac{K\left(V_{gs} - V_{\text{th}}\right)^2}{1 + \gamma\left(V_{gs} - V_{\text{th}}\right)} \tag{6}$$

where $\gamma = [(\mu_o/2V_{\text{sat}}L) + \theta]$; V_{sat} is the saturation velocity and θ is the mobility factor. For $V_{\text{AC}} = A\sin\omega t$ the output current $I_{\text{out}(\gamma)}$ due to γ (using the first two terms of a Taylor series) is

$$\begin{aligned} I_{\text{out}(\gamma)} = {} & 2K(AV_{\text{DC}}\sin\omega t)\left[1 + 3\left(\sqrt{\frac{I_b}{K}}\right)\gamma - 6\left(\frac{I_b}{K}\right)\gamma^2\right] \\ & + K\left[A^3V_{\text{DC}}\left(\frac{1}{4}\sin 3\omega t - \frac{3}{4}\sin\omega t\right)\right. \\ & \left. - AV_{\text{DC}}^3\sin\omega t\right]\gamma^2 \end{aligned} \tag{7}$$

Equation (7) shows that the output current has a modified fundamental compared with the ideal output due to I_b (dc bias current), K and γ. The ratio of the third harmonic to the fundamental (there are higher odd order harmonics not shown here) is a function of γ^2 and A^2 but there is no second harmonic. Fig. 4 shows the simulated FFT using the ideal multiplier in Fig. 2 with a 0.35-µm technology. The fundamental to third harmonic ratio is approximately 690 when providing an output of about 50 μA_p and has a total harmonic distortion of 0.2%. This shows the limit of performance due to the non-ideal square law characteristics. In the present application the multiplier is part of the high loop gain of the feedback system and the accuracy of the fundamental amplitude is not an issue.

B. CMOS Analog Multiplier and Current Amplifier

Fig. 5(a) shows the CMOS multiplier. The ideal buffers of Fig. 2 are replaced by flipped voltage followers [11] rather than source followers or complementary transistors as they provide lower harmonic distortion [12]. Fig. 5(b) shows the differential output current amplifier which drives the floating load Z_L. Common mode feedback is added at the output to stabilize the output common mode voltage. The following current amplifier appropriately combines currents $I_1 - I_4$ and provides a current gain of 10 using high-swing current mirrors [10].

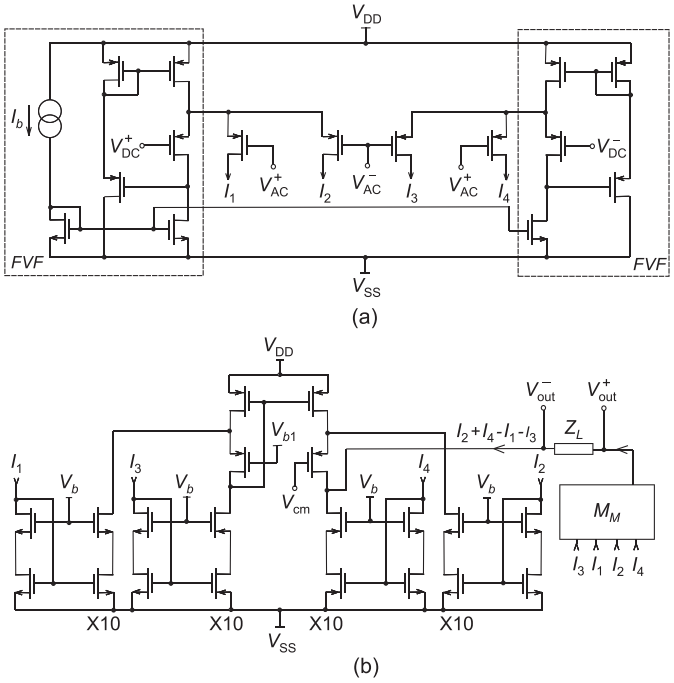

Fig. 5. (a) CMOS version of the analog multiplier in Fig. 2 with flipped voltage followers ($M_{X2,4}$ Fig. 1); (b) Differential current amplifier ($AI_{1,2}$ Fig. 1). M_M is a copy of the left hand current mirrors.

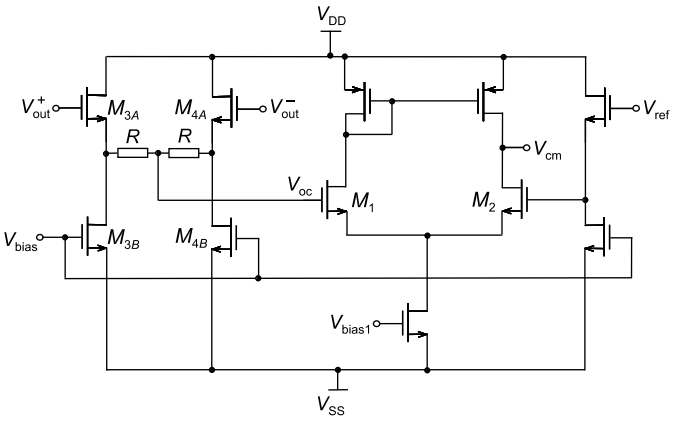

Fig. 6. Common mode feedback circuit.

Feedback is added via common mode connections V_{cm} and V_{out} to suppress any common mode errors. A duplicate circuit provides the drive for the (earthed) sense resistors but without the common mode feedback.

C. Common Mode Feedback

The schematic of the common mode feedback at the output of the current driver is shown in Fig. 6. The two outputs V_{out}^+ and V_{out}^- from the current amplifier are the inputs to the two source followers formed by $M_{3A,B}$ and $M_{4A,B}$. The common mode voltage, V_{oc}, taken from the midpoint of two equal resistors R [13]. V_{oc} is fed to one input of the differential amplifier (M_1, M_2) and the other input is set to the desired reference voltage, V_{ref}. The generated common mode control signal V_{cm} connects to the current amplifier and closes the common mode feedback loop.

TABLE I
COMPARISON OF INTEGRATED CURRENT DRIVERS

Parameter	[6]	[7]	[15]	[16]	[17]	This Work
CMOS Process	0.35 µm	0.35 µm	0.35 µm	0.18 µm	0.35 µm	0.35 µm
Supply Voltage	± 9 V	± 2.5 V	± 2.5 V	1.5 V	± 2.5 V	± 2.5 V
Max Output Current	5 mA_{p-p}	1 mA_{p-p}	500 μA_{p-p}	350 μA_{p-p}	1 mA_{p-p}	1.8 mA_{p-p}
Bandwidth	> 500 kHz	≤1 MHz	10 kHz to 1 MHz	90 kHz	1 MHz	100 kHz to >3 MHz
In-to-Out Phase Delay	12° at 1 MHz	9.5° at 1 MHz	3.6° at 1 MHz	N/A	16° at 1 MHz	1° at 1 MHz, 3° at 3 MHz
Output Impedance	372 kΩ at 500 kHz	360 kΩ at 1 MHz	160 kΩ at 1 MHz	>100 kΩ at 90 kHz	>1 MΩ at 1 MHz	>1 MΩ at 3 MHz
THD	0.69% at 5 mA_{p-p}	<0.1% at 1 mA_{p-p}	0.79% at 500 μA_{p-p}	<1% at 250 μA_{p-p}	N/A	0.4% at 1 mA_{p-p}
Power Consumption	N/A	N/A	5 mW	2 mW	N/A	15 mW

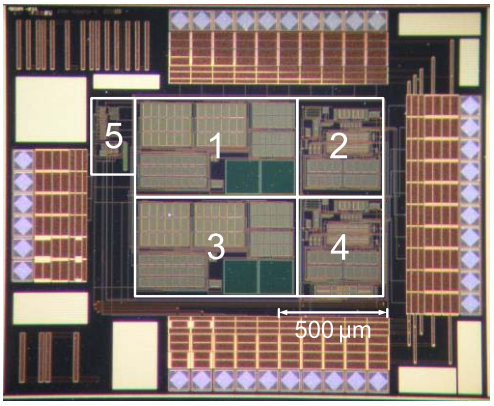

Fig. 7. Chip micrograph of the current driver with compensation. Areas 1 & 3: DDAs; 2 & 4: analog multipliers; 5: switch multipliers and sense resistors.

IV. MEASURED RESULTS AND DISCUSSION

The chip was fabricated in AMS 0.35-μm CMOS process technology with ±2.5 V supplies. The core occupies 1.2 mm^2. The circuit design, simulations and layout were developed with Cadence using the tool kit provided by the foundry. Each of the two on-chip sense resistors R_S, were 1000 Ω. Fourteen chips were tested. A TTi signal generator (TGA1244) provided ±0.5 V differential sine and cosine signals. Square waves for the switched multipliers were generated from the sinewaves via two comparators (AD8561). The chip micrograph is shown in Fig. 7.

A. Transconductance and Phase Compensation

The transconductance of the current driver was measured across a load of 400 Ω at a frequency of 500 kHz. The maximum $V_{cont} = \pm 0.286$ V resulted in a current of 1.8 mA_{p-p}. The measured average transconductance of fourteen chips was 3.15 mA/V over the full range of dc control values, compared to 3.14 mA/V in (1).

The output current amplitude and phase of the current driver were measured at frequencies from 100 kHz to 3 MHz using a 400 Ω load, for fourteen chips as shown in Fig. 8. Fig. 8(a) shows three different current amplitudes of 0.6, 0.8 and 1 mA_{p-p} with and without compensation represented in blue and red respectively. The current amplitude increases with frequency when the compensation is not active as a result of error caused by the phase delay ϕ at the two differential inputs of switch multiplier M_1 (see Fig. 1). This causes inaccuracy in $\pm I_{drive1}$ and a reduction in ac-dc transfer by a factor of cosϕ [9]. Fig. 8(b) shows the significant reduction of the phase error of the current driver due to phase compensation. The current amplitude without compensation varies by 1.8% for 1 mA_{p-p}, while the phase error starts to increase from 500 kHz and reaches 22° at 3 MHz. With compensation, the maximum output of 1 mA_{p-p} has an accuracy of 0.24%, 0.43% and 1.3% at 1 MHz, 2 MHz and 2.5 MHz respectively. With compensation, the phase error reduces to 1° at 1 MHz and 3° at 3 MHz regardless of the current amplitude.

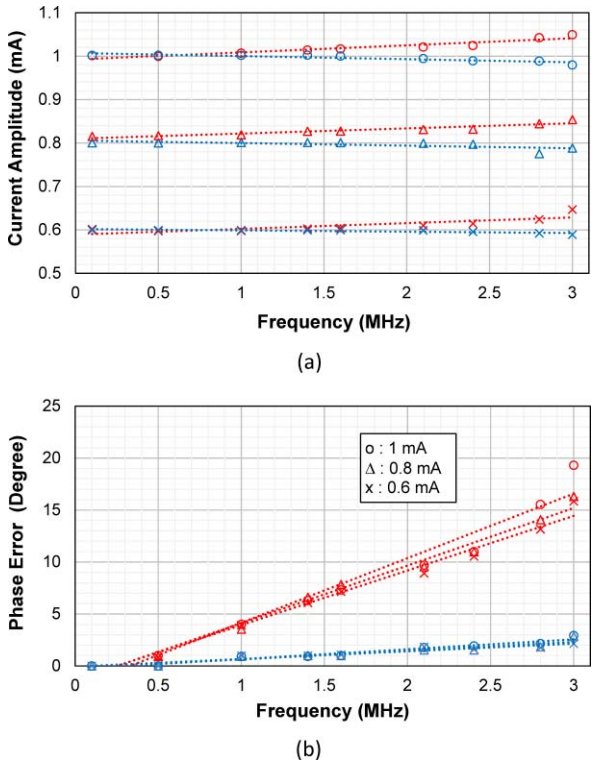

Fig. 8. Comparison of average measured output current and phase error of fourteen chips versus frequency. (a) Current amplitudes of 0.6, 0.8 and 1 mA_{p-p} without compensation (red) and with compensation (blue) in the frequency range of 100 kHz to 3 MHz. The standard deviation (σ) for uncompensated current amplitude is 0.01 and compensated current amplitude is 0.008. (b) Corresponding phase errors for current amplitudes of 0.6, 0.8 and 1 mA_{p-p} without compensation (red) and with compensation (blue) in the frequency range of 100 kHz to 3 MHz. The dotted lines are linear fits.

These fabricated chips have accurate sense resistors; this cannot be generally expected. By adding two internal chip resistors (not implemented here) well matched to R_S, and instead applying ± dc control currents to generate the control voltages V_{cont} in Fig. 1 the resultant $I_{drive1,2}$ amplitudes

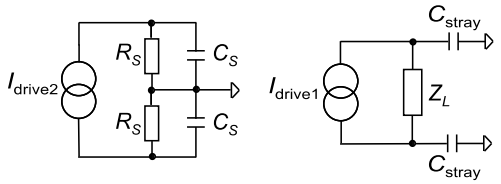

Fig. 9. Effect of stray capacitances in the current driver.

will be an accurate copy of the control currents within the matching accuracy of the resistors.

Although the bandwidth of the current driver is about 7 MHz, the current amplitude and phase measurements were limited to 3 MHz due to the increasing non-linearity of the analog multipliers with frequency. The output impedance was estimated by observing the difference of load current outputs for two different loads (100 Ω and 670 Ω). Based on the measured output voltage and current accuracy limitations, it is estimated that the output impedance is more than a 1000 times larger than the load at 2 MHz, i.e., more than 1 MΩ. The simulated output resistance was 84 MΩ.

The measured THD of the current driver for a current of 1 $mA_{p\text{-}p}$ was 0.25% at 200 kHz rising to 0.4% at 500 kHz. Comparing this with the ideal multiplier in Section III under similar conditions suggests that at lower frequencies a significant part of the total harmonic distortion (THD) is due to the non-ideal square transistors rather than due to the addition of flipped followers and current mirrors. The contribution of the latter increases with frequency.

In vitro measurements (not shown) were also conducted to evaluate the current driver performance when in direct contact with electrodes in physiological solutions of potassium chloride (KCl) with different conductivities to represent different physiological entities [14]. The output currents were measured at frequencies from 100 kHz to 2 MHz. The accuracy at 100 kHz was $< 0.3\%$ and at 2 MHz was $<0.45\%$ for 0.4 mA to 1 mA current amplitudes.

Table I shows the measured performance of the current driver compared to the state of the art integrated current drivers. The phase error, output impedance and maximum operational frequency outperform the other state of the art current drivers in the literature.

B. Effect of Stray Capacitances

Fig. 9 shows the stray capacitances associated with the two output drives. I_{drive1} drives the load Z_L and I_{drive2} drives the two sense resistors R_S. C_{stray} (about 10 pF) is the capacitance associated with the external load due to chip connections, and introduces the 3° delay at 3 MHz which cannot be removed. C_S (femto-Farads) is the capacitance associated with the sense resistors R_S which here are internal. For accuracy R_S is usually external and C_S is then about 5 pF. Since R_S is a part of the compensation feedback any phase delay due to C_S will be cancelled. The phase at frequencies below 1 MHz is near zero and increases to 2° at 2 MHz.

V. Conclusion

An alternative current driver with automatic phase compensation has been designed and tested. The system provides a 1 $mA_{p\text{-}p}$ drive current with an accuracy of 0.43% at 2 MHz and 3° phase error at 3 MHz. The introduction of the phase compensation circuit significantly reduces the input/output phase error of the driver near the pole frequency of the current driver compared to other state of the art systems. Any phase error at the output of the system is due to the presence of stray capacitors. The accuracy of the transconductance of the system is dictated by sense resistor accuracy which can be on chip if dc control currents are used. The current driver can be configured to operate with multi-frequency sinewaves by adding parallel current drivers with their corresponding phase compensation.

References

[1] S. Gabriel, R. W. Lau, and C. Gabriel, "The dielectric properties of biological tissues: II. Measurements in the frequency range 10 Hz to 20 GHz," *Phys. Med. Biol.*, vol. 41, no. 11, pp. 2251–2269, Nov. 1996.

[2] P. Kassanos, L. Constantinou, I. F. Triantis, and A. Demosthenous, "An integrated analog readout for multi-frequency bioimpedance measurements," *IEEE Sensors J.*, vol. 14, no. 8, pp. 2792–2800, Aug. 2014.

[3] G. Qiao *et al.*, "Bioimpedance analysis for the characterization of breast cancer cells in suspension," *IEEE Trans. Biomed. Eng.*, vol. 59, no. 8, pp. 2321–2329, Aug. 2012.

[4] J. J. Ackmann, "Complex bioelectric impedance measurement system for the frequency range from 5 Hz to 1 MHz," *Ann. Biomed. Eng.*, vol. 21, no. 2, pp. 135–146, 1993.

[5] A. S. Tucker, R. M. Fox, and R. J. Sadleir, "Biocompatible, high precision, wideband, improved Howland current source with lead-lag compensation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 1, pp. 63–70, Feb. 2013.

[6] L. Constantinou, I. F. Triantis, R. Bayford, and A. Demosthenous, "High-power CMOS current driver with accurate transconductance for electrical impedance tomography," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 4, pp. 575–583, Aug. 2014.

[7] L. Constantinou, R. Bayford, and A. Demosthenous, "A wideband low-distortion CMOS current driver for tissue impedance analysis," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 2, pp. 154–158, Feb. 2015.

[8] N. Neshatvar, P. Langlois, and A. Demosthenous, "An improved wideband CMOS current driver for bioimpedance applications," in *Proc. ISCAS*, Montreal, QC, Canada, 2016, pp. 2447–2450.

[9] P. J. Langlois, N. Neshatvar, and A. Demosthenous, "A sinusoidal current driver with an extended frequency range and multifrequency operation for bioimpedance applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 3, pp. 401–411, Jun. 2015.

[10] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY, USA: McGraw-Hill, 2001.

[11] R. G. Carvajal *et al.*, "The flipped voltage follower: A useful cell for low-voltage low-power circuit design," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 7, pp. 1276–1291, Jul. 2005.

[12] A. Demosthenous and M. Panovic, "Low-voltage MOS linear transconductor/squarer and four-quadrant multiplier for analog VLSI," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 9, pp. 1721–1731, Sep. 2005.

[13] P. R. Gray, P. J. Hurt, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th ed. New York, NY, USA: Wiley, 2009.

[14] F. Caselli, P. Bisegna, and F. MacEri, "EIT-inspired microfluidic cytometer for single-cell dielectric spectroscopy," *J. Microelectromechan. Syst.*, vol. 19, no. 5, pp. 1029–1040, Oct. 2010.

[15] H. Hong, M. Rahal, A. Demosthenous, and R. H. Bayford, "Comparison of a new integrated current source with the modified Howland circuit for EIT applications," *Physiol. Meas.*, vol. 30, no. 10, pp. 999–1007, 2009.

[16] L. Yan *et al.*, "A 3.9 mW 25-electrode reconfigured sensor for wearable cardiac monitoring system," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 353–364, Jan. 2011.

[17] N. Neshatvar, P. J. Langlois, D. Jiang, and A. Demosthenous, "An integrated CMOS current driver using nonlinear feedback for bioimpedance applications," in *Proc. ISCAS*, Lisbon, Portugal, 2015, pp. 1250–1253.