Single-Pulse Harmonic Modulation for Short Range Biomedical Inductive Data Transfer

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***Abstract*—Short-range, low-power, high data-rate telemetry is an increasingly desirable feature for implantable medical devices (IMDs), and is commonly implemented using an inductive link. Pulse Harmonic Modulation (PHM) provides the desired high data rates and low power consumption, but requires precise pulse timing. This paper presents a modification of PHM, Single-Pulse Harmonic Modulation (SPHM), which offers reduced power consumption and lower implementation complexity. In order to test the SPHM concept, transmitter and receiver circuits were designed in 0.35μm CMOS and simulated. The simulated results suggest that the circuits can transceive data at 50Mb/s, consuming 1.49pJ/b and 2.59pJ/b at the transmitter and receiver respectively, from a 1.2V supply.**

I. Introduction

Short range inductive data telemetry is a key feature of modern implantable medical devices (IMDs). The data rate required for a given IMD however will depend on application. For instance, an implanted stimulator may only require a few kb/s of data rate, such that it can be programmed, whereas a multi-channel neural recording device may require many Mb/s to transmit the neural data. This is particularly relevant for emerging neural recording and ECoG systems with high channel count [1], [2]; as the number of channels increase, the data rate must also increase [3]. Other IMDs requiring high data rates include cochlear implants and visual prostheses.

Despite this growing requirement for robust data telemetry, the power consumption of any data telemetry scheme must also be tightly controlled, since IMDs generally have only small power budgets available. Additionally IMDs are generally small in size, limiting implementation size/complexity. As a result, this compromise drives the design process of most data telemetry schemes used in IMDs.

An attractive feature of inductive data telemetry is the ability to superimpose data telemetry onto a power link, using techniques like passive phase shift keying (PPSK) [4]. While a combined power/data link is attractive for a compact system, the data rate is usually limited by the power carrier frequency. Such systems therefore rarely exceed data rates of a few Mb/s. Such low data rates are unsuitable for transmitting high volumes of recorded data.

To achieve higher data rates it is necessary to employ a dedicated data link, which can safely use a higher carrier frequency, since power transfer efficiency is no longer an issue. Such systems can then employ conventional data modulation schemes such as FSK or QPSK [5]. While providing an improved data rate, these systems still require a carrier to be generated, which can be a concern when trying to conserve power.

Pulse Harmonic Modulation (PHM) is an example of a carrier-less data telemetry scheme that takes advantage of the resonant nature of an inductive link to achieve higher data rates and lower power consumption than other inductive methods [6], [7], [8]. However, implementing PHM requires a pulse-pattern generator that must create a pair of pulses with a precise delay (sub-ns precision) and precise amplitude. Deviation from the optimal delay and amplitude values can result in inter-symbol interference and have a negative impact on performance.

This paper presents a single-pulse PHM implementation (SPHM) that retains the benefits of PHM (low power consumption, high data rate, no carrier required), while reducing the required circuit implementation complexity, reducing the sensitivity to process, voltage, and temperature variations (PVT), and further reducing the power consumption. A transmitter and receiver circuit have been designed and simulated in 0.35μm CMOS to verify the concept.

The paper is structured as follows: Section II briefly reviews the principle of PHM and presents the SPHM approach, Section III covers the design of the transmitter and receiver circuits, Section IV presents the simulated circuit behaviour, and Section V concludes the paper.

II. Theory

A. Pulse Harmonic Modulation

The theory of operation of PHM is first described by Inanlou et. al. [6], and is briefly summarised here. The key behind PHM involves taking advantage of the resonant impulse response provided by relatively high-Q inductive links. Driving such a link with a sharp impulse will generate an oscillation with a rapid rise and slow decay. By carefully generating an opposing 'suppression' impulse with the correct delay and amplitude, an opposing ringing response is generated, cancelling

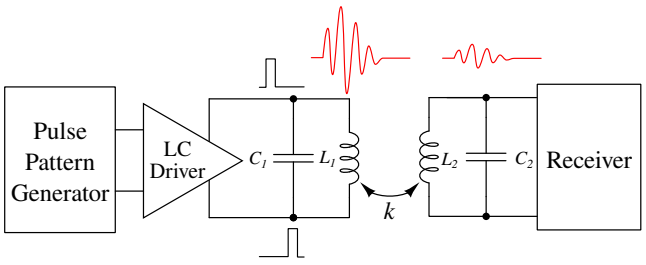

Fig. 1: Block diagram of a PHM data link, showing excitation and suppression pulses.

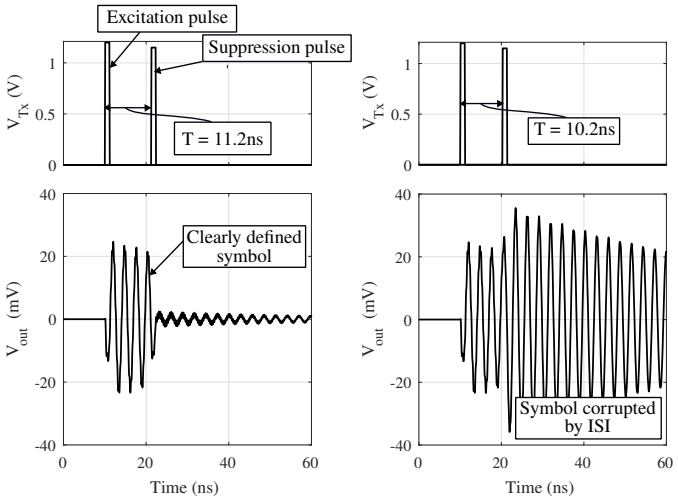

Fig. 2: Simulation of ISI in PHM for different interpulse delays, (a) 11.2ns, (b) 10.2ns. The link resonant frequency here is $\approx$ 350MHz.

the slow decay and leaving a short burst of oscillation [8]. These short bursts can be used to form a bitstream with a much higher data rate than if the oscillations were left to decay naturally. Fig. 1 shows a block diagram of a typical PHM data link, consisting of a pulse pattern generator, two coupled coils, and an RF receiver. The parallel capacitances shown (C_1,C_2), can be formed from system parasitics or by additional capacitors, depending on the receiver bandwidth. Another benefit of PHM is that the receiver requires no local oscillator or mixer to acquire the data, simplifying the circuit design and reducing power consumption.

The key shortfall of this scheme, however, is its sensitivity to the delay and amplitude of the excitation and suppression pulses. Should they vary from optimum values the data can suffer significant inter-symbol interference (ISI), leading to corruption of data bits. This is illustrated in Fig. 2; the correct pulse timing in this example is determined to be 11.2ns, Fig. 2a shows a well defined symbol. However introducing a 1ns error (Fig. 2b) renders the transmitted bit completely hidden by ISI.

This sensitivity to pulse timing must be taken into consideration when designing PHM circuits in CMOS. For instance, PVT variations could easily create wide variations in pulse timing unless techniques such as digital trimming and auto-calibration are used, which add further complexity and cost.

B. Single-Pulse Harmonic Modulation

SPHM modifies PHM, by replacing the precisely timed suppression pulse with a long pulse applied to a 'damping' switch connected across the coils of the link. In this way the symbol is shortened without the need for the interpulse delay to be precise. Fig. 3 shows a basic block diagram of an SPHM system.

The theory of operation of SPHM is described below, and is illustrated in Fig. 4. The incoming data is assumed to be

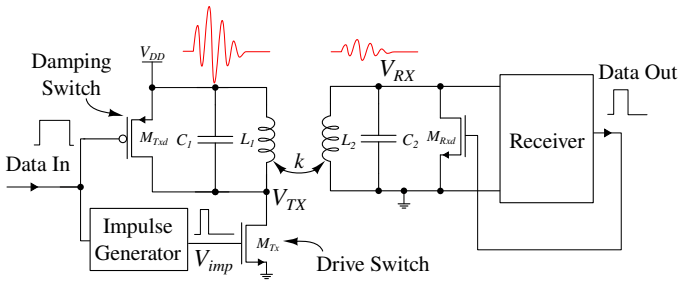

Fig. 3: Block diagram of the SPHM scheme.

between 20% and 50% high to encode a '1', and 100% low to encode a '0'. This restriction is necessary as the data stream is in direct control of the transmit damping switch M_{Txd}. The incoming data also directly drives an impulse generator, which should generate sharp impulses on the rising data edge to drive the transmitter switch M_{Tx}. This impulse must be short in comparison to the natural frequency of the resonant circuit formed by L_1 and C_1. The maximum impulse width, t_{pw}, is defined as [6]:

$$t_{pw(max)} = 2\sqrt{2}\sqrt{L_1 C_1} \tag{1}$$

Defining the impulse width to be sufficiently short (i.e. $t_{pw} \leq t_{pw(max)}$ according to (1)) allows the short pulse to be approximated as an ideal impulse. These impulses trigger the switch M_{Tx}, drawing a burst of current through the tank formed by L_1 and C_1. This will create a sharply rising ringing response, which is detected in the receiver side by L_2 and C_2. The switch M_{Txd} will turn on once the data input returns low. This has the effect of reducing the Q-factor of L_1 and C_1 greatly (the r_{on} of $M_{Txd} \ll R_{P1}$ where R_{P1} is the parallel loss resistance of $L_1||C_1$). This reduction in Q causes the oscillations to rapidly be damped out at the primary side after

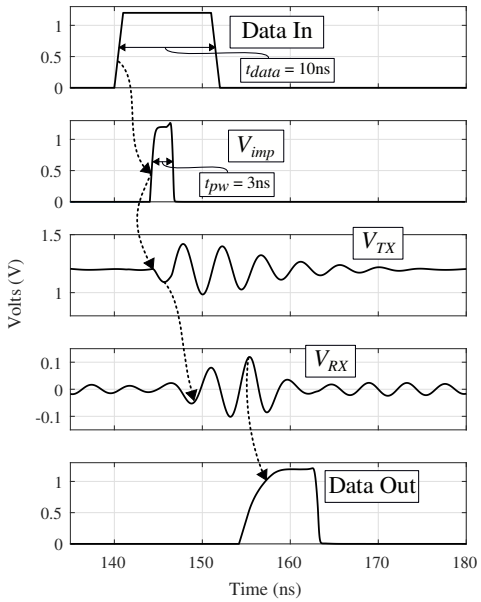

Fig. 4: Example timing diagram for SPHM.

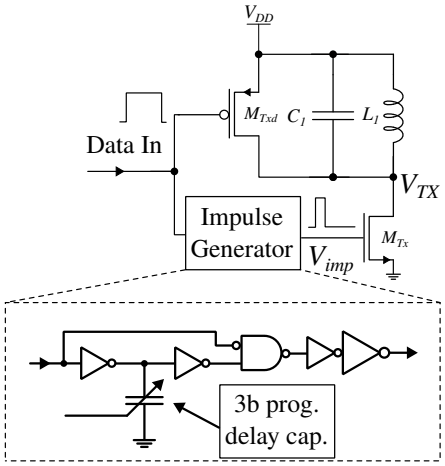

Fig. 5: Block diagram of the transmitter circuit.

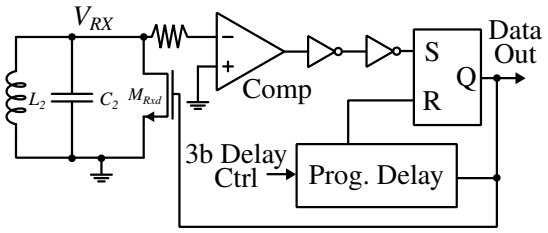

Fig. 6: Block diagram of the receiver circuit.

TABLE I: Link specifications for simulation in accordance with the link in Fig. 1. R_1, R_2 are the series losses for L_1, L_2

L_1, L_2	200nH
C_1, C_2	1pF
R_1, R_2	5Ω
k	0.1

a bit has been transmitted. The same principle is employed at the receiver. When no bit has yet been detected, the receiver damping switch M_{Rxd} is open, so the high Q of $L_2||C_2$ allows the ringing signal to build up. Once the bit has been successfully detected, the receiver drives the gate of M_{Rxd} to short out the receiver input; damping the signal in the same way as M_{Txd} at the transmitter.

Fig. 4 shows that the SPHM scheme exhibits the same short oscillatory bursts that characterise PHM, allowing for carrierless, relatively high rate data transmission. The key benefits of SPHM are as follows: since only one high speed impulse needs to be generated instead of two, the power consumption of the transmitter is reduced. Secondly, there is no strict requirement for precise pulse timing, other than the restriction that the impulse width t_{pw} must be sufficiently short. The details regarding power consumption and resilience to timing variations are discussed in more detail in Section IV.

III. Circuit Design

To test the SPHM concept, transmitter and receiver circuits were designed in 0.35μm CMOS. These circuits are currently under fabrication, and their designs are discussed below.

A. Transmitter

The transmitter is a simple circuit, formed of the transistors M_{Tx}, M_{Txd}, and an impulse generator. Fig. 5 shows the transmitter circuit in more detail.

The impulse generator shown in Fig. 5 functions by combining a programmable delay cell with a simple logic block. The data input is compared with a delayed version of that data; the output is only high when the input data is high and the delayed data is low. As such the pulse width t_{pw} can be modified by altering the capacitance of the 3b programmable capacitor (40fF, 80fF, 160fF). The output inverter chain is tapered to strongly drive the gate of M_{Tx}.

B. Receiver

A block diagram of the receiver circuit is shown in Fig. 6. The core of the receiver circuit is a comparator based on cross-coupled common-gate amplifiers [9], which are ideal for a ground referenced configuration. The operation of the circuit is such that the comparator output will remain low until a large enough deviation is present at V_{RX}, at which point the comparator output will trigger. This triggering sets the output latch, and activates the receiver damping switch M_{Rxd}. The latch will reset itself after a delay defined by the programmable delay block. The programmable delay block uses a series of stacked delay cells as used in the transmitter in order to allow for longer length recovered bits. The series resistor at the comparator input is small (500Ω) and serves two purposes. Firstly it provides some isolation between the reset switch and the comparator input, useful in this case as this type of comparator has a relatively low input impedance. Secondly it effectively provides a small offset at the input of the comparator, to reduce the chance of false triggering.

IV. Simulation Results

The behaviour of the circuit was simulated to determine its data rate capabilities, limits of acceptable data pulse widths, and power consumption of the transmitter and receiver blocks. The results of these simulations are presented in this section.

The transmitter and receiver circuits were simulated on either side of a link with parameters as specified in Table I. These parameters result in a natural resonant frequency $f_{res} \approx$ 355.8MHz. The simulations show a natural resonant frequency closer to 222MHz, due to the additional capacitances seen from the transmitter and receiver interfaces. This frequency would likely be reduced further in the fabricated chip, which would be subject to further parasitic capacitances in the packaging and board. The precise natural frequency is not crucial however, as long as it is sufficiently higher than the data rate so that symbols are recognisable.

The results of a postlayout system-level simulation are shown in Fig. 7, where a pseudorandom sequence of data is transmitted and received, with a nominal data rate of 50Mbps.

The oscillatory bursts in V_{TX} and V_{RX} in Fig. 7 can be seen to have essentially no dead time between them in the case of two consecutive '1's, indicating that 50Mbps is near

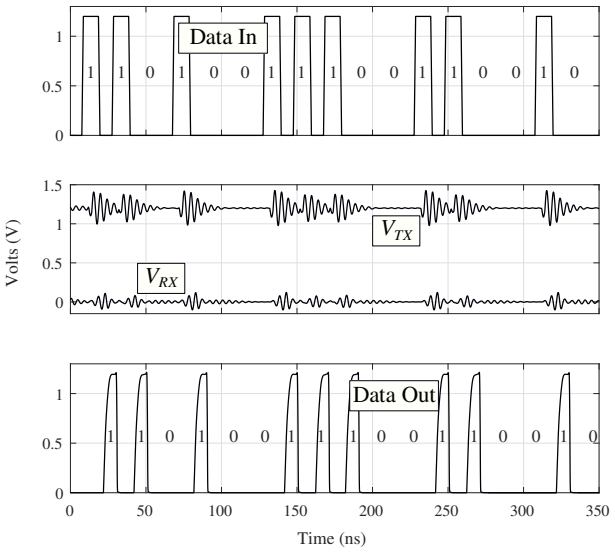

Fig. 7: Simulated timing data for transmission of a pseudorandom sequence at 50Mbps.

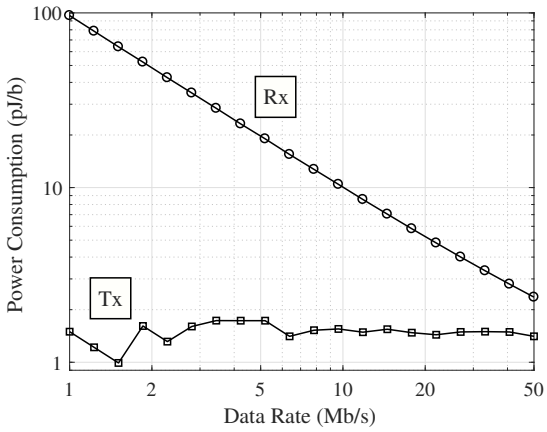

Fig. 8: Power consumption (pJ/b) vs increasing data rate.

the maximum data rate limit for this simulated system. Fig. 8 shows the power consumption in terms of energy per bit (pJ/b) against varying data rate. The data stream used was a stream of consecutive '1's, as this should be the worst case for power consumption. Since the transmitter has very little quiescent power consumption, it maintains an almost constant value averaging at $\approx 1.49\text{pJ/b}$. The receiver power consumption is dominated by quiescent consumption (mostly in the biasing for the comparator), and therefore presents a logarithmic rolloff as the data rate increases. The receiver therefore effectively works more efficiently at higher data rates, achieving 2.59pJ/b at 50Mb/s, compared to 96.52pJ/b at 1Mb/s. The power consumption figures here exclude the power drawn by pad buffers.

To determine the resilience of the system to variations in pulse width/timings, the system was tested with a sequence of consecutive '1's at 50Mb/s, and the pulse width of the incoming data stream (t_{data}) was varied from the nominal 10ns (50% duty). Additionally Monte Carlo variations of the impulse width were simulated, to examine the effect of variations from the nominal pulse width t_{pw}=3ns. The system was observed to successfully transceive in simulations as long as: $3\text{ns} \leq t_{data} \leq 11\text{ns}$ and $2\text{ns} \leq t_{pw} \leq 3.8\text{ns}$. This is in line with (1); t_{data} only needs to be long enough to allow the link to start ringing, but if it is too long ISI will result. Similarly t_{pw} must remain sufficiently short or the generated ringing will have a reduced amplitude.

V. Conclusion and Future Work

The SPHM method of data transmission through an inductive link has been presented, which improves upon traditional PHM. Transmitter and receiver circuits have been designed in 0.35μm CMOS to test the concept, which are currently under fabrication. Simulations of these circuits suggest the method is capable of 50Mb/s data transmission, with a low power consumption.

These simulation results suggest that SPHM is well suited to tackle the increasing demand for higher data rates at lower power consumptions put forward by next-generation multi-channel IMDs [3].

Future work will include comparison of chip measurements with simulation results, as well as development of a rigorous theoretical analysis to facilitate a quantitative optimization procedure.

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