Active Front-End converter applied for the THD reduction in power systems

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Abstract—The Active Front-End (AFE) converter topology is generated by modifying a conventional back-to-back converter, from using a single VSC to use pVCS connected in parallel. The AFE configuration improves the capability, efficiency and reliability of energy conversion devices connected to the power system. In this paper, a novel technique to reduce the total harmonic distortion (THD) in an AFE converter topology is proposed and analyzed. The THD reduction is achieved by applying a phase shift angle in the SPWM switching signals of each AFE converter VSC. To verify the functionality and robustness of the proposed methodology, the power system simulation in Matlab-Simulink is analyzed for a type-4 wind turbine converter with total power output of 9MW. The obtained simulation results show a THD reduction up to 2.5 for AFE connected to the power network.

Index Terms—Active-Front-End, back-to-back, wind energy system.

I. INTRODUCTION

Back-to-back converters play a significant role in modern wind energy systems (WES), since nowadays these are used in wind turbines, as type-3 that constitutes the majority of the commercial applications of variable speed; and type-4 that makes use of B2B to condition and inject the wind power to the AC grid. The B2B converter in a type-4 WT decouples the power network dynamics from the generator; this is advantageous in terms of grid fault ride-through capabilities [1-3]. However, the type-4 wind turbine implementation results in higher cost than type-3 WTs since in each turbine the B2B converter must be full-scale and transfer electric power, up to 10MW [4]. In addition, full-scale B2B injects a higher Total Harmonic Distortion (THD) into the AC grid (due of the magnified size of the B2B converter) [5]. Notwithstanding, by modifying the VSCs structure of a conventional B2B configuration and with the connection of pVSCs in parallel, it is possible to provide a viable and efficient solution to improve the power transfer capacity and reliability in the power systems quality, at a low cost. This topology modification is called Active Front-End (AFE) converter [6-7]. Some examples of AFE converter topology can be found in open literature. In [8], the connection of Front-End converters in parallel is used to generate a power factor of ≈1 at the WES; however, the paper only analyzes the passive VSC in rectifier mode (that is, the three-phase VSC topology is composed by 6 diodes). Additionally, the work in [8] omits the THD current analysis, which, by having a passive VSC, oscillates around 79% [9]. This THD is much higher than the one reported in this research. In [10] the authors present analytically and experimentally the control method for the current balance in an AFE power converter of 600kVA, however, the authors make the AFE converter analysis connecting only two VSCs in parallel, generating: a THD of 4.32% (this is higher than in our research work with THD of 2.2%).

Based on the above, in this article the modeling and analysis of an AFE converter topology is presented. The AFE converter is formed by three VSCs connected in parallel at both ends of the B2B converter and this is used for the THD reduction in power systems. To verify the functionality and robustness of the proposed methodology, a Matlab-Simulink simulation is carried out for a 9MVA converter system.

II. TOPOLOGY OF THE ACTIVE FRONT-END CONVERTERS

A. Active Front-End Converter

The structure of the AFE converter is composed by two VSCs, where, in the rectifier side, a VSC provides power conversion from medium AC voltage to DC voltage levels, and in the inverter side, a VSC generates the AC voltages, from the DC bus, required by the grid [11]. The AFE converter topology is a modification of the conventional B2B converter where instead of a single VSC, several VSCs are connected in parallel, as shown in Figure 1. This topology has the advantage of: minimized size of each VSC unit, which manages a portion of the total nominal power; a reduced ripple on the injected current, which improves the voltages

quality at the Point of Common Coupling (PCC), an increased equivalent switching frequency, generating a smaller passive filters on AC-side and the reduction of switching losses brings a lower THD [12].

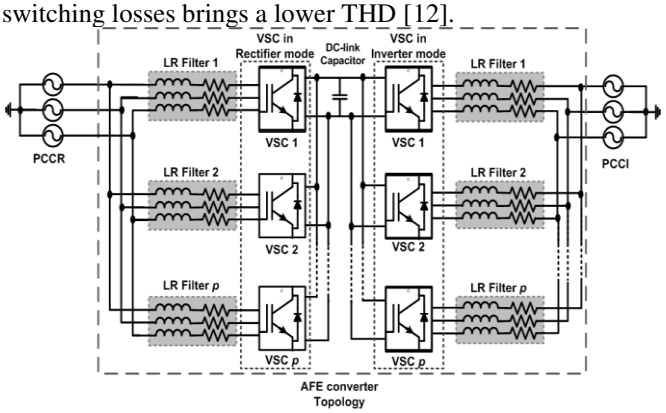

Figure 1 AFE converter topology

III. MODELING OF THE ACTIVE FRONT-END CONVERTER

A. Time-domain relationship of the VSC AC-side rectifier/inverter.

The input-output power transfers between delivering voltage node $\left[v_t(t)\right]_{r,I}^{h,j}$ and the receptions voltage node $\left[v_{PCC}(t)\right]_{r,I}^{h,j}$ along $\left[i(t)\right]_{r,I}^{h,j}$ can be analyzed through the time-domain relationship of the VSC AC-side in the rectifier/inverter given by [13]:

$$\left[\frac{d}{dt}i(t)\right]_{r,I}^{h,j} = \left(\frac{R_{PCC}}{L_{PCC}}\right)\left[i(t)\right]_{r,I}^{h,j} \left(\frac{1}{L_{PCC}}\right)\left[v_t(t)\right]_{r,I}^{h,j}+\left(\frac{1}{L_{PCC}}\right)\left[v_{PCC}(t)\right]_{r,I}^{h,j} \quad (1)$$

where h is the VSC three-phase vector (a,b,c) in rectifier mode, r represents the corresponding elements to the VSC in rectifier mode, j is the VSC three-phase vector (a,b,c) in inverter mode and I represents the corresponding elements to the VSC in inverter mode.

The Equation (1) is represented using the dq reference frame control by equivalent equations based on the Clarke and Park transformation. Then, the dq model derived of the VSC AC-side (1), can be described as:

$$L_{PCC}\left[\frac{d}{dt}i^d(t)\right]_{r,I} = \left(\ {}_0\cdot L_{PCC}\right)\left[i^q(t)\right]_{r,I} \left(R_{PCC}\right)\left[i^d(t)\right]_{r,I}+\left[v_t^d(t)\right]_{r,I} \left[v_{PCC}^d(t)\right]_{r,I} \quad (2a)$$

$$L_{PCC}\left[\frac{d}{dt}i^q(t)\right]_{r,I} = \left(\ {}_0\times L_{PCC}\right)\left[i^d(t)\right]_{r,I} \left(R_{PCC}\right)\left[i^q(t)\right]_{r,I}+\left[v_t^q(t)\right]_{r,I} \left[v_{PCC}^q(t)\right]_{r,I} \quad (2b)$$

The voltages generated by the VSC AC-side are:

$$\left[v(t)\right]_{r,It}^{g,k} = \left(V_{DC}(t)/2\right)\left[m(t)\right]_{r,I}^{g,k} \quad (3)$$

where V_{DC} is the DC-link voltage, g is the dq reference frame components vector of the VSC in rectifier mode and k is the dq reference frame components vector in inverter mode.

The presence of ${}_0L_{PCC}$ in (2a) and (2b) indicates the coupled dynamics between $\left[i^d(t)\right]_{r,I}$ and $\left[i^q(t)\right]_{r,I}$. To decouple such dynamics, $m^d(t)$ and $m^q(t)$ are changed, based in the dq reference frame, i.e.

$$\left[m^d(t)\right]_{r,I} = \left(2/V_{DC}(t)\right)\left[\left[U^d(t)\right]_{r,I} \left(\left(\ {}_0\cdot L_{PCC}\right)\left[i^q(t)\right]_{r,I}\right)+\left[v_{PCC}^d(t)\right]_{r,I}\right] \quad (4a)$$

$$\left[m^q(t)\right]_{r,I} = \left(2/V_{DC}(t)\right)\left[\left[U^q(t)\right]_{r,I}+\left(\left(\ {}_0\cdot L_{PCC}\right)\left[i^d(t)\right]_{r,I}\right)+\left[v_{PCC}^q(t)\right]_{r,I}\right] \quad (4b)$$

where $\left[U^d(t)\right]_{r,I}$ and $\left[U^q(t)\right]_{r,I}$ are two additional control inputs.

By substituting (4a) and (4b) into (2a) and (2b), respectively, a first order lineal system is obtained. Equation (5) describes the VSC AC-side converter plant.

$$\left[U(t)\right]_{r,I}^{g,k} = L_{PCC}\left[di(t)/dt\right]_{r,I}^{g,k} \ R_{PCC}\left[i(t)\right]_{r,I}^{g,k} \quad (5)$$

Equation (5) is represented in the time domain; its representation in the frequency domain is shown in (6); which describe two decoupled, first-order, linear systems, representing the active and reactive power in the VSC AC-side, these are controlled through $\left[U(s)\right]_{r,I}^{g,k}$.

$$\left[U(s)\right]_{r,I}^{g,k} = sL_{PCC}\left[i(s)\right]_{r,I}^{g,k} \ R_{PCC}\left[i(s)\right]_{r,I}^{g,k} \quad (6)$$

Rewriting equation (6), the transfer function representing the VSC plant in rectifier/inverter mode is given, by

$$\left[i(s)\right]_{r,I}^{g,k} = \left[U(s)\right]_{r,I}^{g,k}\left(sL_{PCC}+R_{PCC}\right)^{1} \quad (7)$$

With the purpose of tracking the DC reference commands in the loop, the proportional-integral (PI) compensators are used to obtain:

$$\left[U(s)\right]_{r,I}^{g,k} \ \left[k(s)\right]_{r,I}^{g,k} = \left(\left[i(s)\right]_{r,I}^{gref,kref} \ \left[i(s)\right]_{r,I}^{g,k}\right)\left((kp/s)\left(s+(ki/kp)\right)\right) \quad (8)$$

where kp and ki are the proportional and integral gains, respectively.

The feedback loops $\left[\ (s)\right]_{r,I}^{g,k}$ is:

$$\left[\ (s)\right]_{r,I}^{g,k} = \left[k(s)\cdot i(s)\right]_{r,I}^{g,k} = \left[\left(\frac{kp}{s\cdot L_{PCC}}\right)\left(\frac{s+(ki/kp)}{s+(R_{PCC}/L_{PCC})}\right)\right]_{r,I}^{g,k} \quad (9)$$

The plant pole of (9) is $\left[s = \left(R_{PCC}/L_{PCC}\right)\right]_{r,I}^{g,k}$, which is close to the origin. As a consequence, the magnitude and the phase of the loop gain start to drop from a relatively low frequency. In this context, the selection of a new pole through the PI compensator can avoid this behavior. To do this, the plant pole is eliminated by a zero of the PI compensator, being $\left[s = (ki/kp)\right]_{r,I}^{g,k}$

The relation between the plant pole and the zero of the PI can be obtained as:

$$\left[(kp/\ )/(ki/\ ) = \left(R_{PCC}/L_{PCC}\right)\right]_{r,I}^{g,k} \quad (10)$$

where the subscript τ is the time taken by the closed loop of the first order transfer function to act.

Based on (9) the kp and ki are control gains can be defined as:

$$\left[kp = L_{PCC}/\ \right]_{r,I}^{g,k} \quad (11)$$

$$\left[ki = R_{PCC}/\ \right]_{r,I}^{g,k} \quad (12)$$

Finally, the designer can selected τ in the range from 5ms – 0.5ms based on the final applications.

B. Time-domain relationship of the AFE converter DC-side

With the VSC operating in inverter mode the DC-link control is developed. The time-domain relationship of the DC-link of the AFE converter is given by:

$$\left(d\left(V_{DC}(t)\right)/dt\right)=\left(I_{DC}(t)/C\right)\ \left(V_{DC}(t)/\left(C\times R_{DC}\right)\right) \tag{13}$$

The sum of currents entering to the capacitor is:

$$I_{DC}(t)=\frac{1}{2}\sum_{j=a}^{c} m_l^j(t)i_l^j(t) \tag{14}$$

The functionality of the AFE converter requires that [14]:

$$V_{DC}\quad \left|2\left(v_{PCCL\ L}\right)\right| \tag{15}$$

By assuming a frequency commutation, f_{com}, ten times higher than the line frequency, f_{line}, that is, $f_{com} > 10\ f_{line}$.

C. System parameters design

To determine the values of the $R_{PCCr,I}$ and $L_{PCCr,I}$ elements, the system base parameters are obtained, i.e. the system base current is obtained as:

$$i_{r,I}=2\left(P_{PCCr,I}\right)/3\left(v_{PCCr,I}\right) \tag{16}$$

where $P_{PCCr,I}$ is the power, $v_{PCCr,I}$ is the voltage and $i_{r,I}$ is the current, at the corresponding PCC where each VSC is connected .

The system base impedance is $Z_{r,I}=v_{PCCr,I}/i_{PCCr,I}$; the value of $L_{PCCr,I}$ is selected to be 0.15pu of the system base impedance, that is: $Z_{PCCr,I}=0.15\left(Z_{r,I}\right)$; therefore, $L_{PCCr,I}$ is $L_{PCCr,I}=Z_{PCCr,I}/\ _0$; where ω_0 is the system nominal frequency. The $R_{PCCr,I}$ value varies according to the application, in a range from 0.1Ω to 0.5Ω. The values of the inductance and resistance are used to obtain the system feedback gains, as shown in (11) and (12).

IV. Description of the SPWM Technique Applied in the THD Reduction

The THD reduction is achieved by modifying the SPWM switching signals in each VSC. The above is carried out by a phase shift angle in each the carrier signals of each VSC; the modulating signal angle is not changed. Finally, the output signals (voltage or current) of each VSC are added. The n-harmonics content is given by the Fourier series expansion, i.e.,

$$f(t)=C_0+\sum_{n=1}\left(C_{r,In}\cos\left(n\ _0t+\ \right)\right) \tag{17}$$

where $C_0=a_0/2$, $C_{r,In}=\sqrt{a_{r,In}^2+b_{r,In}^2}$, $\ =\tan^{-1}\left(b_{r,In}/a_{r,In}\right)$ and n is the harmonic number.

The magnitude of each harmonic is calculated by,

$$a_{r,In}=\frac{2}{T}\left(\int_{-T/2}^{T/2} f(t)\cos(n\ _0t)d\ _0t\right) \tag{18}$$

$$b_{r,In}=\frac{2}{T}\left(\int_{-T/2}^{T/2} f(t)\sin(n\ _0t)d\ _0t\right) \tag{19}$$

In this paper, the AFE converter is built with three VSC in parallel. A total phase shift angle analysis at different values is performed, determining the correct phase shift angle between the carrier signals; using this angle in the SPWM generation, it is possible generates the lower THD at the system. The analysis is shown in detail in Table 1.

Table 1 THD equivalent to different phase shift angle.

Total phase shift (θ_p)	Valor θ para cada VCS			%Total Harmonic Distortion (THD)
	θ_1	θ_2	θ_3	
0	0	0	0	6.82%
π/6	0	π/18	π/9	5.73%
π/3	0	π/9	2π/9	3.39%
π/2	0	π/6	π/3	3.45%
2π/3	0	2π/9	4π/9	2.89%
5π/6	0	5π/18	5π/9	3.08%
π	0	π/3	2π/3	6.01%
7π/6	0	7π/18	7π/9	7.04%
4π/3	0	4π/9	8π/9	4.26%
3π/2	**0**	**π/2**	**π**	**2.71%**
5π/3	0	5π/9	10π/9	2.86%
11π/6	0	11π/18	11π/9	3.27%
2π	0	2π/3	4π/3	4.16%

Through Table 1, it is observed that the THD is lower when an angle of 3π/2 divides the number of VSCs placed in parallel, i.e.:

$$_p=(3\ \ /2)/p \tag{20}$$

where p is the number of VSC connected in parallel and θ_p is the carrier signal switching angle of each VSC.

To calculate the THD in the AFE converter, the individually equivalent circuit of each three-phase VSC is analyzed. Three-phase VSC is represented by,

$$\begin{matrix} 2Z_{r,I}i_{r,Ia} & Z_{r,I}i_{r,Ib} & Z_{r,I}i_{r,Ic} \\ Z_{r,I}i_{r,Ia} & 2Z_{r,I}i_{r,Ib} & Z_{r,I}i_{r,Ic} \\ Z_{r,I}i_{r,Ia} & Z_{r,I}i_{r,Ib} & 2Z_{r,I}i_{r,Ic} \end{matrix} = \begin{matrix} v_{r,Ita} & v_{r,Itb} & v_{PCCr,Ia}+v_{PCCr,Ib} \\ v_{r,Itb} & v_{r,Itc} & v_{PCCr,Ib}+v_{PCCr,Ic} \\ v_{r,Itc} & v_{r,Ita} & v_{PCCr,Ic}+v_{PCCr,Ia} \end{matrix} \tag{21}$$

Using Kirchhoff's Current Law (KCL), the currents flowing towards node must be equal to the currents leaving the node, i.e.,

$$i_{r,Ic}=i_{r,Ia}+i_{r,Ib} \tag{22}$$

Replacing equation (22) in (21) gives line-to-line current, i.e.

$$\begin{bmatrix} i_{r,Iab} \\ i_{r,Ibc} \\ i_{r,Ica} \end{bmatrix}=\left(\frac{1}{3Z_{r,I}}\right)\begin{bmatrix} v_{PCCr,Ia} & v_{PCCr,Ib} \\ v_{PCCr,Ib} & v_{PCCr,Ic} \\ v_{PCCr,Ic} & v_{PCCr,Ia} \end{bmatrix}\left(\frac{1}{3Z_{r,I}}\right)\begin{bmatrix} v_{r,Ita} & v_{r,Itb} \\ v_{r,Itb} & v_{r,Itc} \\ v_{r,Itc} & v_{r,Ita} \end{bmatrix} \tag{23}$$

where $v_{PCCr,I}$ represents the PCC voltage, $v_{r,It}$ is the VSC AC-side output voltage and $Z_{r,I}$ the AC-side filter.

The $v_{R,It}$ value depends on their signal modulation. The modulated and carrier signals implement the SPWM technique; these have modulation frequencies of 60Hz (ω_0) and 2000Hz ($f\omega$), respectively. The carrier signal is composed by an up-slope and a down-slope, calculated as,

$$C_{t_1p} = 1 \quad \left((4/f \quad)\left(\quad {}_0t_1 \quad {}_p\right)\right) \tag{24}$$

$$C_{t_2p} = \left((4/f \quad)\left(\quad {}_0t_2 \quad (f \quad /2) \quad {}_p\right)\right) \quad 1 \tag{25}$$

where $C_{1,2p}$ is the composed carrier signal, θ_p is phase shift angle of each VSC, fω is switching frequency of the carrier signal, t_1 is the time for the up-slope, t_2 is the time for the down-slope.

Time t_1 for up-slope is

$$_p \quad t_1 \quad \left((f \quad /2) + \quad _p\right) \tag{26}$$

Time t_2 for down-slope is:

$$\left((f \quad /2) + \quad _p\right) \quad t_2 \quad \left(f \quad + \quad _p\right) \tag{27}$$

Modulated signals in each VSC are described by the carrier signal time, that is:

$$\begin{aligned} M_{t_1p}^{h,j} &= \cos(t_1 + \quad) \\ M_{t_2p}^{h,j} &= \cos(t_2 + \quad) \end{aligned} \tag{28}$$

where h,j are the VSC three-phase vectors in rectifier and inverter mode, respectively, and φ is the corresponding angle of each phase in the modulated signal.

The comparison between modulated and carrier signals defines the SPWM signal, its representation is:

$$\begin{aligned} m_{t_1p}^{h,j} &= \left| M_{t_1p}^{h,j} \quad C_{t_1p} \right| \\ m_{t_2p}^{h,j} &= \left| M_{t_2p}^{h,j} \quad C_{t_2p} \right| \end{aligned} \tag{29}$$

Multiplying the SPWM signal and DC voltage amplitude generates the VSCs output voltage for each phase value, i.e,

$$v_{r,It}^{h,j} = V_{DC} * m_{r,I}^{h,j} \tag{30}$$

The PCC voltage $v_{PCCr,I}^{h,j}$ is,

$$\begin{aligned} v_{t_1PCCr,I}^{h,j} &= VG\left(\cos\left(\quad {}_0t_1 + \quad\right)\right) \\ v_{t_2PCCr,I}^{h,j} &= VG\left(\cos\left(\quad {}_0t_2 + \quad\right)\right) \end{aligned} \tag{31}$$

where VG is AC grid amplitude and ϕ is the corresponding angle of each phase in the three-phase grid.

The output current in each VSC is calculated as,

$$\begin{bmatrix} i_{t_1r,I}^{g,h} \end{bmatrix} = (1/(3Z_{R,I}))\begin{bmatrix} v_{t_1PCCr,I}^{g,h} \end{bmatrix} \quad (1/(3Z_{r,I}))\begin{bmatrix} v_{t_1r,It}^{g,h} \end{bmatrix}$$
$$\begin{bmatrix} i_{t_2r,I}^{g,h} \end{bmatrix} = (1/(3Z_{R,I}))\begin{bmatrix} v_{t_2PCCr,I}^{g,h} \end{bmatrix} \quad (1/(3Z_{r,I}))\begin{bmatrix} v_{t_2r,It}^{g,h} \end{bmatrix} \tag{32}$$

where $Z_{R,I}$ represents the AC-side filter impedance.

The harmonic content spectrum to obtain the THD is required. By using (18), (19) and (32) the spectrum is calculated as,

$$a_{r,In} = (2/T)\left[\left(\int_{\quad _p}^{(f \quad /2)+ \quad _p} \left(i_{t_1r,I}^{h,j} \cos\left(n \quad {}_0t_1\right)\right) d \quad {}_0t_1\right) + \left(\int_{(f \quad /2)+ \quad _p}^{f \quad + \quad _p} \left(i_{t_2r,I}^{h,j} \cos\left(n \quad {}_0t_2\right)\right) d \quad {}_0t_2\right)\right] \tag{33}$$

$$b_{r,In} = (2/T)\left[\left(\int_{\quad _p}^{(f \quad /2)+ \quad _p} \left(i_{t_1r,I}^{h,j} sin\left(n \quad {}_0t_1\right)\right) d \quad {}_0t_1\right) + \left(\int_{(f \quad /2)+ \quad _p}^{f \quad + \quad _p} \left(i_{t_2r,I}^{h,j} sin\left(n \quad {}_0t_2\right)\right) d \quad {}_0t_2\right)\right] \tag{34}$$

For the harmonic content of the output current signal, the magnitude of the individual harmonics is calculated for each VSC and added, i.e.

$$a_{r,In1} + a_{r,In2} + ... + a_{r,Inp} \tag{35}$$

$$b_{r,In1} + b_{r,In2} + ... + b_{r,Inp} \tag{36}$$

where p is the number of VSCs placed in parallel and n is the number of harmonics.

The THD in the VSC output current is,

$$THDi_{r,Iout} = \left| \left(1/C_{r,I1p}\right) \sqrt{\quad \sum_{n=2} C_{r,Inp}^2} \right| * 100 \tag{37}$$

where $C_{R,I,1p}$ is the fundamental harmonic magnitude and $C_{R,Inp}$ is the n harmonic magnitude. It is obtained as $C_{r,Inp} = \sqrt{a_{r,Inp} + b_{r,Inp}}$.

A smaller harmonic content in output current is generated within $R_{PCCR,I}$ and $L_{PCCR,I}$ optimal values. This is achieved having a $THDi_{R,Iout}$ equation based on the LR filter value, i.e.

$$i_{r,Iout} = i_{r,I1} + i_{r,I2} + ... + i_{r,Ip} \tag{38}$$

$$i_{r,Iout} = \left(\left(1/\left(3Z_{r,I}(1)\right)\right)\left(v_{PCCr,I1} \quad v_{r,It1}\right)\right) + \left(\left(1/\left(3Z_{r,I}(2)\right)\right)\left(v_{PCCr,I2} \quad v_{r,It2}\right)\right) + ... + \left(\left(1/\left(3Z_{r,I}(p)\right)\right)\left(v_{PCCr,Ip} \quad v_{r,Itp}\right)\right)$$

V. Results: Case of Study

Figure 1 shows the simulated AFE converter. It contains two infinite buses (considered as an ideal voltage source), one to supply the VSC in rectifier mode and the other to supply the VSC in inverter mode. The VSCs are connected to the infinite buses through a AC-side filter impedance, which are formed by three VSCs connected in parallel and each one is designed at power and voltage of 3MVA and 2.5kV, respectively; generating a maximum power transfer of 9MVA.

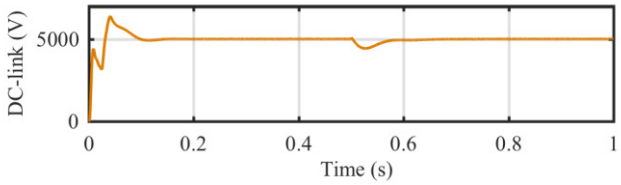

Figure 2 DC-link voltage behavior

To verify the correct power system operation, the DC-link voltage of Figure 2 is generated at 5kV. The VSC in inverter mode injects the needed active power to keep the DC-link constant at 5kV.

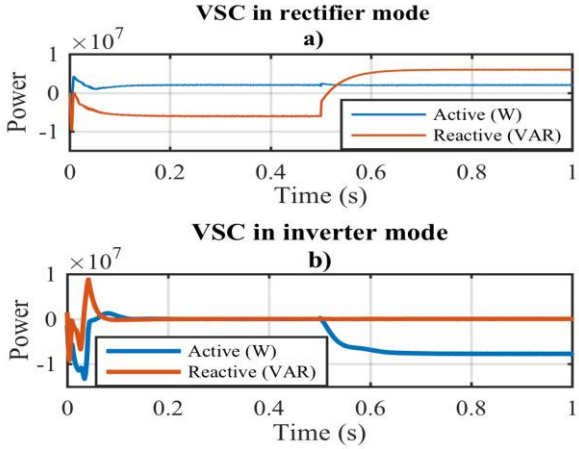

Figure 3 Exchange of active and reactive power in the system

Figure 3a shows an exchange of reactive power, from injecting a power of 6MVA to absorbing a power of 6MVA; this capacity is generated by the VSC in rectifier mode. Figure 3b shows an exchange of active power, generating a power of 7.5MVA; this capacity is generated by the VSC in inverter mode.

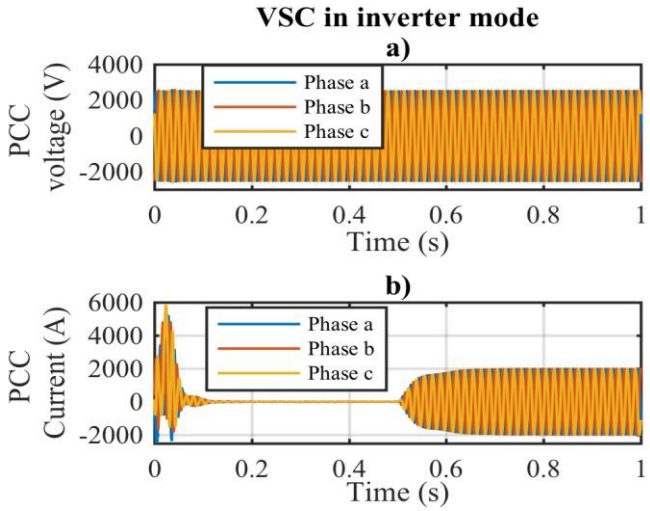

Figure 4 voltage and current behavior at the PCCI

The Figure 4 shows the voltage (Figure 4a) and current (Figure 4b) present at the PCCI when the corresponding phase shift in the carriers of each VSC connected in parallel is performed, according to Equation (20).

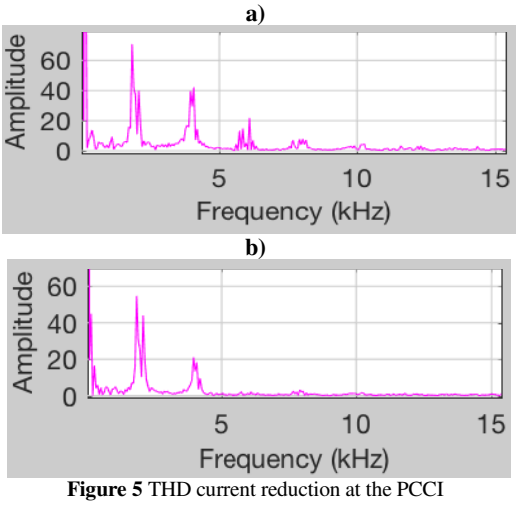

Figure 5 THD current reduction at the PCCI

Figure 5a shows the current THD at the PCCI without any phase shift between carriers of each VSC of the AFE converter, which corresponds to 6.8%. It can be seen that when the corresponding phase shift is performed in the carriers, the current THD is reduced to 2.7%, as shown in Figure 5b. The Figure shows the harmonics magnitude reduction or even their elimination, once the phase shift between carriers is made. The THD was reduced approximately 2.5 times.

CONCLUSIONS

In this paper has been analyzed the AFE converter topology, whose its modification starts from use a single VSC to use pVCS connected in parallel.

This topology has been used for effective THD reduction, through the variation in the SPWM technique applied to each VSC and a phase shift in each carrier signal angle of each VSC, while the keeping constant the modulating signal angle.

Finally, the current output signals of each VSC have been added to obtain the n-harmonics content. By Fourier series expansion a current THD reduction up to 2.5 times was achieved by using the AFE converter topology in the power network.

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