A High-Efficiency Super-Junction MOSFET based Inverter-Leg Configuration using a Dual-Mode Switching Technique

Zhengyang Feng, *Student Member*, *IEEE*, Neville McNeill, and Barry Williams
Department of Electronic & Electrical Engineering
University of Strathclyde
Glasgow, UK
Email: zhengyang.feng@strath.ac.uk, neville.mcneill@strath.ac.uk, barry.williams@strath.ac.uk

***Abstract*—High-efficiency power converters have benefits of minimizing energy consumption, reducing costs, and realizing high power densities. The silicon super-junction MOSFET is an attractive device for high-efficiency applications. However, its highly non-linear output capacitance and the reverse recovery properties of its intrinsic diode must be addressed when used in voltage source converters. A dual-mode switching technique operating in conjunction with intrinsic diode deactivation circuitry is proposed in this paper. The technique is demonstrated in an 800-W inverter-leg configuration operating from a 400-V DC voltage rail and switching at 20 kHz. Intended applications include machine drives. The full-load efficiency reaches approximately 98.7% and no forced cooling is needed.**

Keywords—control, gate driver, inverter, MOSFET, super-junction.

I. Introduction

Converter efficiency maximization is a driving factor in the power electronics industry, for high-efficiency power conversion has benefits of minimizing energy consumption, reducing costs, and realizing high power densities. These benefits make high-efficiency conversion important in applications such as renewable energy systems and hybrid and electric vehicles.

In order to achieve high efficiency and low overall losses, power semiconductor device options include wide band-gap (WBG) devices such as SiC MOSFETs and GaN HEMTs, and silicon super-junction (SJ) devices, of which the SJ MOSFET is well established. Whilst exhibiting excellent performance in against many criteria, WBG devices are costly and exhibit practical application issues such as challenges addressing crosstalk [1]. Conversely, SJ MOSFETs offer a high degree of manufacturability and established reliability [2].

SJ MOSFETs perform well in single-ended power converters when switching with SiC Schottky diodes operating as the freewheeling element [3]. However, the reverse recovery behavior of the intrinsic diode and the non-linear output capacitance C_{oss} of the SJ MOSFET present challenges when used in voltage source converter (VSC) circuits. The reverse recovery charge of the intrinsic diode is significant when the SJ MOSFET operates as a freewheeling device. Furthermore, the non-linear C_{oss} causes excessive high dv/dt especially at high voltage, which may lead to EMI or induce parasitic oscillations and potentially destroy the device [4].

Solutions proposed include the realization of VSCs by means of combined single-ended converters [5]. Other solutions include the implementation of synchronous (or 'triangular') conduction modes [6], [7], adding LC resonant circuitry to realize zero voltage switching [8], [9], or prearranged control strategies such as dead-time optimization [10]. This paper, aiming at the SJ MOSFET in an AC load current situation, proposes a dual-mode switching technique to address the detrimental influence of the MOSFET's output capacitance. This dual-mode switching technique uses minimal extra hardware and functions in conjunction with intrinsic diode deactivation circuitry. The circuit is designed for a 800-W inverter-leg circuit operating on a 400-V DC supply voltage and switching at 20 kHz. The full-load efficiency reaches approximately 98.7% and no forced cooling is needed.

II. Proposed Dual-Mode Switching Technique

A. Intrinsic Diode Deactivation

Fig. 1 shows an inverter bridge-leg that incorporates intrinsic diode deactivation circuitry. The series diodes D_s prevent reverse current flowing into the SJ MOSFETs when they would otherwise be functioning as the freewheeling elements. The external diodes D_{ext} in parallel are SiC Schottky diodes, which replace function of the intrinsic diodes and have excellent reverse recovery characteristics.

B. Non-Linear SJ MOSFET Output Capacitance

Even if the problem of the intrinsic diode is negated, the influence of the MOSFET output capacitance C_{oss} remains adverse. Fig. 2 shows the Q-V characteristic of C_{oss} of a SJ MOSFET. C_{oss} is highly non-linear and can be approximated as a rectangular Q-V curve. Consider when the load current i_L is positive, $TR1$ is off and i_L is flowing through D_{ext2}. If $TR2$ is turned on when $TR1$ is off, then it fully self-discharges its C_{oss}. When $TR1$ next turns on, it therefore has to recharge the C_{oss} of

*TR*2 from 0 V up to the DC link voltage V_{dc}. A relatively large charge has to be sourced before V_a reaches the knee point in Fig. 2 where C_{oss} drops rapidly. A high dv/dt then occurs and consequences include EMI and parasitic oscillations. The switching energy dissipated in *TR*1 due to charging C_{oss} is a minimum of $Q_{oss}V_{dc}$ which is approximated by the area (co-energy) lying under the Q-V curve in Fig. 2.

To minimize switching losses and avoid associated problems, the inverter-leg needs to operate with unipolar PWM modulation to avoid discharging C_{oss} of *TR*2. With a positive i_L, only *TR*1 switches, and *TR*2 is held off throughout the switching cycle. By holding *TR*2 off, its C_{oss} capacitance only partially discharges, down to the reverse breakdown voltage of D_{s2}. Importantly this reverse breakdown voltage is typically such that the C_{oss} capacitance is not discharged to below the knee point in Fig. 2.

Similarly, when i_L is negative, only *TR*2 switches and *TR*1 is held off throughout the switching cycle. However, a problem arises as i_L transitions through zero and bipolar switching is desirable in this region to avoid distortion due to i_L becoming discontinuous.

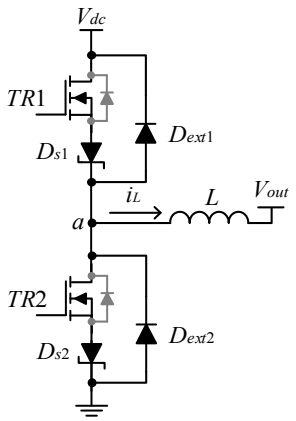


Fig. 1. Voltage source inverter-leg based around MOSFETs equipped with intrinsic diode deactivation circuitry.

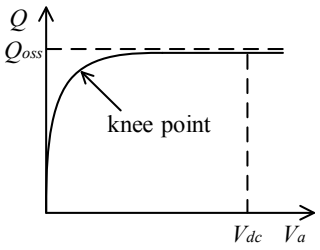


Fig. 2. Q-V characteristic curve of SJ MOSFET.

C. Proposed Dual-Mode Switching Technique

With an AC load current such as that in an inverter, a dual-mode switching control technique is proposed. In the so-called hard switching mode, unipolar PWM modulation is selected for *TR*1 and *TR*2 according to the direction of i_L. In this mode, the MOSFETs are driven in the normal way with rapid switching transitions for low losses. However, at low i_L magnitudes, bipolar PWM modulation is enabled to reduce distortion in the AC current. The problem of high peak currents due to supplying high charges into fully-discharged C_{oss} capacitances that occurs with bipolar modulation is addressed by turning the SJ MOSFETs on slowly (so-called slow switching) and thereby limiting the di/dt in the current conducted by the incoming MOSFET. Importantly, whilst this incurs losses, enabling controlled slow switching only at low i_L magnitudes means aggregate power losses in the circuit are low. Simply slow-switching an inverter with SJ devices under all current levels leads to low efficiency due to the $R_{DS(on)}Q_{oss}$ product exhibited by a die area fabricated using silicon SJ technology [11].

Fig. 3 shows the same Q_{oss} for different i_L values and different current slew rates, di/dt, where lower i_L and lower slew rate lead to lower i_{peak}. In the slow switching mode, this becomes an advantage when operating bipolar PWM modulation under low load current. Different gate resistance is used in the turn-on path to control the switching speed.

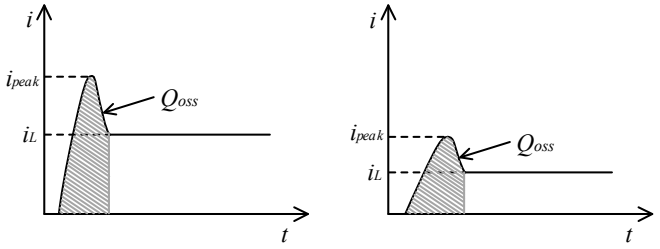


Fig. 3. Same Q_{oss} under different I_{load} and different slew rate.

D. Dual-Mode Driver Circuit

A gate driver circuit was designed to realize the dual-mode switching technique in the inverter-leg. As given by (1), the dv/dt of the driven SJ MOSFET is determined by the gate current I_{gate} and SJ MOSFET reverse capacitance C_{gd}. I_{gate} depends on the Miller plateau voltage V_{MP} and total gate resistance. This resistance consists of two parts, the internal gate resistance of the SJ MOSFET $R_{g(SJ\ MOS)}$ and the changeable external gate resistance R_{gate} on the driver board. By varying R_{gate}, the dv/dt will change according to

$$\frac{\mathrm{d}v}{\mathrm{d}t}=\frac{I_{gate}}{C_{gd}}=\frac{V_{MP}}{(R_{g(SJ\ MOS)}+R_{gate})C_{gd}}. \quad (1)$$

In the driver circuit arrangement, Fig. 4, two different paths are set: a slow switching path and a hard switching path. In the slow switching path, the slow-switching resistor R_s is 220 Ω. In hard switching path, the hard-switching resistor R_h is selected as 10 Ω. The turn-off resistor R_r is also 10 Ω. The hard switching path is active only when the enable signal is on.

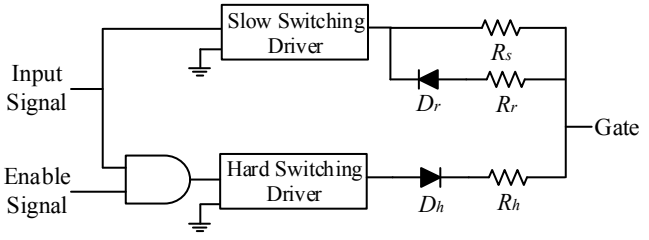


Fig. 4. Driver circuit arrangement for dual-mode switching.

III. Simulation

Simulation results are shown in Fig. 5 for a 400-V, 800-W single-phase inverter switching at 2 kHz with the dual-mode switching technique applied. The switching frequency shown is 2 kHz rather than 20 kHz, for clarity. Fig. 5(a) shows the overall load current i_L and the gate signals. When i_L>2 A, *TR*1 is hard switching and *TR*2 is held off (blue area). When -2 A<i_L<2 A, *TR*1 and *TR*2 are both slow switching in a standard complementary manner (yellow area). When i_L<-2 A, *TR*2 is hard switching and *TR*1 is held off (green area).

With reference to Fig. 5, the slow-switching ratio (SSR) is defined as the proportion of the total period of the fundamental waveform that is occupied by the slow switching period t_1. By changing the SSR ratio, the percentage of slow switching and hard switching is also changed. Considering the effect of charging and discharging of the output capacitor, a smaller SSR is expected to lead to higher efficiency and smaller overshoot inverter-leg output voltage V_{ab}, under one precondition, there is not any distortion caused by discontinuous output current i_L.

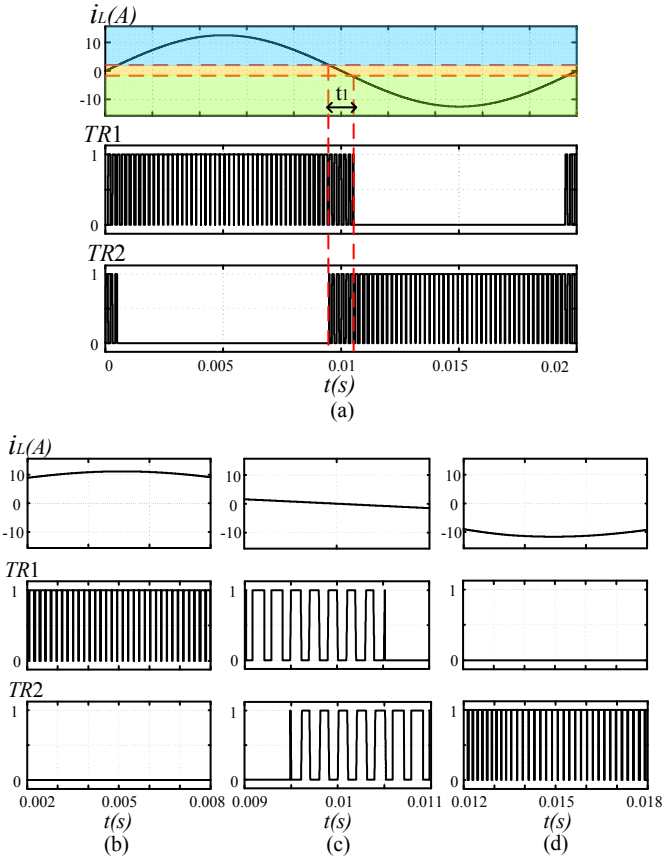


Fig. 5. Simulation results of using dual-mode switching technique in an inverter. (a) Overall i_L and gate signals; (b) hard switching for *TR*1 and *TR*2 is held off; (c) slow switching for both *TR*1 and *TR*2; and (d) hard switching for *TR*2 and *TR*1 is held off.

IV. Experimental Hardware and Losses Calculation

Fig. 6 shows the circuit configuration used for experimentation, Fig. 7 shows the experimental hardware, and details of the power components are given in Table I. Although most machine drives are of a three-phase type, a single inverter-leg was used for experimental purposes, and one end of the load is connected to Point '*b*' at the supply's center-point. The total supply voltage V_{dc} (equal to V_{dc1} + V_{dc2} in Fig. 6) was 400 V. The power throughput was approximately 800 W at a load current i_L of 7.07 A. The switching frequency f_{sw} was 20 kHz for all the experimentation in this paper. Whilst this frequency is relatively high for a machine-drive application, it yields low perceived acoustic noise levels.

For comparison with the proposed technique, the circuit was also operated with high-quality IGBTs co-packaged with fast-recovery anti-parallel silicon diodes. These were used to replace the SJ MOSFETs, operating under the same conditions.

TABLE I. Main Circuit Device Data

*TR*1, 2	IPW60R041P6FKSA1
D_{s1}, D_{s2}	MBR3060PT
D_{ext1}, D_{ext2}	SCS220AEC
L	1 mH

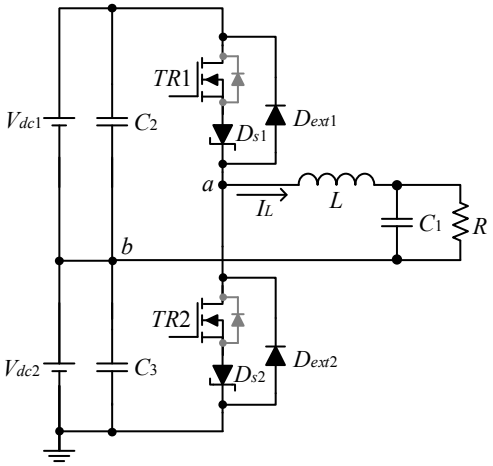


Fig. 6. SJ MOSFET-based single-phase inverter-leg.

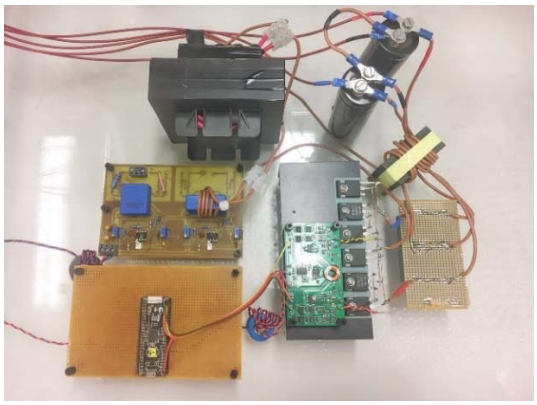


Fig. 7. Experimental hardware.

Fig. 8 shows the gate driver circuit in outline form. The input and enable signals, as shown in Fig. 4, are transmitted to the driver circuit of each power device via opto-couplers. Power for each driver circuit is transmitted by means of a flyback converter incorporating a small toroidal transformer configured with two secondary windings. Although the opto-couplers used have a

high output current capability, IXDN614 driver ICs were included to increase this if required during experimentation.

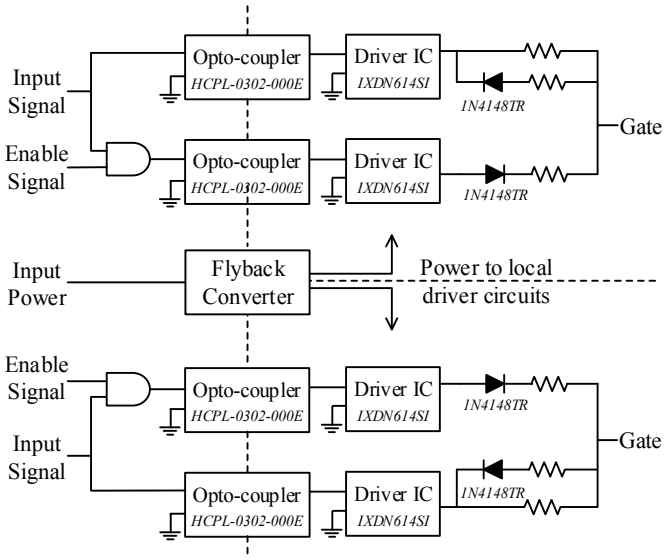


Fig. 8. Outline diagram of dual-mode gate driver used to drive two power devices in an inverter-leg.

Fig. 9. Dual-mode gate driver board.

The microcontroller used in the experimental rig, shown in the bottom-left corner of Fig. 7, is a CYPRESS PSoC 5LP, CY8C5888LTI-LP097 68-QFN type. The microcontroller generates two complementary 20-kHz PWM output signals based on a 50-Hz fundamental-frequency sinusoidal modulation signal. According to a pre-set SSR value, the microcontroller enables hard switching signal during the hard switching periods, and inhibits hard switching during the slow switching periods.

Since all the devices have been selected, the total power dissipation can be estimated. The circuit's operating conditions are: P=800 W, V_{dc}=400 V, f_{sw}=20 kHz. The peak fundamental output voltage V_{peak} is given by

$$V_{peak}=\frac{m}{2}V_{dc}=\frac{0.8}{2}\times 400=160\text{V} \tag{2}$$

and the RMS output voltage $V_{o(RMS)}$ is given by

$$V_{o(RMS)}=\frac{V_{peak}}{\sqrt{2}}=113\text{V}. \tag{3}$$

The output current I_o is calculated from

$$I_o=\frac{P}{V_{o(RMS)}}=7.08\text{A} \tag{4}$$

and I_o has a peak value I_{peak} of 10.01 A.

The forward voltage drop $V_{F(ext)}$ for D_{ext} is estimated at 1.06 V from the manufacturer's datasheet. The power dissipation P_{ext} in this device is given by

$$P_{ext}=V_{F(ext)}I_{peak}\left(\frac{1}{\pi}-\frac{V_o}{2V_{dc}}\right). \tag{5}$$

Data into (5) yields P_{ext} = 1.26 W.

The forward voltage drop $V_{F(s)}$ for D_s is estimated at 0.5 V from the manufacturer's datasheet. The power dissipation P_s in this device is given by

$$P_s=V_{F(s)}I_{peak}\left(\frac{1}{\pi}+\frac{V_o}{2V_{dc}}\right). \tag{6}$$

Data into (6) yields P_s = 2.62 W.

For the IPW60R041P6FKSA1 MOSFET, the on-state resistance $R_{DS(on)}$ is 41 mΩ. The conduction losses P_{cond} are given by

$$P_{cond}=R_{DS(on)}I_{peak}{}^2\left(\frac{1}{4}+\frac{4V_p}{3\pi V_{dc}}\right). \tag{7}$$

Data into (7) yields P_{cond} = 0.70 W.

Adding the results from (5), (6) and (7) yields a total power dissipation attributable to conduction losses of 4.68 W. We have not quantified the switching losses here, and these are assessed experimentally.

For the IKW20N60TFKSA1 IGBT, the on-state conduction voltage drop is estimated as $V_{CE(sat)}$=1.5 V from the manufacturer's datasheet. The conduction loss $P_{cond(IGBT)}$ in this device is given by

$$P_{cond(IGBT)}=V_{CE(sat)}I_{peak}\left(\frac{1}{\pi}+\frac{V_o}{2V_{dc}}\right). \tag{8}$$

Data into (8) yields P_s = 7.86 W.

The anti-parallel diode conduction loss $P_{cond(diode)}$ in the IKW20N60TFKSA1 IGBT is estimated using

$$P_{cond(diode)}=V_F I_{peak}\left(\frac{1}{\pi}-\frac{V_o}{2V_{dc}}\right) \tag{9}$$

where V_F is the estimated forward voltage drop of the diode. V_F was taken as 1.4 V from the manufacturer's datasheet. Putting the data into (9) yields $P_{cond(diode)}$ = 1.66 W. Adding $P_{cond(IGBT)}$ and $P_{cond(diode)}$ yields a total conduction loss of 9.52 W. If k_{sw} is the switching energy dissipation per Ampere, then the switching loss W_{sw} is given by

$$W_{sw}=\frac{2f_{sw}k_{sw}I_{peak}}{\pi}. \tag{10}$$

k_{sw} was estimated at 60 μJ/A, from the graphical data in the manufacturer's datasheet. Putting the data into (10) yields W_{sw} = 7.65 W. Adding the conduction and switching losses gives an expected loss in the IGBT-based circuit of 17.17 W.

V. Experimental Results

A. Results with Proposed Technique

Fig. 10 shows waveforms from the circuit in Fig. 6 when SSR=0.1. Fig. 10(a) shows base-frequency waveforms of i_L and V_{ab}.

In Fig. 10(b), i_L is transitioning through zero twice per switching cycle, so both $TR1$ and $TR2$ are operating in the synchronous conduction mode where soft-switching naturally occurs [6]. The slow switching mode is nonetheless needed at low i_L magnitudes to allow operation in the continuous conduction mode with bipolar switching prior to enabling unipolar switching. Figs. 10(c), (d), (e) show expanded waveforms of this operating mode, during which the rise- and fall-times of V_{ab} are measured as 103.0 ns and 132.0 ns respectively.

In Fig. 10(f), i_L is positive and above the threshold value at which unipolar switching is enabled, so $TR1$ is hard switching and $TR2$ is held off. Fig. 10(g) shows expanded waveforms in this mode. A negative-going overshoot voltage of approximately 52 V appears in V_{ab} when $TR1$ turns off. When $TR1$ is off, D_{ext2} is in its freewheeling period. On the positive-going transition of V_{ab}, the overshoot voltage reaches approximately 40 V.

In Fig. 10(h), i_L is negative and below the threshold value at which unipolar switching is enabled, so $TR2$ is hard switching and $TR1$ is held off. Fig. 10(i) shows expanded waveforms in this mode. A positive-going overshoot voltage of approximately 40 V appears in V_{ab} when $TR2$ turns off. When $TR2$ is off D_{ext1} is in its freewheeling period. On the negative-going transition of V_{ab}, the overshoot voltage reaches approximately 45 V. The rise time and the fall time of V_{ab} are 22.7 ns and 41.5 ns respectively.

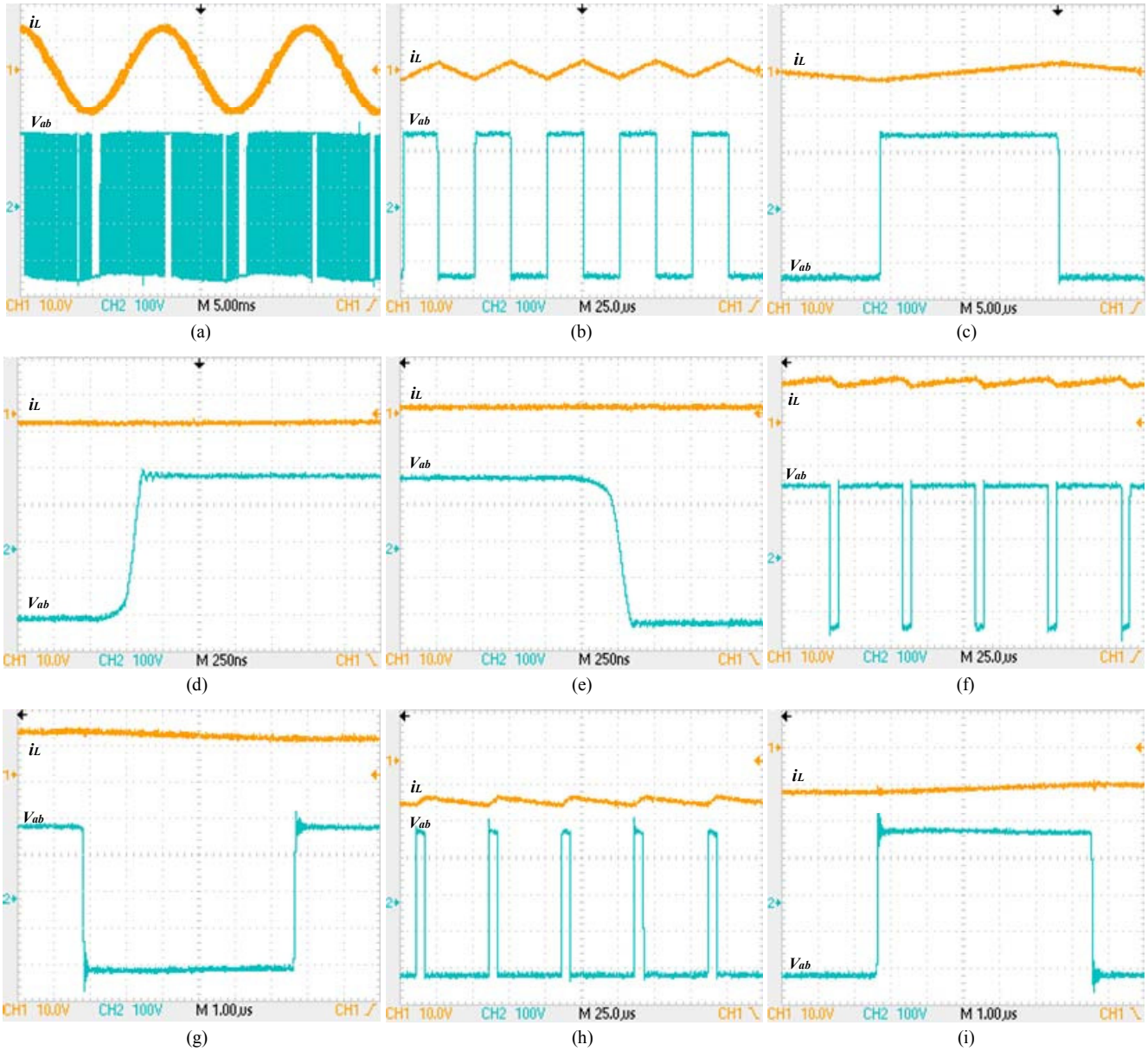


Fig. 10. Waveforms of i_L and V_{ab}.

B. Results with IGBTs

Fig. 11 shows the circuit in which the SJ MOSFETs and associated diodes in Fig. 6 were replaced by IGBTs co-packaged with fast recovery anti-parallel diodes. This circuit was operated under the same conditions as the circuit in Fig. 6. The IGBTs were driven with standard complementary hard-switching gate signals at 20 kHz.

Fig. 12 shows waveforms from the circuit in Fig. 11. In Fig. 10 (a), i_L reaches its highest peak; the rise time and the fall time of V_{ab} are 88.3 ns and 73.1 ns respectively. In Fig. 10(b), i_L reaches its lowest peak, the rise-time and fall-time of V_{ab} are 81.7 ns and 76.0 ns respectively.

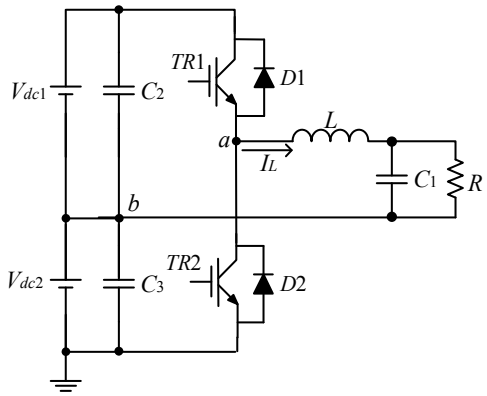
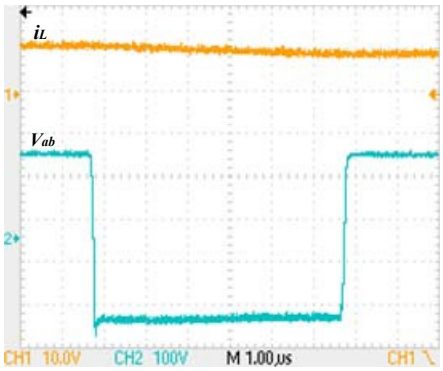
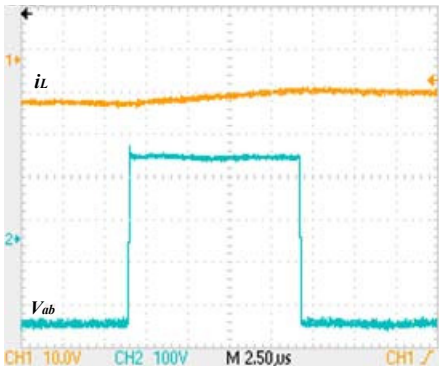


Fig. 11. IGBT-based single-phase inverter used for comparison with the proposed scheme.



(a)



(b)

Fig. 12. Waveforms of i_L and V_{ab}.

C. Thermal Superposition

In order to estimate the efficiencies of the circuits in Figs. 6 and 11, thermal superposition was used to measure the power dissipated by the power devices on the heatsink [12]. This technique is particularly suited for high efficiency measurements, such as those required in this paper. The main steps are as follows:

1. A DC current is passed through one or more of the power devices on the heatsink and the voltage across the devices is measured. As the current and voltage are DC quantities, the power dissipation P_d in the devices can be accurately determined.
2. The temperature D_{temp} of the heatsink above ambient is recorded when it has reached its thermal steady-state. The thermal resistance $R_{\theta hsa}$ of the heatsink to ambient is then calculated using

$$R_{\theta hsa} = \frac{D_{temp}}{P_d}. \tag{11}$$

3. The circuit under test is then run on the heatsink and the temperature rise above the ambient is recorded when it has reached its thermal steady-state. The estimated power dissipation P_{est} is given by

$$P_{est} = \frac{D_{temp}}{R_{\theta hsa}}. \tag{12}$$

As P_{est} has now been obtained, the percentage efficiency $\eta(\%)$ of the circuit can be calculated from

$$\eta(\%) = \frac{P_{in} - P_{est}}{P_{in}} \times 100 \tag{13}$$

where P_{in} is the input power drawn by the circuit under test. Table II gives experimental results. Prior to testing the experimental circuits, the $R_{\theta hsa}$ of the heatsink was determined at 1.60°C/W, and this value was used to subsequently determine P_{est}.

D. Total Harmonic Distortion (THD)

The total harmonic distortion (THD) in i_L is given in Table II. This was obtained by analysing the downloaded oscilloscope waveform data with the MATLAB Powergui FFT Analysis Tool. In the Analysis Tool Preferences, the fundamental frequency of the analyzed signal is 50 Hz and the maximum frequency evaluated by the FFT analysis is 15 kHz. Select the maximum frequency for THD computation equals to maximum frequency in FFT analysis. Then, the percentage THD in the input signal is calculated using:

$$THD(\%) = \frac{\sqrt{\sum_{i=2}^{n} M_i^2}}{M_1} \times 100 \tag{14}$$

where M_i is the root mean square (RMS) value of the harmonic magnitude corresponding to the i^{th} harmonic order.

Fig. 13 shows the harmonics in the output current of the SJ MOSFET single-phase inverter running with an SSR ratio of 0.1. Fig. 14 shows thermal images of the SJ MOSFET-based single-phase inverter, again with SSR=0.1.

TABLE II. EXPERIMENTAL RESULTS

Circuit configuration	SSR ratio	D_{temp} (deg C)	Input voltage (V)	Input current (A)	Input power (W)	Power dissipation (W)	Estimated efficiency (%)	THD (%)
SJ MOSFETs in proposed circuit in Fig. 6, with proposed dual-mode switching technique implemented.	0.1	18.00	400	2.13	852	11.26	98.68	3.95
	0.2	17.57	400	2.06	824	10.98	98.67	5.00
	0.3	17.87	400	2.04	816	11.18	98.63	3.91
	0.4	17.27	400	2.01	804	10.80	98.66	3.22
	0.5	18.13	400	2.02	808	11.34	98.60	4.14
	0.6	19.55	400	2.01	804	12.23	98.48	4.41
	0.7	20.53	400	1.98	792	12.84	98.38	4.64
SJ MOSFETs in circuit in Fig. 6, with complementary slow switching implemented under all conditions.	1	27.27	400	1.88	752	17.05	97.73	4.04
IGBTs in circuit in Fig. 11 with standard complementary hard switching implemented.	—	33.93	400	2.13	852	21.22	97.51	4.76

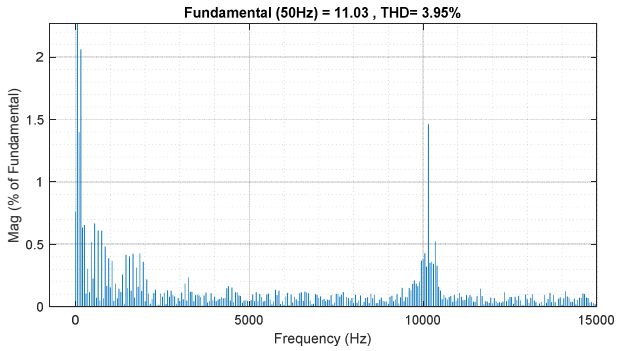


Fig. 13. Harmonics in output current of SJ MOSFET-based single-phase inverter with SSR=0.1.

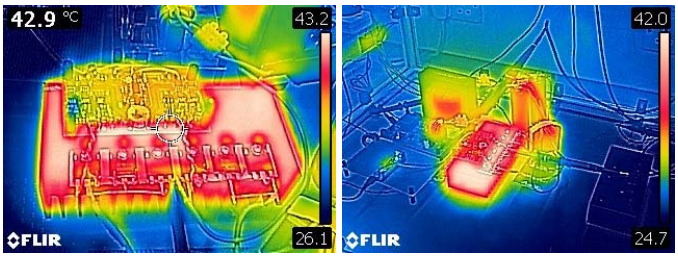


Fig. 14. Thermal images of SJ MOSFET-based single-phase inverter when running with SSR=0.1.

Fig. 15 shows the efficiency results from Table II presented in a bar chart format. When the dual-mode technique is applied to the SJ MOSFET-based inverter-leg, the efficiency shows an increasing trend as the SSR ratio is reduced. The highest efficiency reaches approximately 98.7% as the SSR ratio approaches 0.1, while the efficiency of the IGBT-based inverter-leg is only 97.5%.

Fig. 16 shows the THD analysis results from Table II presented in a bar chart format. With the maximum frequency for THD computation set at 15 kHz, the THD in the output current when using SJ MOSFET-based inverter-leg at an SSR ratio of 0.1 is 3.95%. The THD in the output current when using the IGBT-based inverter-leg is 4.76%. Applying the dual-mode technique can improve efficiency while exhibiting a similar output current quality.

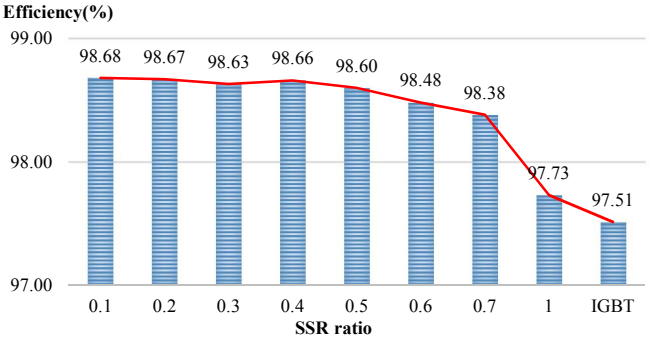


Fig. 15. Efficiency results.

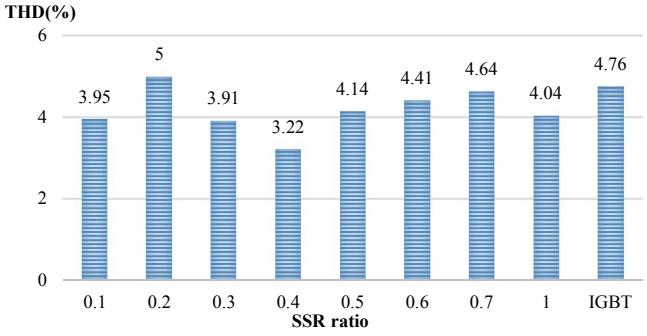


Fig. 16. THD results.

VI. DISCUSSION

The following points are noted.

- The circuitry is intended for use in machine drive applications, and the quoted efficiencies therefore do not account for any choke losses.

- The inverter-leg is operated under open-loop control with gate drive signals generated by the microcontroller. A higher THD is therefore expected than if the circuit were to be operated under closed-loop current control, as is normally the case in typical applications such as machine control.
- The load was at a power factor close to one. No current sensing was incorporated into the proposed scheme. With variable power factors, current sensing would be required to inform the control circuitry which of the three modes, as defined in Fig. 5(a), the circuitry should be operating in.
- Silicon Schottky diodes were used in locations D_{s1} and D_{s2}. Whilst this is a simple arrangement, and was used for experimentation, losses are nonetheless incurred by the forward voltage drop of the diode when in conduction. An alternative solution is to replace the diodes with low-voltage anti-series MOSFETs [13]. These MOSFETs can readily be controlled such that they conduct in reverse as synchronous rectifiers when a drain current is flowing into the main MOSFETs, thereby further reducing losses.

VII. Conclusion

The highly non-linear output capacitance and reverse recovery characteristic of the super-junction MOSFET intrinsic diode have been addressed for the device when used in voltage source converters. A dual-mode switching control technique was proposed to address the disadvantages of the output capacitance. This technique operates in conjunction with intrinsic diode deactivation circuitry. The technique was demonstrated in an 800-W inverter-leg configuration operating from a 400-V DC supply voltage and switching at 20 kHz. The full-load efficiency reached approximately 98.7%, and no forced cooling was needed.

References

[1] S. Jahdi *et al.*, "Temperature and switching rate dependence of crosstalk in Si-IGBT and SiC power modules," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 849-863, Feb. 2016.

[2] F. Udrea, G. Deboy, and T. Fujihira, "Superjunction power devices, history, development, and future prospects," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 720-734, Mar. 2017.

[3] L. Lorenz, G. Deboy, and I. Zverev, "Matched pair of CoolMOS transistor with SiC-Schottky diode - advantages in application," *IEEE Trans. Ind. Appl.*, vol. 40, no. 5, pp. 1265-1272, Sep. 2004.

[4] G. Deboy, O. Haeberlen, and M. Treu, "Perspective of loss mechanisms for silicon and wide band-gap power devices," *CPSS Trans. Power Electron. and Appl.*, vol. 2, no. 2, pp. 89-100, Jun. 2017.

[5] P. Sun, C. Liu, J.-S. Lai, C.-L. Chen, and N. Kees, "Three-phase dual-buck inverter with unified pulsewidth modulation," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1159-1167, Mar. 2012.

[6] W. Yu, H. Qian, and J.-S. Lai, "Design of high-efficiency bidirectional DC–DC converter and high-precision efficiency measurement," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 650-658, Mar. 2010.

[7] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat interleaved triangular current mode (TCM) single-phase PFC rectifier," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 873-882, Feb. 2014.

[8] J. Zhang and J.-S. Lai, "A synchronous rectification featured soft-switching inverter using CoolMOS," in *Proc. IEEE 21st Annu. Appl. Power Electron. Conf. and Expo.*, Dallas, TX, USA, pp. 810-815, Mar. 2006.

[9] H. Bai *et al.*,"Design of an 11 kW power factor correction and 10 kW ZVS DC/DC converter for a high-efficiency battery charger in electric vehicles," *IET Power Electron.*, vol. 5, no. 9, pp. 1714-1722, Nov. 2012.

[10] A. Hopkins, P. P. Proynov, N. McNeill, B. H. Stark, and P. Mellor, "Achieving efficiencies exceeding 99% in a super-junction 5kW DC-DC converter power stage through the use of an energy recovery snubber and dead time optimization," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7510-7520, Sep. 2017.

[11] M. Rana and N. McNeill, "High-frequency and high-efficiency bidirectional DC-DC converter for electric vehicle supercapacitor systems," in *Proc. IET 6th Hybrid Electric Vehicles Conf.*, London, UK, Nov. 2016.

[12] B. W. Williams, "Power Electronics: Devices, Drivers, Applications, and Passive Components," 2006.

[13] D. B. DeWitt, C. D. Brown, and S. M. Robertson, "System and method for reducing body diode conduction," US Patent No. 7508175 (B2), 24 Mar. 2009.