An improved Alternate Arm Converter for HVDC applications

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***Abstract*—This paper presents an Improved Alternate Arm Converter where the director switches of the upper and lower arms of the conventional alternate arm converter are rearranged as a conventional two-level converter. The flying capacitor (i.e. the capacitor across the director switches) in each phase leg facilitates seamless current commutation between the upper and lower arms, and eliminates the need for the main dc-link capacitor across the positive and negative dc rails. The modifications introduced to the power circuit necessitate the proposed converter to adopt a new operating regime that ensures simultaneous conduction of the upper and lower arms of each phase leg as in the modular multilevel converter. The operating principle, modulation methods of the proposed converter, and sizing of its main components are described in detail, and substantiated by simulations.**

***Index Terms*—HVDC, Multilevel converters, Voltage Source Converter**

I. Introduction

Efficient transmission systems are critical for connection of weak ac networks and remote offshore wind farms [1]. Existing multilevel voltage source converter (VSC) based HVdc transmission systems have received universal acceptance from the power industry [2], [3], because they satisfy the requirements of high efficiency and high power quality on both ac and dc sides, while providing internal fault management which is critical for ensuring continuous operation during cell failure [4]–[6].

Reverse-blocking converters are increasingly important as they provide a means to ride-through dc short-circuit faults, with only short periods of power interruption between the connected ac grids. This is achieved without significant impact on voltage stability as the reverse-blocking converters can prevent or control the ac-side contribution to the dc fault current. Hence, reactive power within connected ac grids will no longer flow uncontrollably. In multi-terminal HVdc networks which utilize reverse-blocking converters, dc-link voltage remains at zero after fault clearance, as long as the converter terminals remain blocked. This clearly provides the opportunity for complete replacement of expensive dc circuit breakers with lower-cost dc disconnectors [7].

At present, there are two competing approaches to the realization of dc fault blocking converters. The first approach incorporates Full-Bridge (FB) cells into variants of the Modular Multilevel Converter (MMC), namely the FB MMC and Mixed-cell MMC (MC-MMC) [8]. This approach is attractive due to its efficiency and power quality [9]. However, it is well suited for applications with confined space, such as offshore wind farms. The second approach employs so-called hybrid converters, such as the Alternate Arm Converter (AAC) [10] that combines the basic operation of an MMC or cascaded multilevel converter with a conventional two-level converter. The AAC has, for example, fewer cells than the equivalent MMC, making it suitable for applications with reduced space requirements. However, due to its fundamental operating regime, it has inferior power quality and performance during dc and asymmetric ac faults [11]. Most of these hybrid topologies lack the power quality of an MMC and require filters, thereby making the claim of total converter station footprint reduction debatable.

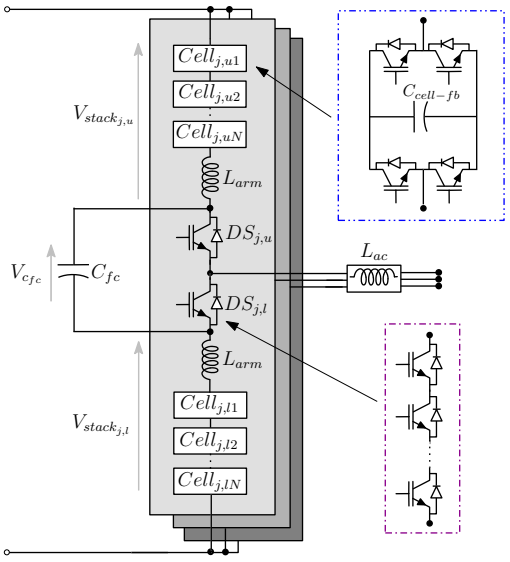


Fig. 1 Phase representation of IAAC.

This paper presents an Improved Alternate Arm Converter (IAAC) that utilizes FB chain-links and a Flying Capacitor (FC) across the upper and lower arm director switches of each phase leg to mimic the fundamental operation of the conventional three-level flying capacitor converter [12]. The

FB chain-link in each arm of the IAAC is rated for a fraction of the full dc-link voltage, while FC based director switches are rated for a half of the dc-link voltage. The operating principle, modulation and energy management of the FB chain-links and FC are described in detail. It is shown that the proposed IAAC generates high-quality sinusoidal output, with similar operation to a converter previously proposed by the authors [13]. Additionally, the arm currents of the IAAC do not exhibit abrupt changes, irrespective of load power factor. These characteristics contribute to a significant improvement in the quality of the ac and dc-side waveforms generated by the proposed converter, making the need of ac and dc filtering unnecessary.

The paper is organized as follows: Section II describes the theoretical principles that underpin the operation and modulation of the proposed converter. Section III presents illustrative simulation results to corroborate the theoretical analysis. Section IV presents the conclusions, where the main findings of this research are summarized.

II. Proposed Converter

A. Converter design and operation

Fig.1 shows one phase leg of the proposed IAAC topology. Each arm of the IAAC consists of series-connected FB cells (FB chain-link) and a Director Switch (DS). A flying capacitor is connected across the director switches of the upper and lower arms of each phase leg. The FC in each phase leg is rated for half of the dc-link voltage V_{dc}. The modulation of the proposed IAAC must therefore utilize the FC of each phase leg to alternatively support the upper and lower arms, principally during the synthesis of voltage levels above $\frac{V_{dc}}{2}$. In contrast, the FB chain-link of each arm is utilized to synthesize voltage levels below $\frac{V_{dc}}{2}$. To extend the modulation index linear range to 1.27 $p.u.$ as in the conventional AAC, the FB chain-link of each arm of the IAAC must be sized to block $\frac{2}{\pi}V_{dc}$.This design extends the voltage generation capability of the FB chain-link of each arm to $\frac{2}{\pi}V_{dc}$, and offers extra redundancy for voltage synthesis in the voltage range between 0 and $\frac{2}{\pi}V_{dc}$, which could be used to ensure the energy balance of the FC and FB cell capacitors. For over-modulation, the ac voltage reference m_{ref_j} that originates from the controller has to be modified as in (1).

$$m_{ref_j} = \frac{4}{\pi} \cdot M \cdot cos(\omega t + \delta_j) \tag{1}$$

Subsequently, the ac reference is normalized for setting the total arm voltages $m_{norm_{j,k}}$ as described in (2).

$$m_{norm_{j,k}} = \frac{1 \pm m_{ref_j}}{2} \tag{2}$$

The normalized reference is manipulated for modulating the FB chain-link $m_{stack_{j,k}}$ and for DS operation $S_{DS_{j,k}}$, as is described in (3) and (4). The modulating voltage references are illustrated in Fig. 2.

$$m_{stack_{j,k}} = \begin{cases} m_{norm_{j,k}} - 0.5 & \text{if } m_{norm_{j,k}} \geqslant 0.5 \\ m_{norm_{j,k}} & \text{if } m_{norm_{j,k}} < 0.5 \end{cases} \tag{3}$$

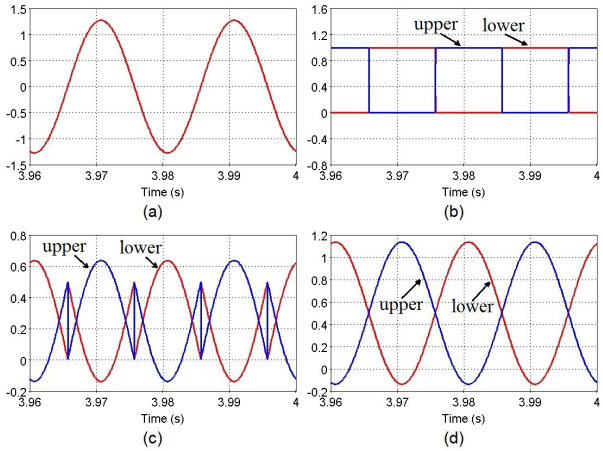


Fig. 2: Modulation voltage references (p.u.) (a) ac voltage, (b) director switches (c) FB chain-link, (d) normalized total arm voltage reference.

$$S_{DS_{j,k}} = \begin{cases} 1 & \text{if } m_{norm_{j,k}} \geqslant 0.5 \\ 0 & \text{if } m_{norm_{j,k}} < 0.5 \end{cases} \tag{4}$$

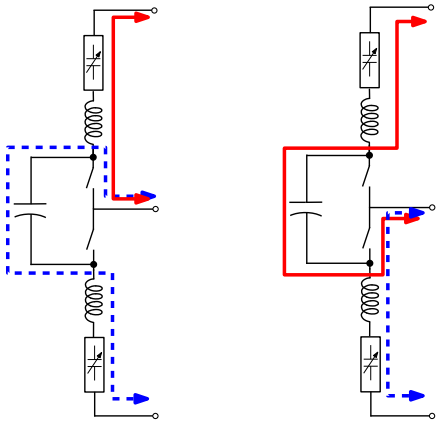
Conventional capacitor voltage balancing techniques such as sorting, tolerance band and cell reference modulation methods can be applied to the chain-links. FC voltage balance is achieved by observing arm current polarity and manipulating the director switches, taking into account the voltage magnitude across the FC. Fig. 3 shows the conduction paths in the upper and lower arms of the IAAC as it synthesizes different output phase voltage levels for positive output phase current (when output current direction is from the converter toward the ac grid). Notice that the two arms of the IAAC conduct simultaneously, and that turning the arm DS on and off bypasses and inserts the FC. The DS in each phase leg operate in a complementary manner, i.e. turning on the upper arm DS precludes the lower arm DS from being turned on). Furthermore, turning on the upper arm DS inserts the FC into the lower arm, and this increases the blocking voltage of the lower arm to 1.137 V_{dc}, whilst the blocking voltage of the upper arm remains at $\frac{2}{\pi}V_{dc}$. This means that with complementary operation of upper and lower arms of the IAAC, as in the MMC case, the entire voltage in the upper arm will be synthesized by the FB chain-link, while the voltage in the lower arm will be synthesized by the combination of FB chain-link and FC. The opposite is true when the lower arm DS is turned on.

The total inertia H_{IAAC} of the converter is described as:

$$H_{IAAC} = 3\frac{E_{phase}}{S} \tag{5}$$

$$E_{phase} = 2\ E_{chain} + E_{fc} \tag{6}$$

where E_{chain} and E_{fc} are the energy stored in chain-link and FC respectively. The stored energy per IAAC is equivalent to inertia constant H_{IAAC} which is in the range of 30-40 kJ/MW.



(a) (b)

Fig. 3: Upper (solid line) and lower (dotted line) arm currents path (a) upper DS conduction, (b) lower DS conduction

The total arm capacitance $C_{arm_{req}}$ must be sized to cater for stored energy requirements E_{chain} and E_{fc} and is calculated according to the chain-link and FC equivalent capacitances, C_{chain} and C_{fc} respectively, as shown in (7).

$$C_{arm_{req}} = \frac{C_{chain} \cdot C_{fc}}{C_{chain} + C_{fc}} \tag{7}$$

Since the blocking voltage of the FB chain-link is $\frac{2}{\pi}V_{dc}$, the number of FB cells per chain-link N_{FB} is described as:

$$N_{FB} = \frac{2\ V_{dc}}{\pi \cdot V_{cell}} \tag{8}$$

where V_{cell} is the voltage across an FB cell.

B. Converter Analysis

The cell capacitor current in each individual cell can be described in terms of arm current $i_{j,k}$ and the switching function $s_{cell-n_{j,k}}$ {-1,0,1} as stated in (9):

$$i_{cell-n_{j,k}} = (1 - s_{cell-n_{j,k}}) \cdot i_{j,k} \tag{9}$$

Each arm voltage (11) is formed by the summation of individual cell voltages $v_{cell-n_{j,k}}$ as described in (10):

$$v_{cell-n_{j,k}}(t) = \frac{1}{C_{cell}} \cdot \int_{t-\Delta t}^{t} \left(i_{cell-n_{j,k}}(t) \right) dt \tag{10}$$

where Δt is the time step of the discrete integration.

$$v_{stack_{j,k}} = \sum_{i=1}^{N_{cell}} \left[(1 - s_{cell-n_{j,k}}) \cdot v_{cell-n_{j,k}} \right] \tag{11}$$

The voltage across the dc link can be expressed in terms of the instantaneous upper and lower arm voltages ($v_{j,u}$, $v_{j,l}$) of the same phase leg, as shown in (12):

$$v_{arm_{j,k}} = v_{stack_{j,k}} + V_{fc} \cdot (1 - S_{DS_{j,k}}) \cdot dV_{fc} \tag{12}$$

where dV_{fc} is the voltage ripple across FC. DS has to be sized according to the voltage which is described in (13).

$$V_{DS} = \frac{V_{dc}}{2} + dV_{fc} \tag{13}$$

Consequently the dc voltage V_{dc} can be defined as:

$$V_{dc} = v_{arm_{j,u}} + v_{arm_{j,l}} \tag{14}$$

The following voltage equations can be defined:

$$e_j = -v_{j,u} - \frac{L_{arm}}{2} \cdot \frac{di_{j,u}}{dt} + L_{ac} \cdot \frac{di_{j,ac}}{dt} + \frac{V_{dc}}{2} \tag{15}$$

$$e_j = v_{j,l} + \frac{L_{arm}}{2} \cdot \frac{di_{j,l}}{dt} + L_{ac} \cdot \frac{di_{j,ac}}{dt} - \frac{V_{dc}}{2} \tag{16}$$

where L_{arm} and L_{ac} are the arm and ac-side inductances respectively (as shown in Fig. 1) and e_j is the ac-side grid phase voltage. The upper and lower arm currents in each phase can be expressed by (17) and (18) respectively:

$$i_{j,u} = \frac{i_{j,ac}}{2} + i_{j,diff} \tag{17}$$

$$i_{j,l} = -\frac{i_{j,ac}}{2} + i_{j,diff} \tag{18}$$

where $i_{j,ac}$ and $i_{j,diff}$ are the ac output phase and differential currents respectively. Current $i_{j,diff}$ flows through the upper and lower arms and can be defined by (19):

$$i_{j,diff} = \frac{i_{j,u} + i_{j,l}}{2} = i_{j,dc} + i_{j,cc} \tag{19}$$

$$i_{dc} = i_{a,dc} + i_{b,dc} + i_{c,dc} \tag{20}$$

where $i_{j,dc}$ and $i_{j,cc}$ are the dc and circulating currents respectively, and the latter occurs due to the unbalanced voltages (21) between the upper and lower arms in each phase

$$v_{j,diff} = \frac{V_{dc}}{2} - v_{j,u} = -\frac{V_{dc}}{2} + v_{j,l} = \frac{v_{j,l} - v_{j,u}}{2} \tag{21}$$

where $v_{j,diff}$ is the differential voltage between the upper and lower arms.

From the preceding analysis it is evident that, in contrast to the AAC, the proposed converter has uninterrupted, symmetrical arm currents.

C. Converter power losses

The semiconductor power losses are calculated using a method previously described by the authors [9], and are compared in Table I for several state of-the-art converters. The table also compares the numbers of semiconductor devices in each converter, with reference to the HB-MMC. Observe

TABLE I: Converters' efficiency

	Cond. Losses [kW]	Sw. Losses [kW]	Semiconductors ratio
HB-MMC	4749	1136	1
MC-MMC	8166	1188	1.50
AAC	8535	1686	1.640
FC-AAC	7324	1973	1.525

that the IAAC has reduced conduction losses compared to the AAC, whilst the IAAC switching losses are increased due to hard-switching of the DS. However, the IAAC has higher efficiency, primarily due to reduced number of semiconductors.

III. Simulations

This section assesses the viability of the IAAC when it is connected to a stiff dc source and a strong ac network, and operates in active and reactive power control mode, with decoupled dq current controller [9]. The simulations were based on the parameters shown in Table II.

TABLE II: Specifications

S [MVA]	1045
V_{DC} [kV]	640
V_{chain}/V_{DS}[kV]	388/375
V_{grid}/V_{conv} [kV]	400/500
Arm inductance [%]	15
Transformer reactance [%]	18
Chain-link capacitance [μF]	54
FC capacitance [μF]	27
N_{cell}	255

Fig. 4(a) to (c) show the FB chain-link, DS and total arm voltages. The total arm voltages are synthesized from the FB chain-link and DS voltages, using the over-modulation mentioned in Section IIA. The FB chain-link provides voltages to enable arm voltages below zero and above V_{dc}. In contrast to the conventional AAC the DS voltages of the IAAC exhibit fast and abrupt switching, which indicates hard switching and which necessitates the series connection of IGBTs in the DS. The need for series connection might be considered as a limitation, as the capability to cater for series connection at hundreds of kV is not widely available. The arm currents in Fig. 4(d) do not exhibit high di/dt as a result of the current path, shown in Fig. 3, available under all operating conditions. Additionally, a second harmonic component appears in the arm currents similar to that of the conventional MMC. Fig.4(e) and (f) respectively show that the chain-link total capacitor voltage and the FC voltage settle at $\frac{V_{dc}}{2}$ and exhibit ripple of $\pm 8\%$. The chain-link capacitor ripple is influenced by the charging and discharging process which depends on arm current sign and the positive/negative voltage insertion of the FB cells. FC capacitor voltage follows the charging and discharging profile according to the ac current sign. Fig. 4(g) and (h) respectively show high-quality ac phase voltage and line current. Finally, Fig. 4(j) shows the high-quality dc current with $\pm 1.5\%$ ripple, indicating that no dc filter is required. The 100Hz harmonic current in each FC is reflected as a low magnitude 300Hz ripple on the dc current, which can be further reduced by increasing the value of FC.

Fig. 5 illustrates the PQ capabilities of the IAAC. The converter successfully operates at various operation points following the active and reactive power, while there is good match between the ac and dc power transfer. The spikes observed on the active power trace at t=2s and t=3s are due to the rapid reactive power reversal demand.

Fig. 6 demonstrates the dc blocking capability of the IAAC during a pole-to-pole dc fault. The fault is initiated at t=2s

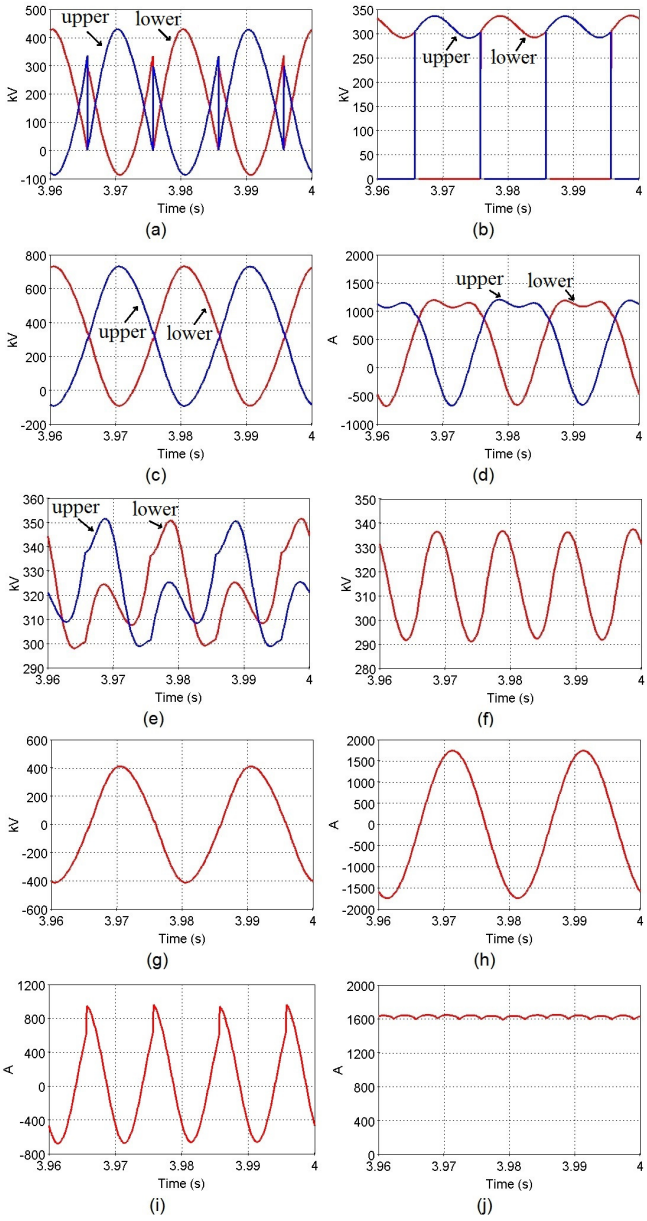


Fig. 4: IAAC results: (a) FB chain-link voltages, (b) DS voltages, (c) arm voltages, (d) arm currents, (e) FB chain-link total capacitor voltages, (f) FC voltage, (g) ac phase voltage, (h) ac current, (i) FC current, (i) dc current.

and immediately dc voltage collapses, while the dc current rises until arm over-current detection activates the converter's

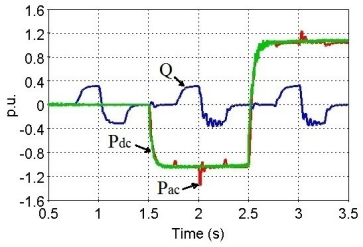


Fig. 5 Active and reactive power capabilities of IAAC

blocking state. It should be noted that due to the absence of any capacitive dc filter, the IAAC dc fault current is reduced compared to that of the conventional AAC with short-overlap control [11]. The converter's blocked state is illustrated in the arm voltages of Fig. 6(c). The arm and FC capacitor voltages maintain constant values as arm current flow has been interrupted.

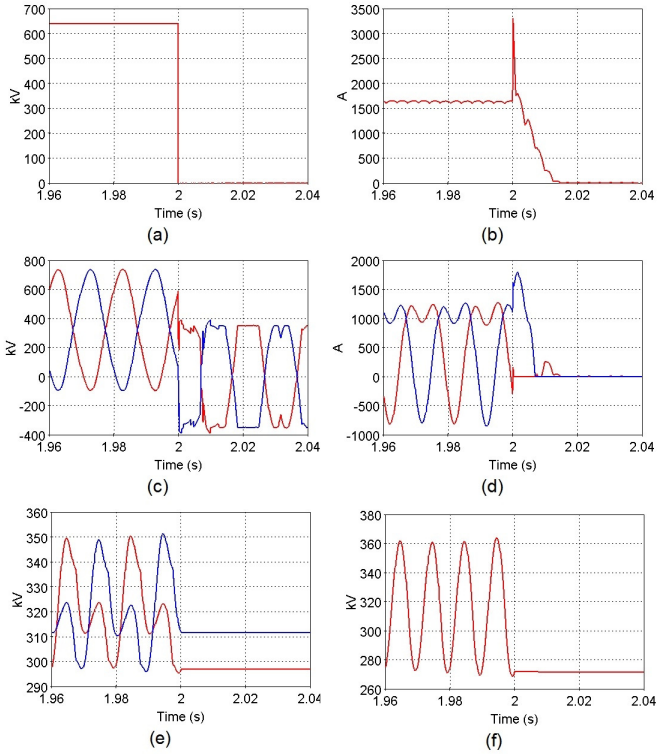


Fig. 6: dc fault blocking capability (a) dc voltage, (b) dc current, (c) Arm voltages, (d) arm currents, (e) FB chain-link total capacitor voltages, (f) FC voltage.

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IV. CONCLUSIONS

This paper proposes an IAAC that offers compact design, high-quality ac and dc side waveforms, and similar semiconductor losses when compared to AAC and MC-MMC topologies. The proposed IAAC replaces the large dc link capacitors required by the conventional short-overlap controlled AAC by three flying capacitors (one per phase leg and each rated for half dc link voltage) that do not discharge during dc faults. The theoretical development and presented, and simulation results show that the proposed IAAC is promising for HVDC applications. The main features of the IAAC are:

- Good efficiency with a reduced number of semiconductors compared to the AAC.
- Continuous arm current operation, which removes the need for dc filters without affecting the efficiency and the complexity of the converter.

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