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# Stretching in Time of GaN Active Gate Driving Profiles to Adapt to Changing Load Current

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***Abstract* — Active gate driving, where the gate signal is actively profiled, has been shown to reduce EMI, overshoot, and switching loss, in silicon power converters. Recently, much faster gate drivers with the ability to profile at a 100 ps resolution have been reported, which has opened up the possibility of actively driving emerging wide-bandgap devices. This could allow Gallium Nitride (GaN) and Silicon Carbide (SiC) FETs to be switched faster than is currently possible, as unwanted switching features such as current ringing at turn-on could be eliminated. However, these drivers have previously only been demonstrated with pre-programmed gate profiles that have been optimized at certain operating conditions, whereas converters typically operate in a range of conditions. In this paper, some limitations of using fixed gate profiles on GaN FETs are reported for the first time, and a new method of profile adaptation is demonstrated. First, the gate profiles in a 400 V GaN bridge-leg are optimized to minimize current ringing at turn-on for a given load current. Then, the load current is varied, showing that the gate signal profile remains close to optimal for ±20% changes in current. Also, over a larger range of at least ±35%, the profiled waveform performs better than a non-profiled gate waveform. It is then demonstrated that by slightly reducing the driver's internal clock frequency with increasing load current, the profile is re-optimized for new load currents. It is concluded that driver clock frequency adaptation may be a means of adapting gate profiles to load current variation and possibly also to temperature variation.**

**Keywords** — ***Active Gate Driving, Arbitrary Waveform Gate Driver, Dynamic Output Resistance Gate Driver, GaN FET, GaN Gate Driver.***

## I. Introduction

Active gate drivers allow switching waveforms of a power electronic converter, e.g. the drain current of a power device, to be "shaped" via the gate signal during the switching transition. For example, turn-on ringing under standard gate driving, as illustrated in Fig. 1(a), can be transformed into a waveform with the same switching speed but with less ringing, Fig. 1(b), and therefore less EMI. The gate signal profile can be set in advance of converter operation (open loop), or sensing mechanisms can be used in a closed loop feedback or adaptive configuration to allow the circuit to react continuously to variations in operating parameters, such as load current. Closed-loop and adaptive active gate driving is well documented for Silicon (Si) power devices. However, due to the short switching time and high slew rates of a Gallium Nitride (GaN) power device, during kilowatt scale power circuit switching transitions, closed-loop or adaptive active gate driving is more challenging.

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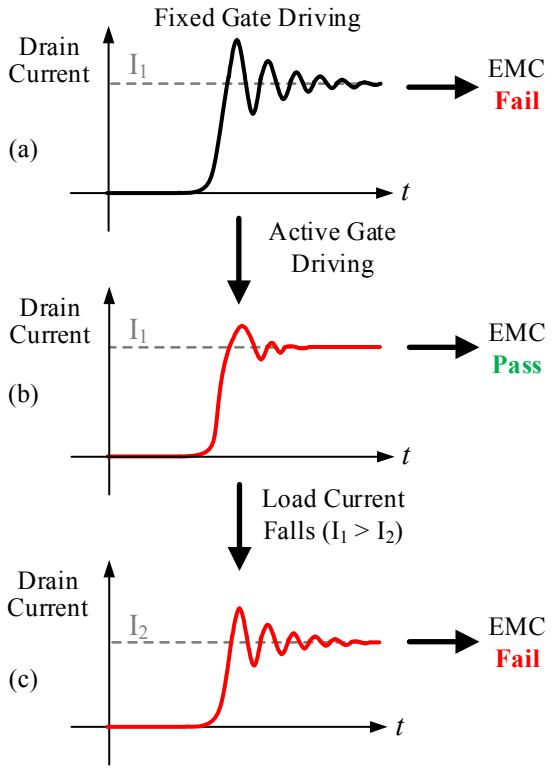


Fig. 1. Illustration of a typical conventional gate drive turn-on current pulse (a) compared to the the benefit offered by open-loop active gate driving (b), and the impact operating point can have on power device drain current in the actively driven case.

Active gate driving of GaN FETs can be categorised by the capabilities of the driver. Single-step closed-loop drivers for GaN have been demonstrated that are able to help combat EMI [1], [2]. Drivers capable of three or more steps have also been shown to be capable at further reducing EMI and targeting overshoot in switching waveforms [3], [4]. A profiling flexibility with even greater time resolution during the switching transition has been shown to enable the reduction of crosstalk and oscillations [5], in addition to overshoot and EMI [5]-[8]. However, reported drivers with this very high time resolution, are currently open-loop with pre-programmed gate driving profiles. These profiles are optimised under specific operation conditions (e.g. fixed current, temperature, and DC voltage levels) and therefore they may not be optimal or even safe at other operating points, as illustrated in Fig. 1(c).

Therefore, this paper investigates this open-loop, high-resolution category of drivers under changing load current. The

aim is to find out when gate profiles need to be updated, and whether there are computationally viable means of doing so. This is a critical step towards being able to deploy active gate driving in real-world GaN converters that operate effectively under varying operating conditions.

The paper is organised as follows: Section II describes the methodology and equipment used to determine the performance of the active gate driving strategy being used in this work as load current changes. Section III discusses the results gathered at the two load points and how the active gate driving strategy was optimised. This is followed by a demonstration of the impact that changing load has upon the active driving strategy, with comparison to unshaped and comparable fixed-strength gate driving. Section IV provides conclusions and further discussion on the finding of this work, highlighting the most important trends and their potential impact to active gate driving, in particular their importance to closing the loop on high speed multi-step active gate driving.

## II. Method and Test Setup

Fig. 2 shows the method used in this work to investigate sensitivity to changes in nominal load current. Trends are determined based upon the ringing introduced by the imposed changes to the operating point.

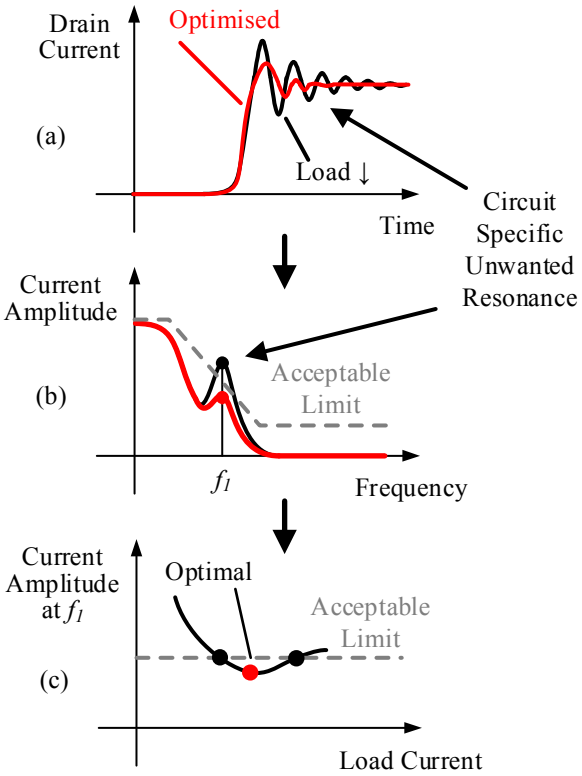


Fig. 2. Example drain-current switching waveforms in the time (a) and frequency (b) domains, showing ringing at frequency $f_1$. Open-loop active driving reduces the ringing to an acceptable level, but load current variations (c) cause ringing to once again breach this limit.

The GaN FET bridge leg, comprising a pair of GaN Systems GS66508P 650 V GaN FETs, used for this work is configured as shown in Fig. 3. It is configured for boost mode operation where load current flows into the switch node. The bridge leg is driven with double-pulse waveforms according to the desired nominal load current flowing in the load inductor, $L_o$ (300 µH). The DC Link, $V_{IN}$, is maintained at 400 V and switching was optimised at a load current, $i_L$, of 10 A, about which it is then varied.

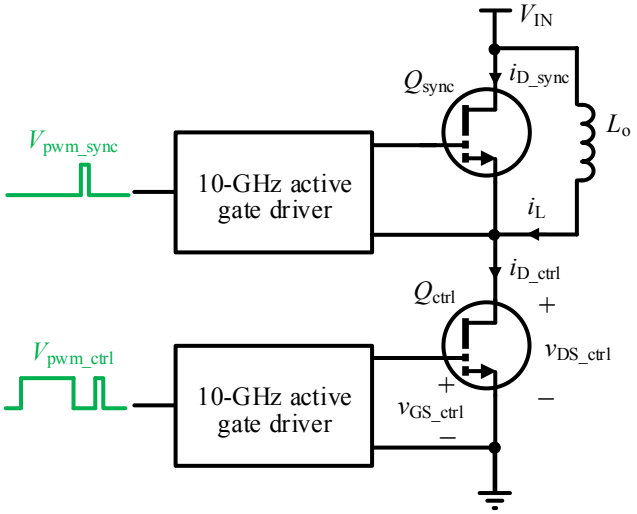


Fig. 3. Diagram of the power circuit configuration used for this work.

Both power devices are driven with active gate drivers (in open loop mode) although the driver for the upper device, $Q_{sync}$, is not performing any profiling and the output of the driver is set to a constant drive strength for turn-on and turn-off transients (i.e. it is acting as a conventional driver). Details of the specific driver architecture, support and programming hardware are provided in [5]-[7].

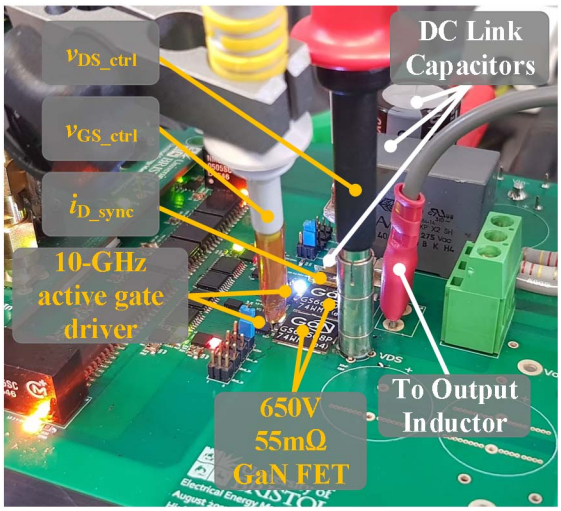


Fig. 4. Photograph of power circuit used for this work indicating major components and probe locations

Fig. 4 illustrates the major components of the experimental hardware as shown in Fig. 3 and their relative proximity to each other. This compact layout is critical for realising the high performance offered by GaN power devices and allowing sub-ns active gate profiling to be as effective as possible.

### A. Experimental Hardware

Fig. 5 shows a schematic of the experimental setup detailing specific instrumentation and equipment used where appropriate. The power circuit current and voltage waveforms are captured by a Rhode & Schwarz RTO1044 4 GHz 10 GSa/s oscilloscope. The chosen operating mode allows for voltage measurements to be ground-referenced as capturing floating reference measurements of high voltages at the bandwidth required is particularly challenging. As indicated in Fig. 5, the gate-source voltage, $vGS_{ctrl}$, of the low side GaN FET, $Q_{ctrl}$, is probed directly by a Rhode and Schwarz RT-ZP10 10:1 500 MHz probe with spring tips for both signal and ground directly probing the gate and source terminals. The drain-source voltage, $vDS_{ctrl}$, is measured by a PMK HV1000 100:1 400 MHz passive voltage probe connecting through a coaxial PCB-mounted probe adapter to the drain and source terminals of the low-side device. These connection techniques ensure that any loop inductance, loading effects, and noise paths introduced are minimized, which is essential for making high bandwidth measurements.

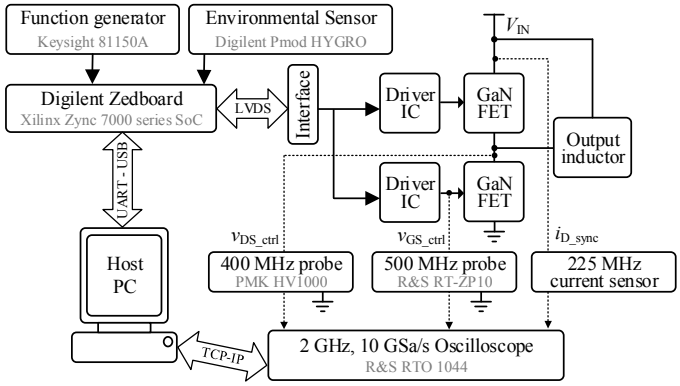


Fig. 5. Top level configuration diagram of the experimental hardware and support equipment.

The drain current of the high-side GaN FET, $iD_{sync}$, is measured by a non-invasive and floating current sensor with a bandwidth of 225 MHz. The load inductor capacitance has been measured to be small and so the load current during a switching transient is assumed to be constant. This allows the low-side device current, $iD_{ctrl}$, to be inferred and introduces low insertion inductance (0.2 nH); a feature that is particularly important so that it has the least influence on the inductance-sensitive GaN switching transient. The GaN Systems GS66508P power devices posses a kelvin source connection meaning the gate loop current is already excluded from the measurement and doesn't have to be accounted for in post-processing.

The raw data for each test is a single-shot capture of a double-pulse event long after the dc-link has been energised to prevent the effect of current collapse [9] impacting the results. After a test sequence is complete, an automated MATLAB script on the host computer collects the captured data from the oscilloscope, together with ambient temperature and humidity data from the Xilinx system shown in Fig. 4. Results for all data sets were also collected on the same day once equipment had reached stable operating temperatures, to minimise the impact of the memory effect that enhancement mode GaN FETs display [9], and to minimise the small day-to-day variation in the asynchronous timing circuits of the active gate driver.

## III. Active Gate Driving Under Changing Load Current

### A. Optimised Gate Driving at a Single Load Point

For all results presented, the same active driving profile was used. The optimisation goal of this profile is to reduce the current oscillations and overshoot peak, whilst minimising transition time, at a nominal load current of 9A. The profile is shown in Fig. 6, and its effect on the power-circuit current is shown in Fig. 7.

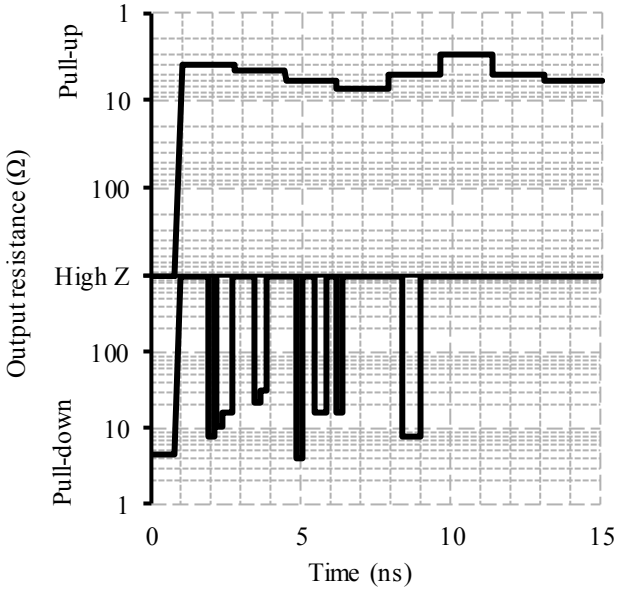


Fig. 6. The gate impedance profile used throughout this work.

The profile employs a general strong pull-up, as is expected of a turn-on transition, varying between 9 Ω and 3 Ω with an average of ~6 Ω across the transition. The very high time resolution of the driver used in this work is then used to apply 100-400 ps pull-down 'tweaks' at hand-tuned points in time to eliminate the source of ringing in the power waveforms, by preventing the aspects of the transition which excite circuit-specific resonances in the power circuit from being generated.

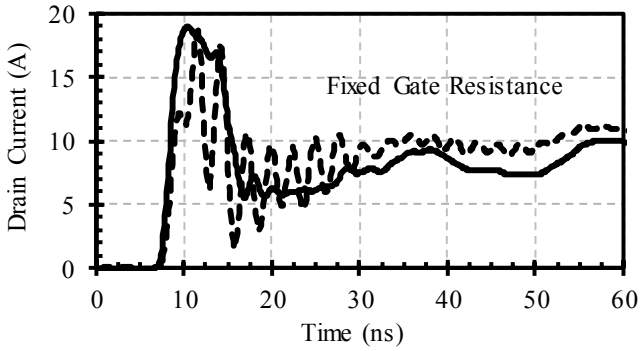


Fig. 7. A comparison between the active gate driving profile used in this work and a comparable fixed gate resistance.

Fig. 7 shows the improvement to the $Q_{ctrl}$ drain current surge and current oscillation that the active gate driving profile

used in this work delivers. With the steady-state load current fixed at 9 A, the lowest fixed gate resistance capable of less than 20 A peak current overshoot is chosen, and its drain current transition shown for comparison.

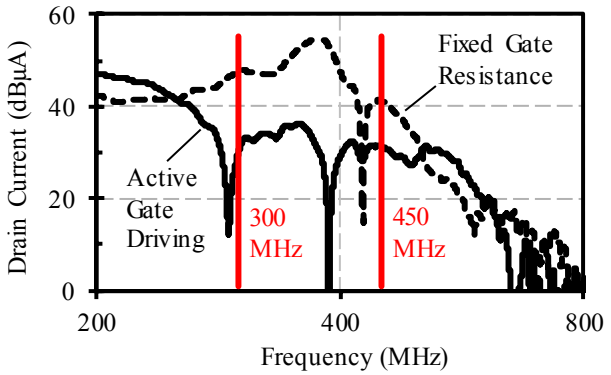


Fig. 8. The calculated spectra of the drain current waveforms shown in Fig. 7

The use of high time-resolution active gate driving profile removes a significant amount of high frequency content in the initial pulse by broadening the peak and eliminating most of the ringing superimposed upon the pulse, whilst offering a slightly higher peak $di/dt$. The active driving profile then almost eliminates continued high frequency (~400 MHz) ringing after the initial current pulse.

This suggests the presence of this undesirable oscillation could be used as a metric by which to judge the effectiveness of the active gate driving profile.

### *B. Impact of Changing Load Current*

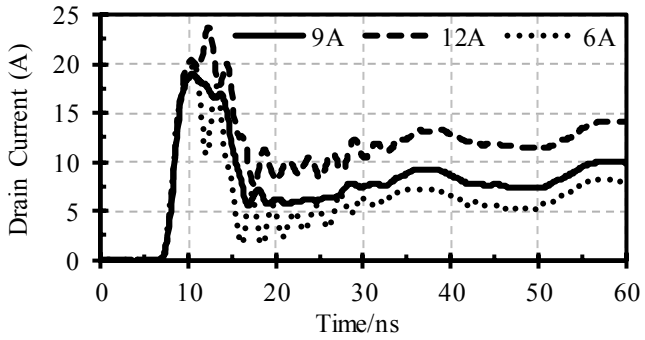


Fig. 9. Drain current switching waveforms for open-loop active gate driving at various load currents, where the gate profile has been optimised for the 9 A case.

Fig. 9 shows in the time domain the impact of changing the steady-state current away from point at which has been optimised. It is varied around 9 by ±3 A. Both 6 A and 12 A traces show the return of the ~400 MHz oscillation seen in Fig. 8, but lowering the steady-state current has resulted in larger peak-peak oscillations in the drain current waveform.

In both cases, the active gate driving profile has become less effective, but decreasing the steady-state current has had a more pronounced effect. It is therefore expected that the frequency spectra of the three waveforms would reflect this and allow the relative impact of a change in steady-state current to be quantified.

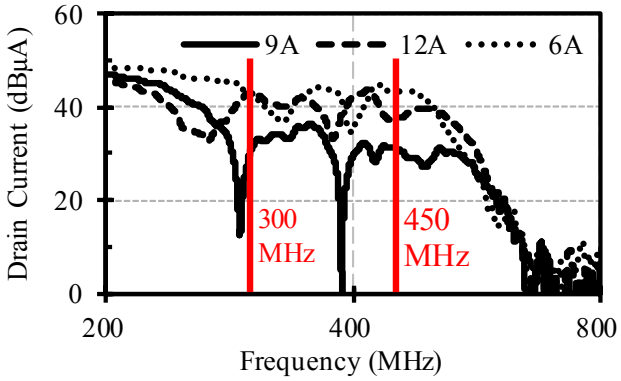


Fig. 10. Calculated spectra of the current switching waveform for 6 A, 9 A and 12 A steady-state loads highlighting the frequency band where this work concentrates (around 400 MHz).

The time-domain data used to produce Fig. 9, which is not a continuous pulse train, is used to calculate the spectral content by padding the data to an effective 100 kHz switching frequency and applying a Tukey (tapered cosine) window with taper factor of 0.25 before performing an FFT.

It is shown that between 300 MHz and 450 MHz, there is significant variation between the three envelopes. In this highlighted 150 MHz band, the 6 A and 12 A traces have an increase of approximately 25%, when the deep minima in the 9 A spectrum is excluded. The 6 A spectrum however has higher peaks in this band and shallower lows suggesting it overall has more spectral content contained in this band. This reinforces the qualitative observation from Fig. 9 that a decrease in steady-state current has more of an impact than an increase.

This increase to either side of an optimal point indicates that a U-shaped curve-of-effectiveness exists about the point at which an active gate driving profile is optimised, as illustrated in Fig. 11.

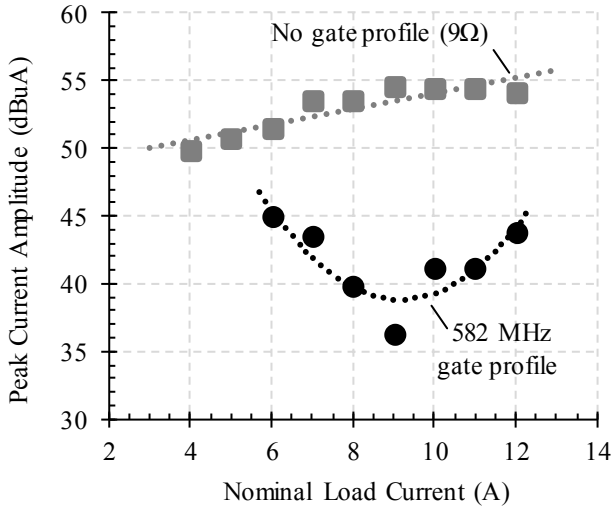


Fig. 11. Peak current magnitude between 300 MHz and 450 MHz plotted against steady state load current

### C. Time Stretching to Track Load Current

The process for developing an optimized waveform, like that used in this work for the objectives stated, is concerned with manipulating the gate of the GaN FET at very specific points in its switching transition. The switching characteristics of GaN FETs, which active gate driving hopes to precisely control, is dependent upon the load current too. This requires the gate driver to compress or stretch the time over which the active gate driving profile is applied to maintain or track performance.

As shown in Fig. 12, the indicated U-shape performance curve exists not only at the load current and clock frequency for which the active gate profile was developed, but that the same gate profile could be re-optimised by tuning the clock frequency at which it is reproduced. Giving rise to another such U-shaped curve, the 607 MHz gate profile, which could be formed about another optimal point.

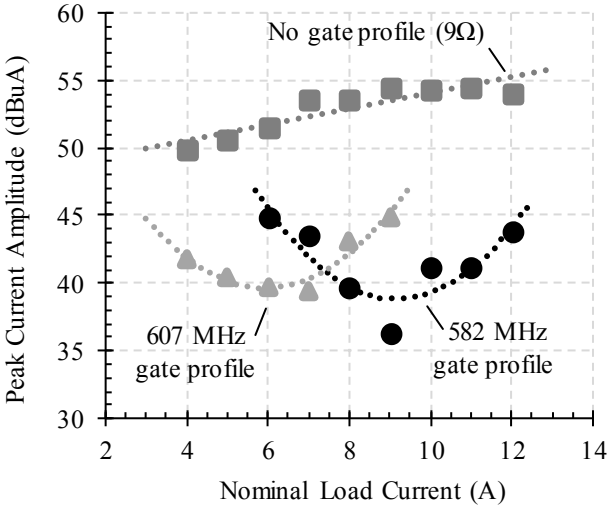


Fig. 12. Peak current magnitude between 300 MHz and 450 MHz plotted against steady state load current with the active drive sequence at two different playback frequencies.

This suggests that, for a given active gate driving profile, performance can be maintained across a much broader load current range than previously thought, without the need to change to an entirely new gate profile.

Furthermore, the results shown in Fig. 12 suggest that, even de-tuned by shifting load current, the active gate driving profile still performs significantly better than a comparable fixed gate resistance at the same load current.

## IV. Discussion and Conclusions

Active gate driving gate profiles have been developed to suppress current ringing in the 300-450 MHz band. The gate signal profiles used in this work remain close to optimal for ±20% changes in current, and over a larger range of at least ±35% the profiled waveforms perform better than a non-profiled gate waveform.

Furthermore, it is shown that a gate drive profile which is becoming non-optimal as the load current changes, can to some extent, be re-optimised by stretching or compressing the gate profile in time, for example by changing the clock frequency of the active gate driver.

Using this method, the problem of maintaining switching performance across a broad operating area, becomes a single-parameter optimisation, which is simpler than optimising all the degrees of freedom of a complex driving pulse such as that of Fig. 6.

It appears from experimentation that the suppression of circuit-specific resonances is achieved primarily by repeated rapid pull-down gate pulses (Fig. 6) during a more gradual pulling-up of the gate. The intention of this work was to stretch or compress the gate profile in time, to compensate for changes in operating conditions. With the driver used in this work, however, the timings of these fast pull-down pulses are not perfectly scaled with the driver's clock frequency, as they are formed in part by asynchronous circuitry that permits pulses to be created that are shorter than the clock period [7]. The resulting profile distortion therefore may be influencing the results.

In conclusion, currently reported open-loop high time resolution active gate driving profiles allow the potential of GaN FETs to be exploited more fully than conventional fixed gate resistance drivers. However, the open loop nature makes their impact on performance dependent upon current operating point versus the operating point at which they were optimised. This work presents a single parameter adaptation measure to permit a fixed active gate driving profile to operate correctly over a wide load current range.

Further work should be carried out to explore if active gate driving profiles can be time-stretched in order to adapt to other operating conditions such as power device temperature and DC link voltage.

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