A Back-illuminated Voltage-domain Global Shutter Pixel with Dual In-pixel Storage

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***Abstract*—A 3.75μm back-illuminated voltage-domain global shutter pixel is presented. The 10T pixel architecture presented contains two independently operable storage branches and supports dual-capture, HDR and CDS functionality. Electronic shielding of the sample diffusions by the vertical photodiode is utilised to reach native and differential parasitic light sensitivities below -73.5dB and -82.5dB at 940nm respectively. A global shutter HDR image capture mode with minimal motion artefacts is also demonstrated.**

***Index Terms*—CMOS image sensors, Active pixel sensors, Photodiodes**

I. Introduction

GLOBAL shutter (GS) image sensors are indispensable for time-gated imaging [1] [2], synchronisation of image capture with an illumination source [3], or for any other applications requiring minimisation of motion artefacts [4]. For GS operation to be possible without per-pixel readout or an external frame store, it is necessary to have in-pixel storage.

GS pixels can be partitioned into two groups based on the implementation of their memory. Approaches involving direct storage of the signal charge gathered by the photodiode are referred to as *charge domain* global shutter pixels (Q-GS), whereas those storing the signal voltage are *voltage domain* global shutter pixels (V-GS). At equal pixel size, the former are well-suited to low light imaging by virtue of their lower noise floor [5], whereas the latter are more versatile, typically have better parasitic light sensitivity (PLS), and are less reliant upon design-specific process optimisation compared to high-performance Q-GS designs. The most common implementation of the memory for Q-GS pixels is with an intermediate pinned diode placed between the photodiode and sense node [5]–[7], although other methods including storage gate [8] and sense node memory also exist [2], [9]. The definition of V-GS pixels could stretch to include digital storage [10] or external memory [11], [12], but by far the most common storage implementation in this class of pixel is capacitors integrated into the pixel. These are typically implemented as MOS capacitors. Because the signal must be buffered for storage in a V-GS sensor, the sense node $\frac{kT}{C}$ reset noise dominates the pixel noise floor. This can be overcome by sampling the reset level within the pixel [13], [14] in addition to the signal, or by AC coupling the signal to a secondary sense node [15].

Regardless of the memory type, GS pixels are generally larger than their rolling shutter (RS) counterparts as a consequence of their relative complexity. Back-illumination (BI) or backside-illuminated (BSI) technology has been successfully exploited by the leading edge of CMOS image sensors to improve pixel performance while simultaneously decreasing RS pixel pitches down to 0.9μm [16]. Thus far, BSI technology has rarely been utilised by global shutter image sensors invariably due to the design challenge of achieving acceptably low parasitic light sensitivity. Without metal light shielding, it is difficult to adequately protect the storage node from degradation during the memory period.

As pixel pitches have decreased, photodiode structures with higher Q_{SAT} per unit area have been developed. Such pixels often utilise some form of in-depth storage to achieve this [17]–[19]. In this work, a vertical photodiode is used to occupy a large proportion of the pixel volume, ensuring good sensitivity, PLS and Q_{SAT} while maintaining a small footprint near the frontside surface of the pixel. We will demonstrate that through judicious sizing of sample capacitors, electronic shielding of the storage nodes and a circuit supporting differential PLS, it is possible to create a V-GS pixel which harnesses the advantages of BSI and retains excellent PLS performance, even into the near-infrared spectrum.

The next section introduces the 10T pixel architecture, its operating modes and the test chips used to generate measurement data. The following sections will then cover the TCAD-based design optimisation of the pixel and the parasitic light sensitivity model using to predict PLS performance. Finally, the measured results from the test chips are presented.

II. The 10T Pixel Architecture

The 10T pixel architecture displayed in Fig. 1 has been implemented at a $3.75\,\mu\mathrm{m}$ pixel pitch in a BSI imaging process ($90\,\mathrm{nm}$ FEOL, $65\,\mathrm{nm}$ BEOL). It is based on a 4T-style pinned photodiode front-end and capacitive storage elements. The capacitors are MOS devices augmented by MOM fringe capacitors.

Two test chips were fabricated, each containing a 1024×800 array of 10T pixels, one having a number of pixel variants exploring the pixel design space, the other having a homogeneous array. An annotated photomicrograph of the former is shown in Fig. 2. The measured results in this work were all obtained from these two devices.

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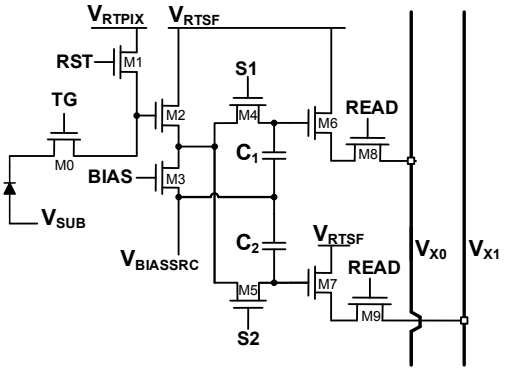


Fig. 1: 10T pixel circuit with two MOS storage capacitors. The pixel has six control signals and four power supplies.

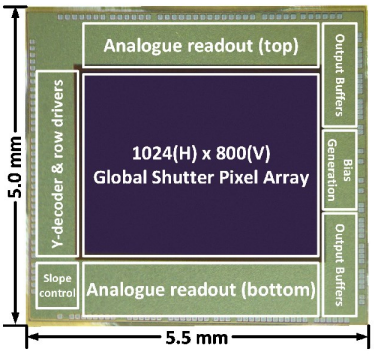


Fig. 2: Photomicrograph of image sensor test chip with homogeneous pixel array.

The sense node is connected via a source follower amplifier to two parallel storage branches, each branch having a dedicated source follower readout. Arranging the dual storage elements in this way allows both storage nodes to be controlled and read independently of each other. Furthermore, the pixel is well-suited to expansion to larger number of storage elements due to the parallel arrangement, although this number is limited to two in this work. This flexibility comes at the cost of an additional two transistors over a sequential storage architecture [13].

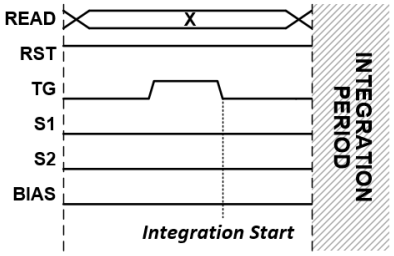
III. Operating Modes and Video Timing

The dual memories in the pixel can be used in one of two ways depending on the application. Either they can be used to capture two separate images, or they can be used to acquire a single image with correlated double sampling (CDS) and improved PLS.

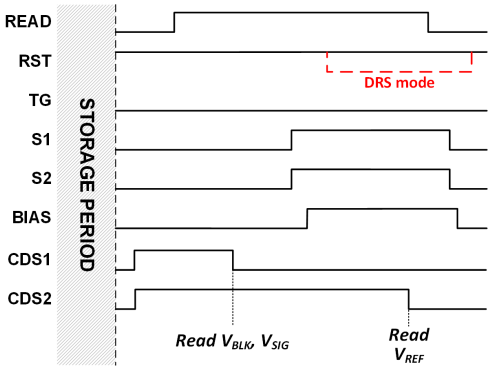
A. Reset and Readout Sequences

The photodiode reset and the readout sequences are common to both operating modes. They are shown in Fig. 3. The sampling sequence is specific to the operating mode; the relevant timing sequences are detailed in the following subsections.

At the beginning of the read sequence illustrated in Fig. 3b, the memories C_1 and C_2 contain the sampled voltage levels



(a) Photodiode reset sequence



(b) Read sequence

Fig. 3: Photodiode reset and pixel read timing sequences are identical for both operating modes. CDS1 and CDS2 are the readout sample control signals.

from the integration period. The CDS1 signals in the column readout circuitry are pulsed and the C_1 and C_2 voltages are sampled by the bottom and top column readouts. Following sampling of this signal, the S1 and S2 switches are enabled, and both output source follower gates are driven to a common reference voltage V_{REF}. The reference voltage is generated by holding the sense node of the pixel in reset. The CDS2 signals are now pulsed and the reference voltages are sampled by the column readout circuit. The first and second column samples are subtracted with an off-chip amplifier to produce the final signal.

B. Delta Reset Sampling Mode

The primary mode of the 10T pixel is to store two separate image signals in the pixel (Fig. 4). This capability supports multiple applications. For motion detection or time-gated imaging, the inter-exposure period can be adjusted without constraints imposed by the readout time; for structured light depth mapping, the image can be captured with and without illumination to allow ambient cancellation. We demonstrate HDR image capture using the dual image capture mode in section VI.

At the end of the integration period, the sense node is reset and the signal charge in the photodiode is transferred to the sense node. At this point, the signal voltage is buffered by the sense node source follower amplifier and can be sampled by either one of the sample capacitors as demonstrated in Fig. 5.

Because both pixel memories contain image signals in this mode, it is not possible to store the sense node black level and perform true CDS. Instead, delta-reset sampling (DRS) must

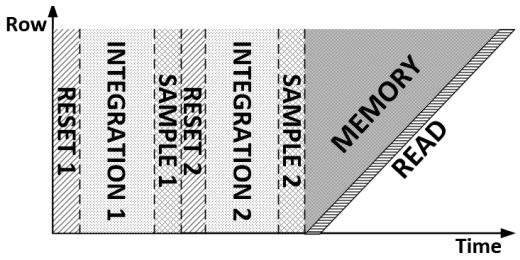


Fig. 4: Delta-reset sampling enables the dual storage elements to capture two separate images. Without inter-frame readout, the inter-capture period can be <5 µs.

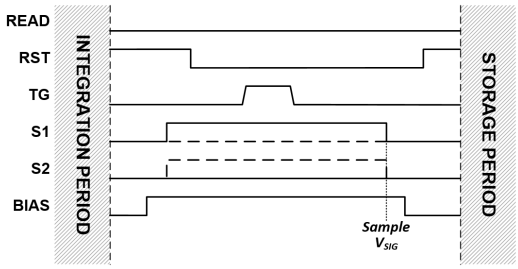


Fig. 5: Signal sampling sequence for the DRS mode. In the sequence indicated by the solid lines, C_1 capacitor is used to sample the signal. The dashed lines indicate the modifications to the procedure required if C_2 is to be used instead.

be used, where the reset level is obtained after the signal. This has the drawback of introducing the sense node reset noise into the signal because the signal sample noise is uncorrelated with the reset sample noise. Neglecting the noise of the output chain itself, the pixel noise in the output signal can be expressed as:

$$v_{DRS} = \sqrt{G^2\left(2\left(\frac{GkT}{C_{SN}}\right)^2 + 2v_{snsf}^2 + \left(\frac{kT}{C_{SMP}}\right)^2\right) + 2v_{opsf}^2} \quad (1)$$

Where G is the source follower gain, C_{SN} is the sense node capacitance, C_{SMP} is the sample capacitance, and v_{snsf} and v_{opsf} are the sense node and output source follower RMS voltage noise contributions respectively. It is important to note that it is possible to reduce the noise floor by keeping the sense node reset gate enabled for the duration of the V_{REF} generation. Doing so prevents an additional uncorrelated sense node sample from being taken, and the multiplicative factor of 2 attached to the $\frac{GkT}{C_{SN}}$ term in (1) is removed. This increases pixel FPN, however, and in the absence of external FPN compensation it is preferable to operate with the higher noise floor.

The noise model is plotted for a variety of sense node capacitance values in Fig. 6 with the measured data from two pixel variants also included. Most immediately apparent is the strong dependence of the noise floor on the sense node capacitance. Although they introduce $\frac{kT}{C}$ noise of their own, the sample capacitors do not have a significant influence on the total read noise, owing to their large size.

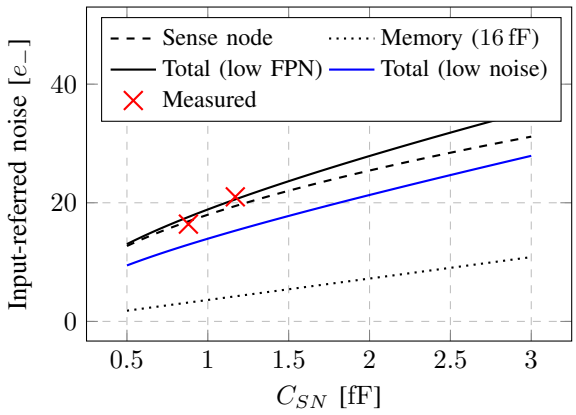


Fig. 6: Input-referred pixel read noise in DRS mode estimated using (1). The non-linear dependence on C_{SN} is due to the sense node reset noise component. Red markers indicate measured data from pixel variants with different CG values.

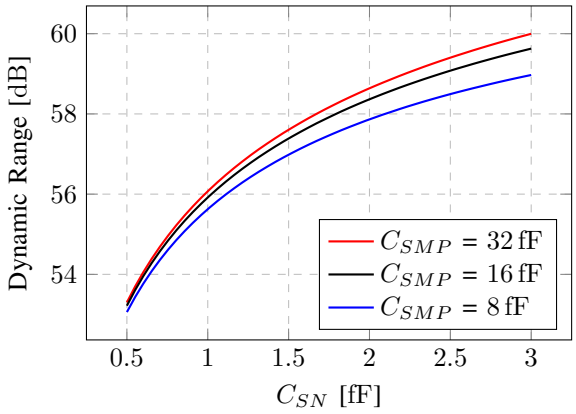


Fig. 7: Dynamic range versus sense node capacitance (DRS mode). A sense-node-limited Q_{SAT} is assumed for all C_{SN}.

The dynamic range of the pixel based on the noise model is plotted in Fig. 7. As suggested by the breakdown of noise contributions, varying the sample capacitance, C_{SMP} around the chosen value of 16 fF shows a very small effect - for C_{SN} at 1 fF, the dynamic range increases by less than 1 dB even when varying C_{SMP} by a factor of four. It is evident that in the dual-capture DRS operating mode, the value of C_{SMP} does not play a major role in determining the noise floor or dynamic range.

C. Correlated Double Sampling Mode

The thermal noise of the sense node reset dominates the pixel read noise. If the two storage nodes are used to sample the pre-transfer sense node reset voltage and the sense node signal voltage resulting from a single integration period, subtracting the two signals will cancel the sense node reset noise component. This will provide a substantial reduction in the pixel noise floor and an associated increase in the dynamic range compared to the DRS mode.

The signal sampling sequence is shown in Fig. 8. The S2 signal is pulsed to store the sense node black level on the C_2 capacitor. The S1 signal is switched high at the same

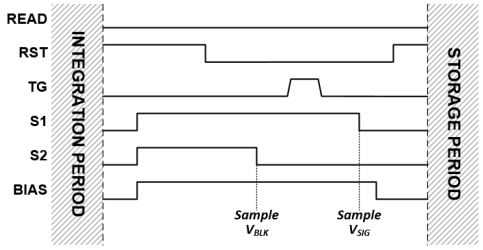


Fig. 8: Signal sampling sequence for the CDS mode.

time to pre-charge the C_1 capacitor to the same voltage and prevent memory effects. The photocharge stored in the PPD is then transferred to the sense node when TG pulses. This is followed by the negative edge of the S1 control signal, which samples the resulting sense node voltage on capacitor C_1. In the version of the readout implemented in this work, the light and black signals are subtracted from the common reference voltage and the final post-CDS signal is obtained via off-chip digital subtraction. The noise floor of the post-CDS signal is given by:

$$v_{CDS} = \sqrt{2\left(G^2(v_{snsf}^2 + \left(\frac{kT}{C_{SMP}}\right)^2) + 2v_{opsf}^2\right)} \quad (2)$$

In this simplified model there is no C_{SN} term and the noise floor is therefore independent of conversion gain (CG). However, if dark current shot noise is taken into account, a C_{SN} dependence will be introduced. This could account for the slight underestimation of the noise floor compared to the measured results shown in Fig. 9.

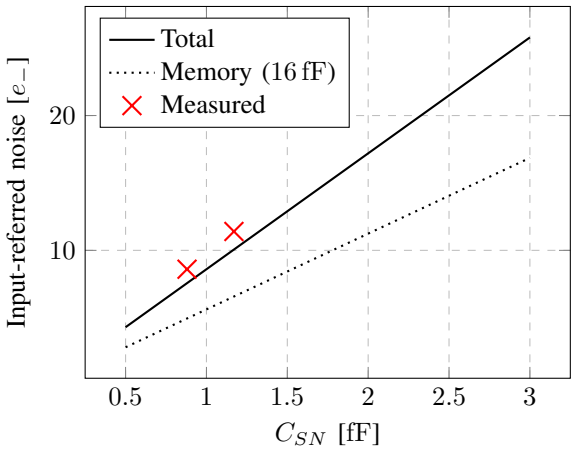


Fig. 9: Input-referred pixel read noise contributions in the correlated double sampling (CDS) mode estimated using (2). Measured data points are indicated with red markers. The values scale linearly with C_{SN} due to the CG change.

As the noise floor in the first-order model is independent of C_{SN} in the CDS mode, the dynamic range will be unaffected. Despite this, C_{SN} will still have an impact on the image quality. DNR_{20dB} is the dynamic range where SNR exceeds $20dB$, and is a better measure of usable dynamic range

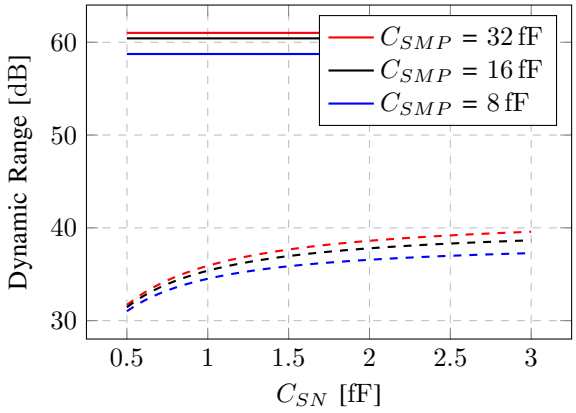


Fig. 10: Dynamic range in CDS mode. The dashed lines represent DNR_{20dB}.

compared to the standard metric; Fig. 10 shows its strong dependence on C_{SN}.

IV. Pixel Simulation & Design

Because of the compact nature of the pixel implementation, TCAD simulations were used to support the design and optimisation process. A model generated by 3D front-end process simulation is shown in Fig. 11. The 10 transistors are arranged in two groups with the remainder of the area on the frontside surface being occupied by the two sample capacitor gates. These are connected to the drains of the S1 and S2 transistors, which have been placed at the periphery of the pixel to minimise incident light intensity and therefore PLS. The transfer gate is situated in the centre of the pixel, with the photodiode directly beneath.

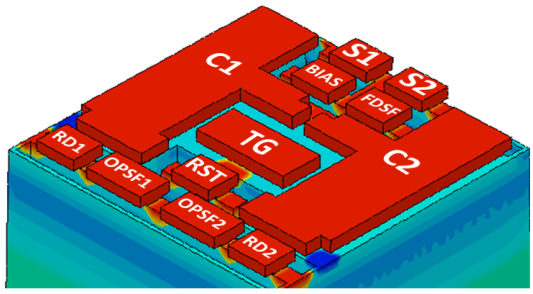


Fig. 11: 3D TCAD process simulation of pixel annotated with component labels.

A cross-section of the simulated vertical photodiode structure is shown in Fig. 12. Charge storage is in a narrow vertical region, enabling a Q_{SAT} in excess of 8 ke- to be achieved while occupying less than 8 % of the available pixel surface area. A dual-fin photodiode design with parallel storage regions connected to a single charge collection region has also been tested and achieved 18 ke- with only a modest increase in required area.

The photodiode extends to cover almost the entire width of the pixel, achieving 90 % coverage of the pixel area at 2 µm below the front-side surface. This serves not only to improve quantum efficiency, but also functions as electronic

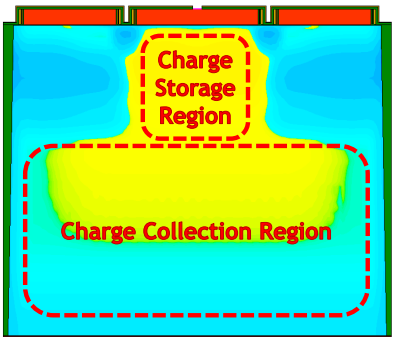


Fig. 12: Simulated doping profile of the vertical photodiode.

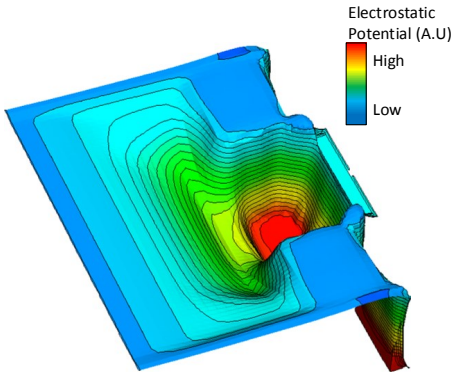


Fig. 13: Electrostatic potential surface plot of photodiode cross-section. Photogenerated electrons are directed towards the potential maximum in the charge storage region.

shielding of the drain terminals connected to the sample gates. The electrostatic potential of the cross-section of Fig. 12 is displayed as a 3D surface plot in Fig. 13, where the electronic shielding and charge collection region can be seen.

As the photodiode possesses a vertical charge storage region, the width of the region instead of its depth is the most influential parameter in determining the depletion potential of the photodiode. This constrains the pixel layout and creates a trade-off between Q_{SAT} and depletion potential.

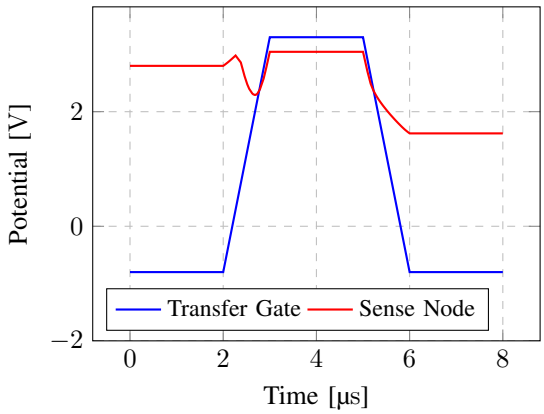


Fig. 14: Transient charge transfer simulation.

A transient simulation of the charge transfer operation from the photodiode to the sense node is shown in Fig. 14. The transfer gate has a very strong capacitive coupling to the sense node and provides a voltage boost in excess of 300 mV during the transfer phase. The sense node voltage initially rises due to the capacitive coupling with the transfer gate, then sharply falls as the collected charge is transported from the PPD to the sense node. On the negative edge of the transfer gate, the portion of the charge held under the transfer gate is injected into the sense node. An asymmetric potential barrier between the sense node and photodiode on the negative edge of the transfer gate pulse permits the lower end of the sense node voltage range to reach below the diode depletion potential; this increases the voltage swing available at the sense node and mitigates the comparatively high depletion potential of the vertical photodiode compared to a planar design.

V. Parasitic Light Sensitivity Model

For any global shutter pixel, it is necessary to ensure that the integrity of the stored signal is not compromised during the memory period. Though integration times in applications using global shutter image sensors are typically very short (often below 100 µs) this is rarely the case for the memory period, which is usually of the order of ms.

There are several contributing factors to the 10T pixel's PLS performance: the ratio of C_{SMP} to C_{SN}, the electronic shielding of the memory node diffusions by the photodiode, and the small size of the diffusions connected to C_1 and C_2. The two distinct operating modes of the 10T pixel have their own PLS characteristics. In the DRS mode, the PLS is given by the ratio of the memory node sensitivity to the photodiode sensitivity, termed 'native PLS'. If operating in the CDS mode, it is referred to as 'differential PLS'. Native PLS can be modelled as:

$$PLS(\lambda)_{NATIVE} = \frac{C_{SN}\int_0^{z_{SI}} A_{MEM}(z)e^{-\alpha z}\mathrm{d}z}{C_{SMP}\int_0^{z_{SI}} A_{PD}(z)e^{-\alpha z}\mathrm{d}z} \quad (3)$$

Where α is the absorption coefficient of silicon for the wavelength of interest, A_{MEM} is the cross-sectional area of the memory diffusion, A_{PD} is the cross-sectional area of the photodiode and z is the distance from the silicon surface. The predicted native PLS value is plotted in Fig. 16 alongside the measured data.

In the differential imaging mode, the parallel storage branches are conducive to creating well-matched storage nodes, since only the differential parasitic signal degrades the stored voltage. Due to the stochastic nature of incident light absorption, the parasitic signal cannot be fully cancelled even if the two memory nodes are perfectly matched, however. Differential PLS in the 10T pixel can be modelled as:

$$PLS(\lambda)_{DIFF} = \beta\frac{C_{SN}}{C_{SMP}} \cdot \frac{\sqrt{2P_0^{-1}t_{mem}^{-1}E_{ph}\int_0^{z_{SI}} A_{MEM}(z)e^{-\alpha z}\mathrm{d}z}}{\int_0^{z_{SI}} A_{PD}(z)e^{-\alpha z}\mathrm{d}z} \quad (4)$$

Where P_0 is the incident optical power, t_{mem} is the duration of the memory period, E_{ph} is the energy of a photon at the

chosen wavelength, and β is a non-ideality factor. In any given frame, it is possible that the parasitic signal generated at each memory node is perfectly balanced, which would yield a PLS of infinity. The PLS model is therefore used to calculate the PLS at a distance β from the mean.

From both (3) and (4), it is clear that unlike its effects on dynamic range and pixel noise floor, C_{SMP} has an important role in determining the PLS performance. The noise model predictions along with measured results are plotted in Fig. 16.

VI. Results

The measured quantum efficiency data in Fig. 15 shows that the use of the vertical photodiode and microlens is successful in fill factor recovery, with a peak QE of over 60 % at 500 nm.

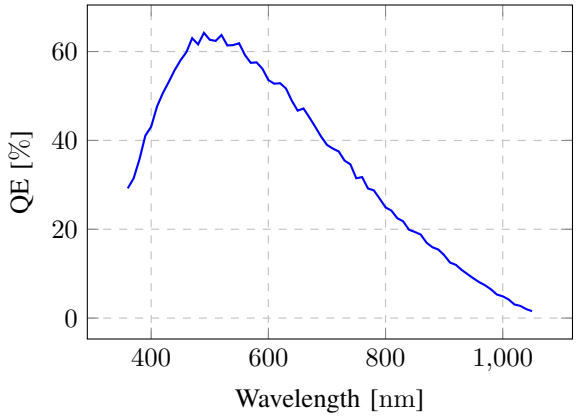


Fig. 15: Quantum efficiency versus wavelength.

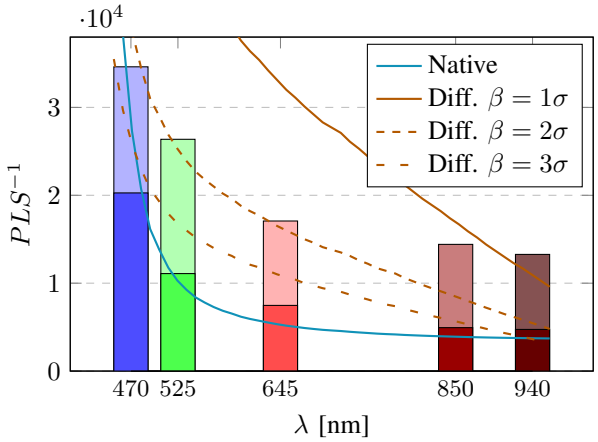
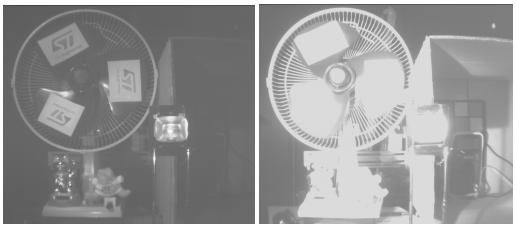


Fig. 16: Measured parasitic light sensitivity overlaid with model predictions. Solid bars represent native PLS, shaded bars represent differential PLS.

Differential PLS was measured at less than 1×10^{-4} for all wavelengths tested, even into the near-infrared region of the spectrum. The improvement in PLS due to the differential storage of the CDS capture mode is even more evident at these longer wavelengths.

The dual capture mode of the 10T pixel can be exploited to expand the dynamic range of the captured information. By adjusting the ratio of the exposure times of the two images, it is possible to capture information from a much wider dynamic range than a single DRS-mode capture would allow. This allows global shutter high dynamic range imaging to be performed.



(a) Short exposure (b) Long exposure

(c) HDR image

Fig. 17: High dynamic range image synthesised from two exposure-bracketed images with a 16:1 exposure ratio.

The results of the HDR imaging mode are displayed in Fig 17. The final HDR image produced contains both the details in the high-light areas and low-light regions of the scene. Because of the very short inter-exposure time between the short and long exposures, there are no visible artefacts from the motion of the fan blade.

Table I contains various measured performance figures.

TABLE I: Performance summary of 10T pixel.

Metric	Value	Units	Comment
CG	181	µV/e-	10T reference variant
Q_{SAT}	≈ 8.5	ke-	Single-fin PPD
Read Noise	16.4 / 8.6	e-	DRS / CDS mode
Dynamic Range	54 / 60	dB	DRS / CDS mode
C_{SMP}	16	fF	
I_{DKPD}	492	e-/s	$T_{junction} \approx 50\,°C$
I_{DKMEM}	393	e-/s	$T_{junction} \approx 50\,°C$
Peak QE	62.5	%	λ = 525 nm
PLS (Native)	≤ -73.5	dB	λ = 940 nm
PLS (Diff.)	≤ -82.5	dB	λ = 940 nm
Pixel FPN	0.54	%	Readout not included
Pixel PRNU	1.25	%	Readout not included

VII. Conclusion and Outlook

It has been shown that it is possible for a BSI V-GS pixel to achieve good performance, and in particular, excellent PLS without metal light shielding. Electronic shielding, sample capacitor size and placement have been shown to provide sufficient protection for the memory node. The high-density vertical photodiode structure provides high QE with a low area footprint and doubles as effective electronic shielding. The dual-capture HDR imaging mode demonstrates the flexibility of the 10T pixel architecture.

Additional new imaging technologies besides backside illumination are applicable to GS pixels. The use of capacitive deep trench isolation [20] to create high-density storage capacitors would permit a substantial reduction in pixel pitch without reducing storage capacitance. Photoconductive film technologies are not ideally-suited to Q-GS pixels due to their inability to have zero-$\frac{kT}{C}$ charge transfer, but would instead be well-suited to V-GS pixels. Similarly, chip-stacking is also expected to provide a new avenue for reduction of pixel pitch and expansion of functionality for V-GS pixels.

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