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Research Article

CMOS Realization of All-Positive Pinched Hysteresis Loops

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Two novel nonlinear circuits that exhibit an all-positive pinched hysteresis loop are proposed. These circuits employ two NMOS transistors, one of which operates in its triode region, in addition to two first-order filter sections. We show the equivalency to a charge-controlled resistance (memristance) in a decremental state via detailed analysis. Simulation and experimental results verify the proposed theory.

1. Introduction

Pinched hysteresis was proposed to be a signature of memristive devices [1, 2], yet it can also be observed in several other nonlinear devices such as nonlinear inductors (capacitors) with quadratic-type current (voltage) dependence [3]. Finding a general model for pinched hysteresis behavior was attempted in [4] for specific devices labeled as memristors [5]. In [6] and from a simplified mathematical point of view, the following model was proposed and shown to exhibit a pinched hysteresis behavior which can fit both charge-controlled and flux-controlled memristance definitions:

$$y(t) = x(t) \times \left(a + \frac{1}{T} \int_0^t x(\tau)\, d\tau \right), \tag{1}$$

where if $y(t) = v(t)$ and $x(t) = i(t)$, the charge-controlled memristance is obtained, while for the alternative setting $y(t) = i(t)$ and $x(t) = v(t)$, the flux-controlled memristance is obtained. In (1), the constants a and T are scaling and integration time constants, respectively. Note that circuit realization of this model for the purpose of emulating its pinched hysteresis behavior in non-solid-state devices requires a multiplier block, an integrator block, and an adder [6]. Several other emulator circuits have recently been proposed in the literature [7–13]. It is important to note that (1) is nonlinear due to the multiplication term and that pinched hysteresis cannot appear in a linear system. It is also possible to include other forms of nonlinearity that apply to the shaping of the loop as a result of shaping the applied excitation. This means replacing $x(t)$ in (1) more generally with $f(x(t))$.

Pinched hysteresis loop is generally observed as a result of applying a bipolar sinusoidal voltage or current excitation signal and is thus symmetrical around the origin. Nonsymmetrical loops can also be obtained when the pinch point is shifted away from the origin. However, an all-positive pinched loop, to the best of our knowledge, has not been demonstrated before. It is the purpose of this work to introduce two simple circuits where this behavior is observed. We rely on the inherent nonlinearity of a MOS transistor to perform the multiplication operation required by (1) in order to obtain a charge-controlled memristance. Recall that a MOS transistor current-voltage relation can be described by

$$i_{ds} = k \left[\left(v_{gs} - V_T \right) v_{ds} - \frac{v_{ds}^2}{2} \right], \tag{2}$$

where i_{ds} is the drain-to-source current, v_{gs} and v_{ds} are, respectively, the gate-to-source and drain-to-source voltage, V_T is the threshold voltage, and k is a constant in A/V^2 units. It is obvious from (2) that a multiplication operation is inherent through the term $(v_{gs} - V_T)v_{ds}$. However, for an NMOS transistor, the current is unidirectional and the condition $v_{gs} > V_T$ is necessary for the transistor to switch on. Therefore, if (2) is successfully reconfigured to implement (1), an all-positive pinched hysteresis loop can be obtained. In the first part of this work, we do not attempt to remove the extra nonlinear term $v_{ds}^2/2$ and therefore it remains affecting the pinched loop. However, this effect is minimized via proper selection of the design parameters. In a later section of the work, we employ a linearization circuit to remove this quadratic term and hence ensure that only the multiplication nonlinearity term remains. As a result and comparing (2) to (1) assuming $v_{ds}^2/2$ is minimized or eliminated, it is clear that the mapping $i_{ds} \rightarrow y(t)$, $v_{ds} \rightarrow x(t)$, and $K(v_{gs} - V_T) \rightarrow a + (1/T)\int_0^t x(\tau)d\tau$ is necessary. To achieve this, we adopt a frequency-domain approach which also allows independent adjustment of the fixed part and the charge-controlled part of the memristance. We stress and clarify the role played by the capacitors in the proposed circuits, which is crucial to the understanding of pinched hysteresis behavior in general, as clearly seen in [17, 18] for solid-state devices as well. Note that, in reconfiguring (2) to realize (1) via this mapping, we are essentially modifying the MOS transistor transconductance such that it is state-controlled, with the state variable being the terminal voltage of the transconductance v_{ds}. The time constant T necessary in (1) can only be obtained with an embedded capacitance (physical or parasitic) [17, 18]. Finally, it must be stated that this paper is concerned with the "pinched hysteresis behavior" as a behavior rather than with proposing yet another memristor emulator. The design concept of the circuits under study here is completely new and relies on a frequency-domain approach rather than a time-domain approach. It also shows for the first time that pinched hysteresis can even be unipolar, something not possible with memristors as they are so defined.

This manuscript is organized as follows. Section 2 looks at the proposed circuits and presents the theory behind their operation that leads to pinched hysteresis behavior. Section 3 computes the memristance of the proposed circuits, with numerical simulations, and presents pinch-off analysis of the proposed circuits. In Section 4, a method to linearize the main transistor in triode is presented which removes the extra nonlinear term $v_{ds}^2/2$ in (2). In Section 5, simulation and experimental results are presented, and finally our conclusions are given in Section 6.

2. The Proposed Circuits

Consider the circuits shown in Figure 1 both consisting of opamp A_1 connected as a buffer and opamp A_2 along with the NMOS transistor M_2 as a simple voltage to current converter which converts the voltage of the noninverting terminal of A_2 into a current i_{in} through NMOS transistor M_1. It is essential for M_1 to remain in triode, hence acting as a transconductance. Both circuits contain a lossy integrator comprising R_1, C_1, and a DC bias voltage V_{dc_1} required to maintain M_1 in triode ($V_{dc_1} > V_T$, $V_{DS_1} < V_{dc_1} - V_T$). The difference between the two circuits can be seen in their high-pass filter sections. In the case of Figure 1(a), it consists of R_2, C_2 with an additional DC source V_{dc_2} providing a DC voltage to the drain of M_1. For Figure 1(b), the high-pass filter is made up of $r_{1,2}, C_2$ and here the drain-to-source DC biasing of M_1 comes from V_{dc_1} through $r_{1,2}$ as αV_{dc_1}, where $\alpha = r_1/(r_1 + r_2)$. Note that maintaining transistor M_1 in triode in both circuits requires that $V_{dc_1} - V_{dc_2} > V_T$ and $(1 - \alpha)V_{dc_1} > V_T$ for Figures 1(a) and 1(b), respectively.

The lossy integrator of each circuit has a response given in the frequency domain which can be written as

$$H_1(\omega) = |H_1(\omega)| \angle -\theta_1 = \frac{1}{\sqrt{1 + \omega^2\tau_1^2}} \angle \tan^{-1}(\omega\tau_1), \quad (3)$$

where $\tau_1 = R_1C_1$. Meanwhile, the high-pass filter in Figure 1(a) has a response

$$\begin{aligned} H_{2a}(\omega) &= |H_{2a}(\omega)| \angle\theta_{2a} \\ &= \frac{\omega\tau_2}{\sqrt{1 + \omega^2\tau_2^2}} \angle\left(90^\circ - \tan^{-1}(\omega\tau_2)\right), \end{aligned} \quad (4)$$

with $\tau_2 = R_2C_2$, and likewise the response of the high-pass filter in Figure 1(b) is

$$\begin{aligned} H_{2b}(\omega) &= |H_{2b}(\omega)| \angle\theta_{2b} \\ &= \alpha\sqrt{\frac{1 + \omega^2\tau_z^2}{1 + \omega^2\tau_p^2}} \angle\tan^{-1}(\omega\tau_z) - \tan^{-1}(\omega\tau_p), \end{aligned} \quad (5)$$

where $\tau_z = r_2C_2$ and $\tau_p = (r_1//r_2)C_2$. Clearly, both high-pass filters provide a leading phase shift by different amounts while DC biasing voltages are allowed to be passed on to the transistor M_1 to set V_{DS_1}. For an input voltage of amplitude A and frequency ω_o in the form $v_{in}(t) = A\sin(\omega_o t) + V_{dc_1}$, it follows that the time dependent V_{GS} voltage of M_1 is

$$V_{GS_1}(t) = A|H_1(\omega_o)| \sin(\omega_o t - \theta_1) + V_{dc_1}, \quad (6)$$

while the time dependent V_{DS} voltages in Figures 1(a) and 1(b) are, respectively,

$$\begin{aligned} V_{DS_1}(t) &= A|H_{2a}(\omega_o)| \sin(\omega_o t + \theta_{2a}) + V_{dc_2}, \\ V_{DS_1}(t) &= A|H_{2b}(\omega_o)| \sin(\omega_o t + \theta_{2b}) + \alpha V_{dc_1}, \end{aligned} \quad (7)$$

where, for (7), $A < V_{dc_2}$ and $A < \alpha V_{dc_1}$, respectively. Substituting (6)-(7) into (2) yields after considerable simplification

$$\begin{aligned} i_{in_a}(t) = &-\widehat{A}\cos(2\omega_o t - \theta_1 + \theta_{2a}) + \widehat{B}\sin(\omega_o t - \theta_1) \\ &+ \widehat{C}\sin(\omega_o t + \theta_{2a}) + \widehat{D}\cos(2\omega_o t + 2\theta_{2a}) \\ &+ \widehat{E} + \widehat{I}_{off}, \end{aligned} \quad (8)$$

Table 1: Summary of the coefficients in (8) and (9) for Figures 1(a) and 1(b).

Coefficient	Figure 1(a)	Figure 1(b)
$\widehat{A}$	$\frac{1}{2}kA^2\lvert H_1(\omega_o)\rvert\lvert H_{2a}(\omega_o)\rvert$	$\frac{1}{2}kA^2\lvert H_1(\omega_o)\rvert\lvert H_{2b}(\omega_o)\rvert$
$\widehat{B}$	$kA\lvert H_1(\omega_o)\rvert V_{\mathrm{dc}_2}$	$\alpha kA\lvert H_1(\omega_o)\rvert V_{\mathrm{dc}_1}$
$\widehat{C}$	$kA\lvert H_{2a}(\omega_o)\rvert(V_{\mathrm{dc}_1} - V_{\mathrm{dc}_2} - V_T)$	$kA\lvert H_{2b}(\omega_o)\rvert[(1-\alpha)V_{\mathrm{dc}_1} - V_T]$
$\widehat{D}$	$\frac{1}{4}kA^2\lvert H_{2a}(\omega_o)\rvert^2$	$\frac{1}{4}kA^2\lvert H_{2b}(\omega_o)\rvert^2$
$\widehat{E}$	$\widehat{A}\cos(\theta_1 + \theta_{2a}) - \widehat{D}$	$\widehat{A}\cos(\theta_1 + \theta_{2b}) - \widehat{D}$
$\widehat{I}_{\mathrm{off}}$	$k[(V_{\mathrm{dc}_1} - V_T)V_{\mathrm{dc}_2} - \frac{1}{2}V_{\mathrm{dc}_2}^2]$	$\alpha k[(1 - \frac{\alpha}{2})V_{\mathrm{dc}_1} - V_T]V_{\mathrm{dc}_1}$

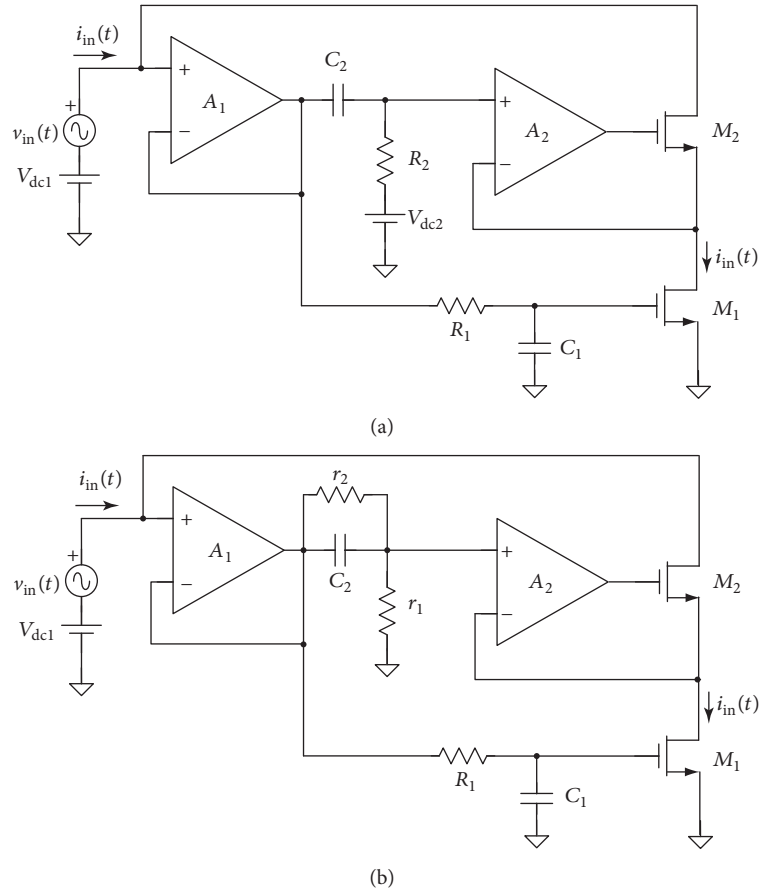

Figure 1: The proposed nonlinear circuits with unipolar pinched hysteresis loop.

for Figure 1(a), and

$$\begin{aligned} i_{\mathrm{in}_b}(t) = &-\widehat{A}\cos(2\omega_o t - \theta_1 + \theta_{2b}) + \widehat{B}\sin(\omega_o t - \theta_1) \\ &+ \widehat{C}\sin(\omega_o t + \theta_{2b}) + \widehat{D}\cos(2\omega_o t + 2\theta_{2b}) \\ &+ \widehat{E} + \widehat{I}_{\mathrm{off}}, \end{aligned} \tag{9}$$

for Figure 1(b). The coefficients of the $\sin(\cdot)$ and $\cos(\cdot)$ terms in (8) and (9) are given in Table 1. Note that, with the exception of $\widehat{I}_{\mathrm{off}}$, all coefficients in Table 1 are frequency dependent. This implies that it is necessary to choose proper values for time constants in order to observe the hysteresis behavior.

Close inspection of (8) under the assumption that $\theta_{2a} \cong \pi/2 - \theta_1$ shows that it can be rewritten in the dimensionless form

$$\begin{aligned} &y(t) + y_{\mathrm{off}} \\ &\quad = x(t)\left|H_1(\omega)\right|\left[1 - \omega\left|H_{2a}(\omega)\right|\int_0^t x(\tau)\,d\tau\right] \\ &\qquad + \frac{\left|H_{2a}(\omega)\right|}{\omega}\dot{x}(t) - \frac{\left|H_{2a}(\omega_o)\right|^2}{2\omega^2}\left[\dot{x}(t)\right]^2 + x_{\mathrm{off}}, \end{aligned} \tag{10}$$

where $x(t) = \sin(\omega t - \theta_1)$ represents an already phase shifted input signal. The term in the square brackets is clearly similar to (1) while additional $\dot{x}(t)$ and $\dot{x}^2(t)$ terms outside the

Table 2: Summary of several analog circuits with pinched hysteresis and actual analog memristor emulators to date and their designs. MB: multiplier block; OPA: operational amplifier; CCII: second-generation current conveyors; AH: additional hardware, which may be in the form of buffers, multiplexers, diodes, inverters, switches, and so forth; I/D: incremental/decremental memristance emulation. The number (#) of transistors refers to the discrete number of external transistors. *An OTA was used here in place of an OPA.

Reference [ ]	MB	OPAs	CCIIs	# of trans.	AH	Quadrant	I/D
[6]	1	—	3	—	Yes	2	Both
[7]	—	1*	2	—	No	2	I
[8]	1	—	2	—	No	2	I
[9]	—	2	1	2	No	2	D
[10]	1	5	—	10	Yes	2	Both
[11]	—	2	1	1	No	2	I
[12]	—	—	3	1	No	2	I
[13]	1	2	—	—	Yes	2	D
[14]	1	—	2	—	Yes	2	I
[15]	—	1*	1	2	No	2	Both
[16]	—	—	4	—	Yes	2	NA
This work	—	2	—	2	No	1	D

brackets are unwanted and will result in a nonsymmetrical loop. Note that the offset terms y_{off} and x_{off} present are a result of the input being DC level shifted. However, using (10) and assuming that ω is sufficiently large such that the second and third terms are negligible and in addition translating the origin to $(x_0, y_0) = (x_{\text{off}}, y_{\text{off}})$, we obtain

$$y(t) = x(t) \times \left[\left|H_1(\omega)\right| - \omega \left|H_{2a}(\omega)\right| \left|H_1(\omega)\right| \int_0^t x(\tau)\, d\tau \right], \tag{11}$$

which compared to (1) has the slightly modified form $y(t) = x(t) \times (a + (ab/T) \int_0^t x(\tau)d\tau)$, where $a = |H_1(\omega)|$ and $b = -|H_{2a}(\omega)|$.

Finally, in comparison with other circuits which also exhibit pinched hysteresis behavior and some of which are labeled as analog memristor emulators as shown in Table 2, about half of them use discrete multiplier blocks which are inefficient. By far, the vast majority use second-generation current conveyors with the only commercial one being the AD844, and several use additional hardware in the form of buffers, multiplexers, diodes, and switches. If the total component count is used as a figure of merit, then the proposed circuits of Figure 1 have the lowest count with their main drawback being operation in one quadrant. Note that even though our proposed circuits are listed among those identified as "memristors" or "memristor emulators," we refrain from labeling our proposed circuits as "memristor emulators" and simply label them as among circuits having pinched hysteresis behavior.

3. Charge-Controlled Resistance (Memristance) Calculation

Using (11) and setting $x(t) = i(t)/I_{\text{ref}}$, $y(t) = v(t)/I_{\text{ref}}R_s$, where I_{ref} is an arbitrary reference current and R_s is an arbitrary scaling resistor, the memristance value for Figure 1(a) can be obtained as

$$R_{m_a} = R_s \left|H_1(\omega)\right| \left[1 - \frac{\omega \left|H_{2a}(\omega)\right|}{I_{\text{ref}}} q(t) \right], \tag{12}$$

where $q(t)$ is the electrical charge. Note that since the input signal has a fixed $\omega = 1/T$, we can rewrite this memristance as

$$R_{m_a} = R_s \left|H_1\left(\frac{1}{T}\right)\right| \left[1 - \frac{1}{T} \frac{\left|H_{2a}(1/T)\right|}{I_{\text{ref}}} q(t) \right], \tag{13}$$

which has a fixed resistive part equal to $R_s|H_1(1/T)|$ and a charge-controlled part equal to $R_s|H_1(1/T)||H_{2a}(1/T)|$. It is thus clear that while the transfer function H_1 controls the magnitude of both parts, H_{2a} can change the magnitude of the charge-controlled part alone. Note that this memristance is decremental [6]. Furthermore, note that, for sufficiently high frequency such that $\omega \gg 1/\tau_1$, $|H_1(\omega)| \approx 1/\omega\tau_1$ and it follows that the fixed part of the realized memristance is approximately $R_s(T/\tau_1)$. However, for sufficiently high frequency such that $\omega \gg 1/\tau_2$, we also note that $|H_{2a}(\omega)| \approx 1$ and therefore the realized memristance can be approximated as

$$R_{ma} \approx R_s \left(\frac{T}{\tau_1}\right) \left[1 - \frac{R_s}{T \times 1V} q(t) \right]. \tag{14}$$

We can further express the electrical charge as $q(t) = C_1 v_{C_1}(t)$ since the only capacitor in the circuit in this case capable of

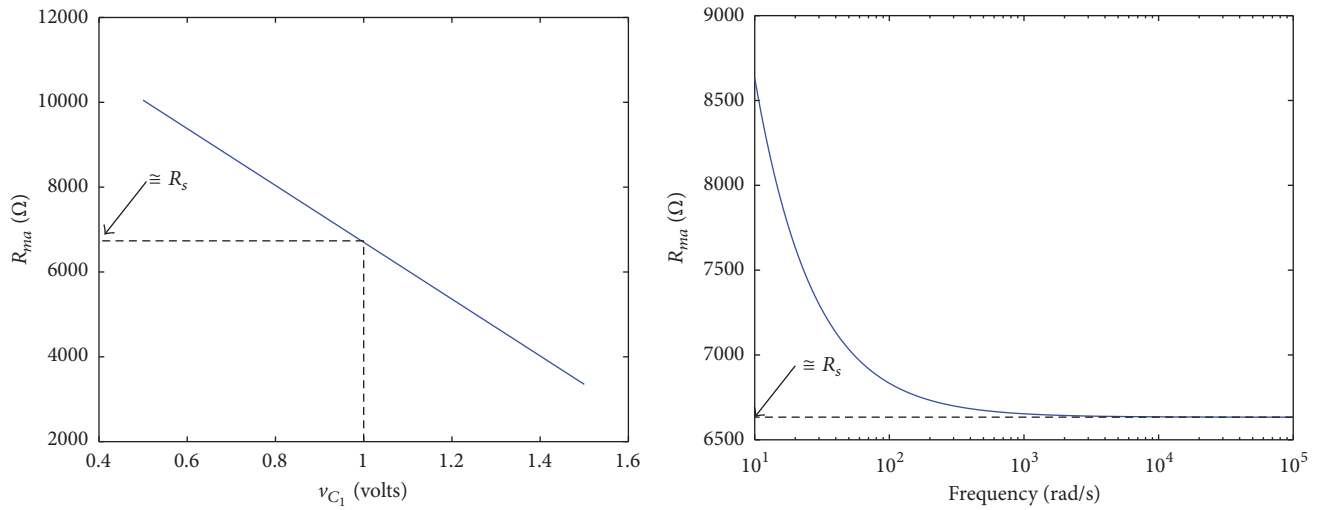

FIGURE 2: (a) Plot of memristance R_{ma} versus capacitor voltage $v_{C_{1n}} = v_{C_1}/1V$ when $m = v_{C1n}/100$, $R_s = 6.7\,\text{k}\Omega$, $R_{\text{off}_a} = 12.67\,\text{k}\Omega$, and $\omega \gg 1/\tau_1$. (b) Plot of R_{ma} versus frequency when $C_1 = 10\,\mu\text{F}$.

holding a charge is C_1 following the fact that $|H_{2a}(\omega)| \approx 1$. Accordingly,

$$R_{ma} \approx \left(\frac{R_s T}{R_1 C_1}\right)\left[1 - \frac{R_s}{T} C_1 v_{C_{1n}}(t)\right]$$
$$R_{ma} = \frac{R_s^2}{R_1}\left(\frac{T}{R_s C_1} - v_{C_{1n}}(t)\right), \tag{15}$$

where $v_{C_{1n}}(t)$ is the normalized (by $1V$) voltage across C_1. In a final step, we may freely express the period T of the applied signal as a ratio of $R_s C_1$ (i.e., $T = mR_s C_1$) leading to the simplified expression

$$R_{ma} \approx \frac{R_s^2}{R_1}\left(m - v_{C_{1n}}(t)\right) = R_s\left(m - v_{C_{1n}}(t)\right), \tag{16}$$

if we select the arbitrary reference resistance as $R_s = R_1$. Note that, for the condition $\omega \gg 1/\tau_1$ to be satisfied, it follows that $m \ll 1$.

The expression in (16) is significantly important for two aspects:

(i) It shows that although the circuit has an all-positive input resistance, theoretically and according to (16), the memristance is not always positive. However, it remains positive because the origin has been already shifted to $(x_0, y_0) = (x_{\text{off}}, y_{\text{off}})$. With reference back to the origin $(x_0, y_0) = (0, 0)$, (16) then becomes

$$R_{ma} \approx R_s\left(m - v_{C1n}(t)\right) + R_{\text{off}_a}, \tag{17}$$

where $R_{\text{off}_a} = V_{\text{dc}_1}/V_{\text{dc}_2}/k[(2 - V_{\text{dc}_2}/V_{\text{dc}_1})V_{\text{dc}_1} - V_T]$. Figures 2(a) and 2(b) show the variation of the memristance versus the capacitor voltage v_{C_1} and versus frequency ω, respectively. In Figure 2(a), for the values chosen: $m = v_{C_1}/100$, $V_{\text{dc}_1} = 1\,\text{V}$, $V_{\text{dc}_2} = 0.4\,\text{V}$, $V_T = 0.35\,\text{V}$, and $k = 0.15\,\text{mA/V}^2$, we obtain $R_{\text{off}_a} = 12.67\,\text{k}\Omega$. Correspondingly, selecting a suitable reference current such as $I_{\text{ref}} = 0.15\,\text{mA}$ leads to a nominal value for R_s of $6.7\,\text{k}\Omega$ (i.e., $I_{\text{ref}} R_s \approx 1\,\text{V}$). For Figure 2(b), we fixed $v_{C_1} = 1\,\text{V}$ and $C_1 = 10\,\mu\text{F}$ and show the decremental nature of the memristance whereas the frequency increases when R_{ma} asymptotically approaches R_s.

(ii) It highlights the significance and necessity of the existence of a capacitor in order to hold the charge. In this circuit, this capacitor is C_1; however, in solid-state devices, this capacitor may well be a parasitic capacitor or equivalent of parasitic capacitances as observed in [17, 18]. It thus appears to the authors that it is not possible to isolate the appearance of pinched hysteresis loops from the existence of a capacitive effect.

In a similar manner, the memristance of the circuit in Figure 1(b) can be obtained as

$$R_{m_b} = R_s\left|H_1\left(\frac{1}{T}\right)\right|\left[\alpha - \frac{1}{T}\frac{\left|H_{2b}(1/T)\right|}{I_{\text{ref}}} q(t)\right], \tag{18}$$

which unlike (13) has a fixed resistive part equal to $\alpha R_s|H_1(1/T)|$ but an identical charge-controlled part. Noting that $|H_{2b}(1/T)| = \alpha$ for $1/T \gg 1/\tau_1$ and making the same assumptions as before, a generalized expression for R_{mb} can be given as

$$R_{mb} \approx \alpha\frac{R_s^2}{R_1}\left(m - v_{C_{1n}}(t)\right) + R_{\text{off}_b}$$
$$R_{mb} = \alpha R_s\left(m - v_{C_{1n}}(t)\right) + R_{\text{off}_b}, \tag{19}$$

where $R_{\text{off}_b} = 1/\alpha k[(2 - \alpha)V_{\text{dc}_1} - V_T]$.

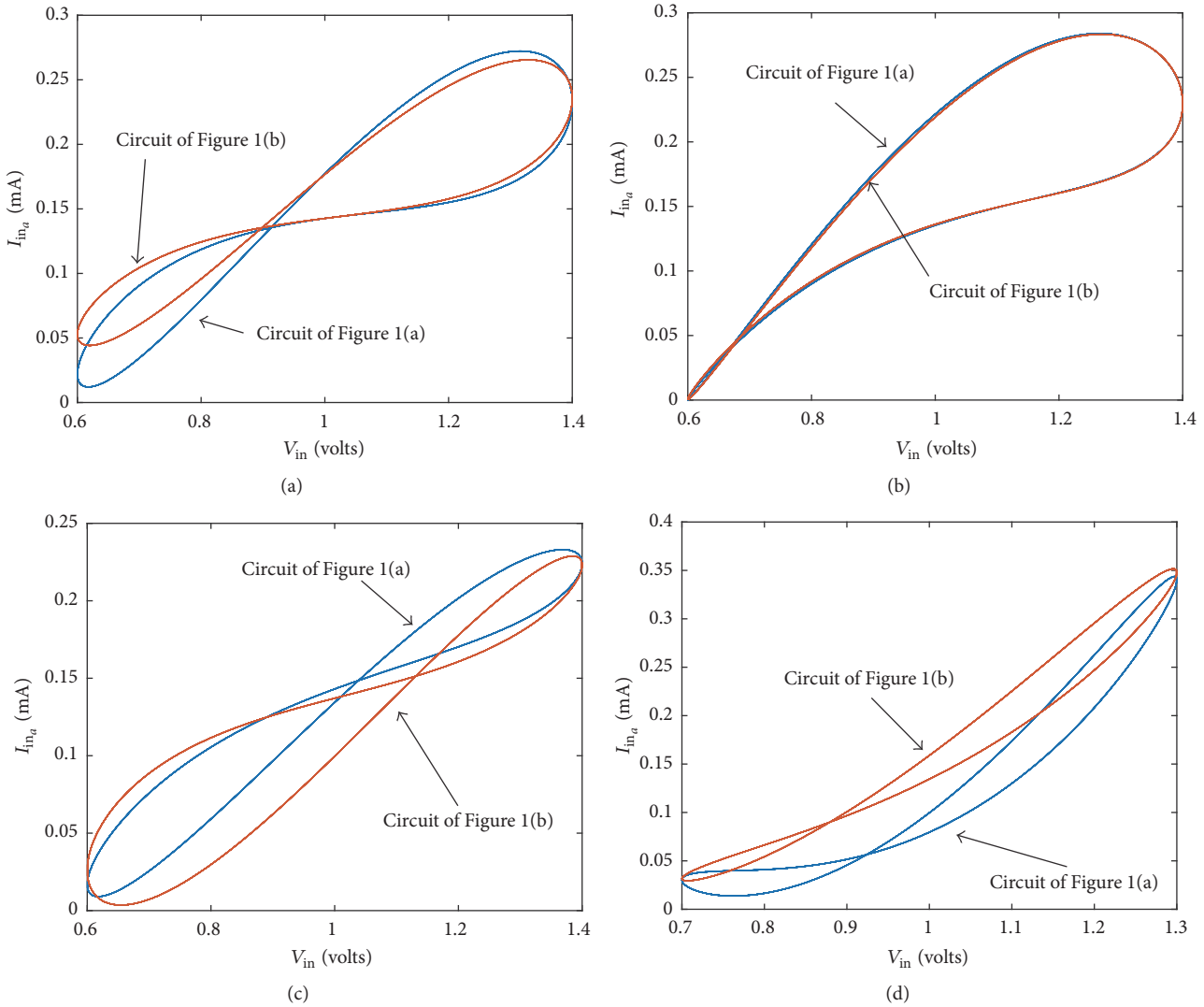

FIGURE 3: Matlab simulation of the *I-V* characteristics of Figures 1(a) and 1(b) as given by (8) and (9), respectively. (a) $\tau_2 = \tau_1 = \tau_z$, $\tau_p = \alpha\tau_z$ with $\alpha = 0.4$. (b) $\tau_2 = 10\tau_1 = \tau_z$, $\tau_p = \alpha\tau_z$ with $\alpha = 0.4$. (c) $\tau_2 = \tau_1 = \tau_z$, $\tau_p = \alpha\tau_z$ with $\alpha = 0.286$ and $V_{\text{dc}_2} = 0.3$ V. (d) $\tau_2 = \tau_1 = 0.1\tau_z$, $\tau_p = \alpha\tau_z$ with $\alpha = 0.33$, $V_{\text{dc}_2} = 0.3$ V, and $A = 0.5$ V and $A = 0.3$ V for Figures 1(a) and 1(b), respectively.

3.1. Numerical Simulations. Sample Matlab plots of (8) and (9) are shown in Figures 3(a)–3(c) to normalized values of $k = 1\ \text{mA/V}^2$, $A = 0.4$ V, $V_{\text{dc}_1} = 1$ V, and $V_T = 0.35$ V. In the first of the plots shown in Figure 3(a), $\tau_2 = \tau_1 = \tau_z$, $\tau_p = \alpha\tau_z$ with $\alpha = 0.4$ and the applied sinusoidal voltage frequency $\omega_o > 1/\tau_1$ and $V_{\text{dc}_2} = 0.4$ V. Note that having $\alpha = 0.4$ is equivalent to setting $V_{\text{dc}_2} = \alpha V_{\text{dc}_1}$ and that $\theta_{2b} \approx \theta_{2a} = \pi/2 - \theta_1$. In this figure, we see that neither loop is symmetrical which is attributed to the $\dot{x}(t)$ and $\dot{x}^2(t)$ terms (see (10)) and the phase shift term introduced by the lossy integrator. In the second plot, shown in Figure 3(b), $\tau_2 = 10\tau_1 = \tau_z$, $\tau_p = \alpha\tau_z$ with $\alpha = 0.4$ and $V_{\text{dc}_2} = 0.4$ V as before but $\theta_{2a} \approx \theta_{2b} \cong 0$. The pinched loops from the two circuits are nearly identical and the upper lobe is far bigger than the lower one. In Figure 3(c), $\tau_2 = \tau_1 = \tau_z$, $\tau_p = \alpha\tau_z$ with $\alpha = 0.286$, $V_{\text{dc}_2} = 0.3$ V, and $\theta_{2b} \approx \theta_{2a} = \pi/2 - \theta_1$. Clearly, as α or V_{dc_2} decreases, the upper lobe decreases in size and the pinch point increases. Note the reduced value of A for the circuit (Figure 1(a) or (8)). This implies that the circuit of Figure 1(a) must work with reduced input amplitudes compared to the circuit of Figure 1(b), unless V_{dc_1} and V_{dc_2} are adjusted in tandem. This is not the case for the circuit of Figure 1(b) where DC bias voltages are related by α which is fixed for $\omega_o > 1/\tau_1$.

Finally, in Figure 3(d), $\omega < 1/\tau_1$ with $\tau_2 = \tau_1 = 0.1\tau_z$, $\tau_p = \alpha\tau_z$, $\alpha = 0.33$, and $V_{\text{dc}_2} = 0.3$ V. Under these conditions, $\theta_{2b} \ll \theta_{2a} = \pi/2 - \theta_1$, and decreased amplitudes must now be used in the circuit of Figure 1(b) or (9) compared to the circuit of Figure 1(a) or (8). Therefore, we select $A = 0.5$ V and $A = 0.3$ V for the two circuits, respectively, in this case.

3.2. Pinch Point Analysis. The unique form of (8) and (9) allows for a closed-loop solution of the pinch-off point in

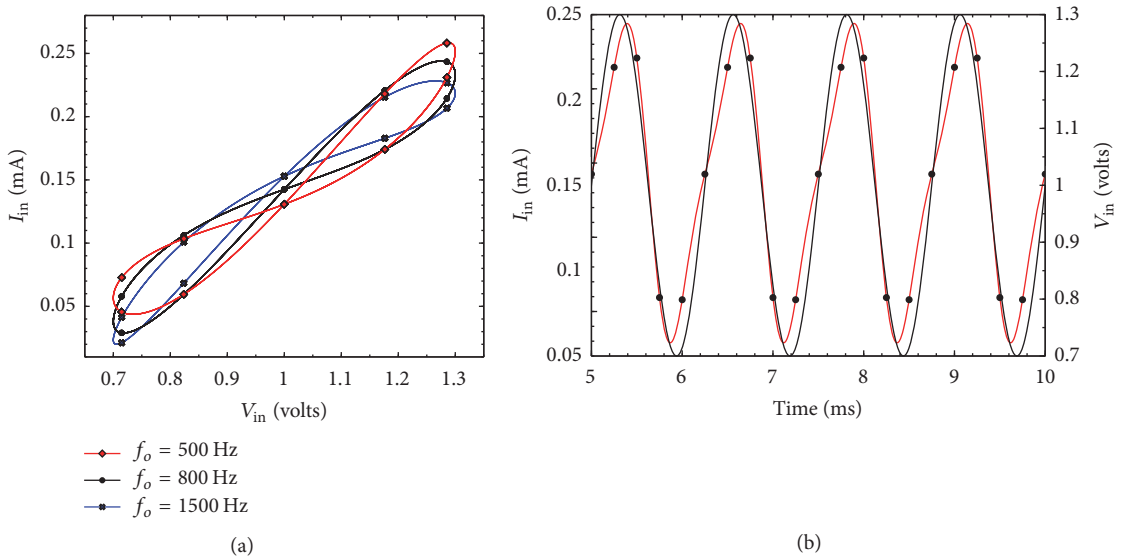

FIGURE 4: (a) Matlab simulation of the *I-V* characteristic of Figure 1(a) governed by (8) to $A = 0.3$ V, $\tau_2 = \tau_1 = 500\,\mu$s, $V_{dc_1} = 1$ V, $V_T = 0.35$ V, $k = 1$ mA/V^2, and $V_{dc_2} = 0.325$ V. (b) Input voltage $v_{in}(t)$ and current $i_{in_a}(t)$ plotted as a function of time at a frequency of $\omega = 2\pi \times 800$ rad/s.

these circuits. It can be shown after considerable simplification that (8) and (9) have a pinch-off point $[\widehat{V}_{in_p}, \widehat{I}_{in_p}]$ given by

$$\begin{aligned}
\widehat{V}_{in_p} &= V_{dc_1} - A\widehat{X}(\Theta),\\
\widehat{I}_{in_p} &= -\widehat{A}\cos\left[2\sin^{-1}(X(\Theta)) + \theta_{2a,2b} - \theta_1\right]\\
&\quad - \widehat{B}\sin\left[\sin^{-1}(X(\Theta)) - \theta_1\right]\\
&\quad - \widehat{C}\sin\left[\sin^{-1}(X(\Theta)) + \theta_{2a,2b}\right]\\
&\quad + \widehat{D}\cos\left[2\sin^{-1}(X(\Theta)) + 2\theta_{2a,2b}\right] + \widehat{E}\\
&\quad + \widehat{I}_{off},
\end{aligned} \tag{20}$$

where

$$\widehat{X}(\Theta) = \frac{\left(\widehat{B}/2\right)\sin(-\theta_1) + \left(\widehat{C}/2\right)\sin(\theta_{2a,2b})}{\widehat{A}\sin(\theta_{2a,2b} - \theta_1) - \widehat{D}\sin(2\theta_{2a,2b})}, \tag{21}$$

and the subscripts a, b refer to (8) and (9), respectively. The frequency dependent nature of (20) makes their analysis difficult; however, several observations can be deduced. First, $\widehat{X}(\Theta)$ can be positive or negative depending on the values of θ_1, θ_{2a}, and θ_{2b} as observed in Figure 3. In addition, C_2 plays an important role even though it is not the main charge holding or integrating capacitor. In Figure 1(a), its minor role is to block V_{dc_1} as V_{dc_2} is passed, but in both circuits, its main contribution is to add a leading phase shift opposed to the lagging phase shift caused by C_1. For example, in the circuit of Figure 1(b), in the absence of C_2, that is, if $C_2 = 0$, then $\sin(\theta_{2b}) = \sin(2\theta_{2b}) = 0$, because $\theta_{2b} = 0$, and with $|H_{2b}(\omega)| = \alpha$, (21) reduces to $\widehat{X}(\Theta) = V_{dc_1}/A$, setting $\widehat{V}_{in_p} = 0$. That is, no pinch point will occur.

Secondly, under the assumption $\tau_2 = \tau_1$, we find that $\widehat{V}_{in_p} = V_{dc_1}$ when $\tan(\theta_1) = \widehat{C}/\widehat{B}$ or when $V_{dc_2} = (V_{dc_1} - V_T)/2$. Under this condition, M_1 remains in triode so long as $V_{dc_1} > 3V_T$ which is easily satisfied. For the general case when $\tau_2 = \beta\tau_1$, implying that $\theta_{2a} \neq \pi/2 - \theta_1$ (unless $\beta = 1$), the general solution to $\widehat{X}(\Theta) = 0$ yields

$$V_{dc_2} = \frac{\beta}{(\beta+1)}\frac{\left(\tau_1^2\omega^2 + 1\right)}{\left(\beta\tau_1^2\omega^2 + 1\right)}\left(V_{dc_1} - V_T\right). \tag{22}$$

Likewise, the value for α in the circuit of Figure 1(b) that results in $\widehat{V}_{in_p} = V_{dc_1}$ can be expressed as

$$\alpha = 1 - \frac{V_T}{V_{dc_1}} - \frac{\omega\tau_1\csc(\theta_{2b})}{\left(\omega^2\tau_1^2 + 1\right)}\sqrt{\frac{1 + \omega^2\tau_p^2}{1 + \omega^2\tau_z^2}}. \tag{23}$$

In both general cases, (22) and (23) are frequency dependent, the exception being when $\beta = 1$ for (22), but both can be minimized for frequency dependance by ensuring that $\omega\tau_1 > 1$, $\omega\tau_z > 1$, and $\omega\tau_p > 1$. Sample plots of the *I-V* characteristic for the circuit of Figure 1(a) governed by (8) to the conditions $A = 0.3$ V, $\tau_2 = \tau_1 = 500\,\mu$s, $V_{dc_1} = 1$ V, $V_T = 0.35$ V, $k = 1$ mA/V^2, and $V_{dc_2} = (V_{dc_1} - V_T)/2 = 0.325$ V are shown in Figure 4(a).

Note that because $\beta = 1$ and $V_{dc_2} = (V_{dc_1} - V_T)/2$, $\widehat{V}_{in_p} = V_{dc_1}$ is independent of the input frequency which is verified at the three frequencies $f_o = [500, 800, 1500]$ Hz, as theoretically predicted. In Figure 4(b), $v_{in}(t)$ and $i_{in_a}(t)$ are plotted as a function of time.

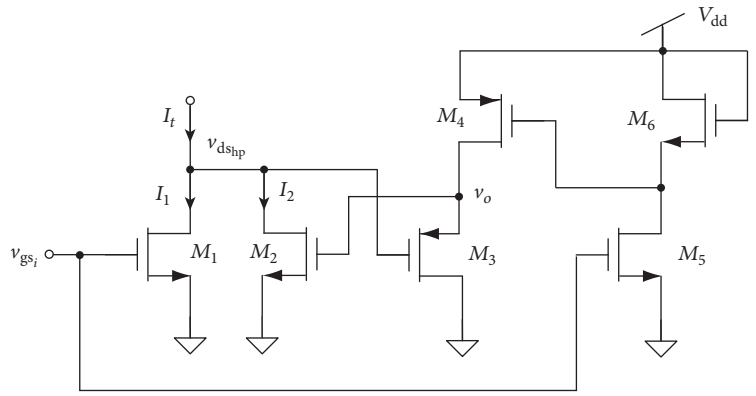

Figure 5: An improved linear resistor obtained by replacing M_1 in Figure 1 with transistors M_{1-6}.

Finally, no pinch point occurs when $\widehat{X}(\Theta) = V_{dc_1}/A$ or $\widehat{X}(\Theta) = -V_{dc_1}/A$ and if $\beta = 1$ this happens at the two frequencies $\omega_{1,2}$:

$$\omega_1 = \frac{1}{\tau_1}\sqrt{\frac{2V_{dc_2} + V_T}{3V_{dc_1} - 2V_{dc_2} - V_T}},$$
$$\omega_2 = \frac{1}{\tau_1}\sqrt{\frac{2V_{dc_1} - 2V_{dc_2} - V_T}{V_{dc_1} + 2V_{dc_2} + V_T}}. \tag{24}$$

Furthermore, if $V_{dc_2} = (1/2)(V_{dc_1} - V_T)$, a unique frequency at which no pinch point exists is

$$\omega_1 = \omega_2 = \frac{1}{\sqrt{2}\tau_1}. \tag{25}$$

In the case of Figure 1(b), no easy closed-loop form of the solution exists, but when $\tau_z = \tau_1$ the frequencies at which the pinch point occurs can be obtained by numerically solving, for ω, the equation

$$\gamma_1\omega^4 + \delta_1\omega^2 + 2(\alpha - 1)V_{dc_1} + V_T = 0, \tag{26}$$

when $\widehat{X}(\Theta) = V_{dc_1}/A$ or

$$\gamma_2\omega^4 + \delta_2\omega^2 + \left(2\alpha V_{dc_1} + V_T\right)\left(\tau_1 - \tau_p\right) + 2V_{dc_1}\tau_p = 0, \tag{27}$$

when $\widehat{X}(\Theta) = -V_{dc_1}/A$, where

$$\begin{aligned}
\gamma_1 &= \tau_p^3\tau_1 V_{dc_1} + \left[(\alpha - 1)V_{dc_1} + V_T\right]\tau_p^2\tau_1^2 + \alpha\tau_p\tau_1^3 V_{dc_1},\\
\delta_1 &= \left[(\alpha - 2)\tau_p^2 + (\alpha + 1)\tau_p\tau_1 + (2\alpha - 1)\tau_1^2\right]V_{dc_1}\\
&\quad + \left(\tau_1^2 + \tau_p^2\right)V_T,\\
\gamma_2 &= \tau_p^4\tau_1 V_{dc_1} + \left[(2 - \alpha)V_{dc_1} - V_T\right]\tau_p^3\tau_1^2\\
&\quad + \left(V_T - V_{dc_1}\right)\tau_p^2\tau_1^3 + \alpha\tau_p\tau_1^4 V_{dc_1},\\
\delta_2 &= \left[(2 - \alpha)V_{dc_1} - V_T\right]\tau_p^3 + \left(V_{dc_1} + V_T\right)\tau_p^2\tau_1\\
&\quad + \left[(2 - \alpha)V_{dc_1} - V_T\right]\tau_p\tau_1^2\\
&\quad + \left[(2\alpha - 1)V_{dc_1} + V_T\right]\tau_1^3.
\end{aligned} \tag{28}$$

4. Linearization of M_1

It is possible to reduce the distortion in M_1 as a result of the $V_{ds}^2/2$ term in (2) by a number of techniques. One such technique is bisection of the input range first popularized by [19–21] and exploited by many others. Consider therefore the circuit shown in Figure 5 where M_1 is replaced by transistors M_{1-6}. Voltages v_{gs_i} and $v_{ds_{hp}}$ form the output voltages of the lossy integrator and high-pass filters, respectively. Transistors $M_{1,2}$ are identical in size as are $M_{3,4}$ and $M_{5,6}$. Transistors $M_{3,4}$ and $M_{5,6}$ are to function as an adder as first proposed by [22] in the use of low voltage multipliers. Under the correct bias conditions, it follows that $v_o = v_{gs_i} + v_{ds_{hp}}$, and then given that both M_1 and M_2 have the same v_{ds} and each drain current is governed by $I_1 = k[(v_{gs_i} - V_T)v_{ds_{hp}} - v_{ds_{hp}}^2/2]$ and $I_2 = k[(v_o - V_T)v_{ds_{hp}} - v_{ds_{hp}}^2/2]$, the total current I_t through M_1 and M_2 simplifies to $I_t = I_1 + I_2 = 2k(v_{gs_i} - V_T)v_{ds_{hp}}$ or an equivalent resistance of $R_{eq} = 1/2k(V_{gs_i} - V_T)$. Under these conditions, (8) and (9) change to

$$\begin{aligned}
i_{in_a}(t) &= -\widetilde{A}\cos\left(2\omega_o t - \theta_1 + \theta_{2a}\right) + \widetilde{B}\sin\left(\omega_o t - \theta_1\right)\\
&\quad + \widetilde{C}\sin\left(\omega_o t + \theta_{2a}\right) + \widetilde{A}\cos\left(\theta_1 + \theta_{2a}\right) + \widetilde{I}_{off},
\end{aligned} \tag{29}$$

and for Figure 1(b)

$$\begin{aligned}
i_{in_b}(t) &= -\widetilde{A}\cos\left(2\omega_o t - \theta_1 + \theta_{2b}\right) + \widetilde{B}\sin\left(\omega_o t - \theta_1\right)\\
&\quad + \widetilde{C}\sin\left(\omega_o t + \theta_{2b}\right) + \widetilde{A}\cos\left(\theta_1 + \theta_{2b}\right) + \widetilde{I}_{off},
\end{aligned} \tag{30}$$

where the new coefficients $\widetilde{A}$, $\widetilde{B}$, and $\widetilde{C}$ are given in Table 3. Comparing (8)-(9) with (29)-(30) and likewise Tables 1 and 3, one notices fewer terms for the linearized resistor, with coefficients $\widetilde{A} = \widehat{A}$ and $\widetilde{B} = \widehat{B}$. In addition, both $\widetilde{C} > \widehat{C}$ and

Table 3: Summary of the coefficients of the input current $i_{\text{in}}(t)$ of Figures 1(a) and 1(b) in response to an input voltage $v_{\text{in}}(t)$ when M_1 is replaced by a linearized resistor such as the one shown in Figure 5.

Coefficient	Figure 1(a)	Figure 1(b)
$\widetilde{A}$	$\frac{1}{2}kA^2\left\|H_1(\omega_o)\right\|\left\|H_{2a}(\omega_o)\right\|$	$\frac{1}{2}kA^2\left\|H_1(\omega_o)\right\|\left\|H_{2b}(\omega_o)\right\|$
$\widetilde{B}$	$kA\left\|H_1(\omega_o)\right\|V_{\text{dc}_2}$	$\alpha kA\left\|H_1(\omega_o)\right\|V_{\text{dc}_1}$
$\widetilde{C}$	$kA\left\|H_{2a}(\omega_o)\right\|\left(V_{\text{dc}_1}-V_T\right)$	$kA\left\|H_{2b}(\omega_o)\right\|\left[V_{\text{dc}_1}-V_T\right]$
$\widetilde{I}_{\text{off}}$	$k\left[\left(V_{\text{dc}_1}-V_T\right)V_{\text{dc}_2}\right]$	$\alpha k\left[V_{\text{dc}_1}-V_T\right]V_{\text{dc}_1}$

$\widetilde{I}_{\text{off}} > \widehat{I}_{\text{off}}$, with all other terms in the coefficients being equal. The corresponding new pinch point $[\widetilde{V}_{\text{in}_p}, \widetilde{I}_{\text{in}_p}]$ is given by

$$\widetilde{V}_{\text{in}_p} = V_{\text{dc}_1} - A\widetilde{X}(\Theta), \tag{31}$$

$$\begin{aligned}\widetilde{I}_{\text{in}_p} = &-\widetilde{A}\cos\left[2\sin^{-1}\left(\widetilde{X}(\Theta)\right)+\theta_{2a,2b}-\theta_1\right]\\ &-\widetilde{B}\sin\left[\sin^{-1}\left(\widetilde{X}(\Theta)\right)-\theta_1\right]\\ &-\widetilde{C}\sin\left[\sin^{-1}\left(\widetilde{X}(\Theta)\right)+\theta_{2a,2b}\right]\\ &+\widetilde{A}\cos\left(\theta_1+\theta_{2a,2b}\right)+\widetilde{I}_{\text{off}},\end{aligned} \tag{32}$$

where

$$\widetilde{X}(\Theta) = \frac{\left(\widetilde{B}/2\right)\sin\left(-\theta_1\right)+\left(\widetilde{C}/2\right)\sin\left(\theta_{2a,2b}\right)}{\widetilde{A}\sin\left(\theta_{2a,2b}-\theta_1\right)}. \tag{33}$$

The benefits to linearizing M_1 are immediately clear upon close inspection of (31)–(33). In particular, for the circuit of Figure 1(a) in the general case when $\tau_2 = \beta\tau_1$, the general solution to $\widetilde{X}(\Theta) = 0$ now yields

$$V_{\text{dc}_2} = \frac{\beta\left(\tau_1^2\omega^2+1\right)}{\left(\beta^2\tau_1^2\omega^2+1\right)}\left(V_{\text{dc}_1}-V_T\right), \tag{34}$$

which, for $\beta = 1$, implies that, for $\widetilde{V}_{\text{in}_p} = V_{\text{dc}_1}$, V_{dc_2} is chosen such that $V_{\text{dc}_2} = V_{\text{dc}_1} - V_T$. Of course, under these conditions, the composite linearized resistor is at the edge of the triode and a more practical solution would be for a given $\beta \neq 1$, ω, and τ_1 to simply choose $\beta(\tau_1^2\omega^2+1)/(\beta^2\tau_1^2\omega^2+1) > V_{\text{dc}_2}/(V_{\text{dc}_1}-V_T)$. For the circuit of Figure 1(b) employing a linearized M_1, the choice of α does not affect the pinch point; however, the value of V_{dc_1} that results in $\widetilde{V}_{\text{in}_p} = V_{\text{dc}_1}$ is given by

$$V_{\text{dc}_1} = \frac{V_T}{1-\omega\tau_1\csc\left(\theta_{2b}\right)\sqrt{\left(1+\tau_p^2\omega^2\right)/\left(1+\tau_z^2\omega^2\right)\left(1+\tau_1^2\omega^2\right)}}, \tag{35}$$

which is still frequency dependent, but minimization is still possible if $\omega\tau_1 > 1$, $\omega\tau_z > 1$, and $\omega\tau_p > 1$. Last but not least, no pinching occurs for the circuit of Figure 1(a) using the linearized resistor at frequencies

$$\begin{aligned}\omega_1 &= \frac{1}{\tau_1}\sqrt{\frac{V_{\text{dc}_2}+V_T}{2V_{\text{dc}_1}-V_{\text{dc}_2}-V_T}},\\ \omega_2 &= \frac{1}{\tau_1}\sqrt{\frac{2V_{\text{dc}_1}-V_{\text{dc}_2}-V_T}{V_{\text{dc}_1}+2V_{\text{dc}_2}+V_T}}\end{aligned} \tag{36}$$

assuming $\tau_2 = \tau_1$ and at

$$\begin{aligned}\omega_1 &= \sqrt{\frac{2V_{\text{dc}_1}-V_T}{V_{\text{dc}_1}\tau_1\tau_p-\tau_1^2\left(V_{\text{dc}_1}-V_T\right)}},\\ \omega_2 &= \sqrt{\frac{\left(2V_{\text{dc}_1}-V_T\right)\tau_p+V_T\tau_1}{\left(\tau_1^3-2\tau_1^2\tau_p-\tau_p^2\right)V_{\text{dc}_1}+\left(\tau_p-\tau_1\right)\tau_1^2V_T}},\end{aligned} \tag{37}$$

for the circuit of Figure 1(b) when $\tau_z = \tau_1 = \alpha\tau_p$.

5. Simulation and Experimental Results

The circuits in Figures 1(a) and 1(b) were simulated and built experimentally. In the sections that follow, simulations of Figures 1(a) and 1(b) without and with linearization of M_1 were conducted. For the experiments, off-the-shelf discrete components were used without linearization of M_1.

5.1. Simulation Results: Without M_1 Linearization. For simulation purposes, Cadence was used employing the Design Kit offered by the AMS 0.35 μm CMOS process. The opamp utilized in simulations is demonstrated in Figure 6, where the bias scheme was $V_{\text{DD}} = -V_{\text{SS}} = 5$ V and $Io = 300\,\mu$A. The MOS transistors' aspect ratio is given in Table 4 with $R_c = 140\,\Omega$ and $C_c = 2$ pF to achieve a phase margin of 60°. Also, the aspect ratio of transistor M_1 in Figure 1(a) was 100 μm/1 μm; for M_2, the aspect ratio was 12 μm/2 μm and thus its gain factor was $k = 1$ mA/V^2.

The resistor and capacitor values used in simulations were $R_1 = 820\,\Omega$ and $C_1 = C_2 = 470$ nF and, therefore, $\tau_1 = \tau_2$. The DC voltages were $V_{\text{dc}_1} = 2$ V and $V_{\text{dc}_2} = 0.74$ V. Considering a sinusoidal input with 700 mV amplitude and variable frequency, the obtained i_{in_a}-v_{in} characteristics, for $f = 600$ Hz, 1 kHz, and 1.5 kHz, are demonstrated in Figure 7. The time-domain behavior of the scheme in Figure 1(a) is demonstrated in Figure 8 for a 1 kHz input voltage. Likewise,

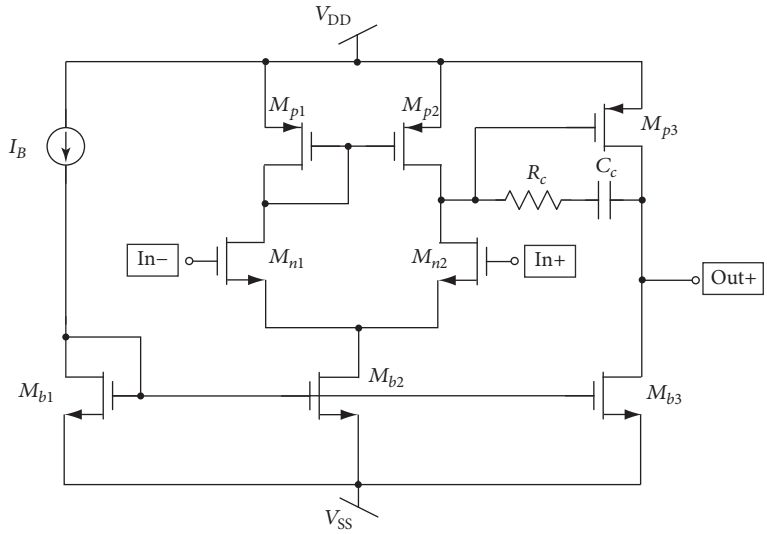

Figure 6: Opamp used in simulations.

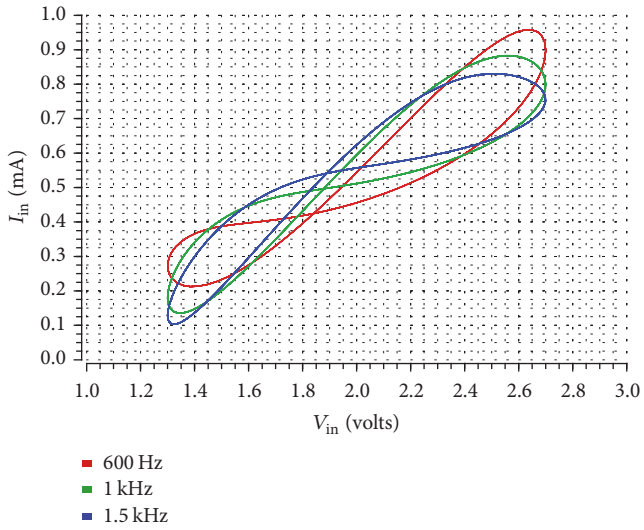

Figure 7: Simulated i_{in_a}-v_{in} characteristics for f = 600 Hz, 1 kHz, and 1.5 kHz.

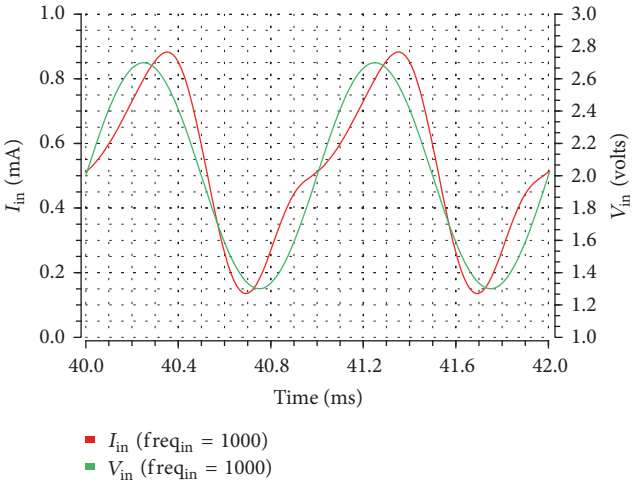

Figure 8: Time-domain behavior of the circuit in Figure 1(a) for f = 1 kHz.

Table 4: MOS transistors' aspect ratio for Figure 6.

Transistor	W/L
M_{b1}	50 μm/2 μm
M_{b2}-M_{b3}	100 μm/2 μm
M_{n1}-M_{n2}	200 μm/0.5 μm
M_{p1}-M_{p2}	50 μm/0.5 μm
M_{p3}	200 μm/0.5 μm

the obtained i_{in_b}-v_{in} characteristics, for Figure 1(b) for f = 400 Hz, 700 Hz, and 2 kHz, are demonstrated in Figure 9 with the corresponding time-domain behavior shown in Figure 10 for a 700 Hz input voltage.

The effect of r_2 in the operation of the topology in Figure 1(b) has also been studied under the conditions $r_2 = 0.4r_1$, $0.56r_1$, and $0.7r_1$, which sets α = 0.26, 0.36, and 0.41, respectively. The derived $i_{in_b} - v_{in}$ characteristics, for f = 700 Hz, are given in Figure 11.

5.2. Simulation Results: With M_1 Linearization. The improved linear resistor shown in Figure 5 was also used for linearizing transistor M_1. The power supply voltage was equal to 2 V and the aspect ratio of M_1-M_2 and M_5-M_6 was 1 μm/2 μm, while for M_3-M_4 it was 3.2 μm/2 μm. Considering a sinusoidal input with 700 mV amplitude and variable frequency, the obtained i_{in_a}-v_{in} characteristics, for the circuit in Figure 1(a), derived at the same conditions as in the previous subsection, and for f = 600 Hz, 1 kHz, and 1.5 kHz, are demonstrated in Figure 12. The corresponding

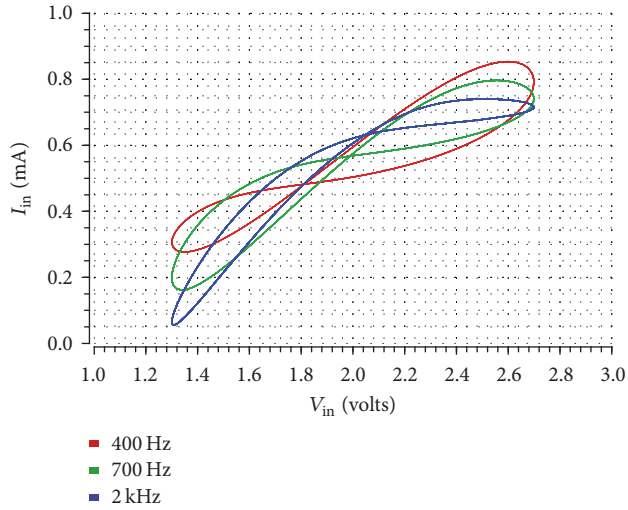

FIGURE 9: Simulated i_{in_b}-v_{in} characteristics for f = 400 Hz, 700 Hz, and 2 kHz.

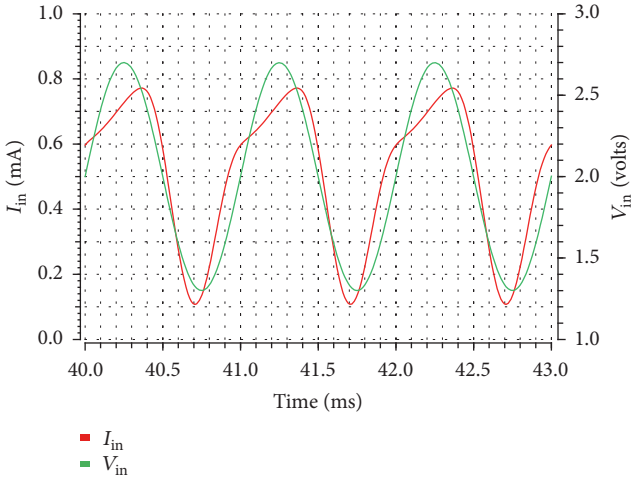

FIGURE 10: Time-domain behavior of the circuit in Figure 1(b) for f = 700 Hz.

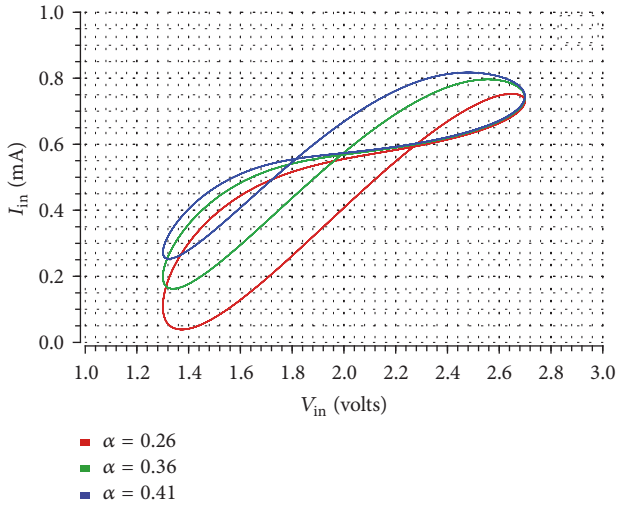

FIGURE 11: Simulated i_{in_b}-v_{in} characteristics for α = 0.26, 0.36, and 0.41.

time-domain behavior is depicted in Figure 13 for a 1 kHz input voltage.

In a similar way, the plots for the circuit in Figure 1(b), obtained at the same conditions as in the previous subsection, are given in Figure 14. The time-domain behavior is given in Figure 15 for a 700 Hz input voltage.

5.3. Experimental Results. In the first of a series of experimental tests, the circuit of Figure 1(a) was constructed using 741 opamps powered by a ±15 V supply. The resistor and capacitor values used were $R_1 = R_2 = 820\,\Omega$ and $C_1 = C_2 = 470$ nF ensuring that $\tau_1 = \tau_2$. Transistors M_1 and M_2 were taken from Fairchild's dual complementary pair CD4007CN chip. The DC biasing voltages used were V_{dc_1} = 4.6 V, $V_{dc_2} = 1.12$ V, and = 1 V_{pp}. The current i_{in_a} was measured by inserting a 10 Ω resistor in series with v_{in} and measuring the voltage drop across this resistor using an instrumentation amplifier with a gain of 10; that is, $i_{in_a} = v_{10\Omega}$. The results of v_{in} versus i_{in_a} are shown in Figure 16 for several frequencies starting at 1 kHz with the pinch point remaining nearly constant for $V_{dc_2} = 1.12$ V. Note that this result is consistent with (22) where SPICE models for the CD4007 (the actual value of V_T is both foundry and process dependent but unfortunately actual data on the CD4007CN chips used was not available) place V_T in the order of around 2~2.3V. Bending of the lobes can be observed towards a downward trend when the frequency is decreased below 1 kHz and upwards when the frequency is increased above 1 kHz. The usable range of this circuit was found to be from 300 Hz to 10 kHz. Note that the lower frequency limit on the operation of the circuit (300 Hz) is also consistent with (25) where, for $V_{dc_2} = (1/2)(V_{dc_1} - V_T)$, $R_1 = 820\,\Omega$, $C_1 = 470$ nF, with $\tau_1 = \tau_2$, yields a calculated value of $\omega_{1,2} = 292$ Hz. The upper frequency limit was observed when the lobes

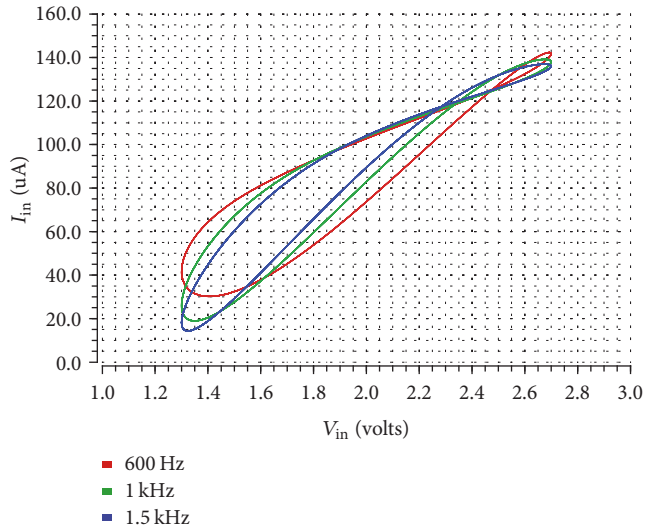

FIGURE 12: Simulated i_{in_a}-v_{in} characteristics for the circuit in Figure 1(a) with f = 600 Hz, 1 kHz, and 1.5 kHz and linearization of M_1.

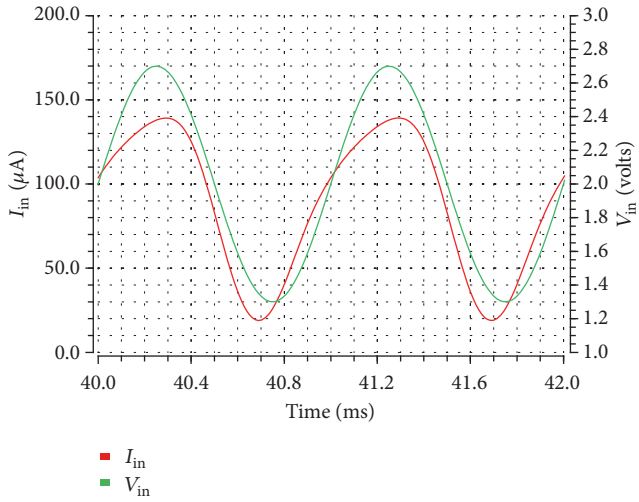

FIGURE 13: Time-domain behavior of the circuit in Figure 1(a) for f = 1 kHz and linearization of M_1.

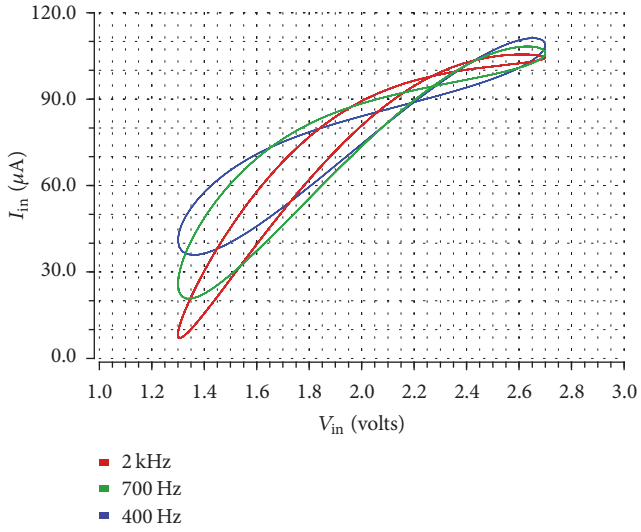

FIGURE 14: Simulated i_{in_b}-v_{in} characteristics for the circuit in Figure 1(b) with f = 400 Hz, 700 Hz, and 2 kHz and linearization of M_1.

of the pinch hysteresis were too close to be distinguishable and in addition would also be set by limitations associated with A_2 losing gain in its closed-loop configuration with M_2.

In a second experimental test, the circuit of Figure 1(b) was set up and the resistor and capacitor values used were $R_1 = r_2 = 2\,\text{k}\Omega$ and $C_1 = C_2 = 470\,\text{nF}$ ensuring that $\tau_z = \tau_1$. The current i_{in_b} was likewise measured through a 10 Ω resistor using an instrumentation amplifier set to a gain of 10. Resistor r_1 was adjusted by a potentiometer at a value of $r_1 = 1031\,\Omega$ which set $\alpha = 0.34$. Input voltages were set at $V_{dc_1} = 4\,\text{V}$ and $A = 3\,\text{V}_{pp}$ and the initial frequency was set at 700 Hz. The results shown in Figure 17 indicate that the pinch point and symmetry of the lobes are highly dependent on the input frequency. For this configuration, pinching was lost for frequencies below 300 Hz and above 10 kHz.

Finally, it should be mentioned that the circuits of Figures 1(a) and 1(b) were also tested using different time constants such as $\tau_1 \neq \tau_2$ and $\tau_1 \neq \tau_z$ and all results not shown here were consistent with the expected theory.

6. Conclusion

Two simple nonlinear circuits that exhibit unipolar pinched hysteresis behavior were presented in this paper. The multiplication-type nonlinearity between a state variable and its past history, as given in (1), is fundamental in obtaining pinched hysteresis although the past history can also be replaced by the rate of change of the present state as shown in [3]. In this work, this multiplication is simply achieved

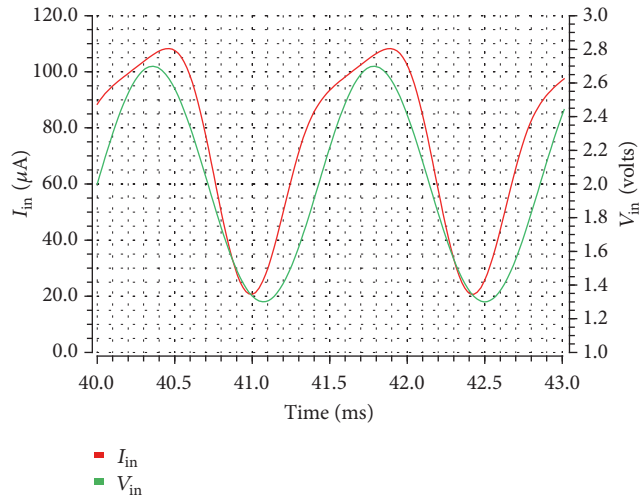

FIGURE 15: Time-domain behavior of the circuit in Figure 1(b) for $f = 700$ Hz and linearization of M_1.

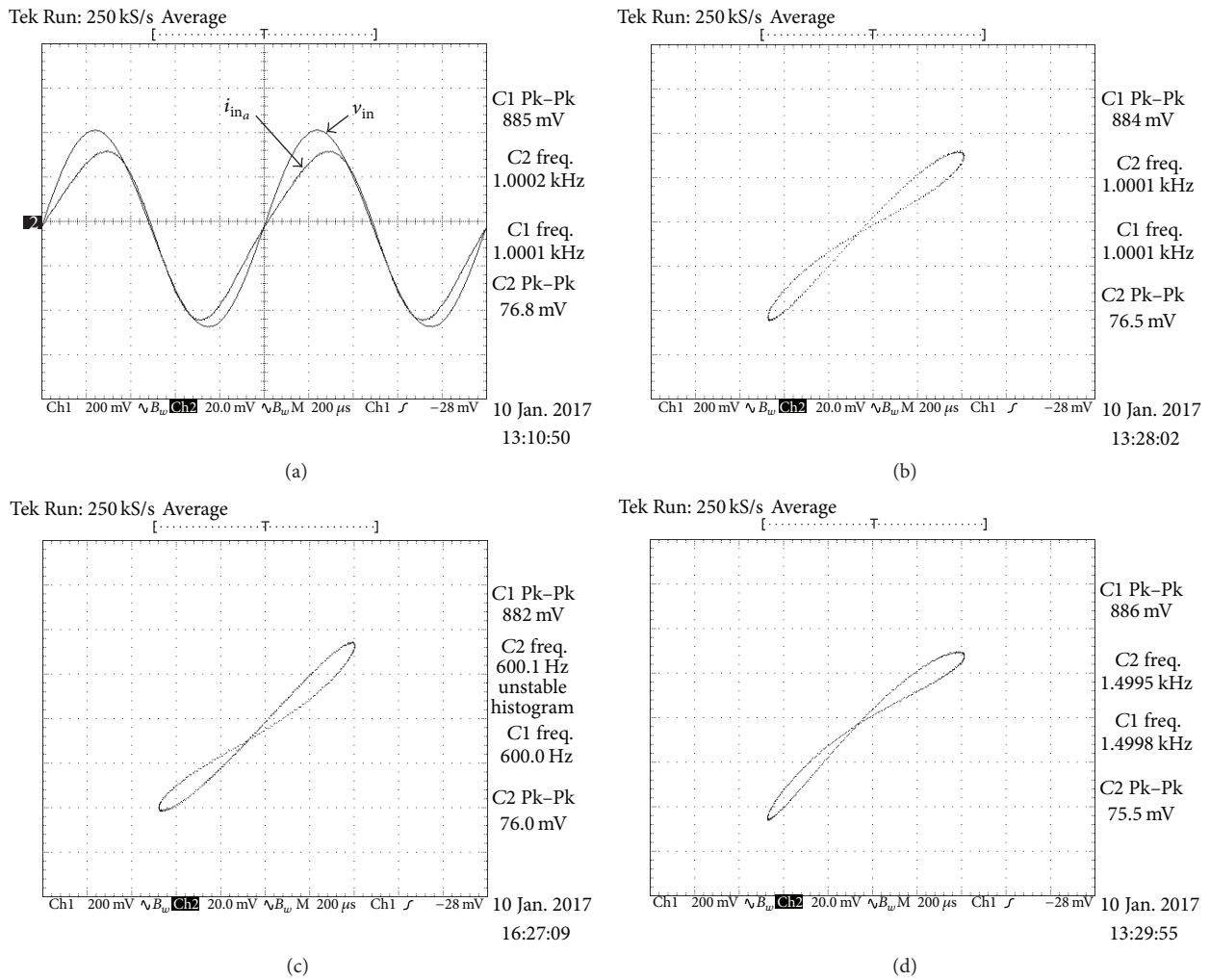

FIGURE 16: (a) Experimental results of the plot of $v_{in}(t)$ and $i_{in_a}(t)$ at 1 kHz for the circuit of Figure 1(a). (b) Oscilloscope trace of the pinched hysteresis loop of the memristor emulator circuit of Figure 1(a) at 1 kHz, (c) at 600 Hz, and (d) at 1.5 kHz.

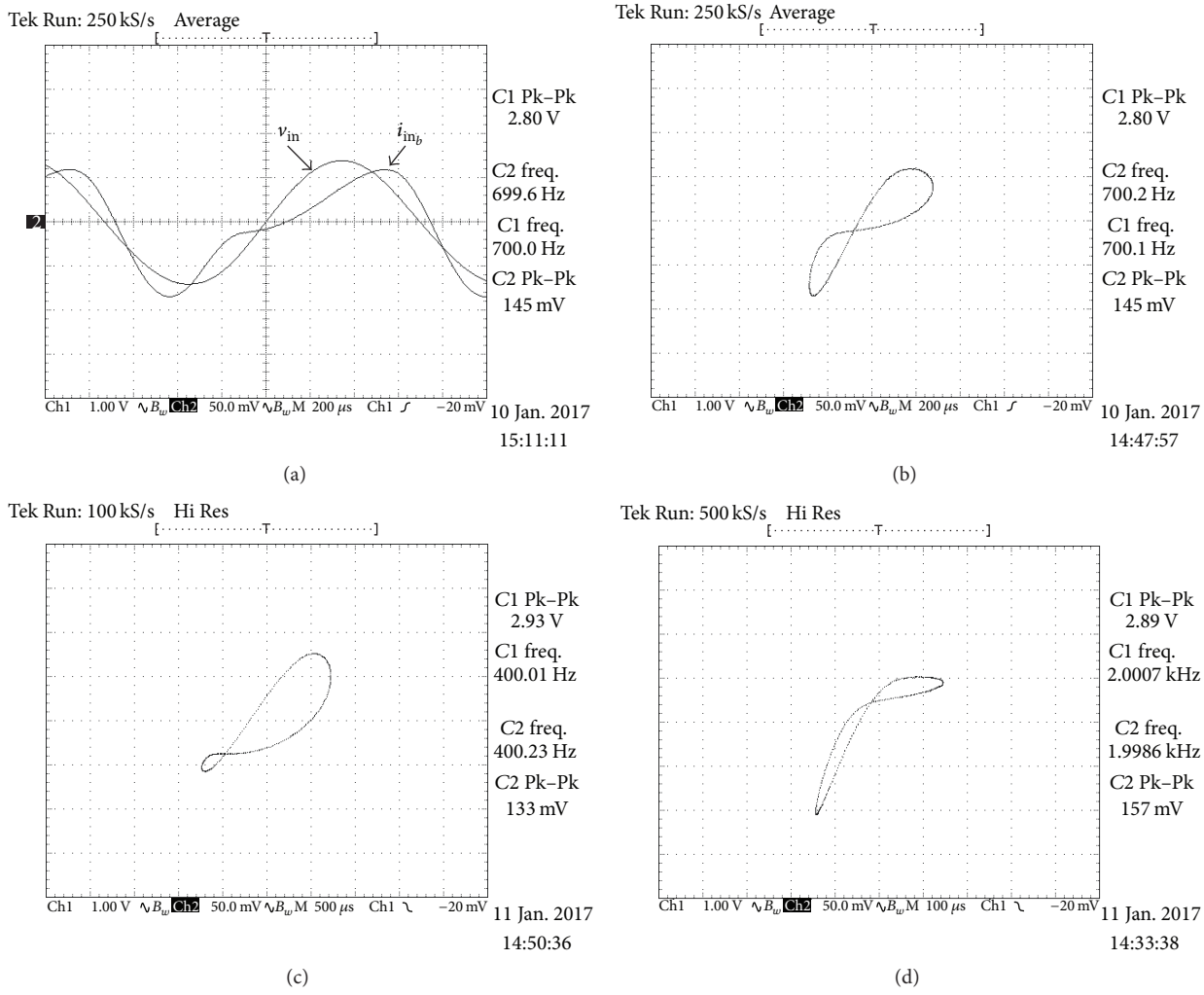

FIGURE 17: (a) Experimental results of the plot of $v_{in}(t)$ and $i_{in_b}(t)$ at 700 Hz for the circuit of Figure 1(b). (b) Oscilloscope trace of the pinched hysteresis loop at 700 Hz, (c) at 400 Hz, and (d) at 2 kHz.

using the MOS transistor transconductance equation. The proposed circuits have been analyzed, their pinch points were determined, and their behavior was verified in Matlab and experimentally. A method of linearization that enables the elimination of undesired higher-order nonlinear terms was also examined and verified via simulations in Cadence. Of significant importance in this work is the clarification of the role played by the charge holding capacitor in the value of the charge-controlled memristance. We argue that, in all solid-state devices that have been fabricated and that show pinched hysteresis, a parasitic capacitor combined with a modulation-type (multiplication-type) nonlinearity is behind the appearance of this behavior. Arguably, the authors of [18] conclude that both "memory resistance and memory capacitance must coexist."

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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