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Research Article

An Improved Control Strategy for a Four-Leg Grid-Forming Power Converter under Unbalanced Load Conditions

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This paper proposes an improved multiloop control strategy for a three-phase four-leg voltage source inverter (VSI) operating with highly unbalanced loads in an autonomous distribution network. The main objective is to balance the output voltages of the four-leg inverter under unbalanced load conditions. The proposed control strategy consists of a proportional-integral (PI) voltage controller and a proportional current loop in each phase. The voltage controller and the current control loop are, respectively, used to regulate the instantaneous output voltage and generate the pulse width modulation (PWM) voltage command with zero steady-state tracking error and fast transient response. A voltage decoupling feedforward path is also used to enhance the system robustness. Since the outer voltage loop operates in the synchronous reference frame, tuning and stability analysis of the PI controller is far from being straightforward. In order to cope with this challenge, the stationary reference frame equivalent of the voltage controller in the rotating frame is derived. Subsequently, a systematic design based on a frequency response approach is provided. Simulation results are also carried out using the DIgSILENT PowerFactory software to verify the effectiveness of the suggested control strategy.

1. Introduction

Poor operational efficiency, gradual depletion of fossil-fuel resources, and environmental pollution are the main problems associated with traditional power systems [1–3]. These serious issues have led to a considerable attempt to generate power using renewable energy sources (RES) at the low voltage level [4, 5]. For applications in renewable energy and distributed generation (DG), there is a need to use power electronic inverters to convert DC power into a controlled AC power [6]. Conventionally, the inverters used in distribution networks behave like voltage sources when they operate independently [7]. On the other hand, they behave as current sources, when they are directly connected to the utility grid [8]. The change of operational mode from autonomous mode to grid-connected mode or vice versa may cause the change of their controllers' scheme. The most important distinguishing feature of a voltage source inverter (VSI) is that there is no need to change its controller, when the operation mode is changed [7]. Therefore, it is commonly used in distribution networks, due to its proper capability to operate in both grid-connected and islanded modes [8]. Here, the autonomous operation of VSIs is considered. However, to achieve a stable and secure operation, a number of technical and regulatory issues have to be resolved before VSIs can become commonplace in distribution networks.

Since most traditional six-switch inverters are designed for three-phase three-wire systems, their controllers are quite suitable for balanced three-phase loads. In many low voltage distribution systems, the loads can be a mixture of single-phase and three-phase ones, resulting in unbalanced voltage problems [9]. Unbalance voltage conditions can lead to adverse effects on equipment and the electric distribution system [10]. Malfunction of protection devices, power electronic converters, and adjustable speed drives are the main challenges caused by unbalanced loads in distribution

networks [9, 10]. To cope with this challenge, a neutral line is needed to provide a current path for unbalanced loads in a three-phase four-wire system. Hence, it is important to use a proper inverter topology to balance the output voltages of critical loads.

So far, various VSI topologies are introduced for proper operation in a three-phase four-wire distribution network. The use of a three-leg inverter topology in three-phase four-wire systems with a costly and bulky Δ-Y transformer is popular due to trapping zero sequence currents in the Δ winding. In this topology, the control of the inverter is only responsible for compensating the voltage drops caused by positive and negative sequence currents on the output filter of the inverter in the Δ side of the transformer. Nonetheless, the zero sequence currents may cause voltage drops in the Y-side of the transformer that the three-leg inverter cannot handle this challenge [11]. The three-leg inverter with a split DC-link capacitor has also been extensively used in the literature because of its simple structure [12, 13]. However, it needs an expensive and a large capacitor to achieve equal voltage sharing between the split capacitors. Moreover, capacitor voltage balancing is another challenge with this topology [14]. The three-phase four-leg VSI plays an important role in the proper operation of three-phase four-wire distribution networks because of its superior performance characteristics in handling unbalanced conditions. The provision of the fourth leg in four-leg VSIs can result in controlling the phase voltages independently. Indeed, the independently controlled phase voltages allow four-leg inverters to provide balanced output voltages even under unbalance load conditions.

To date, various control methods have been proposed in the literature to balance the output voltage of a three-phase four-leg VSI in autonomous mode. The proportional-resonant (PR) controller in the stationary reference frame has been commonly used for balancing the output voltage of the four-leg inverter due to its superior performance in eliminating the steady-state error, while regulating sinusoidal signals [17]. However, it is sensitive to frequency variations and the phase shift of current sensors. The proportional-integral (PI) controller in the *dq* frame is also widely used and works well with pure DC signals [15, 16, 18, 19]. This approach operates based on the extraction of the symmetrical components of the unbalanced signals in the *dq* frame. Nonetheless, the use of filters to obtain the symmetrical components of the unbalanced signals leads to low crossover frequency, which may cause a slow dynamic response. In another approach, a combination of the *dq* frame and the stationary reference frame is utilized to compensate distorting effects of nonlinear and unbalanced loads in a standalone distribution system [20]. The integral controllers in the *dq* frame are responsible for compensating the positive and negative sequence distortions, while a zero-damping bandpass filter is employed in the stationary reference frame to compensate the zero sequence distortion. However, the effectiveness of the proposed scheme is only presented for the steady-state condition, and the zero steady-state error for the zero sequence component is not truly achieved.

In this paper, an improved per-phase control scheme for a three-phase four-leg VSI operating with highly unbalanced loads in an autonomous distribution network is presented. The main objective is to effectively balance the output voltages of the four-leg inverter under extremely unbalanced load conditions. The proposed control strategy consists of an outer voltage loop and an inner current loop in each phase. The outer voltage controller and the inner capacitor loop are, respectively, utilized to regulate the instantaneous output voltage and currents. A voltage decoupling feedforward is also used to improve the system robustness. The main advantages of the method are the simplicity, low steady-state voltage tracking error, and fast transient response.

The rest of this paper is organized as follows. Section 2 describes the model of the four-leg inverter. Section 3 presents the proposed per-phase multiloop control of the four-leg inverter in the *dq* frame. The stationary reference frame equivalent model of the PI controller in the *dq* synchronous reference frame is derived in Section 4. The design of the current loop and the voltage control are presented in Sections 5 and 6, respectively. The carrier-based pulse width modulation (PWM) method for the generation of the inverter output voltages is also explained in Section 7. Simulation results are provided in Section 8. Finally, the conclusion gives a brief summary and critique of the findings.

2. System Modeling

Figure 1 shows the power stage of a four-leg grid-forming inverter and its LC output filter connected to unbalanced loads in an autonomous three-phase four-wire distribution network [21]. Since the LC filter yields better performance than the L filter and is less complicated than the LCL filter, the LC filter represents a suitable compromise for the system intended for use in this paper. The LC filter parameters are chosen such that the unwanted components in the four-leg inverter output voltage are attenuated effectively and the inverter current ripple is reduced admissibly using the method presented in [17]. The loads can be placed either in line-to-line or line-to-neutral connection. It is worth noting that the neutral line of the autonomous four-wire system is provided by connecting the fourth legs of the four-leg inverter to the neutral point of loads. The additional leg regulates the load zero sequence voltage [22]. To minimize the switching frequency ripple imposed on the neutral current inverter (I_n), a neutral inductor (L_n) is also used.

The carrier-based pulse width modulation (PWM) technique is selected to produce three output voltages independently because of its simplicity and ease of implementation [23]. Since the four-leg inverter is assumed to be powered by an ideal constant DC voltage source, no controller is needed to regulate the DC-link voltage, and it is possible to consider that the DC-link voltage is constant throughout this study [5]. Table 1 presents the parameters of the four-leg VSI.

To describe the behavior of the circuit depicted in Figure 1, the following quantities for voltages and currents can be defined:

$$V_{\text{pwm}} = \begin{bmatrix} V_{Af} & V_{Bf} & V_{Cf} \end{bmatrix}^T, \tag{1}$$

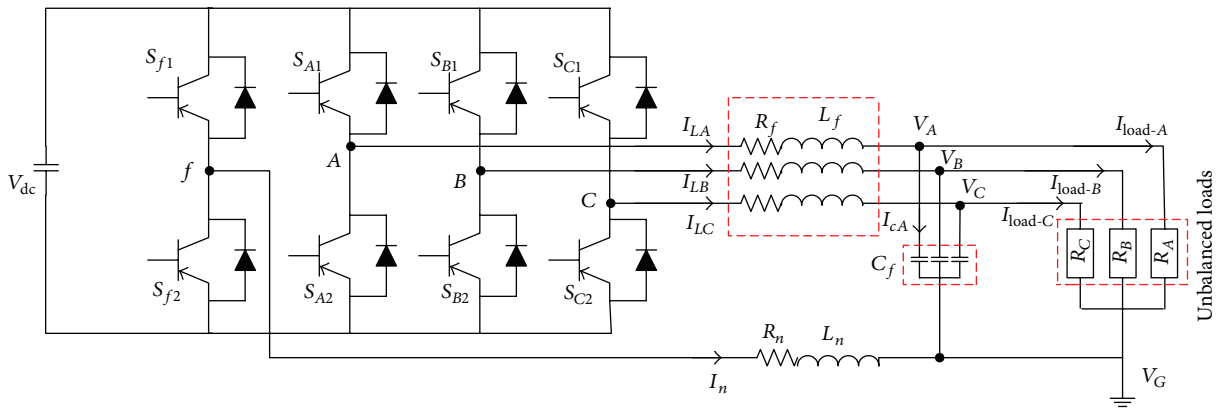

Figure 1: Power stage of a three-phase four-leg VSI.

Table 1: System parameters.

Parameter	Description	Value
f_s	Switching frequency	5 kHz
w_f	Fundamental frequency	$2\pi 60$ rad/s
L_f and L_n	Filter inductance	0.1 mH
C_f	Filter capacitance	300 μF
R_f and R_n	Resistor of the filter inductance	10 mΩ
V_{dc}	DC-link voltage	300 V

where V_{pwm} is the vector of three-phase inverter output line-to-neutral PWM voltages.

$$I_{inv} = \left[I_{lA} \;\; I_{lB} \;\; I_{lC}\right]^T,$$
$$I_{load} = \left[I_{load\text{-}A} \;\; I_{load\text{-}B} \;\; I_{load\text{-}C}\right]^T, \quad (2)$$
$$V_{load} = \left[V_A \;\; V_B \;\; V_C\right]^T.$$

By applying Kirchhoff voltage and current laws to the power stage of the three-phase four-leg VSI, the following equations can be obtained [21].

$$V_{load} = R_f I_{inv} + L_f \frac{dI_{inv}}{dt} + V_{pwm} - R_n I_n - L_n \frac{dI_n}{dt}.$$
$$I_{inv} = I_{load} + C_f \frac{dV_{load}}{dt}. \quad (3)$$

The control system tuning and stability analysis of the four-leg inverter can be performed on a per-phase basis [7]. Hence, the power stage of the four-leg inverter is modeled according to the principles of the per-phase basis so that only a single-phase representation of the inverter is used for the analysis and design [9]. Figure 2 illustrates the per-phase representation of the four-leg inverter for one phase to neutral connection [2, 9]. As can be seen, the fundamental component of the switched voltage of each phase and the connected load to that phase are modeled as an ideal controlled voltage source (uV_{dc}, which u is the control variable) and a current source (I_o), respectively. In this figure, I_L and V_c are also

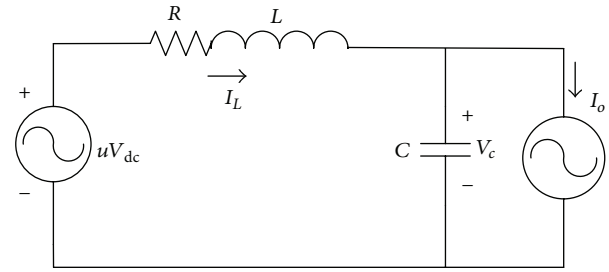

Figure 2: Basic per-phase representation of the four-leg inverter in each phase.

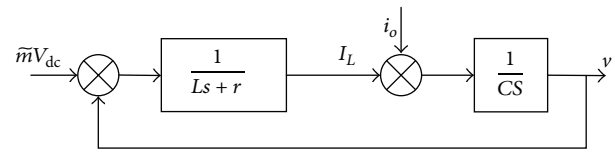

Figure 3: Average switching model of the four-leg VSI in each phase.

the respective phase inductor current and capacitor voltage, respectively.

For implementation of a single-phase system in the synchronous reference frame, it is necessary to generate a pseudo-two-phase system [2]. In this two-phase system, one component is obtained from the original single-phase system (α) and an orthogonal signal (β) must be created from the original single-phase signal. Based on Figure 2, the differential equations representing the model of the single-phase system in the $\alpha\beta$ frame can be written as

$$L\frac{di_{l,\alpha\beta}}{dt} = uV_{dc,\alpha\beta} - v_{c,\alpha\beta} - Ri_{l,\alpha\beta},$$
$$C\frac{dv_{c,\alpha\beta}}{dt} = i_{l,\alpha\beta} - i_{o,\alpha\beta}. \quad (4)$$

The average switching model of the four-leg VSI in each phase is depicted in Figure 3. This is obtained by assuming that the switching frequency is much higher than the fundamental frequency. As can be seen from Figure 3, $\widetilde{m}$ (the function of modulating signal) is used instead of the control variable,

which represents the average value of u over one cycle of switching frequency.

3. Per-Phase Control Scheme

The independently controlled phase voltages allow the four-leg inverter to provide balanced output voltages under highly unbalanced load conditions. The per-phase control scheme is used in this paper due to its superior performance in providing balanced output voltages under extremely unbalanced load conditions. In this control scheme, three legs are switched independently from each other so that voltages can be regulated in their output filter capacitors. The fourth leg of the inverter provides a zero voltage at the neutral point of the inverter using the proposed controller and carrier-based PWM technique [23].

The implementation of the independent control of the single-phase system in the dq frame needs to create a secondary orthogonal signal from each original phase signal through a complex orthogonal signal generation (OSG) technique [5]. Several attempts have been made in the literature to generate an orthogonal signal from an original single-phase signal such as second-order generalized integrator, Kalman filter, and first-order all-pass filter (APF) methods [24–27]. In this paper, the orthogonal signal is generated based on the reference values of the d- and q-axes [28, 29]. The proposed method exhibits improved steady-state and dynamic performances in comparison with the inverters equipped with the conventional orthogonal signal generation techniques.

The structure of the suggested control scheme for phase "A" is presented in Figure 4. The control system consists of an inner current loop and an outer voltage loop in each phase. The main function of the external voltage loop is to control the instantaneous output voltages within the standard limits. The inner current loop is also adopted to generate the switching states of the PWM modulator. In addition, it improves the transient and steady-state performances of the proposed control scheme. A voltage decoupling feedforward (v^*) is also used to enhance the control system robustness [2]. It is noteworthy that the capacitor current is employed as the feedback signal in the inner loop due to its superior performance in rejecting disturbances rather than the inductor current. Furthermore, the use of the capacitor current is much easier and more cost-effective than the inductor current. According to the basic principles of control theory of cascaded control, these loops can be designed independently as long as the dynamics of the voltage loop is designed to be slower than the internal current controller [2].

The voltage loop operates in the synchronous reference frame, whereas the inner current loop functions in the stationary coordinate system. In the outer loop, V_{cA} is the A-phase output voltage of the filter capacitor to the neutral line. V_α and V_β are the real and the orthogonal components of V_{cA} in the stationary reference frame, respectively. The dq components of the A-phase output voltage of the filter capacitor can be generated by applying the Park transformation, after creating the pseudo-two-phase system. A simple phase locked loop (PLL) is used to obtain the $\sin\theta$ and $\cos\theta$ terms [30]. The PI controllers are utilized in the voltage loop to regulate the instantaneous output voltages in the dq frame. The reference voltages for the three phases have equal amplitudes but are separated from the other voltages by a phase angle of 120°. The q-component of the reference voltages in each phase (V_q^*) is set at 0, whereas the d-component (V_d^*) is set at the peak value of the reference phase voltage.

The reference signal of the internal current loop is provided by employing the inverse Park transformation to the output signals of the output voltage controller. As shown in Figure 4, only the α-axis quantity generated by the outer voltage loop is fed to the internal current controller for compensation. It is the real signal of the two-phase system. Afterwards, the inner loop generates the switching states of the PWM using a simple proportional controller. The design approach of the proposed control strategy is discussed in detail in the following sections.

4. Stationary Reference Frame Representation of the PI Controller in the dq Frame

In the proposed control strategy, the PI controller regulates the instantaneous output voltages of the inverter in the synchronous reference frame, whereas the simple proportional controller regulates the current in the stationary reference frame. Hence, the stability analysis and design of the whole closed-loop system is not straightforward. To successfully cope with this challenge, the stationary frame equivalent model of the PI controller is derived in this section [26, 27]. The equivalent model of the used PI controller in the stationary reference frame is depicted in Figure 5. In this block, $i^*_{c,\alpha\beta}$ stands for outputs, whereas $E_{\alpha\beta}$ stands for inputs. The G_P is the transfer function of the proportional gain (K_P), and G_I is the transfer function of the integral controller (K_I).

The equivalent model of the PI controller depicted in Figure 5 can be considered as a two-input-two-output system. It can be explained in the time domain as

$$\begin{bmatrix} i^*_{c,\alpha}(t) \\ i^*_{c,\beta}(t) \end{bmatrix} = \begin{bmatrix} \cos(w_f t) & -\sin(w_f t) \\ \sin(w_f t) & \cos(w_f t) \end{bmatrix} \left\{ \begin{bmatrix} G_{PI}(t) & 0 \\ 0 & G_{PI}(t) \end{bmatrix} * \left\{ \begin{bmatrix} \cos(w_f t) & \sin(w_f t) \\ -\sin(w_f t) & \cos(w_f t) \end{bmatrix} \begin{bmatrix} E_\alpha(t) \\ E_\beta(t) \end{bmatrix} \right\} \right\}, \quad (5)$$

where $*$ is the convolution operator.

The Laplace transformation is used for both sides of (5). After some mathematical manipulation it can be written as

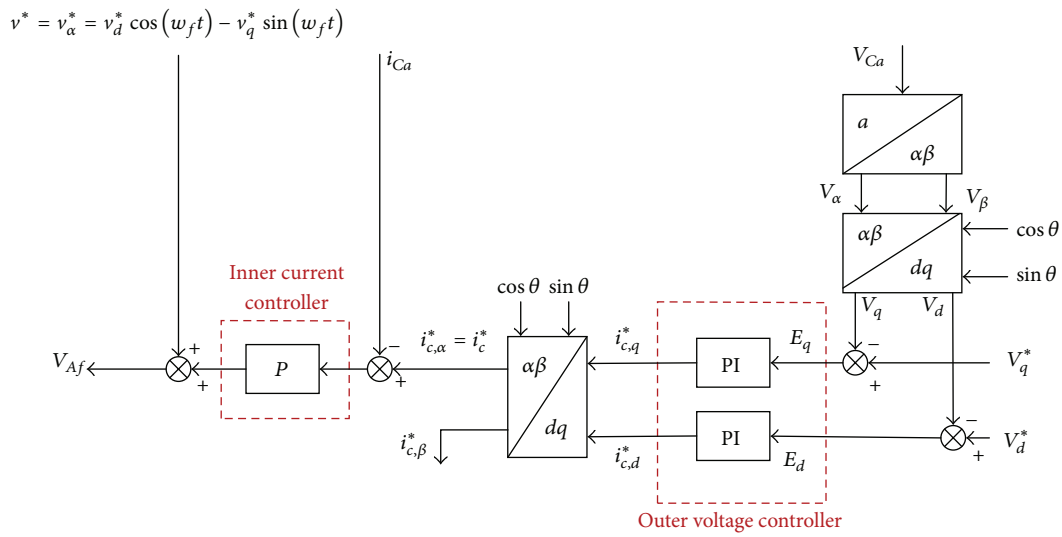

FIGURE 4: Per-phase cascaded controller for the four-leg inverter in phase "A."

$$\begin{bmatrix} i_{c,\alpha}^*(s) \\ i_{c,\beta}^*(s) \end{bmatrix} = \frac{1}{2} \begin{bmatrix} G_{PI}(s+jw_f) + G_{PI}(s-jw_f) & -jG_{PI}(s+jw_f) + jG_{PI}(s-jw_f) \\ +jG_{PI}(s+jw_f) - jG_{PI}(s-jw_f) & G_{PI}(s+jw_f) + G_{PI}(s-jw_f) \end{bmatrix} \begin{bmatrix} E_\alpha(s) \\ E_\beta(s) \end{bmatrix}. \quad (6)$$

In (6), G_{PI} can be replaced by $K_P + K_I/s$. After performing some mathematical manipulation this yields

$$\begin{bmatrix} i_{c,\alpha}^*(s) \\ i_{c,\beta}^*(s) \end{bmatrix} = \begin{bmatrix} K_P + \dfrac{K_I s}{s^2 + w_f^2} & -\dfrac{K_I w_f}{s^2 + w_f^2} \\ \dfrac{K_I w_f}{s^2 + w_f^2} & K_P + \dfrac{K_I s}{s^2 + w_f^2} \end{bmatrix} \begin{bmatrix} E_\alpha(s) \\ E_\beta(s) \end{bmatrix}. \quad (7)$$

Lastly, the transfer function of the real reference current $i_{c,\alpha}^*$ to the real voltage error E_α by replacing $E_\beta(s) = ((w_f - s)/(w_f + s))E_\alpha(s)$ can be obtained as

$$i_{c,\alpha}^*(s) = \frac{a_3 s^3 + a_2 s^2 + a_1 s + a_0}{s^3 + w_f s^2 + w_f^2 s + w_f^3} E_\alpha(s) = H(s) E_\alpha(s), \quad (8)$$

where $a_3 = K_P$, $a_2 = K_P w_f + K_I$, $a_1 = K_P w_f^2 + 2w_f K_I$, and $a_0 = K_P w_f^3 - K_I w_f^2$.

$H(s)$ is the stationary reference frame representation of the PI controller in the dq frame. Figure 6 shows the Bode plot of transfer function $H(s)$ for a typical controller in $w_f = 2\pi 60$ rad/s. From this figure, it can be concluded that for fundamental frequency, the phase and amplitude characteristics of the PI controller in the dq frame are equivalent to the PR controller in the stationary reference frame. The use of this technique considerably simplifies the stability analysis and control parameter design.

5. Design of the Current Controller

The block diagram of the inner current loop is presented in Figure 7. A simple proportional controller is used for injecting clean current to the PWM [28, 29]. In spite of the complex structure of the PI compensator, the proportional controller provides more simplicity for the stability analysis and control parameter design. Moreover, it can prevent unwanted phase delays from the reference signal [5]. However, the use of the proportional controller in the internal loop requires a high proportional gain to eliminate the steady-state error. To successfully overcome this challenge, a feedforward path is adopted to simultaneously improve the performance of the inner loop and reduce the required control effort.

Since it can be assumed that Z is the load impedance and $i_o = v/Z$, the closed-loop transfer function of the inner loop can be written as

$$G(s) = \frac{i_c}{i_c^*} = \frac{CZKs}{LCZs^2 + (CZ(r+K) + L)s + (r+Z)}. \quad (9)$$

It is obvious that the performance of the internal controller significantly depends on the load impedance and controller parameters. The Bode plot of the corresponding transfer function with a typical value for the proportional compensator in different loading conditions is shown in Figure 8.

It can be seen that the minimum bandwidth can be achieved at the nominal load. Hence, the proportional gain of the current controller must be tuned under nominal loading conditions to ensure the expected bandwidth in the inner loop. The proportional gain value of the current loop can

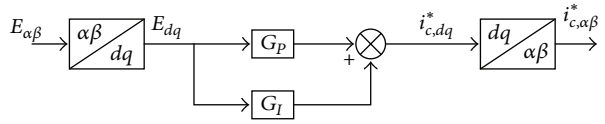

Figure 5: Equivalent control block.

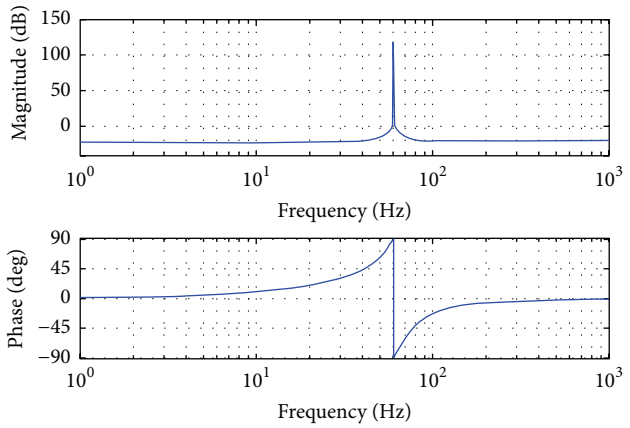

Figure 6: Bode plot of transfer function $H(s)$ for $K_P = 0.1$ and $K_I = 10$.

be calculated using $|G(jw_{bi})|^2 = 1/2$ and assuming that w_{bi} is the required bandwidth of the inner loop. Hence, the proportional gain can be obtained as

$$K = \frac{L + rCZ + \sqrt{2rCZ\left(rCZ + L\right) + L^2\left(2 + C^2Z^2w_{bi}^2\right)}}{CZ}. \quad (10)$$

Basically, the required bandwidth must be selected lower than the switching frequency to put a limit on the inner loop response to the switching noise. Hence, it is chosen as one-fourth of the switching frequency. From (10) and with $w_{bi} = 2\pi(0.25 \times (f_s = 5\,\text{kHz}))\,\text{kHz} \cong 8\,\text{krad/s}$, the proportional gain of the inner current loop is set on 1.

6. Design of the Voltage Controller

The next step after determining the gain of the inner loop is to design the outer voltage loop. The block diagram of the cascaded controller and its simplified block diagram are illustrated in Figure 9. In this figure, the internal controller and the external loop are, respectively, replaced by $G(s)$ and $H(s)$. Moreover, $v^* = v^*_\alpha = v^*_d\cos(w_f t) - v^*_q\sin(w_f t)$ is the voltage decoupling feedforward to enhance the system robustness. The Bode plots of the open-loop transfer function of the simplified block diagram for $K = 1$, $K_P = 0.1$, and $K_I = 0$ under different loading conditions are depicted in Figure 10. The effect of various loading conditions on the outer loop performance can be investigated from this figure. It can be observed that the stability of the closed-loop system and the phase margin under light-load or no-load conditions are moderately decreased.

To guarantee the proper performance of the inverter in all load conditions, the PI regulator is designed under light-load conditions. Since, under light-load conditions, the load impedance tends to infinity ($Z \to \infty$), the transfer function of (9) can be approximated as

$$\frac{i_c}{i_c^*} \cong \frac{K}{Ls + r + K}. \quad (11)$$

Additionally, by assuming that the inverter operates under the light-load condition, the open-loop and closed-loop transfer functions of the control system can be written as (12) and (13), respectively:

$$\frac{v}{v^* - v} = \frac{K\left(a_3s^3 + a_2s^2 + a_1s + a_0\right)}{LCs^5 + bs^4 + bw_fs^3 + bw_f^2s^2 + (r+K)Cw_f^3s}. \quad (12)$$

$$\frac{v}{v^*} = \frac{K\left(a_3s^3 + a_2s^2 + a_1s + a_0\right)}{LCs^5 + bs^4 + \left(bw_f + Ka_3\right)s^3 + \left(bw_f^2 + Ka_2\right)s^2 + \left((r+K)Cw_f^3 + Ka_1\right)s + Ka_0}. \quad (13)$$

In the PI controller, the proportional gain and the integral parameter should be accurately selected to ensure a fast transient response and zero tracking steady-state error. The selection of the proportional gain is a compromise between the stability of the controller and the desired voltage regulation bandwidth. In this study, the proportional gain is chosen so that the required bandwidth (w_{bv}) can be achieved for (13). On the other hand, the integral gain is chosen so that the minimum steady-state error for the outer loop can be ensured. In this case, the selection of the proportional parameter is performed based on this assumption that the dynamic of the voltage loop is unaffected by the integral gain. In other words, the proportional gain is responsible for the transient response, whereas the steady-state response is determined by the integral parameter at the fundamental frequency. Hence, it can be assumed that $K_I = 0$, during tuning the proportional parameter. Based on this assumption, the transfer function of the closed-loop system in the frequency domain and under light-load condition can be rewritten as

$$\frac{v}{v^*} = \frac{K_PK}{K_PK - LCw^2 + j(r+K)Cw}. \quad (14)$$

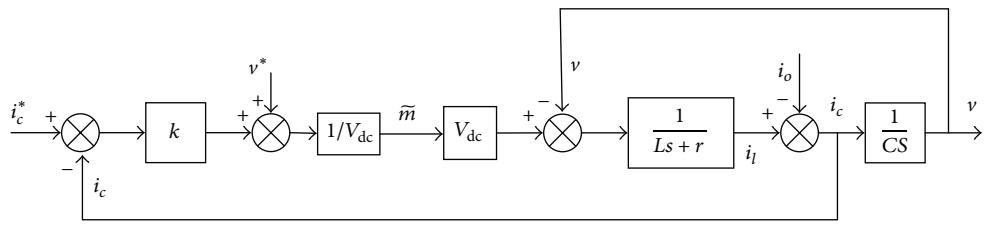

Figure 7: Block diagram of inner current control loop.

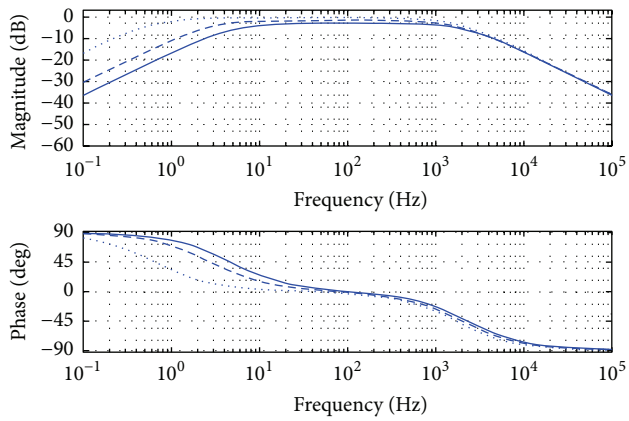

Figure 8: Bode plots of $G(s)$ for $K = 1$, under (solid line) nominal load, (dashed line) one-fifth of nominal load, and (dotted line) one-tenth of nominal load.

Assuming that the expected bandwidth is w_{bv}, K_P can be obtained as

$$K_P = \frac{Cw_{bv}\left[\sqrt{2L^2w_{bv}^2 + K^2} - Lw_{bv}\right]}{K}. \tag{15}$$

In practice, in order to achieve a satisfactory tradeoff between the disturbance rejection and the proper transient response in inverter applications, the system bandwidth must be selected between ten times of the fundamental frequency and one-tenth of the switching frequency. In this study, it is chosen as 550 Hz, which is a value between 600 Hz and 500 Hz. Consequently, the system bandwidth and the proportional gain can be determined as $w_{bv} = 2\pi \times 550\,\text{Hz} \simeq 3\,\text{krad/s}$ and 0.15, respectively. The next step is to determine the integrator gain of the PI controller. The stability analysis is used to achieve an accurate value for integral parameter. The use of the Routh-Hurwitz criterion can be satisfied by the integrator objectives in the voltage loop. The system characteristic polynomial can be written as

$$LCs^5 + bs^4 + \left(bw_f + Ka_3\right)s^3 + \left(bw_f^2 + Ka_2\right)s^2 + \left((r+K)Cw_f^3 + Ka_1\right)s + Ka_0 = 0. \tag{16}$$

By applying the Routh-Hurwitz criterion, the system stability analysis can discriminate as

$$K > 0,$$
$$K_P > 0, \tag{17}$$
$$K_I < K_P \times w_f.$$

The proportional gain of the PI controller has been already determined. Therefore, the value of $K_P \times w_f$ can be calculated equal to 55. To evaluate the performance of the system stability, the open-loop Bode plots of $H(s)G(s)/Cs$ for different values of K_I are depicted in Figure 11. What is interesting in this figure is that K_I has no effect on the phase margin. It is noteworthy that an infinitive magnitude at the fundamental frequency provides a zero steady-state error. However, it has a considerable influence on the operation of the controller in the area near the fundamental frequency. Additionally, based on the stationary reference frame equivalent of the integral term in Figure 6, which affects the system performance in vicinity of the fundamental frequency, the integral gain should be minimized to ensure that the integral term does not affect other frequencies. Indeed, this gain should be selected enough lower than the stability criterion in applications where variations of the fundamental frequency are expected, which may happen in the case of autonomous grids. Hence, the choice of K_I should be done based on a tradeoff between eliminating the steady-state error and not affecting other frequencies. Based on this compromise and the Routh-Hurwitz criterion, K_I is chosen to be 42.

7. The Carrier-Based PWM Method for the Generation of the Inverter Output Voltage

Kim and Sul [23] propose a voltage modulation technique on the basis of a triangular carrier wave for three-phase four-leg VSIs to make three lines to neutral output voltages using an additional leg. In this modulation method, the concept of offset voltage is implemented using a single carrier. The method has a strong performance and can be implemented easily. Therefore, it is used in this study to generate the inverter output voltage.

The block diagram of the used PWM scheme is shown in Figure 12. In this figure, V_{Af}, V_{Bf}, V_{Cf} are the "α" component generated by the proposed cascaded controller. N stands for the fictive midpoint of the DC link, and V_{fN} is the offset voltage, which is calculated quite different from three-phase three-leg VSI using (18). The output voltages of the four-leg

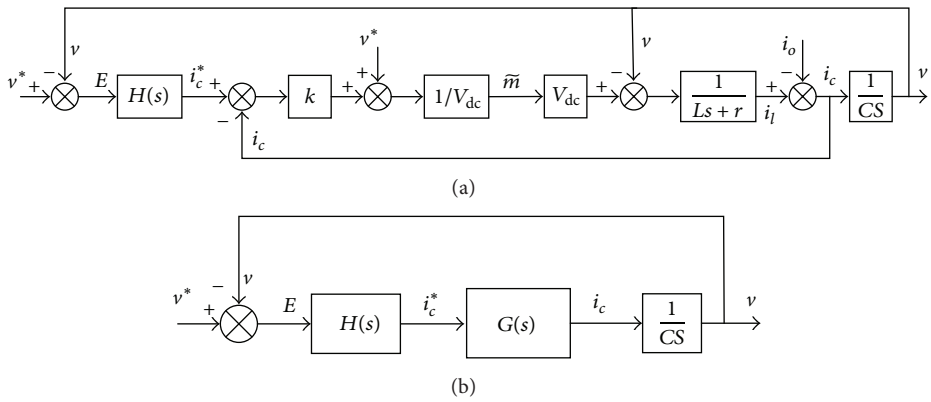

FIGURE 9: (a) Block diagram of the suggested control scheme. (b) Its simplified representation.

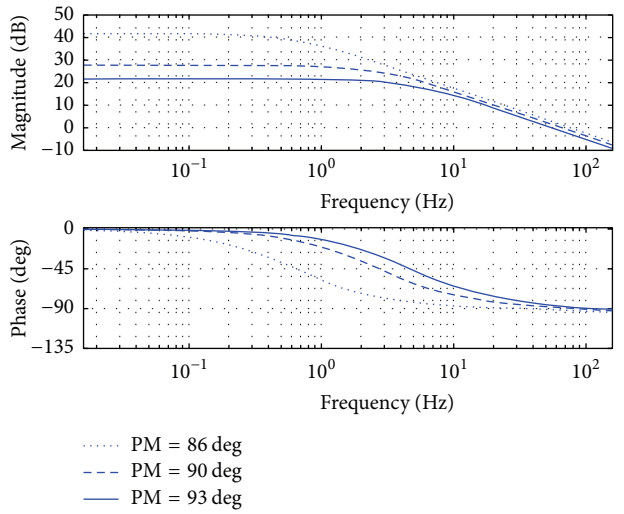

FIGURE 10: Bode plots of $H(s)G(s)/Cs$, for $K = 1$, $K_P = 0.1$, and $K_I = 0$, under (solid line) nominal load, (dashed line) one-fifth of nominal load, and (dotted line) one-tenth of nominal load.

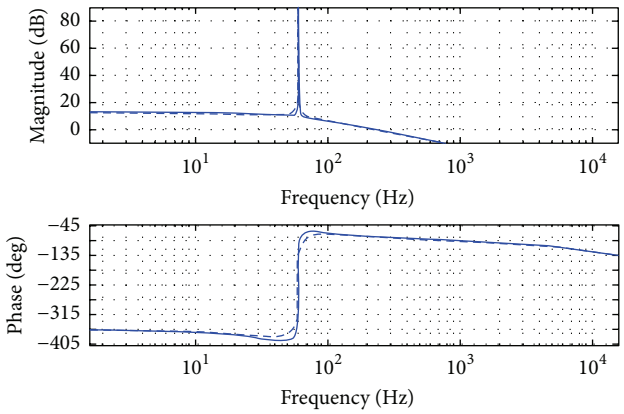

FIGURE 11: Open-loop Bode plots of $H(s)G(s)/Cs$, for $K = 1$, $K_P = 0.15$, and $K_I = 10$ (solid line), for $K = 1$, $K_P = 0.15$, and $K_I = 20$ (dashed line).

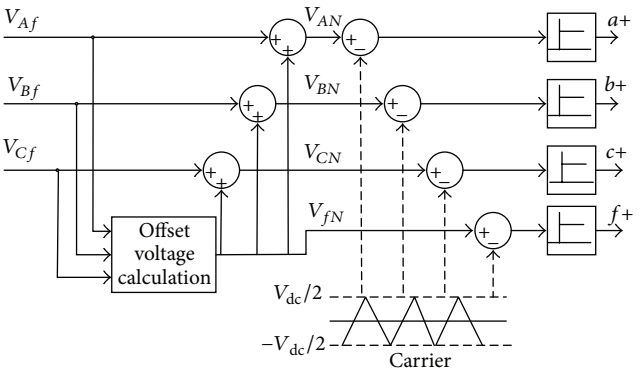

FIGURE 12: Block diagram of the used PWM scheme for the four-leg inverter.

inverter (V_{AN}, V_{BN}, V_{CN}) and pertaining constraint can be obtained by (19) and (20). Moreover, the ON-times of the upper switch of respective legs can be obtained as (21):

$$V_{fN} = \text{mid}\left(-\frac{V_{\max}}{2}, -\frac{V_{\min}}{2}, -\frac{V_{\max} + V_{\min}}{2}\right). \quad (18)$$

$$V_{AN} = V_{Af} + V_{fN},$$

$$V_{BN} = V_{Bf} + V_{fN}, \quad (19)$$

$$V_{CN} = V_{Cf} + V_{fN},$$

$$-V_{\text{dc}} \le V_{Af}, V_{Bf}, V_{Cf} \le V_{\text{dc}}, \quad (20)$$

$$T_A = \frac{T_s}{2} + \frac{V_{AN}}{V_{\text{dc}}} T_s,$$

$$T_B = \frac{T_s}{2} + \frac{V_{BN}}{V_{\text{dc}}} T_s,$$

$$T_C = \frac{T_s}{2} + \frac{V_{CN}}{V_{\text{dc}}} T_s, \quad (21)$$

$$T_F = \frac{T_s}{2} + \frac{V_{fN}}{V_{\text{dc}}} T_s,$$

where T_s is the period of the triangular carrier.

Table 2: System parameters for the simulation study.

Load voltage	155.56 V/phase (peak)
Frequency	60 Hz
Current controller parameter	$K = 1$
PI voltage controller parameters	$K_P = 0.15$, $K_I = 42$
Balanced load	$R_A = R_B = R_C = 8\,\Omega$
Unbalanced loads	(1) $R_A = 10\,\Omega$, $R_B = 7\,\Omega$, $R_C = 8\,\Omega$ (2) $R_A = R_B = 8\,\Omega$, $R_C = \infty$ (3) $R_B = 8\,\Omega$, $R_A = R_C = \infty$

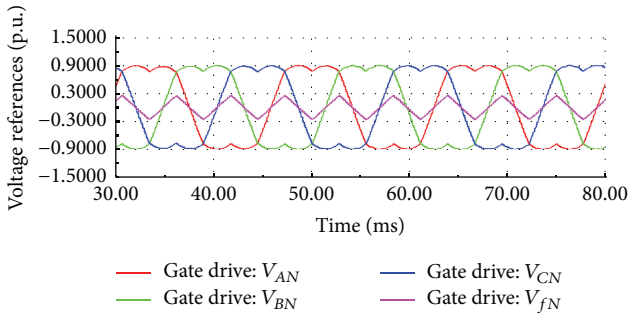

Figure 13: Three-phase pole voltage references and the offset voltage reference.

8. Simulation Results

To validate the performance of the proposed control strategy, the test system of Figure 1 has been simulated in the DIgSILENT PowerFactory software. The four-leg VSI is equipped with the suggested control scheme. The types of loads are resistive, and other parameters of the system are presented in Table 2. Different simulation case studies under various load scenarios are carried out to determinate the effectiveness of both the steady-state and the transient performances of the suggested control scheme.

8.1. Steady-State Performance. The evaluation of the steady-state behavior of the proposed control strategy is made for a three-phase balanced load ($R_A = R_B = R_C = 8\,\Omega$) and three various unbalanced load cases, including ($R_A = 10\,\Omega$, $R_B = 7\,\Omega$, $R_C = 8\,\Omega$), ($R_A = R_B = 8\,\Omega$, $R_C = \infty$), and ($R_B = 8\,\Omega$, $R_A = R_C = \infty$).

8.1.1. With a Three-Phase Balanced Load. The purpose of this part is to investigate the steady-state performance of the suggested controller strategy when a three-phase balanced load is connected to the four-leg VSI. The balanced load includes a resistor of $8\,\Omega$ for each phase. The three-phase pole voltage references (V_{AN}, V_{BN}, V_{CN}) and the offset voltage reference (V_{fN}) are shown in Figure 13. It can be seen from this figure that the three-phase four-leg VSI has the considerable ability to provide desired pole voltage references with the expected amplitude for the three-phase balanced load.

The output waveforms of load voltages, load currents, and neutral current for the four-leg VSI for the balanced load are also depicted in Figure 14. The results indicate that the proposed control strategy is capable of regulating the fundamental component of the load voltage close to the desired peak for the balanced load.

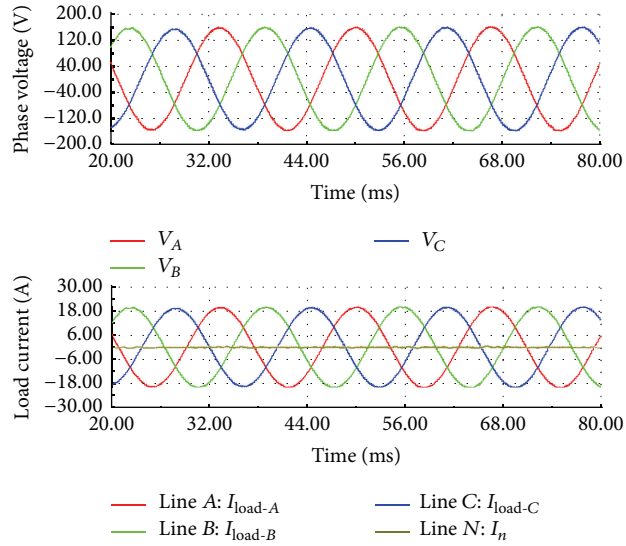

Figure 14: Steady-state load voltages, load currents, and neutral current for the balanced load.

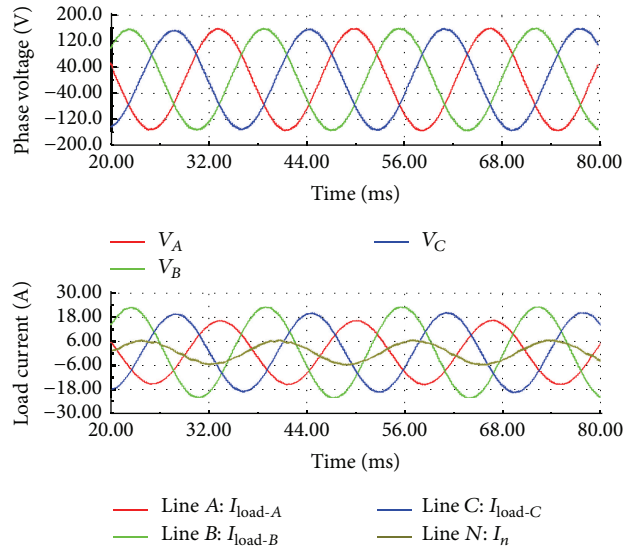

Figure 15: Steady-state load voltages and currents for the unbalanced load ($R_A = 10\,\Omega$, $R_B = 7\,\Omega$, and $R_C = 8\,\Omega$).

8.1.2. With Single-Phase and Three-Phase Unbalanced Loads. In this part, the steady-state performance of the proposed control strategy for various unbalanced load cases, including ($R_A = 10\,\Omega$, $R_B = 7\,\Omega$, $R_C = 8\,\Omega$), ($R_A = R_B = 8\,\Omega$, $R_C = \infty$), and ($R_B = 8\,\Omega$, $R_A = R_C = \infty$) are investigated. The simulation results of load voltages and currents for these different unbalanced load scenarios are depicted in Figures 15–17. Since the control structure adopts separate controller for each phase, the unbalanced loads have no influence on the

Table 3: Comparison of two control strategies in steady-state.

Load type	Conventional control scheme				Proposed control strategy			
	Load peak voltages (V)			PVUR (%)	Load peak voltages (V)			PVUR (%)
	Phase A	Phase B	Phase C		Phase A	Phase B	Phase C	
Balanced	155.32	155.55	155.54	0.096	155.50	155.54	155.56	0.021
Unb. 1	155.25	155.52	155.58	0.128	155.38	155.49	155.56	0.062
Unb. 2	155.15	155.56	155.6	0.184	155.23	155.52	155.75	0.173
Unb. 3	155.55	155.65	155.15	0.192	155.79	155.25	155.45	0.188

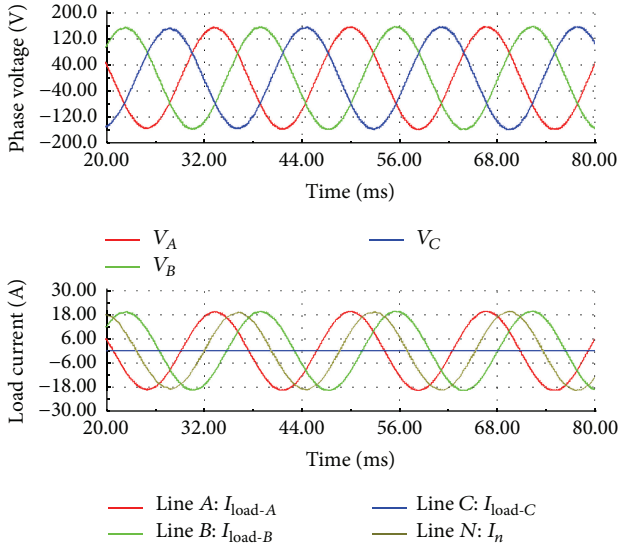

Figure 16: Steady-state load voltages and currents for the unbalanced load ($R_A = R_B = 8\,\Omega$, and $R_C = \infty$).

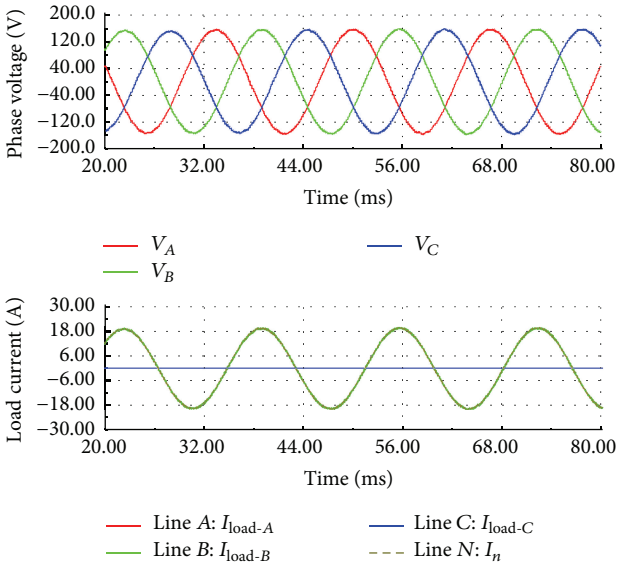

Figure 17: Steady-state load voltages and currents for the unbalanced load ($R_B = 8\,\Omega$, $R_A = R_C = \infty$).

voltage controller performance, and the load voltages remain balanced. From these figures, it is apparent that the proposed control technique has a significant ability to provide balanced output voltages for the four-leg VSI even under extremely unbalanced load condition containing a single-phase load between the phase and neutral.

According to the IEEE standards, the voltage imbalance needs to be maintained low, below 2% for sensitive loads [30, 31]. The performance of the suggested multiloop control strategy has been compared with the conventional control scheme [15, 16], with the same specification for the inner and outer control loops. In order to evaluate the value of phase voltage unbalance rate (PVUR), the magnitudes of the fundamental components of the three-phase voltages and the PVUR of all tested scenarios for both the conventional and the suggested control schemes are presented in Table 3. The results show that the load voltages can remain balanced in steady-state for both the conventional and the proposed control scheme at all tested conditions. Moreover, the value of the PVUR is maintained below 2% at all tested conditions for both control strategies. However, the steady-state performance of the suggested per-phase control scheme is improved because of avoiding the use of slow filter-based symmetrical components calculators.

8.2. Transient Performance. In this part, the evaluation of the transient behavior of the proposed control strategy is made for a three-phase unbalanced load ($R_A = 10\,\Omega$, $R_B = 7\,\Omega$, and $R_C = 8\,\Omega$). To verify the transient performance of the proposed voltage control strategy a step change in the d-components of voltage references ($V_{d\text{ref}}$) in all phases of the four-leg inverter is applied and then returns to its initial voltage value (while keeping $V_{q\text{ref}} = 0$).

For the A-phase a step change from 155.56 to 75 V (peak) at 26 ms is applied and then returns to its initial voltage value at 79 ms. The transient behaviors of the voltage reference ($V_{A,d\text{ref}}$) and the actual voltage ($V_{A,d}$) of the respective phase are shown in Figure 18. The d-reference voltage (peak) value in phase "B" ($V_{B,d\text{ref}}$) is step changed from 155.56 to 140 V (peak) at 39 ms, afterwards back to 155.56 V at 79 ms. Figure 19 also depicts the transient response of the voltage ($V_{B,d\text{ref}}$) reference and the actual voltage ($V_{B,d}$) of the b-phase.

For the C-phase also a step change from 155.56 to 135 V (peak) at 46 ms is applied and then returns to its initial voltage value at 79 ms. Figure 20 illustrates the waveforms of the voltage ($V_{C,d\text{ref}}$) reference and actual voltage ($V_{C,d}$) of the pertaining phase. As can be seen, the voltage controllers in each phase demonstrate very fast dynamic, and the actual voltages are capable of following closely their references. The

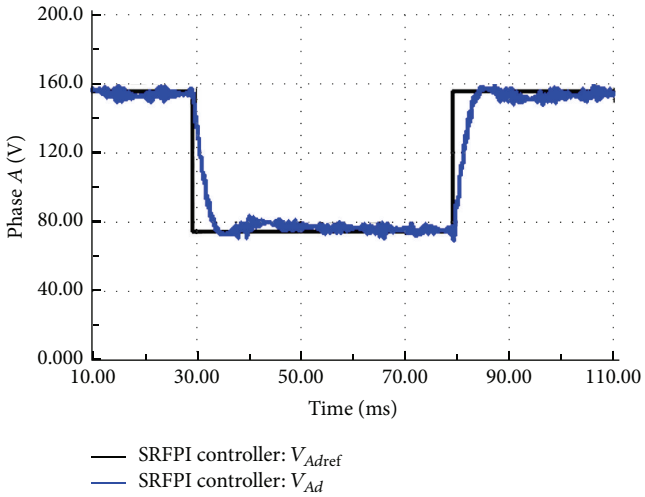

FIGURE 18: Transient response of the PI controller to step changes in phase "*A*."

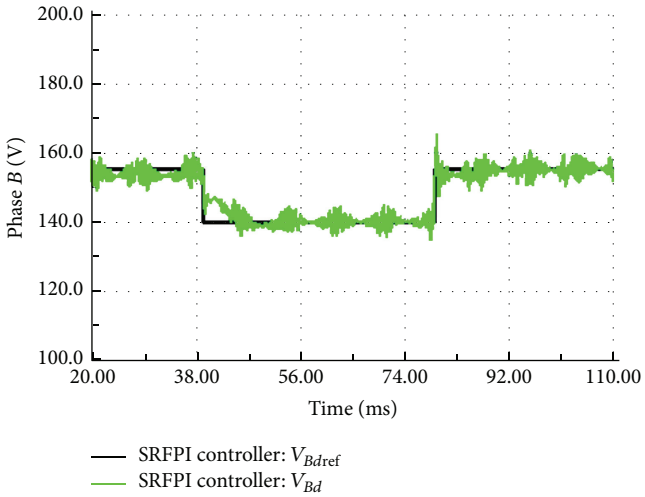

FIGURE 19: Transient response of the PI controller to step changes in phase "*B*."

PI controllers take about 1 cycle to track reference voltage in each phase. It is apparent that the proposed controller can change the load voltages close to their references with very fast dynamic.

8.2.1. Comparison between the Conventional and the Proposed Control Scheme. In this part, the transient performance of the proposed control strategy has been compared with the conventional control scheme [15, 16], with the same specification for the voltage and current controller. In this simulation, while the three-phase four-leg grid-forming unit is initially supplying a balanced load (8 Ω/ph), a single-phase inductive load ($R = 20\,\Omega$ and $L = 2$ mH) is added between phases "*A*" and "*C*" at 0.3 s. After 0.2 s, the connected load between phase "*C*" and neutral is changed from the nominal load to pure resistance of 5.7 Ω. Lastly, the nominal load between phase "*A*" and neutral is disconnected at 0.7 s.

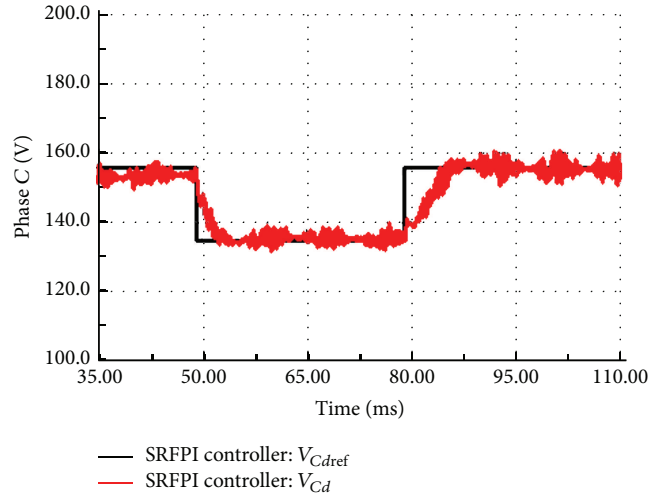

FIGURE 20: Transient response of the PI controller to step changes in phase "*C*."

The output waveforms of load voltages under varying unbalanced load conditions are depicted in Figure 21, for both the conventional and the suggested control schemes. As can be seen, both control strategies can keep the load voltages balanced in steady-state under varying unbalanced load conditions. To compare the speed of response of two control schemes, the transient load voltages for both control strategies are provided with zoomed Figures. It can be seen that the load voltage waveforms are unaffected by the load transients in the proposed scheme. Comparing the two results, it can be seen that no significant changes in the load voltages can be observed with the proposed scheme. While there exist at least three line cycles transient with the conventional approach, the results show that the suggested controller has a significant ability to balance the output voltages under severe unbalanced load conditions with zero steady-state error and fast dynamic response.

9. Conclusion

In this study, a new per-phase cascaded voltage-current control strategy for a three-phase four-leg VSI operating with highly unbalanced loads in an autonomous distribution network is presented. The suggested control scheme provides balanced output voltages for the four-leg inverter even under extremely unbalanced loading conditions. It consists of an outer voltage loop in each phase to regulate the instantaneous output voltages and an inner current loop in each phase to improve both the steady-state and transient behaviors of the control system. The frequency response approach is used for tuning and stability analysis. The transient and steady-state performances of the suggested control scheme are investigated using simulation studies. The simulation results show that the suggested controller has a significant ability to balance the output voltages under severe unbalanced load conditions with zero steady-state error and fast dynamic response.

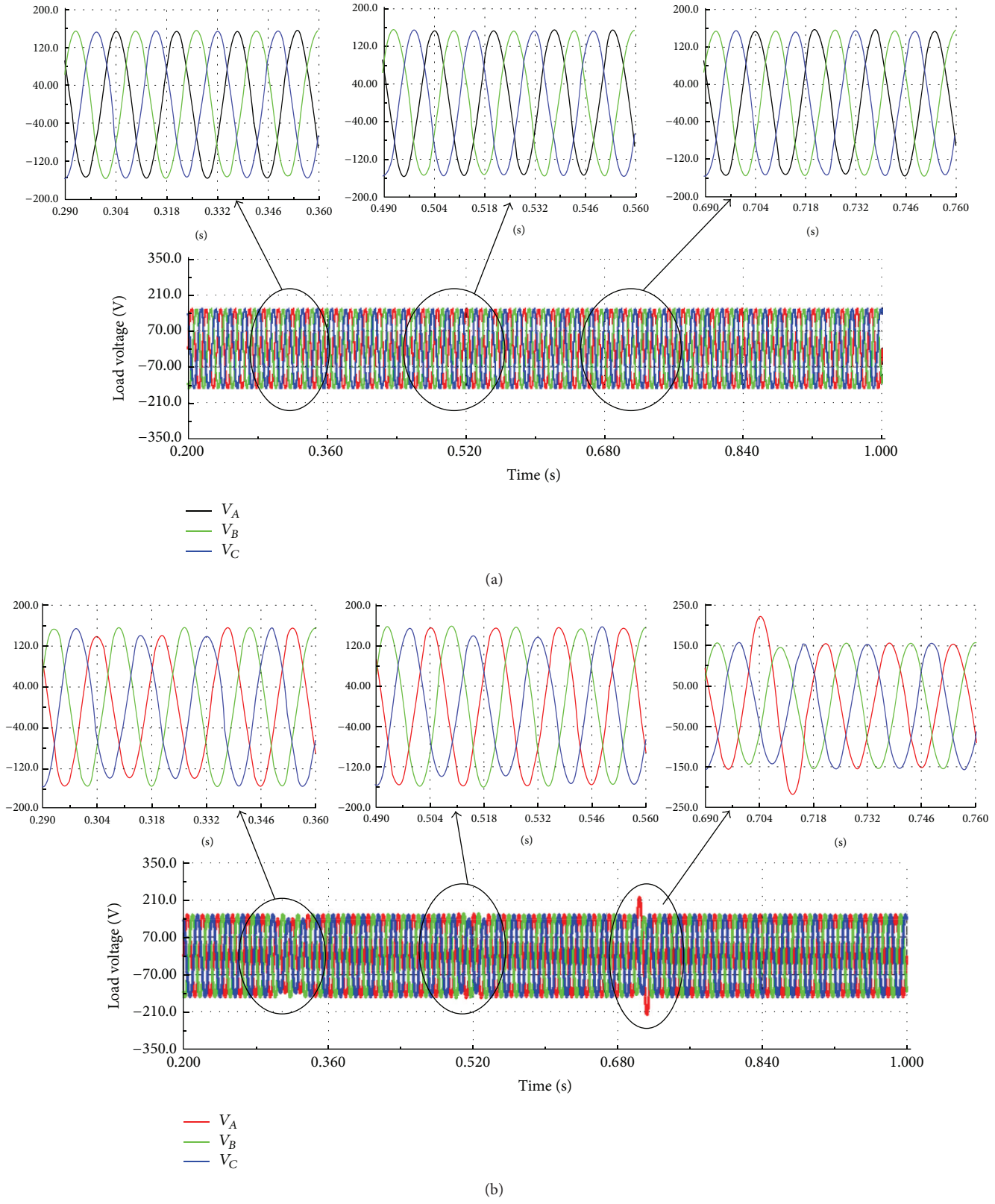

FIGURE 21: Waveforms of output voltages of the four-leg inverter for different load condition. (a) Proposed control scheme. (b) Conventional scheme [15, 16].

Competing Interests

The authors declare that they have no competing interests.

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