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Research Article

Designing All-Pole Filters for High-Frequency Phase-Locked Loops

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Since the phase-locked loop (PLL) circuit was proposed in the 1930s, it is being used for a lot of situations when precise frequency and phase references are required. Among these applications, synchronous telecommunication networks experienced a strong development in order to support the explosive information traffic that the modern society demands. Consequently, bandwidth became a decisive parameter, implying higher and higher frequencies for the clock signals exchanged between the nodes of the networks and detected by PLLs. The necessity to improve clock precision that follows the bandwidth increase provoked the improvement of the filter component of the PLLs, avoiding instability and high-frequency components in the reference signals. Here, a technique of designing this kind of filter is presented, considering second-order filters, implying third-order PLLs. Simulations show that following this technique produces very fast tracking processes, enabling precise operation even for very high frequencies.

1. Introduction

Phase-locked loop (PLL) was conceived by de Bellescize in 1932 [1] and has been used to generate frequency and phase signals for several types of applications such as demodulation, digital signal transmission, and clock recovering in synchronous networks. In the last thirty years, digital electronics revolution produced high speed integrated service networks based on master-slave time distribution systems with very precise central clocks sending signals to slave nodes that, by using cheap and precise PLLs, reconstruct the necessary time basis [2].

Along this time, the implementation of circuits to execute the PLL functions evolved from analog to digital circuits and even software PLLs are now used in engineering applications [1], including synchronous communication networks.

Considering telecommunication services, a first view could indicate that multiplier phase detectors have been replaced by digital phase and frequency detectors with charge pump [3]. In spite of this, due to bandwidth requirements, the development of optical clock detectors is based on multiplier phase detection and they are very useful in high speed networks [4–6].

Consequently, the double-frequency jitter, which is less critical in the digital versions of phase and frequency detectors, becomes more significant with the development of high speed optical networks and master oscillation drifts spoil the synchronous state reachability [7, 9]. To solve this problem, one can use high-order filters in the PLL, increasing the order of the whole loop, but providing adequate high-frequency operation.

Here, some design strategies for PLL filters are proposed, in order to avoid double-frequency jitter effects, decreasing considerably acquisition times and allowing good synchronism performance for network nodes built with PLLs.

The filters to be chosen are all-pole for which there are results about how to avoid bifurcations and undesired oscillations [10]. The idea is to present different filter options to implement PLLs with free-running frequencies of hundreds of GHz.

In Section 2, some general PLL principles are discussed in a very brief way, emphasizing the liner approximation

and the transfer functions of the filter and of the whole loop. Section 3 is about the root locus peculiarities of the PLL all-pole transfer functions with order greater than 2. In Section 4, the designing method is presented with Section 5 showing some examples to illustrate the robustness and generality of the procedure. Section 6 shows and compares results between the presented methodology and the usual light-wave technology validating the described procedure and showing its improvements. Section 7 presents some concluding remarks.

2. General PLL Principles

The main PLL function is to generate an output signal $v_o(t)$ having phase $\theta_o(t)$ that is related to phase θ_i of an input signal $v_i(t)$ so that the difference $\theta_i(t) - \theta_o(t)$ maintains a constant value as time passes; that is, the signals $v_i(t)$ and $v_o(t)$ reach the same frequency [1].

As shown in Figure 1, PLLs are composed of three fundamental blocks: a phase detector (PD), a linear low-pass filter F, and a voltage controlled oscillator (VCO). The PD compares the phase of the input signal $v_i(t)$ with the phase of the VCO output signal $v_o(t)$, in order to achieve a constant phase error as described above. Filter (F) is supposed to eliminate high-frequency components generated by the PD operation. Filter (F) also has the function of defining the PLL dynamics [11].

When a PLL is used for clock extraction, the input signal comes from the transmission medium, which may be pairs of copper wires, microwave radio links, or optical fibers. This input signal contains a component characterized by the frequency of the clock used in the generation of the transmission signal.

The other components of the input signal interact in the PD with the signal $v_o(t)$ and a large portion of these components are eliminated by the action of the loop filter. A small fraction of these components, with small effective power, will fall within the filter passing band and their effect will be perceived as noise in the PLL dynamics [1, 11].

Consequently, clock extraction operation can be described as the synchronization of the VCO with the clock frequency component from the input signal. Thus, in Figure 1, the input signal $v_i(t)$ and the VCO output signal $v_o(t)$ are supposed to be periodic and given by

$$\begin{aligned} v_i(t) &= A\sin\left(\omega_o t + \theta_i(t)\right), \\ v_o(t) &= V_o\cos\left(\omega_o t + \theta_o(t)\right). \end{aligned} \tag{1}$$

In high-frequency PLL implementations, object of this work, the PD is commonly a signal multiplier with a multiplying factor denoted by K_m [4, 5]. Considering, additionally, that the filter eliminates the double-frequency terms, the error signal v_d is

$$v_d(t) = K_d\sin\left(\theta_i(t) - \theta_o(t)\right), \tag{2}$$

with $K_d = K_m A V_o/2$, called detection gain and measured in volt/rad.

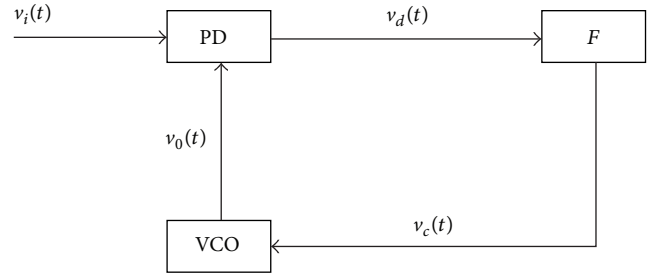


Figure 1: PLL block diagram.

Here, the lock-in mode is considered and, consequently, the PLL is operating around the synchronous state and the right side of (2) can be written considering small phase errors; that is, $\sin(\theta_i(t) - \theta_o(t)) = \theta_i(t) - \theta_o(t)$ [7].

Besides, the filter is considered to be all-pole [10, 12] with transfer function:

$$F(s) = \frac{V_c(s)}{V_d(s)} = \frac{a_0}{P(s)}, \tag{3}$$

with $P(s) = s^n + a_{n-1}s^{n-1} + \cdots + a_1 s + a_0$ and a_i being positive constants.

Finally, as the VCO phase is controlled by v_c following

$$\dot{\theta}_o(t) = K_v v_c(t), \tag{4}$$

with K_v being called VCO constant and measured in rad/s·V, the transfer function for the whole linear PLL is as follows:

$$G(s) = \frac{\Theta_o(s)}{\Theta_i(s)} = \frac{a_0 K}{sP(s) + a_0 K}. \tag{5}$$

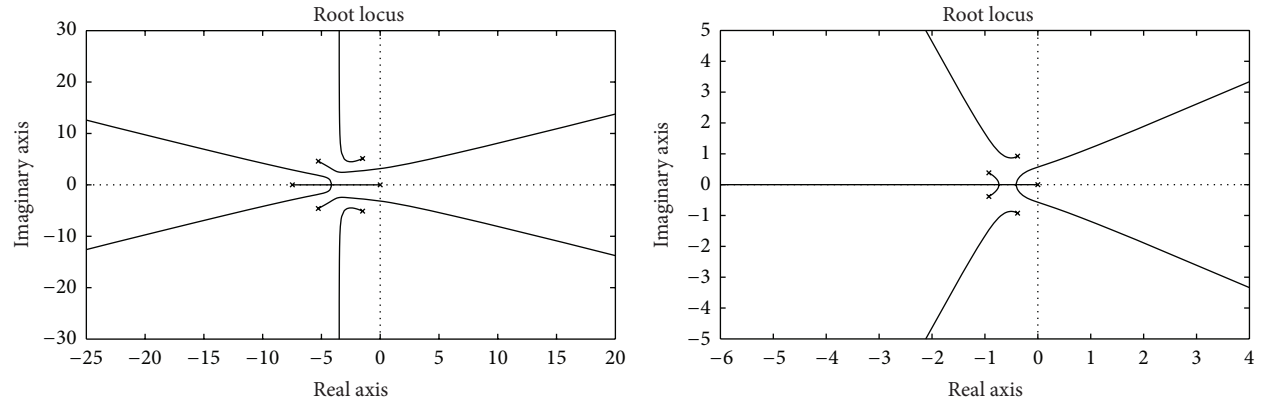
In PLL jargon, $K = K_v K_d$ is called loop gain and is measured in s^{-1} [1]. This parameter is important to calculate the synchronization range of the linear PLL, that is, the maximum angular frequency difference between $v_o(t)$ and $v_i(t)$ for a synchronous state to be reachable. Calling $|\Delta\omega|$ the modulus of this angular frequency difference, synchronization is possible if [10, 11]

$$|\Delta\omega| \leq K. \tag{6}$$

To give an idea of the meaning of (6), in typical optical communication systems, a 20 Gbits/s system with a tolerance of 10 ppm for the clock signal is considered. Under these conditions, the necessary loop gain to extract the clock needs to be greater than $1.256{\cdot}10^6\ s^{-1}$. As a consequence of this high gain, the filter needs to be carefully designed, in order to combine synchronization conditions and stability.

3. All-Pole PLLs with Order Greater Than 2: Root Locus Properties

As shown in the last section, the whole loop PLL transfer function given by (5) has an all-pole form, with the following properties:



(a) Normalized 6th-order Bessel type

(b) Normalized 4th-order Butterworth type

Figure 2: Root locus for all-pole PLL transfer functions: examples.

(i) the branches of the root locus of $G(s)$ start at the zeros of $sP(s)$. In particular, one of the branches starts at the origin, which is one of the poles of $sP(s)$ [13];

(ii) the branch of the root locus of $G(s)$ starting at the origin always enters the left half plane [10];

(iii) all branches of the root locus of $G(s)$, as $s \to \infty$, tend to infinity along asymptotes inclined relative to the real axis by angles of $\pi/(n+1), 3\pi/(n+1), 5\pi/(n+1), \ldots$ [13];

(iv) pairs of symmetrical root locus branches that go to infinity along asymptotes not coincident with the real axis and forming angles of magnitude less than $\pi/2$ with the real axis create pairs of imaginary poles when crossing the imaginary axis. In general, the crossings of different pairs of branches occur at different values of K. The values of K at each crossing will be the solutions of the equation $\Delta_{n-1}(K) = 0$, where Δ_{n-1} is the $(n-1)$-th Hurwitz minor of the polynomial $sP(s) + K$ [10];

(v) the onset of instability will happen at gain K_I, corresponding to the first crossing of the imaginary axis in the root locus of $sP(s) + K$;

(vi) all root locus branches that cross the imaginary axis never come back [10]. This property only holds if the zeros of $P(s)$ are all located in the left half-plane;

(vii) the consequence of the last property is that the crossings of the imaginary axis will always occur two at a time, corresponding to the conjugate complex roots contained in symmetrical branches of the root locus.

Considering these properties, root locus of transfer functions given by (5) has the general appearance shown in Figure 2, which exemplifies the root locus of normalized PLLs, that is, with a 3 dB gain at angular frequency 1 rad/s. Figure 2(a) presents a 6th-order Bessel filter [14, 15] in the loop and Figure 2(b) presents a 4th-Butterworth filter [14, 15] in the loop. As can be seen, it is possible to characterize the onset of instability for a transfer function according to (5) by the value of K_I of the loop gain. Such a value of loop gain is associated with a pair of imaginary poles of transfer function.

Table 1: Stability threshold for standard filters.

Order	Butterworth	Chebyshev	Bessel	Gaussian
2	1.4142	2.3998	3.0000	2.1974
3	0.7500	0.9205	2.0833	1.1665
4	0.5719	0.6106	1.8883	0.8688
5	0.4705	0.4499	1.8069	0.7195
6	0.3982	0.3501	1.7598	0.6264
7	0.3444	0.2910	1.7286	0.5613

As a practical consequence of these properties, PLLs present a range of positive values of K, such that, for all values in that range, all poles of transfer function $G(s)$ of (5) are located in the left side of the complex plane, implying that the system is stable. Another consequence is that a stability threshold may be defined for any system described by this transfer function.

This stability threshold K_I is defined as the value of the gain K for which the first pair of root locus branches crosses the imaginary axis. Thus, all PLL systems described by a transfer function (5), operating with $K < K_I$, are stable.

There are other additional considerations to choose K, but only values lesser than K_I must be used. Determination of stability threshold K_I is discussed in the Appendix, where some algorithms are presented. As a matter of illustration, Table 1 shows values of K_I for some normalized standard filter types, considering $G(s)$ order.

4. Design Method

In this section, a new method for designing filters for PLLs is presented. The method is based on the definition of a standard form for the transfer function [14, 15] for the loop filter. The procedure is divided into two stages: gain calculation and denormalization of the transfer function.

4.1. Defining the Transfer Function Gain. As the permitted VCO gain range is defined, as shown in the former section, the next step is to choose a value for this parameter. In order to do this, some objectives must be conciliated.

The first is to obtain a PLL able to operate with high gains in optical digital communication systems [8] and also capable of operating in face of the phenomenon so-called "jitter."

A second point is that PLL transfer functions $G(s)$ amplify frequency variations in the input phase signal if there are overshoots in the frequency response of $|G(s)|^2$, or, in other words, if there are angular frequencies ω such that $|G(j\omega)|^2 > 1$.

Consequently, $|G(j\omega)|^2$ showing overshoots must be avoided. Calling $D(s)$ the denominator polynomial of $G(s)$, one of the ways to attain this objective is to impose $|D(j\omega)|^2$ monotonically increasing.

Considering that $D(s) = sP(s) + a_0K$ and $|D(j\omega)|^2 = D(j\omega)D(-j\omega)$, it follows that $|D(j\omega)|^2$ assumes the following form: $|D(j\omega)|^2 = \omega^{2n+2} + \cdots + (a_0^2 - 2a_1a_0K)\omega^2 + (a_0K)^2$, with a_0 and a_1 being the coefficients of $P(s)$ from (5).

By using an analogous reasoning to the *"maximally flat at $\omega = 0$"* approach used in the Butterworth approximation [14, 15], in the ideal situation, all coefficients of powers of ω different from $2n + 2$ and 0 must be zero, in order to vanish the derivatives of $|D(j\omega)|^2$ up to the order $2n + 1$ at $\omega = 0$.

This is not possible, since several coefficients of $|D(j\omega)|^2$ do not depend on K. But, since the main objective is to have $|D(j\omega)|^2$ with monotonically increasing behavior and, in the normalized case, only the angular frequencies of the first order are responsible to characterize the pass-band, the stability condition can be guaranteed.

Therefore, the most significant nonconstant term in $|D(j\omega)|^2$ is related to ω^2, since the next term corresponds to ω^4, being smaller or of the same order of magnitude as ω^2. If the parameter K is reduced, the coefficient of the ω^2 term is $(a_0^2 - 2a_1a_0K)$ for all loop filter transfer functions with orders equal to or greater than 2, increasing up to reach a_0^2 for $K = 0$.

This coefficient of ω^2 passes through zero when K is given by

$$K_R = \frac{a_0}{2a_1}. \tag{7}$$

If K_R is further decreased up to a value smaller than K_I, 10 to 20% reductions are enough to have $|D(j\omega)|^2$ monotonically increasing and therefore free of overshoots. When K_R is greater than K_I, 50% reductions in the value given by (7) imply that $|D(j\omega)|^2$ is monotonically increasing and therefore free of overshoots.

4.2. Denormalizing the Transfer Function. Suppose that the aim is to obtain a PLL transfer function $G(s)$ following an all-pole filter transfer function. Since all standard filter types have transfer functions expressed in normalized form, that is, transfer functions with 3 dB frequency equal to 1, then the normalized coefficient a_0 and the normalized denominator $P(s')$ are known, where s' is the normalized complex variable.

Following this procedure, one can precisely define the PLL transfer function $G(s)$, with the transfer function $F(s)$ of the loop filter being automatically defined by $G(s)$.

The expression for the normalized PLL loop transfer function $G(s')$ is given by

$$\begin{aligned} G(s') &= \frac{b_0'}{s'^{n+1} + b_n's'^n + b_{n-1}'s'^{n-1} + \cdots + b_1's' + b_0'} \\ &= \frac{b_1'K_R}{s'^{n+1} + b_n's'^n + b_{n-1}'s'^{n-1} + \cdots + b_1's' + b_1'K_R}, \end{aligned} \tag{8}$$

where $n + 1$ is the order of the PLL. The normalized loop gain $K_R = b_0'/b_1'$ and the normalized coefficients $b_n', \ldots, b_0'$ are assumed to be determined by the chosen type of filter [12, 14–16].

In order to implement the desired transfer function $G(s)$ and the loop filter transfer function $F(s)$, it is necessary to denormalize $G(s')$ given by (8) by using the appropriate angular frequency ω_d that plays an important role in defining loop gain K. Additionally, designing all-pole filter [12, 16] requires the definition of the group delay function $D(\omega)$, evaluated at $\omega = 0$, or simply $D(0)$.

As shown in [12, 16], the group delay at $\omega' = 0$, corresponding to a normalized transfer function given by (8), is as follows:

$$D_N(0) = \frac{b_1'}{b_0'} = \frac{1}{K_R}. \tag{9}$$

The denormalized PLL transfer function $G(s)$ has the same form as (8) but with coefficients $b_{n-1}, \ldots, b_1$ and loop gain K. Thus, the group delay function at $\omega = 0$ corresponding to the $G(s)$ should be given by the same form as (9), but with K replacing K_N; that is,

$$D(0) = \frac{1}{K}. \tag{10}$$

Besides, for a normalized low-pass frequency transformation, the normalized group delay $D_N(\omega')$ and the group delay $D(\omega)$, as shown in [12], are related by

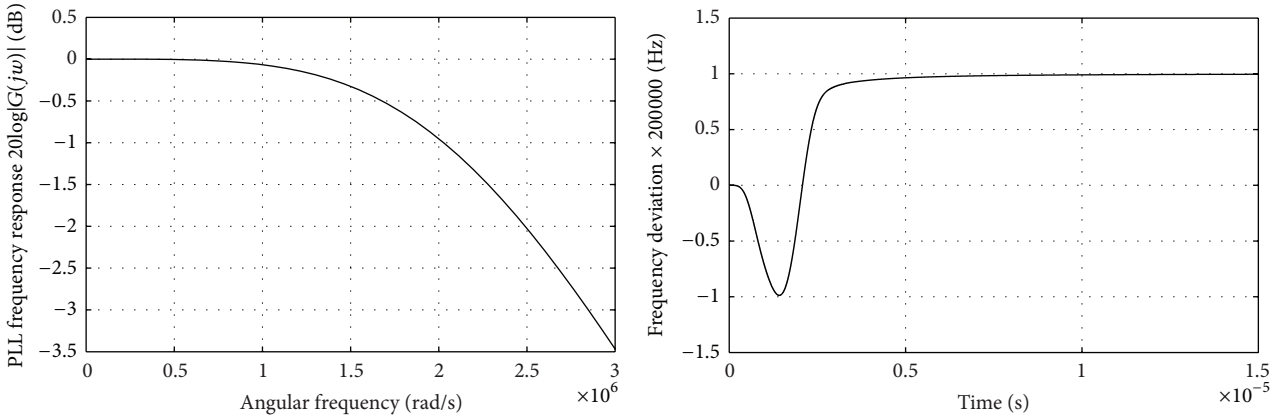
$$D(\omega) = \frac{D_N(\omega')}{\omega_d}, \tag{11}$$

and, consequently:

$$K = \omega_d K_R. \tag{12}$$

Thus, since K_R, calculated by the procedure defined in Section 4.1, is determined by coefficients b_0' and b_1', in order to obtain a PLL transfer function with a given K, the standard filter must be denormalized to a frequency ω_d, by using (12). Then, the substitution $s' = s/\omega_d$ in (5) results in the PLL transfer function:

$$\begin{aligned} G(s) &= \frac{\omega_d^{n+1}b_1'K_R}{s^{n+1} + \omega_d b_n's^n + \omega_d^2 b_{n-1}'s^{n-1} + \cdots + \omega_d^{n+1}b_1'K_R} \\ &= \frac{b_1K}{s^{n+1} + b_{n-1}s^n + \cdots + b_1s + b_1K}, \end{aligned} \tag{13}$$



(a) PLL frequency response

(b) PLL capture performance

Figure 3: PLL with a 5th-order Butterworth filter.

with w_d being the quotient between the 3 dB angular frequency of the chosen standard filter and the 3 dB angular frequency of the normalized transfer function.

5. Application Examples

Here, the described procedure is applied to three types of PLL all-pole filters: a 5th-order Butterworth, a 5th-order Chebyshev, and an arbitrary 3rd-order filter. For each case, the PLL frequency response and the capture performance are presented, showing that the developed design procedure allows very fast signal tracking. The results were obtained by simulations with MATLAB [17] and considering the linear PLL model with phase error belonging to the interval $[-\pi, \pi]$ [18].

5.1. 5th-Order Butterworth. A 5th-order Butterworth filter was designed by using the methodology described here and the following parameters were assumed or calculated: $K_I = 0.4705\,(\text{rad/s})/\text{V}$; $K_R = 0.1545\,(\text{rad/s})/\text{V}$; $K_v = 1.256 \cdot 10^6\,(\text{rad/s})/\text{V}$; $\omega_N = 8.133 \cdot 10^6$ (normalized); $\omega_{3\,\text{dB PLL}} = 2.85 \cdot 10^6$ rad/s; and $\omega_{3\,\text{dB FILTER}} = 8.13 \cdot 10^6$ rad/s.

Simulation results are shown in Figure 3: PLL frequency response (Figure 3(a)) and capture performance (Figure 3(b)). It can be observed that the 3 dB bandwidth is about half of the sum frequency of the input signal with the VCO center frequency and tracking time is about 10 μs.

In this case, the reference loop gain K_R resulted in a PLL frequency response free of overshoots, without the need of reducing this value.

5.2. 1 dB-Ripple 5th-Order Chebyshev. A 1 dB-ripple 5th-order Chebyshev filter was designed by using the methodology described here and the following parameters were assumed or calculated: $K_I = 1.2317\,(\text{rad/s})/\text{V}$; $K_R = 0.5022\,(\text{rad/s})/\text{V}$; corrected $K_R = 0.4018\,(\text{rad/s})/\text{V}$; $K_v = 1.256 \cdot 10^6\,(\text{rad/s})/\text{V}$; $\omega_N = 2.8117 \cdot 10^6$ (normalized); $\omega_{3\,\text{dB PLL}} = 3.0643 \cdot 10^6$ rad/s; and $\omega_{3\,\text{dB FILTER}} = 3.8087 \cdot 10^6$ rad/s.

Simulation results are shown in Figure 4: PLL frequency response (Figure 4(a)) and capture performance (Figure 4(b)). It can be observed that the 3 dB bandwidth is less than half of the sum frequency of the input signal with the VCO center frequency and the tracking time is about 11 μs.

In this case, the reference loop gain K_R was corrected to 80% of the value determined by (7), resulting in a PLL frequency response with 0.077 dB overshoot.

5.3. Nonstandard Filter. To show the robustness of the procedure, a nonstandard third-order all-pole filter is designed to work as the PLL filter, implying a 4th-order PLL. In this case, the chosen filter transfer function is as follows:

$$F(s) = \frac{9}{s^3 + 7s^2 + 8s + 9}. \tag{14}$$

The following parameters were assumed or calculated: $K_I = 2.0\,(\text{rad/s})/\text{V}$; $K_R = 0.75\,(\text{rad/s})/\text{V}$; $K_v = 1.256 \cdot 10^6\,(\text{rad/s})/\text{V}$; $\omega_N = 1.883 \cdot 10^6$ (normalized); $\omega_{3\,\text{dB PLL}} = 2.89 \cdot 10^6$ rad/s; and $\omega_{3\,\text{dB FILTER}} = 3.84 \cdot 10^6$ rad/s.

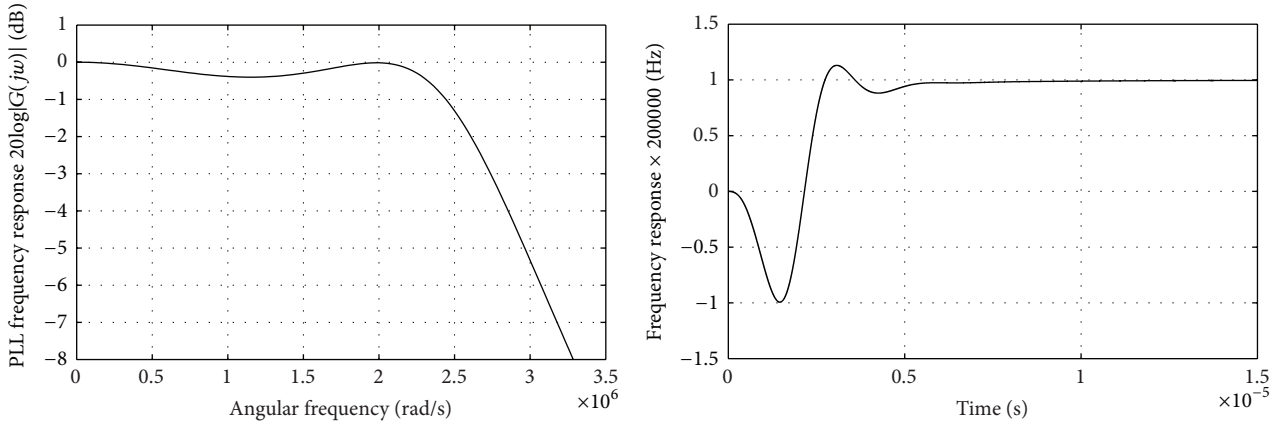
Simulation results are shown in Figure 5: PLL frequency response (Figure 5(a)) and capture performance (Figure 5(b)). It can be observed that the 3 dB bandwidth is less than half of the sum frequency of the input signal with the VCO center frequency and the tracking time is about 11 μs.

In this case, the reference loop gain K_R was corrected to 89% of the value determined by (7), resulting in a PLL frequency response with 0.011 dB overshoot.

The examples have shown that, despite the different structures presented for the filters, the tracking time is almost the same in the analyzed cases. Consequently, it could be conjectured that the tracking time performance depends only on a good choice for the gain.

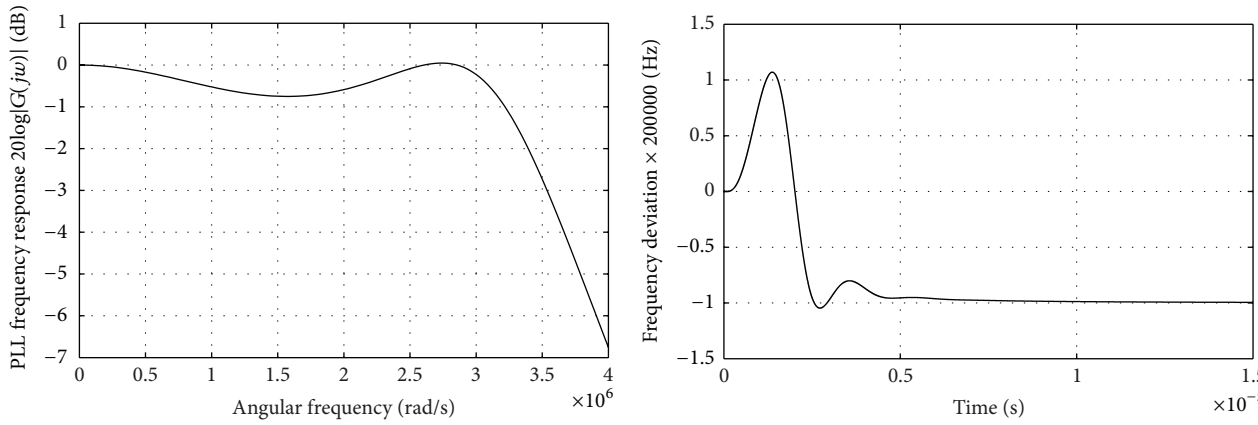
6. Designing for Light-Wave Technology

In order to show comparisons between the methodology developed here and results presented for synchronization concerning light-wave networks, the reference work presented in [5] will be discussed.



(a) PLL frequency response (b) PLL capture performance

Figure 4: PLL with a 5th-order Chebyshev filter.



(a) PLL frequency response (b) PLL capture performance

Figure 5: PLL with a third-order nonstandard filter.

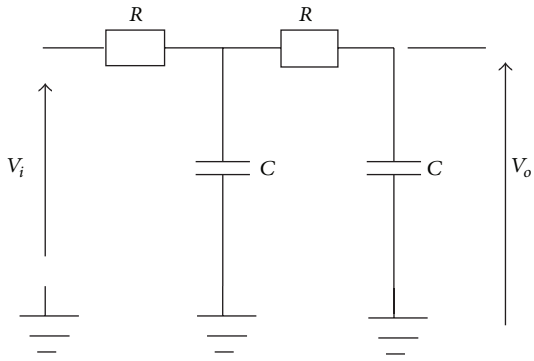


Figure 6: *RC* filter for PLL.

There, the authors describe an *RC* filter used in the PLL, shown in Figure 6, with a transfer function given by

$$F(s) = \frac{V_o(s)}{V_i(s)} = \frac{a_0}{s^2 + a_1 s + a_0}, \tag{15}$$

with $a_0 = 1/RC$ and $a_1 = 3/RC$.

Results obtained in [5] show the loop behavior for loop gains ranging from 500 Hz to 1 MHz and undesirable self-sustained oscillations appear around 1 MHz gain.

Here, the filter was redesigned starting with a normalized form that considers $R = C = 1$, corresponding to $K_I = 3$ (rad/s)/V and $K_R = 0,1667$ (rad/s)V. With the values used in [5], $RC = 1.034 \cdot 10^6$ s and, consequently, $a_0 = 9.35317 \cdot 10^{11}\ s^{-2}$ and $a_1 = 2.90135 \cdot 10^6\ s^{-1}$. Since a_0 and a_1 are denormalized by ω_N^2 and ω_N, respectively, it follows that $\omega_N = 967.118 \cdot 10^3$.

For the situation with loop gain $K = 1.885 \cdot 10^6$ (rad/s)/V, considering the calculated ω_N, the corresponding denormalized K is 1.9491 (rad/s)/V, well above the value of $K_R = 0.1667$ (rad/s)/V and near $K_I = 3$ (rad/s)/V. This proximity suggests that the PLL with this loop filter and with $K = 1.885 \cdot 10^6$ (rad/s)/V is still stable, but with damped oscillatory behavior during input phase transients.

This behavior is observed in the capture process shown in Figure 7, obtained in a simulation with a loop filter with the same R and C values as used in [5] and with $K = 1.885 \cdot 10^6$ (rad/s)/V. Comparing these results with the results

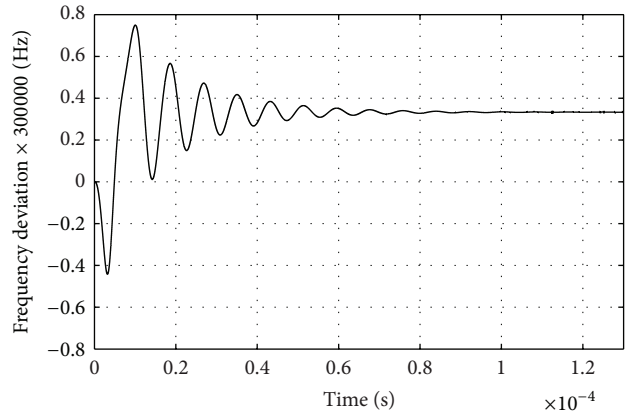
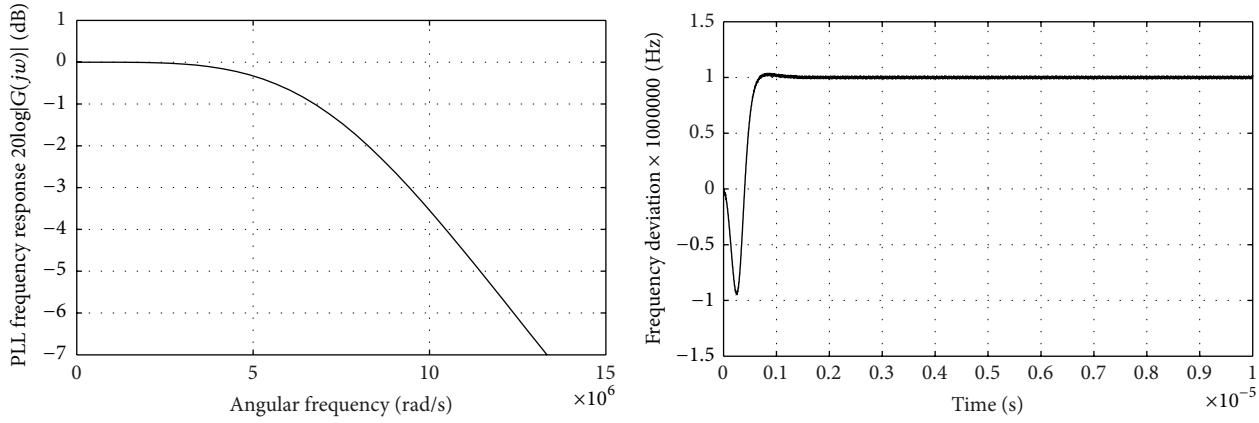


Figure 7: PLL capture with the *RC* filter.



(a) PLL frequency response

(b) PLL capture performance

Figure 8: PLL with a redesigned *RC* filter.

presented in [5], it can be concluded that they are the same, validating the design and simulation procedures followed here.

Additionally, these procedures can be applied as an improvement to the design presented in [5], taking the same PLL *RC* filter and considering a loop gain corresponding to 1 MHz as, in this case, the PLL proposed in [5] fails to capture the synchronous state.

The denormalization factor is $\omega_N = 37.692 \cdot 10^6$, considerably higher than that presented in [5]. Consequently, $RC = 2.653 \cdot 10^{-8}$ s that is feasible with $R = 22\,\Omega$ and $C = 1.21$ nF. Simulation results are shown in Figure 8: PLL frequency response (Figure 8(a)) and capture performance (Figure 8(b)). It can be observed that the tracking time has order of magnitude equal to 1.5 μs.

7. Conclusions

Methods for the implementation of PLL with order greater than 2 were presented, providing the possibility of adjustment of loop gain K for arbitrary large values. The obtained PLLs are stable with a relatively large margin of robustness.

It was shown that, starting with normalized forms of the loop transfer functions, parameters defining the limits of instability for the PLLs can be calculated, permitting one to obtain transfer functions free of or with acceptable overshoots.

The procedure has shown that the loop filters to be used in PLLs may be scaled to permit the use of arbitrarily high loop gains.

With the availability of wide-band operational amplifiers, with gain-bandwidth products greater than 100 MHz, it can be anticipated that there are no serious limitations to the practical implementation of PLLs with the filter types discussed here.

Such PLLs could be useful in the implementation of clock recovery in large speed optical communication systems, as well as in other digital high speed systems.

Appendix

Algorithm for the Calculus of K_I for $n = 2$ to 5. Using some properties from the theory of equations and considering the expression of $P(s)$ as described in this work,

(i) $n = 2$: $K_I = a_1$;

(ii) $n = 3$: $K_I = (a_2a_1 - a_0)/a_2^2$;

(iii) $n = 4$: $K_I = (a_1 - a_3 \cdot d)d/a_2^2$, where d is one of the roots of the equation $d^2 - a_2d + a_0 = 0$. Both values of d must be used, giving two possible values for K_I. The smallest positive value must be chosen;

(iv) $n = 5$: $K_I = (a_1 - a_3 \cdot d + d^2) \cdot d/a_0$, where d is one of the roots of the equation $a_4d^2 - a_2d + a_0 = 0$. Both values of d must be used, giving two possible values for K_I. The smallest positive value must be chosen.

If only negative values are obtained for K_I, the proposed transfer function is not suitable for the use as a PLL loop filter, since the resulting loop will be unstable.

General Algorithm for the Calculus of K_I. Consider that the denominator of $G(s)$ can be written as

$$sP(s) + a_0K = A(s) + a_0K + sB(s), \tag{A.1}$$

where $A(s)$ and $B(s)$ are even polynomials and the loop gain K_I causes the branches of the root locus of $G(s)$ to cross the imaginary axis at a pair of pure imaginary roots $\pm j\omega_C$.

Making $s = j\omega_C$ results in

$$A(j\omega_C) + a_0K_I + j\omega_CB(j\omega_C) = 0. \tag{A.2}$$

Then, real and imaginary parts of the last equation are zero and

(i) $B(j\omega_C = 0)$;

(ii) $K_I = -A(j\omega_C)/a_0$.

As $A(j\omega_C)$ and $B(j\omega_C)$ are even polynomials in ω, the value of ω_C is obtained as the positive root of (A.1) and by substituting this value in (A.2) it is possible to obtain K_I. Negative values of K_I mean that the proposed transfer function is not suitable for usage as loop filter of a PLL.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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