

Research Article

Cascadable Current-Mode First-Order All-Pass Filter Based on Minimal Components

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A novel current-mode first-order all-pass filter with low input and high output impedance feature is presented. The circuit realization employs a single dual-X-second-generation current conveyor, one grounded capacitor, and one grounded resistor, which is a minimum component realization. The theoretical results are verified using PSPICE simulation program with TSMC 0.35 μm CMOS process parameters.

1. Introduction

Current-mode circuit design using current conveyor has received a considerable attention owing to its potential advantages such as wider dynamic range, greater linearity, wide bandwidth, simple circuitry, and low power consumption [1]. Considering these advantages of current conveyor, recently several current mode first-order all-pass filters employing different types of current conveyor such as second-generation current conveyor [2–4], four terminal floating nullor [5], third-generation current conveyor [6], differential voltage current conveyor [7, 8], current differencing buffered amplifier [9], current operational amplifier [10], and dual-X second-generation current conveyor [11, 12] have been reported. These reported filters reveal some useful features depending on the individual topology as summarized in Table 1. The comparison between the proposed circuit and the previously reported circuits is based on the use of number of active elements, number of grounded passive components, and low input and high output impedance feature(s). In general, the input impedance should be lower in comparison to the output impedance to avoid loading problem while cascading such current-mode circuits to form larger system.

In this paper, a novel cascadable current-mode (CM) first-order all-pass filter is proposed. The circuit uses a

dual-X second generation multioutput current conveyor (DX-MOCCII), a grounded resistor, and a grounded capacitor, which is ideal for IC implementation. The circuit offers low-input impedance and high-output impedance feature and also free from matching constraints. Nonideal gain and parasitic effects of the DX-MOCCII on the transfer function of the proposed filter are also analysed.

2. The Proposed Circuit

Dual-X second-generation current conveyor [13] is a useful and versatile active element, which has found several applications in analog signal processing [14–18]. The DX-MOCCII symbol is shown in Figure 1 and is characterized by the following port relationships:

$$\begin{bmatrix} I_Y \\ V_{X+} \\ V_{X-} \\ I_{Z1+} \\ I_{Z2+} \\ I_{Z1-} \\ I_{Z2-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{X+} \\ I_{X-} \end{bmatrix}, \quad (1)$$

where the suffixes refer to the respective terminals. The active element is characterized by high input impedance at

TABLE 1: Comparison of various current-mode all-pass filters.

References	No. of active elements	Single active element	No. of resistors and capacitors	All-grounded passive elements	Low input impedance	High output impedance	Component matching constraint
Higashimura and Fukui [2]	1-CCII	Yes	4	No	No	Yes	Yes
Higashimura [5]	1-FTFN	Yes	3	No	No	No	Yes
Toker et al. [9]	1-CDBA	Yes	2	No	No	Yes	No
Maheshwari and Khan [6]	1-CCIII	Yes	2	No	No	No	No
Kilinç and Çam [10]	1-COA	Yes	2	No	No	Yes	No
Minaei and Ibrahim [7]	1-DVCC	Yes	3	No	No	Yes	Yes
Khan et al. [3]	2-MOCCII	No	2	Yes	No	Yes	No
Maheshwari [8]	1-DVCC	Yes	2	Yes	No	Yes	No
Minaei and Yuce [4]	2-DOCCII	No	2	Yes	Yes	Yes	No
Minaei and Yuce [11]	1-DXCCII	Yes	4	Yes	No	Yes	Yes
Beg et al. [12]	1-DX-MOCCII	Yes	4	Yes	No	Yes	Yes
Proposed Circuit	1-DX-MOCCII	Yes	2	Yes	Yes	Yes	No

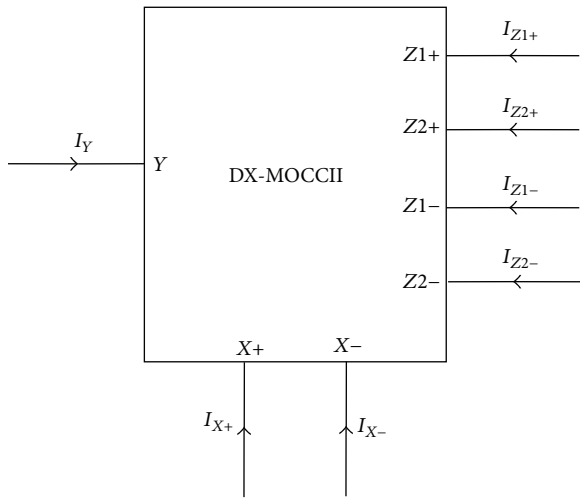


FIGURE 1: Symbol of DX-MOCCII.

the Y terminal, high output impedance at the $Z1+$, $Z2+$, $Z1-$, and $Z2-$ terminals, and low impedance at the $X+$ and $X-$ terminals.

The proposed current-mode (CM) first-order all-pass filter employing a DX-MOCCII, a grounded capacitor, and a grounded resistor is shown in Figure 2. Routine analysis of the circuit, using (1), yields the following transfer function:

$$\frac{I_{out}}{I_{in}} = - \left(\frac{s - (1/CR)}{s + (1/CR)} \right). \quad (2)$$

The frequency-dependent phase response of (2) is

$$\Phi = -2 \tan^{-1}(\omega RC). \quad (3)$$

From (3), it can be seen that the proposed circuit can provide a phase shift between 0° and -180° at output terminal (I_{out}).

The salient features of the proposed circuit are the use of single active element, two grounded passive components, and providing low input and high output impedance. As all the passive components used are in grounded form, it is suitable for integrated circuit implementation and also reduces the associated parasitic effects [19].

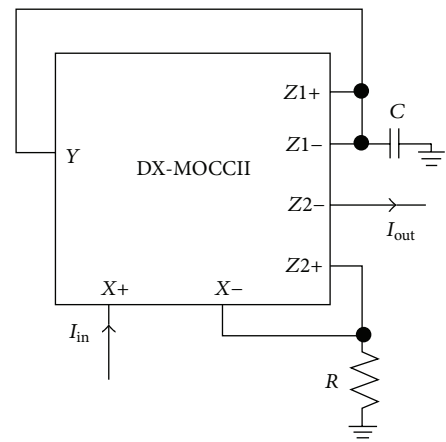


FIGURE 2: Proposed cascable current-mode first-order all-pass filter.

By interchanging the resistor (R) with a capacitor (C) in Figure 2, an additional circuit can be derived from the proposed circuit. However, the use of capacitor at the $X-$ terminal degrades the high frequency operation [20].

3. Nonideal Analysis and Parasitic Effects

3.1. Non-Ideal Analysis. Taking the nonidealities of the DX-MOCCII into account, the port relationship of the voltage and current terminals of the active element can be rewritten as

$$\begin{bmatrix} I_Y \\ V_{X+} \\ V_{X-} \\ I_{Z1+} \\ I_{Z2+} \\ I_{Z1-} \\ I_{Z2-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \beta_1 & 0 & 0 \\ -\beta_2 & 0 & 0 \\ 0 & \alpha_1 & 0 \\ 0 & -\alpha_2 & 0 \\ 0 & 0 & \alpha_3 \\ 0 & 0 & \alpha_4 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{X+} \\ I_{X-} \end{bmatrix}. \quad (4)$$

Here, α_1 and α_2 are the current transfer gains from $X+$ terminal to $Z1+$ and $Z2+$ terminals, α_3 and α_4 are the current transfer gains from $X-$ terminal to $Z1-$ and $Z2-$ terminals,

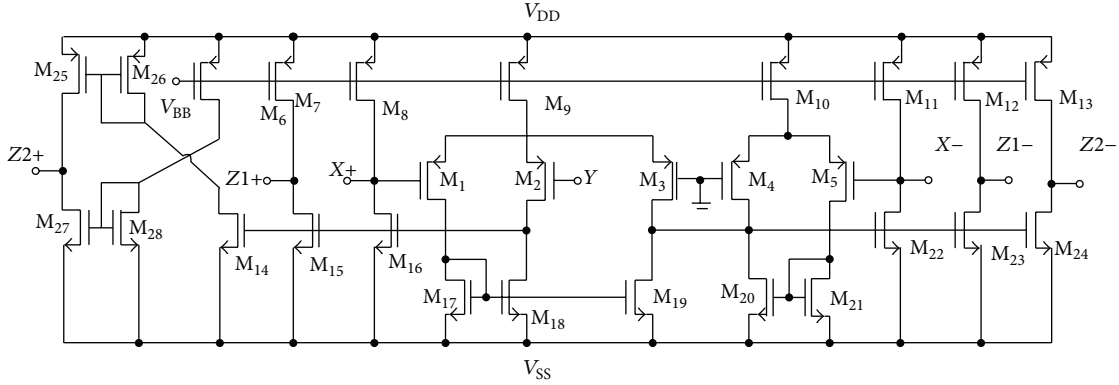


FIGURE 3: CMOS implementation of DX-MOCCII.

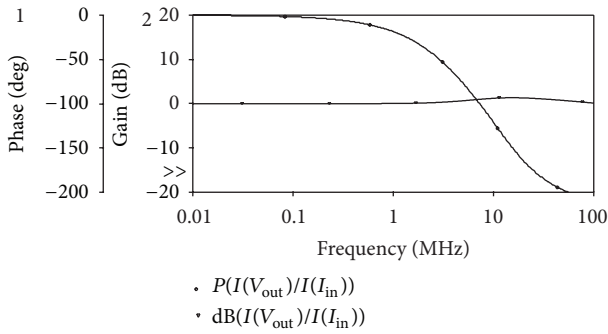


FIGURE 4: Simulated gain and phase responses of the all-pass filter.

respectively, and β_1 and β_2 are the voltage transfer gains from input to $X+$ and $X-$ terminals, respectively. More specifically, $\alpha_1 = (1 - \varepsilon_1)$, $\alpha_2 = (1 - \varepsilon_2)$, $\alpha_3 = (1 - \varepsilon_3)$, $\alpha_4 = (1 - \varepsilon_4)$, $\beta_1 = (1 - \delta_1)$, and $\beta_2 = (1 - \delta_2)$, where ε is the current transfer error (tracking error) and δ is the voltage transfer error (tracking error) of the DX-MOCCII. However, these transfer gains differ from unity by the voltage and current tracking errors of the DX-MOCCII.

The proposed circuit is reanalyzed by taking the tracking errors of the nonideal MO-DXCCII into account, and the modified current transfer function is given as

$$\frac{I_{out}}{I_{in}} = -\alpha_2\alpha_4 \left(\frac{s - (\beta_2\alpha_1/CR\alpha_2)}{s + (\beta_2\alpha_3/CR)} \right). \quad (5)$$

Equation (5) reveals that the nonidealities do affect the filter gain and the pole frequency as well as the zero frequency. Assuming matched current transfer gains (α_1 and α_3) the phase characteristics would not be affected. The sensitivities of pole frequency (ω_o) and gain (H) with respect to active and passive components are derived from (5). These are as follows:

$$\begin{aligned} S_{C,R}^{\omega_o} &= -1, & S_{\alpha_3,\beta_2}^{\omega_o} &= 1, & S_{\alpha_1,\alpha_2,\alpha_4,\beta_1}^{\omega_o} &= 0, \\ S_{C,R}^H &= 0, & S_{\alpha_1,\alpha_3,\beta_1,\beta_2}^H &= 0, & S_{\alpha_2,\alpha_4}^H &= 1. \end{aligned} \quad (6)$$

From the results, it is evident that the sensitivities are within unity in magnitude, thus ensuring a low sensitivity performance.

TABLE 2: Aspect ratios of the transistors.

Transistors	W (μm)	L (μm)
M_1 - M_2	1.4	0.7
M_3 - M_5	2.8	0.7
M_{17} - M_{18}	2.4	0.7
M_{19} - M_{21}	4.8	0.7
M_6 - M_{16} , M_{22} - M_{28}	9.6	0.7

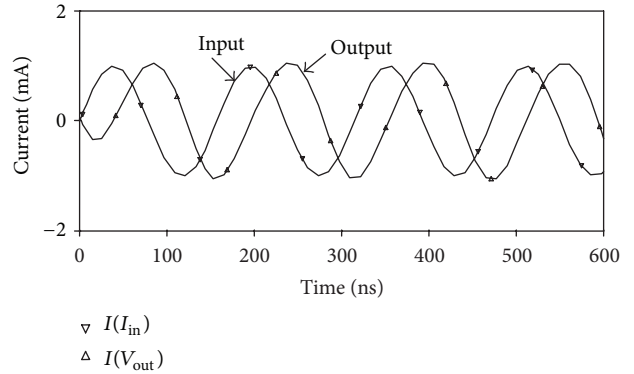


FIGURE 5: Time-domain input and output responses of all-pass filter.

3.2. *Parasitic Effects.* Next study is carried on the effect of device parasitics on the performance of the proposed circuit. The various parasitics are a low value parasitic serial resistance R_X at X the terminal Y exhibits a high value parasitic resistance R_Y in parallel with low value capacitor C_Y , and the terminals Z exhibit a high value parasitic resistance R_Z in parallel with low value capacitance C_Z . The main among these are the Y and Z terminals parasitic capacitances and the X terminal's parasitic resistances. A reanalysis of the proposed circuit yields the modified transfer function as

$$\frac{I_{out}}{I_{in}} = - \left(\frac{sRC' - sRC_{Z2+} - 1}{s^2RR_XC'C_{Z2+} + s(RC' + R_XC' + RC_{Z2+}) + 1} \right), \quad (7)$$

where $C' = C + C_{Z1-} + C_{Z1+}$.

From (7), the effect of capacitance C_{Z2+} becomes non-negligible at very high frequencies. Most of the parasitic

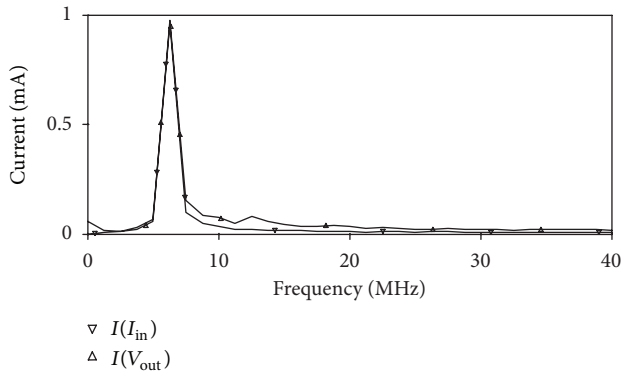


FIGURE 6: Fourier spectrum of the input and output.

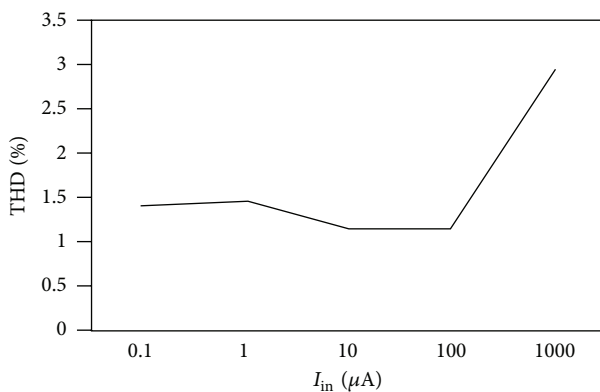


FIGURE 7: THD variation at output (I_{out}) with sinusoidal signal amplitude at 6.36 MHz.

capacitances get absorbed with the external grounded capacitor, as are in shunt with it. Also the parasitic resistance gets absorbed with the external grounded resistor, as it is in series with it. Such a merger will cause a slight deviation in circuit parameters, which can be corrected by predistorting the passive element values used in the circuit.

4. Simulation Results

To demonstrate the performance of the proposed circuit, the PSPICE simulation program is used. In the simulation, the TSMC 0.35 μm CMOS process parameters were used. The CMOS implementation of DX-MOCCII is shown in Figure 3 [13]. The aspect ratios of the CMOS transistors of the DX-MOCCII are listed in Table 2. DC supply voltages of $\pm 1.8\text{ V}$ and biasing voltage of $V_{BB} = -0.7\text{ V}$ were used. The proposed circuit of Figure 2 was designed with $R = 1\text{ k}\Omega$ and $C = 25\text{ pF}$ to obtain a pole frequency of 6.36 MHz. The gain and phase responses are shown in Figure 4, where a phase shift of 90° at a pole frequency of 6.27 MHz is obtained, which is close to the theoretical designed value. The time-domain input and output responses of the circuit at the pole frequency are shown in Figure 5. Also, the Fourier spectrum of input signal and output signal is shown in Figure 6. Next, the amplitude of the input sinusoidal signal is varied from $0.1\text{ }\mu\text{A}$ to $1000\text{ }\mu\text{A}$,

and the total harmonic distortion (THD) curve is plotted at a pole frequency of 6.36 MHz and is shown in Figure 7.

5. Conclusion

In this paper, a new current-mode cascadable all-pass filter is presented. The proposed circuit uses single DX-MOCCII, a grounded resistor, and a grounded capacitor, which is the minimum component realization for an active RC filter circuit. The circuit requires no matching constraints and low active and passive sensitivities and employs grounded passive components only, which makes it suitable for integrated circuit implementation. The circuit also exhibits the feature of low-input impedance and high-output impedance. The PSPICE simulation results of the proposed circuit are in good agreement with the theoretical results.

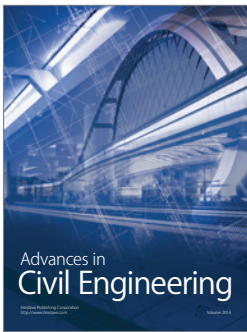
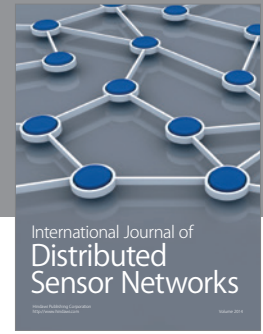
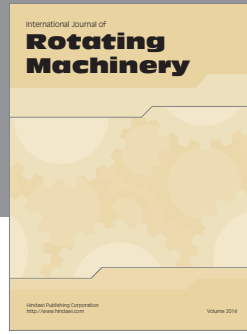
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