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Research Article

Transition Frequencies and Negative Resistance of Inductively Terminated CMOS Buffer Cell and Application in MMW LC VCO

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This paper investigates the transition frequencies (f_{trans}) of an inductively terminated CMOS source follower buffer for negative resistance behavior at which the effective shunt resistance looking into the source of the buffer cell changes sign. Possible limiting frequencies of oscillation are determined based on resonators formed by a grounded gate inductor and a parasitic capacitance at the gate of the negative resistance buffer cell. The range of frequencies of oscillation of this negative resistance buffer cell for variations in the different circuit parameters/elements is explored. Following this, a millimeter wave (MMW) oscillator is simulated using the IBM 130 nm CMOS process technology which can operate at 70 GHz. High-frequency MOSFET model was used for these simulations. The cell had an extremely low power dissipation of under 3 mW. Extensive Monte Carlo simulations were carried out for manufacturability analysis considering up to 50% variation in process and geometrical parameters, supply voltage, and ambient temperature. Noise analysis and a simulated estimate of the phase noise in an MMW LC VCO application is also reported.

1. Introduction

Developing cost-effective advanced microwave communication systems using Millimeter wave (MMW) oscillators, or MMW voltage controlled oscillators (VCOs) on low-cost nanometric bulk CMOS process technologies is of immense interest in the semiconductor and circuit design research community. Design of MMW Oscillators and VCOs in III-V compound semiconductors and Si-Ge Heterojunction devices [1–4] has been reported for many years, but in recent times vast effort has been focused on CMOS MMW implementations [5–8]. In this regard, investigation of the high-frequency behavior and maximum possible oscillation frequency of CMOS negative resistance cell is crucial as CMOS devices have inherently lower unity-gain frequency (f_T) compared to III-V compound semiconductor FET and Si-Ge HBT devices. Recently Veenstra and van der Heijden [9] proposed the maximum possible oscillation frequency of a negative resistance cell as f_{trans}, which is defined as a frequency where the effective negative resistance of the cell R_X turns from negative to positive. The well known cross-coupled CMOS negative resistance cell has the disadvantage of a f_{trans} which is hard-limited by device size and bias drain. CMOS imitations of cross-coupled and other bipolar cells to overcome these f_{trans} limitations has been largely unsuccessful [7]. On the other hand, CMOS versions of Colpitts and Clapp (or Clapp-Gouriet) oscillators were found to have higher f_{trans} than a cross-coupled CMOS pair but suffers from severe deterioration of f_{trans} with output loading at the drain node, and, needed a critical output buffer stage. Recently, the authors in [7] suggested an LC degenerated negative resistance cell to extend considerably the f_{trans} into the 100 GHz MMW range. The f_{trans} was found to be bounded by $1/\sqrt{L_s C_s}$ where L_s and C_s constitute the source degeneration. In this paper we further investigate to reach the ultimate boundary of GHz MMW range of a CMOS negative resistance cell and propose a parasitic resonated CMOS negative resistance source follower buffer-cell using a gate inductor and a parasitic gate capacitance.

2. Transition Frequencies and Negative Resistance of CMOS Buffer Cell

Figure 1 shows the circuit diagram of an NMOS source follower Mb with gate and source inductors and an LC

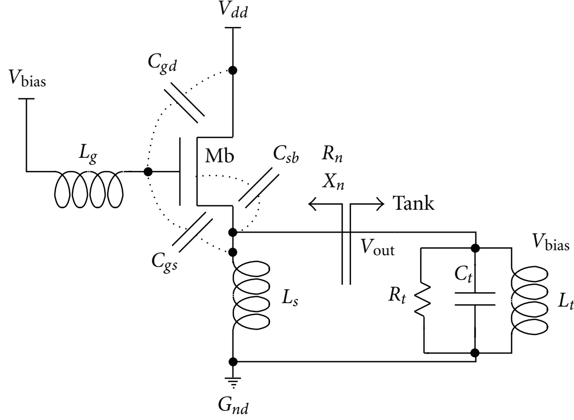

Figure 1: Proposed CMOS source follower buffer for negative resistance and MMW LC VCO application.

tank cascaded at the source for operation as LC VCO. The distributed gate resistance (R_g) is in series with the inductor L_g and contributes to the Q-degradation of L_g. However, R_g is known to be lower than the base resistance of a bipolar device [10] and can be reduced considerably through a careful folded multifinger layout structure [11]. The source inductor L_s works as a DC path and as an AC choke for the output AC signal connection to the tank (consisting of R_t, C_t and L_t). The transistor's main parasitic capacitances reactive in RF operation are indicated with dotted lines, where, C_{gs} is the gate-to-source capacitance, C_{gd} is the drain-to-gate capacitance and C_{sb} is the source-to-body capacitance. Although the body of Mb is connected to ground, there is an AC body effect due to L_s, charging and discharging C_{sb}. The main difference between this proposed circuit and that in [7] is that the tank circuit in the proposed design (being a common-drain configuration) is placed at the source terminal whereas that in [7] (being a common-source with source degeneration configuration) is placed at the drain terminal. The body (p-substrate) is connected to the ground in both cases. Also, the f_{trans} is explored from the parallel combination of the gate inductor and the parasitic gate capacitance in the proposed buffer cell compared to the parallel combination of the source inductor and source capacitance in the design in [7]. Figure 2(a) shows the negative resistance buffer cell with the embedded small signal high-frequency equivalent circuit of the buffer device Mb, where g_m is the transconductance and g_{mb} is the body transconductance of the buffer device. All other model components have their usual meaning for a hybrid-π model. C_{pg} and C_{pd} are parasitic capacitances at the gate and the drain of Mb. In Figure 2(b) the embedded model is slightly simplified by setting R_d (the drain access resistance) and R_i (the equivalent nonquasi-static resistance) to be reasonably negligible [7, 12] resulting in C_{pd} and C_{db} becoming terminated to AC ground at both ends. Next, in Figure 2(c) the body-effect transconductance current source ($g_{mb}V_{bs}$) has been simplified into a simple conductance (g_{mb}) since the voltage-dependent body-effect transconductance current source is due to a voltage across its own terminals for a common-drain configuration [13]. In addition, being parallel to R_{ds}, it is combined as a single conductance with $1/R_{ds}$, as $(g_{mb}+1/R_{ds})$. It is to be noted that the lumped source resistance R_s (a small value in the range of few ohms) in the π-model is actually a distributed source diffusion resistance which is (based on the definition of g_{mb} and R_{ds}) physically interlaced (inter-located) with the source-end location of g_{mb} and R_{ds} as indicated by the diagram in Figure 2(g). Hence for ease in analysis, $(g_{mb} + 1/R_{ds})$ can be moved to the other terminal of the lumped R_s without altering the behavior of the circuit significantly as shown in the Figure 2(c). The effect of $(g_{mb} + 1/R_{ds})$ on the overall performance of the oscillator is still included through its effect on the tank circuit at the output. However, it is well known that for the source follower configuration $(g_{mb} + 1/R_{ds})$ does not dominate the impedance looking into the source of the buffer cell and hence in any case would not have significant effect on the frequency of oscillation. The model in Figure 2(c) can be modified as shown in Figure 2(d), where a current source $g_m V_{gs}$ first enters the gate node g from the grounded drain, and then leaves the gate node g and enters the source node s [14]. The algebraic sum of the respective currents at the nodes g and s are still the same as in Figure 2(c), and hence, Figure 2(d) is equivalent to Figure 2(c). Now since the current source $g_m V_{gs}$ is controlled by the voltage V_{gs} across it, $g_m V_{gs}$ can be replaced with the resistance $1/g_m$ as shown in Figure 2(e). Finally, the Thevenin's equivalent admittance (Y_{TH}) between the source and the ground looking into the source (with the parallel combination of all the passive components between the source terminal S and the ground disconnected being absorbable as components in the LC tank) is shown in Figure 2(f). Y_{TH} is investigated for transition frequencies (f_{trans}) and negative resistance of the source-follower buffer to work as a negative resistance cell. The parasitic capacitances C_{pg} and C_{gd} can form resonators with the gate inductor L_g. Limiting values of f_{trans} can thus be possibly found in terms of L_g, C_{gd}, and C_{pg} for operation as a MMW LC oscillator. From Figure 2(f) if R_g and R_s are initially neglected, the Thevenin's equivalent input admittance $Y_{\text{in}} = Y_{\text{TH}} = i_{\text{in}}/v_{\text{in}}$ is given by

$$Y_{\text{in}} = \frac{\left[g_m - \omega^2 L_g\left(C_{pg} + C_{gd}\right)g_m\right]}{\left[1 - \omega^2 L_g C_{gs} - \omega^2 L_g\left(C_{pg} + C_{gd}\right)\right] + j2g_m L_g\omega} + \frac{j\left[\omega C_{gs} - \omega^3 L_g\left(C_{pg} + C_{gd}\right)C_{gs}\right]}{\left[1 - \omega^2 L_g C_{gs} - \omega^2 L_g\left(C_{pg} + C_{gd}\right)\right] + j2g_m L_g\omega}. \tag{1}$$

Rationalizing by multiplying both the numerator and the denominator by $[1 - \omega^2 L_g C_{gs} - \omega^2 L_g(C_{pg} + C_{gd})] - j2g_m L_g\omega$,

$$\text{RE}[Y_{\text{in}}] = \frac{g_m\left[1 - \omega^2 L_g\left(C_{pg} + C_{gd}\right)\right]}{\left[1 - \omega^2 L_g C_{gs} - \omega^2 L_g\left(C_{pg} + C_{gd}\right)\right]^2 + 4g_m^2 L_g^2\omega^2} \cdot \left[1 + \omega^2 L_g C_{gs} - \omega^2 L_g\left(C_{pg} + C_{gd}\right)\right]. \tag{2}$$

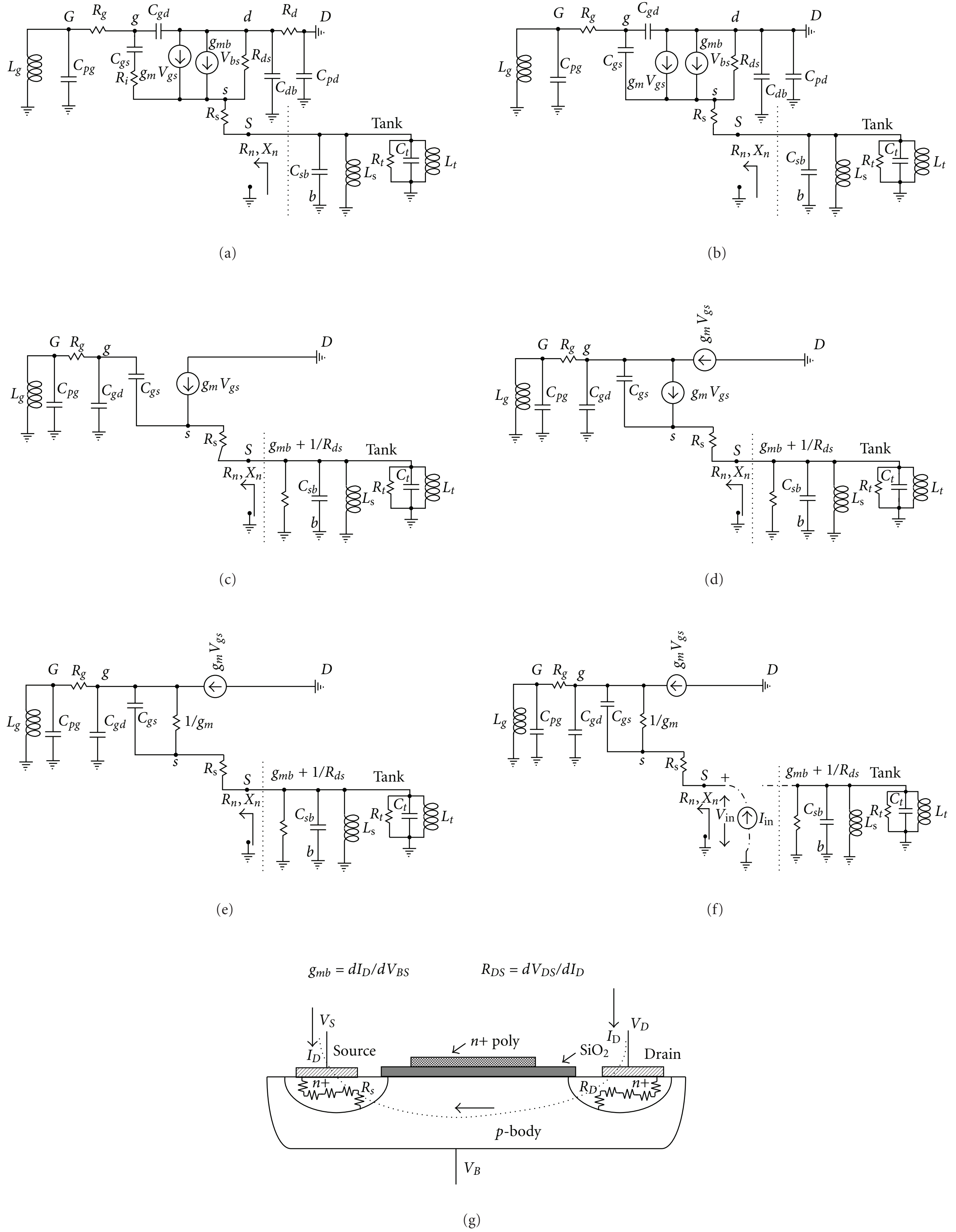

FIGURE 2: A small signal lumped RF model of the proposed negative resistance source follower buffer cell, (b)–(e) its subsequent transformations (neglecting the small resistances R_d and R_i) leading to the final lumped model in (f) to find $Y_{TH}(= 1/R_{TH})$ and (g) NMOS cross-section showing the interlaced location of the distributed source resistance with respect to R_{ds} and g_{mb}.

The two roots of the numerator indicates that the parallel resistance looking into the source, $R_n = 1/Re[Y_{in}]$ changes sign at $\omega = 1/\sqrt{L_g(C_{pg}+C_{gd})}$ and $\omega = 1/\sqrt{L_g[(C_{pg}+C_{gd})-C_{gs}]}$ which are the two approximate transition frequencies of the buffer cell and operation of buffer cell as negative resistance is possible in the region bounded by these two frequencies and constitute the limit for the frequency of oscillation of the buffer cell. Smaller values of L_g and parasitic capacitance can lead to possible higher frequencies at which the negative resistance behavior may be sustainable.

Next for more comprehensive analysis, the transition frequencies and the negative resistance behavior is explored using MATLAB with the inclusion of the effects of R_s and R_g (R_d is found to be noncritical in this regard [12] specially being a common-drain configuration). In this case $Y_{\text{in}}(s)$ in the Laplace domain is a ratio of long polynomials, and, is given by

$$Y_{\text{in}} = \frac{\mathfrak{A}+\mathfrak{B}}{\mathfrak{C}+\mathfrak{D}\left(s^2C_{gd}L_g+s^3C_{gd}R_gL_gC_{pg}+sC_{gd}R_g+s^2L_gC_{pg}+1\right)}. \tag{3}$$

where $\mathfrak{A}$ denotes $(g_ms^2C_{gd}L_g + g_ms^3C_{gd}R_gC_{pg}L_g + g_msC_{gd}R_g + g_ms^2L_gC_{pg} + g_m)$, $\mathfrak{B}$ denotes $(s^3C_{gs}C_{gd}L_g + s^4C_{gs}C_{gd}R_gC_{pg}L_g + s^2C_{gs}C_{gd}R_g + s^3C_{gs}L_gC_{pg} + sC_{gs})$, $\mathfrak{C}$ denotes $(2g_msL_g + 2g_ms^2L_gC_{pg}R_g + 2g_mR_g + s^2C_{gs}L_g + s^3C_{gs}L_gC_{pg}R_g + sC_{gs}R_g)$, and $\mathfrak{D}$ denotes $(1 + R_Sg_m + R_SC_{gs}s)$ Making the substitution, $s = j\omega$, and collecting the real and imaginary terms, the denominator D is given by

$$\begin{aligned} D = &\Big(1 - 2g_m\omega^2L_gC_{pg}R_g + 2g_mR_g - \omega^2C_{gs}L_g \\ &- \omega^2C_{gd}L_g - \omega^2L_gC_{pg} - \omega^2R_Sg_mC_{gd}L_g \\ &- \omega^2R_Sg_mL_gC_{pg} + R_Sg_m + \omega^4R_SC_{gs}C_{gd}R_gL_gC_{pg} \\ &- \omega^2R_SC_{gs}C_{gd}R_g\Big) \\ &+ j\Big(2g_m\omega L_g - \omega^3C_{gs}L_gC_{pg}R_g + \omega C_{gs}R_g \\ &- \omega^3C_{gd}R_gL_gC_{pg} + \omega C_{gd}R_g + \omega R_Sg_mC_{gd}R_g \\ &- \omega^3R_Sg_mC_{gd}R_gL_gC_{pg} - \omega^3R_SC_{gs}C_{gd}L_g \\ &-\omega^3R_SC_{gs}L_gC_{pg} + \omega R_SC_{gs}\Big). \end{aligned} \tag{4}$$

Also, replacing $s = j\omega$, and collecting the real and imaginary terms, the numerator N is given by,

$$\begin{aligned} N = &\Big(g_m + \omega^4C_{gs}C_{gd}R_gC_{pg}L_g - \omega^2g_mL_gC_{pg} \\ &-\omega^2g_mC_{gd}L_g - \omega^2C_{gs}C_{gd}R_g\Big) \\ &+ j\Big(\omega C_{gs} - \omega^3g_mC_{gd}R_gC_{pg}L_g + \omega g_mC_{gd}R_g \\ &-\omega^3C_{gs}C_{gd}L_g - \omega^3C_{gs}L_gC_{pg}\Big). \end{aligned} \tag{5}$$

Next, rationalizing by multiplying both numerator and denominator by D^* (complex conjugate of D),

$$\text{RE}[Y_{\text{in}}] = \text{RE}\left[\frac{N}{D}\right] = \text{RE}\left[\frac{N\cdot D^*}{D\cdot D^*}\right] = \frac{X}{|D|^2}, \tag{6}$$

where

$$\begin{aligned} X = &\Big(g_m + \omega^4C_{gs}C_{gd}R_gC_{pg}L_g - \omega^2g_mL_gC_{pg} \\ &- \omega^2g_mC_{gd}L_g - \omega^2C_{gs}C_{gd}R_g\Big) \\ &* \Big(1 - 2g_m\omega^2L_gC_{pg}R_g + 2g_mR_g - \omega^2C_{gs}L_g \\ &- \omega^2C_{gd}L_g - \omega^2L_gC_{pg} - \omega^2R_Sg_mC_{gd}L_g \\ &- \omega^2R_Sg_mL_gC_{pg} + R_Sg_m \\ &+ \omega^4R_SC_{gs}C_{gd}R_gL_gC_{pg} - \omega^2R_SC_{gs}C_{gd}R_g\Big) \\ &+ \Big(\omega C_{gs} - \omega^3g_mC_{gd}R_gC_{pg}L_g + \omega g_mC_{gd}R_g \\ &- \omega^3C_{gs}C_{gd}L_g - \omega^3C_{gs}L_gC_{pg}\Big) \\ &* \Big(2g_m\omega L_g - \omega^3C_{gs}L_gC_{pg}R_g + \omega C_{gs}R_g \\ &- \omega^3C_{gd}R_gL_gC_{pg} + \omega C_{gd}R_g + \omega R_Sg_mC_{gd}R_g \\ &- \omega^3R_Sg_mC_{gd}R_gL_gC_{pg} - \omega^3R_SC_{gs}C_{gd}L_g \\ &- \omega^3R_SC_{gs}L_gC_{pg} + \omega R_SC_{gs}\Big), \\ |D|^2 = &\Big(1 - 2g_m\omega^2L_gC_{pg}R_g + 2g_mR_g \\ &- \omega^2C_{gs}L_g - \omega^2C_{gd}L_g - \omega^2L_gC_{pg} \\ &- \omega^2R_Sg_mC_{gd}L_g - \omega^2R_Sg_mL_gC_{pg} + R_Sg_m \\ &+\omega^4R_SC_{gs}C_{gd}R_gL_gC_{pg} - \omega^2R_SC_{gs}C_{gd}R_g\Big)^2 \\ &+ \Big(2g_m\omega L_g - \omega^3C_{gs}L_gC_{pg}R_g + \omega C_{gs}R_g \\ &- \omega^3C_{gd}R_gL_gC_{pg} + \omega C_{gd}R_g + \omega R_Sg_mC_{gd}R_g \\ &- \omega^3R_Sg_mC_{gd}R_gL_gC_{pg} - \omega^3R_SC_{gs}C_{gd}L_g \\ &-\omega^3R_SC_{gs}L_gC_{pg} + \omega R_SC_{gs}\Big)^2. \end{aligned} \tag{7}$$

$R_n = 1/\text{RE}[Y_{\text{in}}]$ is then computed for various circuit parameters by executing several MATLAB m-file programs. In these simulations, nominal values of $C_{pg} = 5$ fF, $C_{gd} = 5$ fF, $L_g = 0.2$ nH, $C_{gs} = 15$ fF, $g_m = 0.015$ S, $R_g = 25.9$, Ω and $R_s = 12.7\ \Omega$ for a 130 nm IBM CMOS process technology were initially set and one of the component values were varied to explore the changes in the transition frequencies and the negative resistance (R_n) behavior. Figure 3 shows the variation of R_n due to g_m varying between 0.01 S and 0.022 S. There are two f_{trans} in this case almost anchored at 80 GHz and 220 GHz irrespective of the variation of g_m,

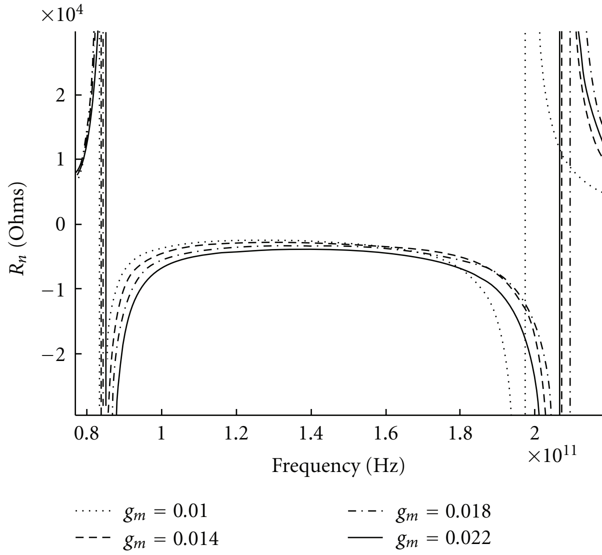

Figure 3: Variation of R_n with g_m.

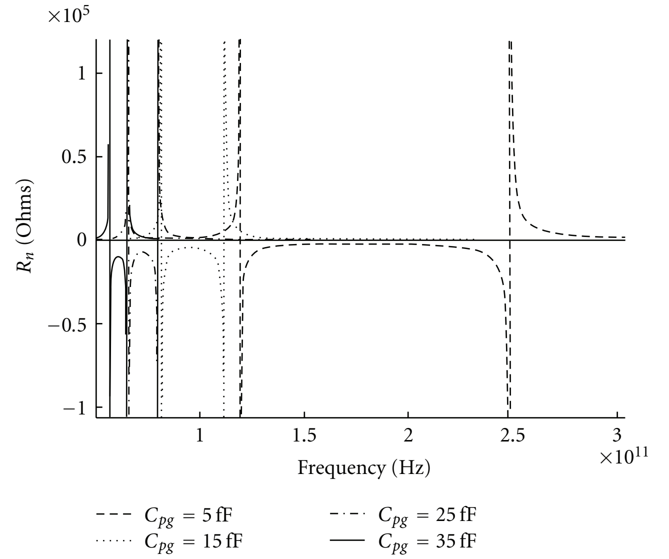

Figure 4: Variation of R_n with gate-to-ground parasitic capacitance C_{pg}.

and a R_n maxima (its smallest magnitude) is achieved at around 130 GHz which is also largely invariant with g_m only increasing slightly with lower values of g_m. Figure 4 shows that, different values of the parasitic gate capacitance C_{pg} lead to a different set of transition frequencies with the range and interval of the f_{trans} becoming higher with lower values of C_{pg}. In addition, the negative resistance maxima is achieved at lower values of C_{pg}. MMW LC VCO operation in the 150 GHz to 225 GHz may be possible with a $C_{pg} = 5$ fF. Figure 5 shows the variation of R_n with L_g. With too low a value of L_g the negative resistance behavior ceases, but using reasonably low $L_g = 0.06$ nH operation near 300 GHz may be possible. Larger values of L_g leads to lower f_{trans} frequencies and lower values of the R_n maxima. Also, the f_{trans} for close L_g values overlap to some extent as can be observed in Figures 5, 6, and 7 shows the effect of reducing R_g and R_s respectively, on R_n, which mostly consist of a higher value of the upper f_{trans} and more so in case of a reducing R_s. The range of the negative resistance behavior also becomes wider with the possibility of operating close to 350 GHz. The f_{trans} frequencies and the possible range of negative resistance maxima values are thus found to be limited only by technology scaling [15] and the parasitic capacitances of the MOS device.

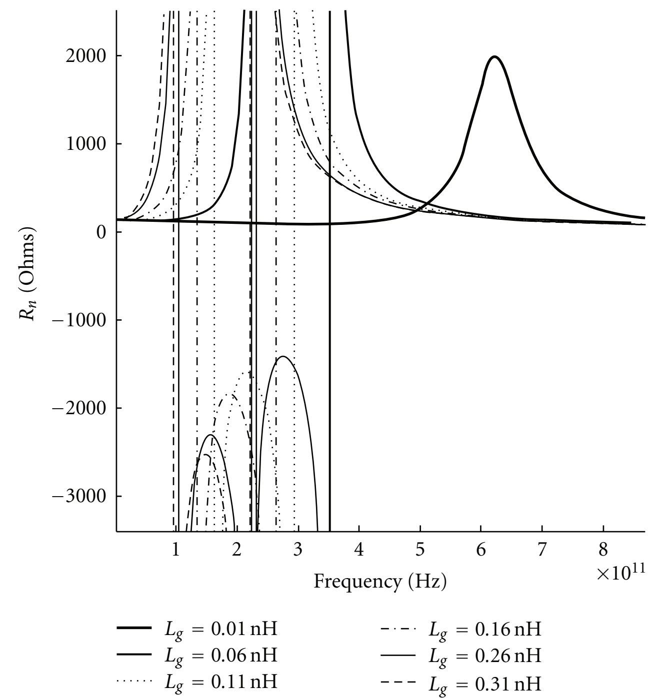

Figure 5: Variation of R_n with gate-to-ground inductance L_g.

3. Phase Noise Considerations in the Negative Resistance Buffer Cell

Figure 8 shows a practical noise inserted circuit diagram for the negative resistance source-follower buffer cell. The main device noise sources are the thermal gate current noise, the thermal drain current noise, and the flicker noise ($1/f$ noise). The drain current noise power spectral density [16] of the MOSFET is given by $\overline{I^2_{n_t d,\text{Mb}}(f)} = 4KT\gamma g_m/\alpha\ \text{A}^2/\text{Hz}$, while the gate current noise power spectral density is given by, $\overline{I^2_{n_t g,\text{Mb}}(f)} = 4KT\delta\omega^2\alpha C^2_{gs}/5g_m\ \text{A}^2/\text{Hz}$. In these noise expressions, K is the Boltzman constant, T is the temperature in absolute scale, γ and δ are, respectively, the coefficients of the channel thermal noise and the gate thermal noise which depends on the channel length of the MOSFET device. Also, $\alpha = g_m/g_{d0}$, with g_{d0} being the zero-bias drain-to-source (channel) conductance (@ zero V_{DS}) of the MOSFET device [16]. The gate current noise in the MOSFET is due to the gate-oxide capacitive coupling of the random channel charge fluctuations at radio frequencies, which is

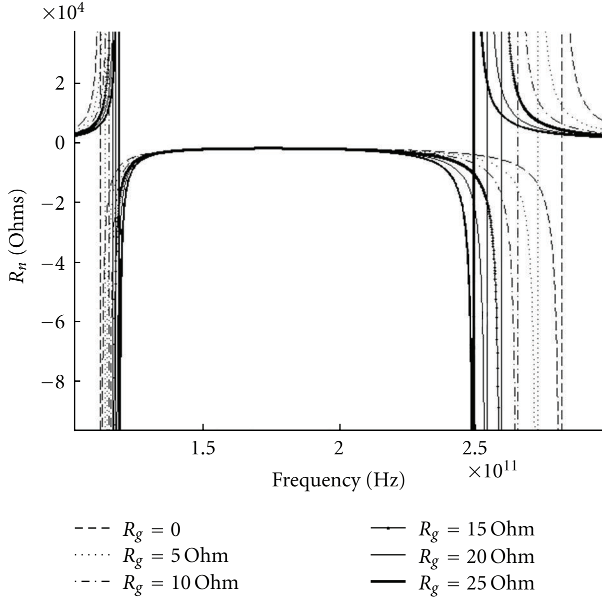

Figure 6: Variation of R_n with gate resistance R_g.

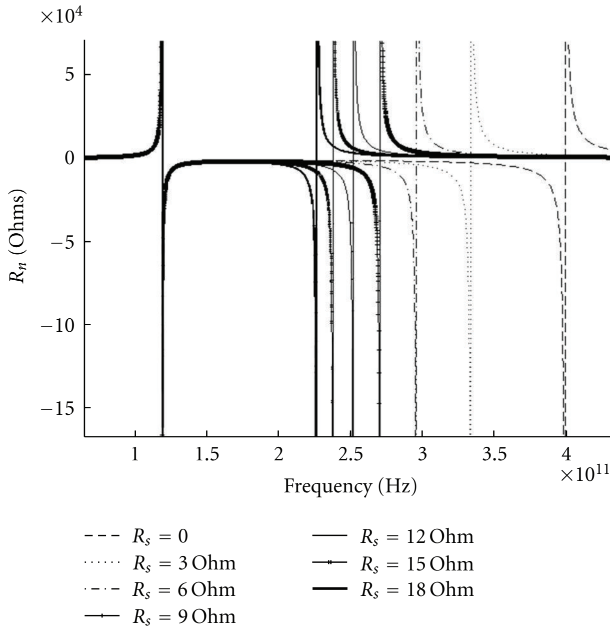

Figure 7: Variation of R_n with source resistance R_s.

thus cross-correlated with the drain current noise. This cross-correlation is given by a factor, c_{Mb} for the MOSFET Mb, with, $\overline{i_{n_t d,\mathrm{Mb}}(f).i^*_{n_t g,\mathrm{Mb}}(f)} = c_{\mathrm{Mb}}\sqrt{\overline{i^2_{n_t g,\mathrm{Mb}}(f)}.\overline{i^2_{n_t d,\mathrm{Mb}}(f)}}$. For long-channel MOSFETs $\gamma = 2/3$, $\delta = 4/3$ and $c = j\ 0.395$. Short channel effects changes these factors considerably. Using C_{Mb}, the correlated and the uncorrelated parts of the gate current noise are, $\overline{I^2_{n_t gc,\mathrm{Mb}}(f)} = \overline{I^2_{n_t g,\mathrm{Mb}}(f)} * |c_{\mathrm{Mb}}|^2$ and $\overline{I^2_{n_t gu,\mathrm{Mb}}} = \overline{I^2_{n_t g,\mathrm{Mb}}} * (1 - |c_{\mathrm{Mb}}|^2)$, respectively, for the MOSFET Mb. The flicker noise ($1/f$ noise) is given by, $\overline{I^2_{n_f d,\mathrm{Mb}}(\mathrm{f})} = (K_f I_D/L^2 C_{\mathrm{ox}})(1/f)$ A^2/Hz [17, 18], where the flicker noise coefficient $k_f \approx 10^{-28}$ F-A, L is the device channel length, I_D is the bias drain current and C_{OX} is the oxide capacitance per unit channel area. The total mean squared output noise current power $\overline{I^2_{\mathrm{no}}}$ parallel to the tank at the source of Mb is then given by

$$\overline{\mathrm{I}^2_{\mathrm{no}}} = \mathrm{I}^2_{\mathrm{n_t gu,Mb}} + \left(\sqrt{\overline{\mathrm{I}^2_{\mathrm{n_t gc,Mb}}(\mathrm{f})}} + \sqrt{\overline{\mathrm{I}^2_{\mathrm{n_t d,Mb}}(\mathrm{f})}}\right)^2 + \overline{\mathrm{I}^2_{\mathrm{n_f d,Mb}}(\mathrm{f})}. \tag{8}$$

Or after expanding the cross-correlation,

$$\begin{aligned}\overline{I^2_{\mathrm{no}}} &= \overline{I^2_{n_t g,\mathrm{Mb}}(f)} + \overline{I^2_{n_t d,\mathrm{Mb}}(f)} \\ &\quad + 2|c_{\mathrm{Mb}}|\sqrt{\overline{I^2_{n_t g,\mathrm{Mb}}(f)} \cdot \overline{I^2_{n_t d,\mathrm{Mb}}(f)}} + \overline{I^2_{n_f d,\mathrm{Mb}}(f)}.\end{aligned} \tag{9}$$

Or

$$\begin{aligned}\overline{I^2_{\mathrm{no}}} &= \frac{4KT\delta\omega^2\alpha C^2_{gs}}{5g_m} + \frac{4KT\gamma g_m}{\alpha} \\ &\quad + 2|c_{\mathrm{Mb}}| * 4KT\omega C_{gs}\sqrt{\frac{\delta\gamma}{5}} + \frac{K_f I_D}{L^2 C_{ox}}\frac{1}{f}\ A^2/Hz.\end{aligned} \tag{10}$$

This composite device noise current manifests as a phase noise “skirt” [19] of the output frequency of oscillation across the tank circuit at the source terminal of the buffer cell. Figure 9 shows a typical plot of oscillator phase noise in terms of the normalized single-sideband noise spectral density ($L(\Delta\omega)$ in dBc/Hz at a frequency offset of $\Delta\omega$) which consists of three separate regions, a $1/f^3$ region at very small offsets, a $1/f^2$ region, and a constant noise floor extending into higher frequency offsets from the oscillator center frequency [20]. All the white noise components (such as thermal drain current noise and induced gate noise) fold into phase noise near the oscillator center frequency in the $1/f^2$ $(= 1/(\Delta\omega^2))$ region, while, the low frequency flicker noise (i.e., MOS $1/f$ noise) is upconverted into close-in phase noise in the $1/f^3$ $(= 1/(\Delta\omega^3))$ region. Any noise current source with *noise current power spectral density* (PSD), $\overline{i^2_n(f)}$, at the buffer cell output, containing $1/f^p$ noise will have a$1/f^{p+2}$ region in the phase noise spectrum. The flat noise floor would arise from the white noise floor of output pad devices which is not filtered by the LC tank of the buffer cell. As can be seen from (10) there is a tradeoff between bias current and device dimension for minimizing the phase noise of a VCO (voltage controlled oscillator) implementation using the buffer cell.

4. Spice Simulation Results

In order to verify the theoretical derivations of f_{trans} and negative resistance of the inductively terminated CMOS source-follower buffer cell, SPICE simulations (using Tanner Tools Pro T-SPICE V.12 and Synopsys HSPICE-RF) were conducted. The IBM 0.13 μm 8M1P CMOS process with level 49 typical device parameters were used for this purpose.

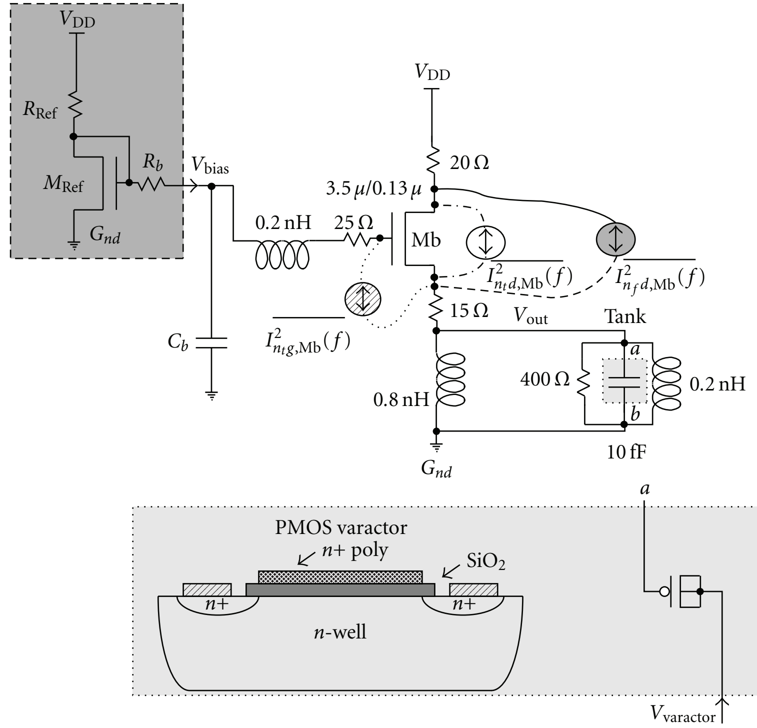

FIGURE 8: A practical noise inserted CMOS negative resistance buffer cell with component values, bias circuit, and varactor tuned tank.

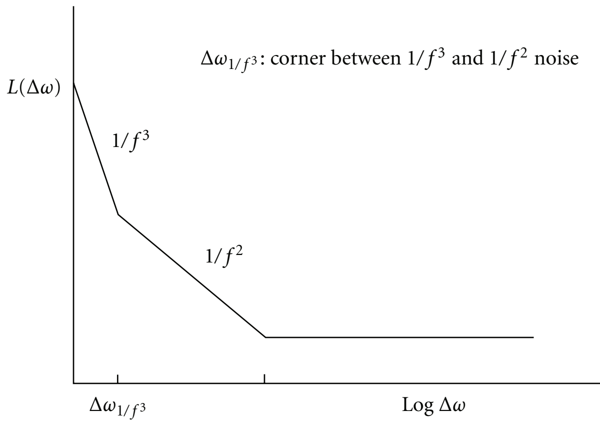

FIGURE 9: Typical phase noise plot of output oscillation versus offset $\Delta\omega$ from the center frequency of the negative resistance buffer cell.

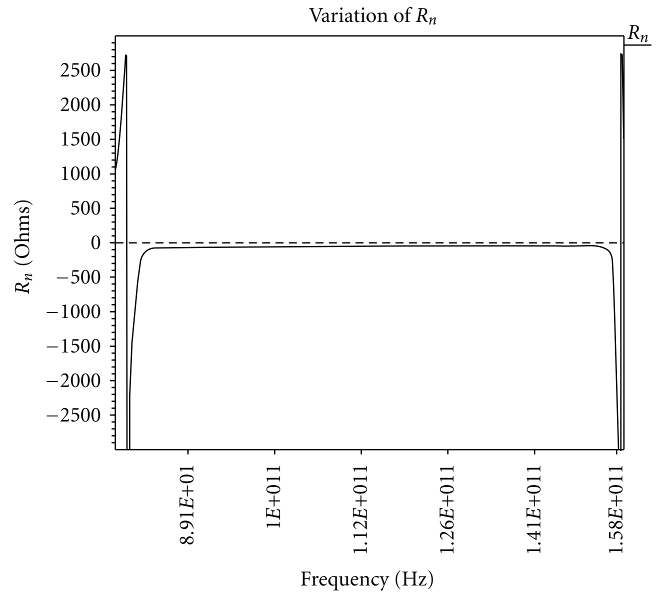

FIGURE 10: SPICE simulation of the negative resistance behavior of the buffer cell.

These level 49 SPICE parameters accounted for the RF performance constraints due to all the parasitic junctions, overlap and fringe capacitances associated with the gate, drain, source, and body of the MOSFET device. The circuit in Figure 8 was used for the simulations. The required gate bias voltage can be set using an appropriate current mirror as shown. C_b is a large shunt capacitor in order to AC ground the V bias connection to the inductively terminated gate of Mb. Also, an PMOS varactor implementation [21, 22] of the tank capacitor for tuning purpose (as an MMW VCO) is also depicted in the Figure. The varactor is tuned by applying a variable positive DC voltage at the V varactor terminal with the gate terminal connected to DC ground as shown in the circuit. The unity gain frequency ($f_T \approx g_m/C_{gs}$) of the NMOS device Mb in the oscillator circuit of Figure 8 was above 150 GHz, and hence, oscillations at high GHz range was achievable using this device. Additional

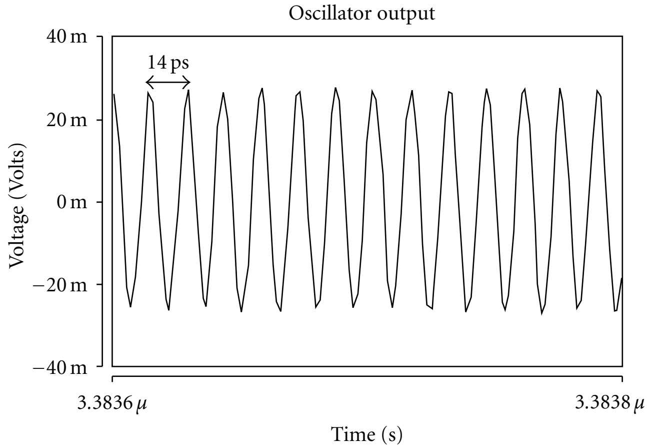

Figure 11: Transient output of the CMOS negative resistance buffer-cell oscillator of Figure 8 indicating a time period of around 14 picoseconds.

resistances for R_d, R_s, and R_g were augmented to consider deteriorations of high-frequency behavior due to parasitic terminal resistances. R_d has a slightly higher value than R_s considering that the drain area near the channel is sometimes lightly doped (lightly doped drain, LDD) to prevent short channel hot carrier effect and hence may have a slightly higher resistance compared to the source area. In addition, the drain-to-body region near the channel of a saturated MOSFET is often depleted of carriers and hence will have somewhat higher resistance than the source-to-body region near the channel. A low-Q tank was used with a resonant frequency of 100 GHz. The overall frequency of oscillation is determined by the overall reactance due to the tank and the reactive component of the negative resistance cell. In order to simulate the negative resistance behavior of the buffer cell the circuit in Figure 8 was simulated by removing the tank circuit and applying an AC signal at the source node. The inductor L_S was replaced with a large DC feed choke whose RF impedance is large compared to the impedance looking into the source node and almost all of the AC current flows into the source node. A negative resistance (as shown in Figure 10) in the range of around hundred ohms was observed which is roughly close to the values obtained through MATLAB simulations. Also, the transition frequencies were approximately close to the analytical values limited mostly by the device parasitics. Figure 11 shows the transient output of the CMOS negative resistance buffer-cell oscillator of Figure 8 indicating an output power of −19 dBm (25 mVpk) which is lower than the −5 dBm (126 mVpk) reported for the single-ended output of the VCO in [7]. On the other hand, the simulation indicates a time-period of only around 14 picoseconds for the buffer cell VCO, and Figure 12 shows the frequency spectrum (H-SPICE generated 131072-point FFT using Kaiser window) for the buffer cell oscillator output, indicating a fundamental frequency of around 70 GHz. In order to compare the proposed negative resistance buffer cell with the VCO cell of [7], a single-ended version of the VCO cell in [7] was simulated using the same 130 nm IBM CMOS process technology. The same output LC tank as the proposed buffer cell was attached to the drain terminal of this VCO cell in [7] for the simulations. In this case a wider device with higher drain current than the proposed buffer cell was required to sustain oscillations for the same drain resistance, and, an oscillation frequency of only ≈50 GHz. was achieved. This comparative performance of the design in [7] with respect to the proposed VCO design would not be altered significantly if R_d were not higher than R_s (or, if the values of R_d and R_s were swapped) in any possible variations in design, layout, fabrication or device operation. The time-constant due to any output buffer/pad parasitic capacitance will always be higher at the drain node (for the design in [7]) compared to that at the source node (for the proposed design) due to the smaller resistance looking into the source node compared to that looking into the drain node. The impedance looking into the source node of Mb is the sum of R_s and $1/g_m$, whereas, the impedance looking into the drain node is the sum of R_d and the source degenerated impedance looking into the drain, which is much larger than the sum of the resistances at the source. Consequently, the pole at the drain node would be closer to the origin in the s-plane compared to the pole at the source node. For this reason, the proposed buffer cell is inherently capable of operating at higher oscillation frequencies compared to the design in [7]. The simulated tuning range using the varactor for the buffer cell is in the range of 66 GHz to 79 GHz which is higher than the tuning range of the single-ended VCO (fundamental port) of the design in [7]. The push-push differential form of the design in [7] had an optional 114 GHz output which is obtained by canceling the fundamental and summing the second harmonics from the two single-ended outputs. This requires significant 2nd harmonic currents and proper phasing of current waveforms. Similar differential form for the buffer cell can also be created with ≥140 GHz optional VCO output. In addition, this buffer cell consumed under 3 mW compared to the reported 3.6 mW (excluding the additional 4.8 mW dissipation in the output buffer) by the design in [7]. In accordance with the simulations carried out for both the circuits, with the required wider device size for sustained oscillations in case of the VCO in [7], the proposed buffer cell is expected to be more energy efficient than the VCO in [7] for certain application scenarios. The source inductor can be implemented (absorbed) by the wirebond inductance and an output buffer may be needed to drive the bonding pad and package parasitics. Also, a Total Harmonic Distortion (THD) of at least −50 dB is achieved by the proposed buffer cell oscillator as indicated by the frequency spectrum in Figure 12. This proposed negative resistance cell will thus find wide applications in 60-GHz WLAN and automotive radar systems compared to previously published MMW VCO circuits in [5–7].

4.1. Monte Carlo Simulations for Manufacturability. In order to verify the design for manufacturability (practical implementation) extensive Monte Carlo simulations were also carried out using a Gaussian distribution function and up to

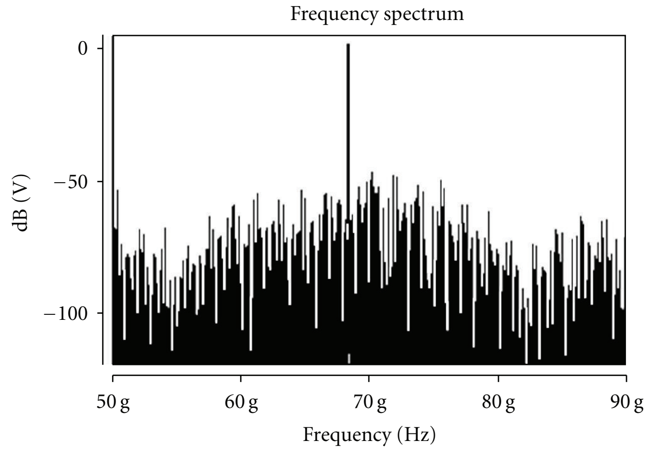

Figure 12: Frequency spectrum for the buffer cell oscillator output indicating a fundamental frequency of around 70 GHz.

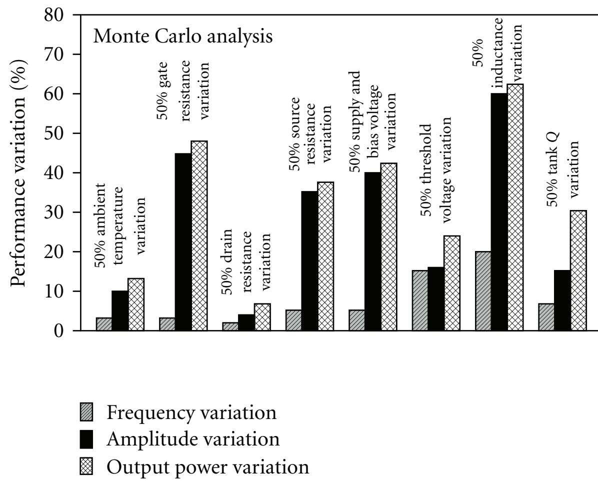

Figure 13: Bar chart of overall temporal Monte Carlo simulations for manufacturability for 50% variation in the process, circuit, and environmental parameters.

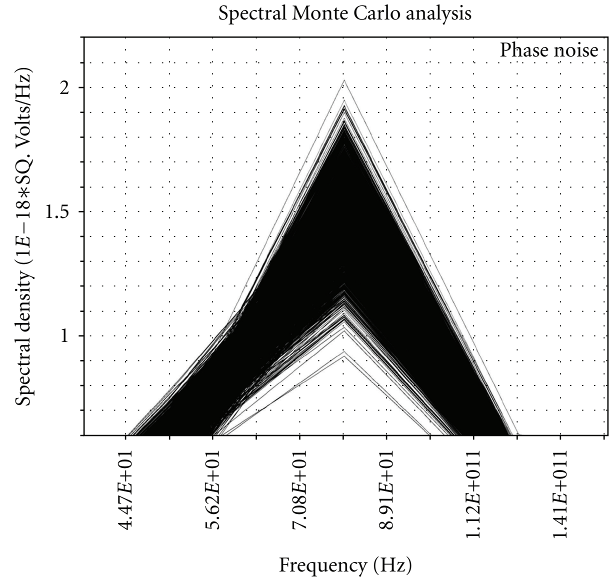

Figure 14: Monte Carlo simulation of phase noise "skirt" near a center frequency of ≈77 GHz for the proposed buffer cell oscillator.

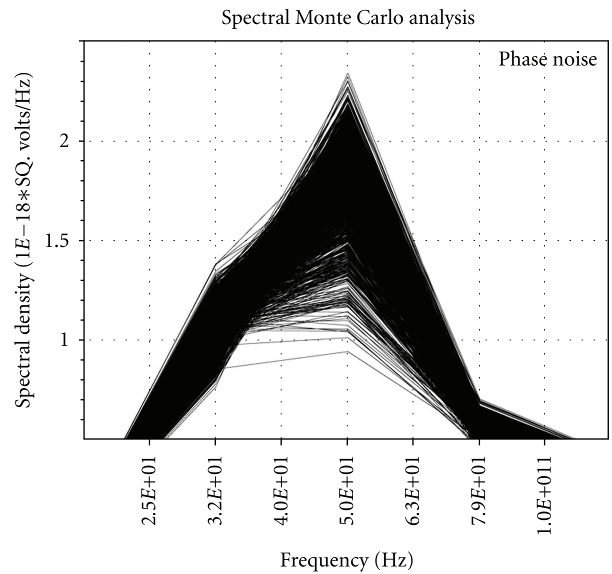

Figure 15: Monte Carlo simulation of phase noise "skirt" near a center frequency of ≈50 GHz for the VCO cell in [7].

50% variation in process and geometrical parameters, supply voltage, and ambient temperature. The degradation of tank Q due to substrate leakage is one of the major high-frequency effects in the high GHz range in silicon integrated circuits. A bar chart is shown in Figure 13 comparing the results of all the temporal Monte Carlo simulations including the temperature variation. As can be seen from the comparison of the different bar plots, the common-drain configuration results in very small effect of the drain resistance variation, while, as expected, fluctuation of inductance (due to process and geometry variations) has the largest effect on the oscillation frequency. Gate resistance can be reduced by layout techniques discussed in [11] thereby considerably reducing its detrimental effect on f_{trans}. The sensitivity of the oscillator frequency with threshold voltage variation is due to the variation of the overdrive voltage resulting in a variation of the charging (pull-up)/discharging (pulld-own) current at the source node. The variation of the oscillator output power with the various parameters is also shown in the Figure 13 indicating a trend similar to that of the amplitude variation. It can thus be concluded from these thorough Monte Carlo simulations that the presented LC VCO design using the source-follower negative resistance cell is quite robust and it achieves an oscillation frequency of 70 GHz under worst possible process degradations. The results being reported here are thus expected to be roughly close to measured results from a monolithic fabrication of the proposed buffer-cell using the 130 nm CMOS process. In order to estimate the phase noise of the buffer-cell oscillator, input referred noise current power source across the LC tank

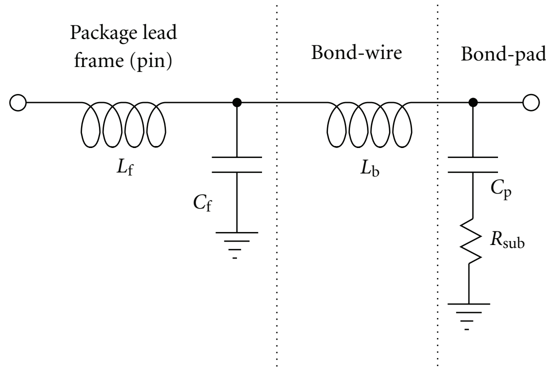

FIGURE 16: Lumped-element model of package pin, wirebond, and bondpad.

(as discussed in Section 3) is assumed. The rough estimate of the phase noise was determined, using (a) the standard T-SPICE noise models ($\gamma = 0.66$ for drain current noise) and the noise simulation setup and (b) considering the effect of noise folding due to nonlinearity related intermodulation products [19, 23] of the form $2\omega_0 - \omega_n$, with, $2\omega_0$, being the oscillator second harmonic and ω_n being the noise tones in the vicinity of ω_0. An approximate Monte Carlo simulation (2000 simulation iterations with Process, Voltage and Temperature variations) of the phase noise spectrum for the proposed buffer cell (centered @ ≈77 GHz) is shown in Figure 14, indicating noise-shaping by the bandpass behavior of the output LC-tank centered at around 77 GHz (in close agreement with the FFT spectrum of Figure 12). The spectral density is given in 10^{-18} Sq. Volts/Hz. With carrier signal level at around 17.68 mV RMS and approximate worst case phase noise at an offset of 600 KHz $\approx 2 * 10^{-18}$ Sq. Volts/Hz, the approximate phase noise with respect to the carrier (@ 77 GHz) is around –142 dBc/Hz at an offset of 600 KHz from the carrier. Considering all possible noise sources (e.g., injected circuit noise and other sources of thermal and $1/f^p$ noise, etc.) in a monolithic RF system, the actual measure of the phase noise is expected to be worse (higher) (>−125 dBc/Hz). Allowable channel spacings are often constrained by achievable carrier phase noise performance at a close-in offset frequency [24], and narrow channel spacing in the hundreds of KHz is a reasonable consideration in evaluating the phase noise performance of an oscillator at such an offset from the oscillator's center frequency. Figure 15 shows the result of similar phase noise simulation for the single-ended version of the VCO cell of [7]. The center frequency in this case (using the same LC tank) was around 50 GHz thus indicating lower achieved single-ended oscillation frequency by the VCO design in [7] compared to the proposed negative resistance buffer cell under similar simulation conditions. Also, as can be seen from the simulation, the phase noise skirt surrounding the center frequency is more irregular with wide variations with variations in process and environmental parameters compared to that for the proposed buffer cell VCO. The estimated simulated phase noise in this case is around −137 dBc/Hz (600 KHz offset from the carrier) which is higher compared to the proposed buffer cell VCO. As mentioned, it is understood that in a practical monolithic implementation the phase noise is expected to be much higher, but based on the Monte Carlo simulations, the proposed buffer cell VCO is expected to have an overall better phase noise performance compared to the design in [7].

4.2. Packaging and Bond-Wire Considerations. Figure 16 shows the composite lumped model of a typical packaged RF signal output interconnect path consisting of package lead frame (pin), bond-wire, and bond-pad [25]. In this model, L_f and L_b are, respectively, the lead-frame pin and bond-wire inductances whose values depend on the frequency and the type of packaging, C_f and C_p are, respectively, the lead-frame pin and bond-pad capacitances whose values mostly depend on the type of package. Also, R_{sub} (substrate resistance) accounts for the finite Q-factor of the package. Packaging issues were not discussed in [7] and the output buffer was used to drive an on-wafer 50 Ω probe on the probe pad. Such buffers are easily designed using a source follower to match its output impedance ($1/g_m$) to 50 Ω transmission line characteristic impedance. For packaging consideration at such high RF/MW frequencies, the flip-chip or control-collapse-chip-connection (C4) option utilizing solder bumps may be desirable for direct connection of RF output to 50 Ω PCB transmission line. For other possible packaging options (such as Ball Grid Array) off-chip microstrip line matching to 50 Ω may be necessary. In such a case, in order to minimize ground path inductance [25], several pins (wire bonded to separate die grounds) should be connected to the PCB ground plane and also downbonded to the package (carrier) substrate (package ground plane). In order to use bond wire for the source inductor L_S, several parallel bond wires may be needed along with down-bonding to package substrate (package ground plane) in order to bring down the source inductance to the desired value (≈0.8 nH in this case) from a value of 1 to 2 nH for each bond wire.

5. Conclusion

An MMW LC VCO exploring the transition frequencies (f_{trans}) and the negative resistance of an inductively terminated source follower buffer cell has been proposed. The f_{trans} frequencies and possible range of negative resistance maxima values has been found to be limited only by technology scaling and the parasitic capacitances of the MOS device. A f_{trans} of over 250 GHz can be obtained for a circuit using 130 nm CMOS process technology, and simulated oscillations at 70 GHz (limited only by the tank's reactance) was demonstrated using a low-Q LC tank at the source output. Extensive Monte Carlo simulations prove that the presented design is quite robust to process degradations and high GHz substrate leakage in a practical implementation as well as to significant power supply scaling. A noise analysis was also carried out.

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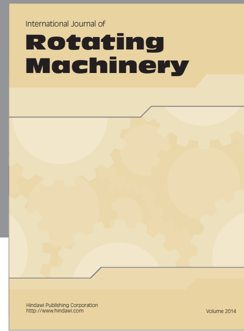
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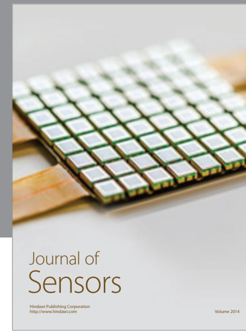
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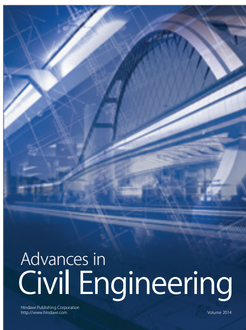
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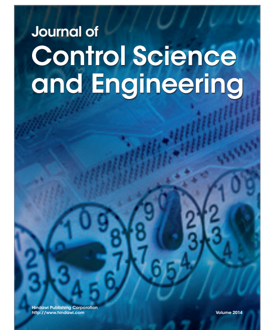
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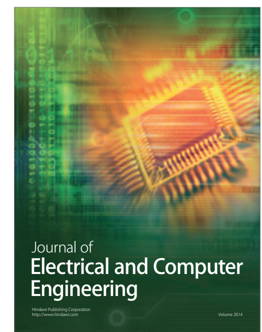
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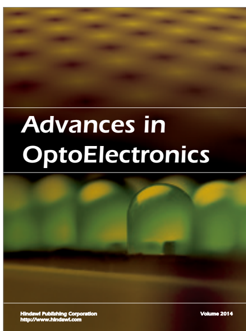
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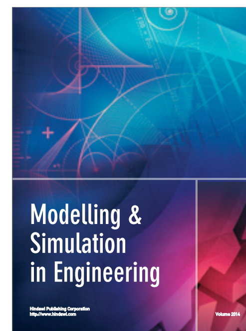
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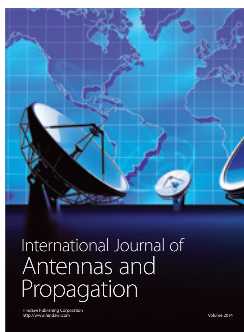
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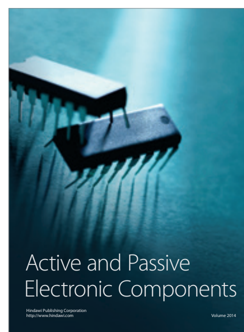
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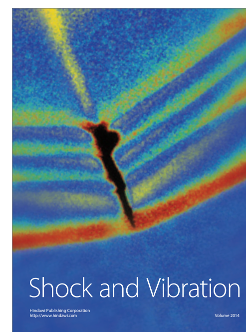
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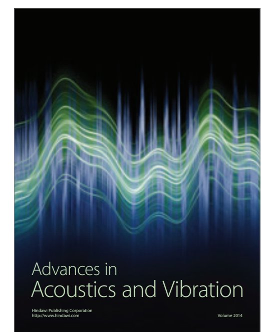
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