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Research Article

Parallel PWMs Based Fully Digital Transmitter with Wide Carrier Frequency Range

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The carrier-frequency (CF) and intermediate-frequency (IF) pulse-width modulators (PWMs) based on delay lines are proposed, where baseband signals are conveyed by both positions and pulse widths or densities of the carrier clock. By combining IF-PWM and precorrected CF-PWM, a fully digital transmitter with unit-delay autocalibration is implemented in 180 nm CMOS for high reconfiguration. The proposed architecture achieves wide CF range of 2 M–1 GHz, high power efficiency of 70%, and low error vector magnitude (EVM) of 3%, with spectrum purity of 20 dB optimized in comparison to the existing designs.

1. Introduction

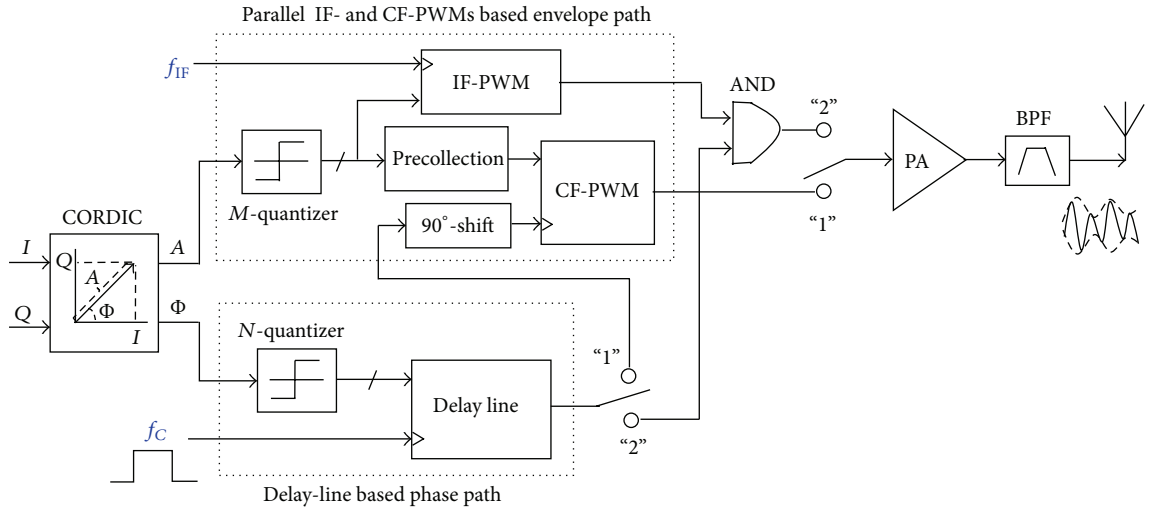
Wireless communication is becoming more and more important and ubiquitous in modern society. To support numbers of communication standards in small and same handheld devices, there are growing demands for flexible transmitters and receivers supporting multimode communications with high efficiency. Recently, lots of researches have been conducted in RF reconfigurable transceivers using novel hardware implementation. This paper focuses on fully digital wireless transmitters.

The existing design [1, 2], employing all-digital phase-locked loop (ADPLL) and delta-sigma modulator, introduces large fractional spurs and requires strict energy match between power branches. The existing transmitters with quadrature [3, 4] or delay-line [5, 6] based intermediate-frequency (IF) pulse-width modulation (PWM), are not apt for low carrier-frequency (CF) applications, under which the band-pass filter (BPF) fails to suppress IF component or harmonics closer to the carrier. The existing radio-frequency (RF) PWM [7] or direct digital frequency synthesizer (DDFS) [8] based transmitters, aiming for low CF conditions, are not considered as fully digital designs, since analogue feedback or mixed-signal configurations are used. The existing architecture [9] employing outphasing amplification technique is not widely used in commerce due to strict matching requirements between dual paths and distortion and efficiency degradation caused by RF power combiner.

In this paper, delay-line based CF-PWM with precorrection logic is proposed, where the only carrier clock is employed to ensure spectrum purity under low CF conditions. By combining IF-PWM for high CF and precorrected CF-PWM for low CF, a fully digital transmitter is presented with wide CF range and high efficiency. A unit-delay autocalibration loop for delay lines is also proposed with reconfigurable carrier frequency f_C.

2. Architecture

Figure 1 shows the proposed fully digital transmitter with parallel IF- and CF-PWMs. The coordinate rotation digital computer (CORDIC) algorithm accomplishes the conversion from I/Q to polar coordinate A/Φ [10]. The wide CF range of 2 M–1 GHz is divided into low f_C band of 2 M–100 MHz and high f_C band of 80 M–1 GHz. About 20 MHz frequency overlap area is chosen to avoid the switching jitter between high and low f_C bands. Under low CF band, the transmitter working in mode "1" and CF-PWM enabling, multibit phase component Φ is mapped to 1/4-period position of the carrier clock, and multibit envelope component A is converted to precorrected pulse width of the carrier clock. For high CF case, mode "2" and IF-PWM enabling, phase Φ is conveyed



"1": low carrier frequency
"2": high carrier frequency

Figure 1: Proposed fully digital transmitter with parallel IF- and CF-PWMs.

by rising-edge position of the carrier clock, and envelope A is represented by pulse width of an IF clock and subsequently converted to pulse density of the carrier clock. The position- and pulse-modulated carrier clock, amplified by a switched-mode class-D power amplifier (PA), is reshaped to the phase- and envelope-modulated sinusoidal carrier by an BPF with CF or IF harmonics suppressed.

The output sinusoidal amplitude y and input duty cycle d of the BPF conform to (1), according to Fourier series expansion of periodic square wave [7]. For IF-PWM mode, it is the pulse densities rather than pulse widths of the carrier clock that represent baseband envelopes; the BPF handling standard square waves with a fixed duty cycle of 0.5 does not encounter any nonlinear distortion. However, for CF-PWM one, the pulse widths or duty cycles on behalf of baseband envelopes are variable. That is, the BPF not only introduces envelope distortions, but also degrades original rising-edge phases hidden in the modulated carrier due to zero-crossing point deviations. Therefore, to ensure the modulation linearity of CF-PWM mode, an envelope precorrection module with an inverse function of (1) is added to compensate for the envelope offset, and 1/4-period (90°-shifted point) positions rather than rising-edge (zero-crossing point) positions of the carrier clock are modulated to convey phase components without distortion as follows:

$$y = \begin{cases} \dfrac{2}{\pi}, & \text{IF-PWM } (d = 0.5), \\ \dfrac{2}{\pi} \sin(\pi \times d), & \text{CF-PWM.} \end{cases} \tag{1}$$

For CF-PWM mode, only CF clock is involved in signal modulations, whereas IF clock or aliasing is avoided and carrier harmonics are effectively eliminated by BPF. Under IF-PWM condition with less limitation or enough margin between f_C and signal bandwidth, although IF clock f_{IF} is introduced, the BPF could still suppress IF interferences by setting reasonable relations between f_C, f_{IF}, and BPF bandwidth B_{RF}, following (2)

$$\frac{f_C}{B_{RF}} \le 50, \qquad \frac{f_{IF}}{B_{RF}} \ge 2.5,$$
$$k + 1 > \frac{f_C}{f_{IF}} \ne k + 0.5 > k, \quad k = 10 \sim 19. \tag{2}$$

With 6th order BPF, IF spurs lower than −80 dB are ensured when f_{IF} is more than 5 times farther than the BPF corner and when the tenth-order or higher IF harmonics with less power locate around the carrier band. With normalized envelope values higher than 0.1, there is at least one whole carrier clock transmitted to convey baseband components during each IF period. In addition, the ratio f_C/f_{IF} should not be a multiple of 0.5 to avoid IF harmonics located at $2f_C$ down-converts with the carrier at f_C into the signal band. Here, $f_{IF} = f_C/15.4$.

3. Implementation

3.1. IF-PWM Mode. Figure 2 shows delay-line based IF-PWM mode for the proposed transmitter. Multibit phase components are mapped to the rising-edge positions of the carrier clock with a fixed duty cycle of 0.5 by employing an N-level quantizer and an N-stage delay line where the continuous phases of 0–360° are equidistantly quantized to N discrete values. Multibit envelope components are converted to the pulse widths of the IF clock, which are subsequently converted by AND operation to the pulse densities of the carrier clock with the fixed pulse width inversely proportional to f_C. Under enough margins and perfect values between f_C, f_{IF}, and B_{RF}, the BPF effectively suppresses the IF spurs or harmonics. Modulation

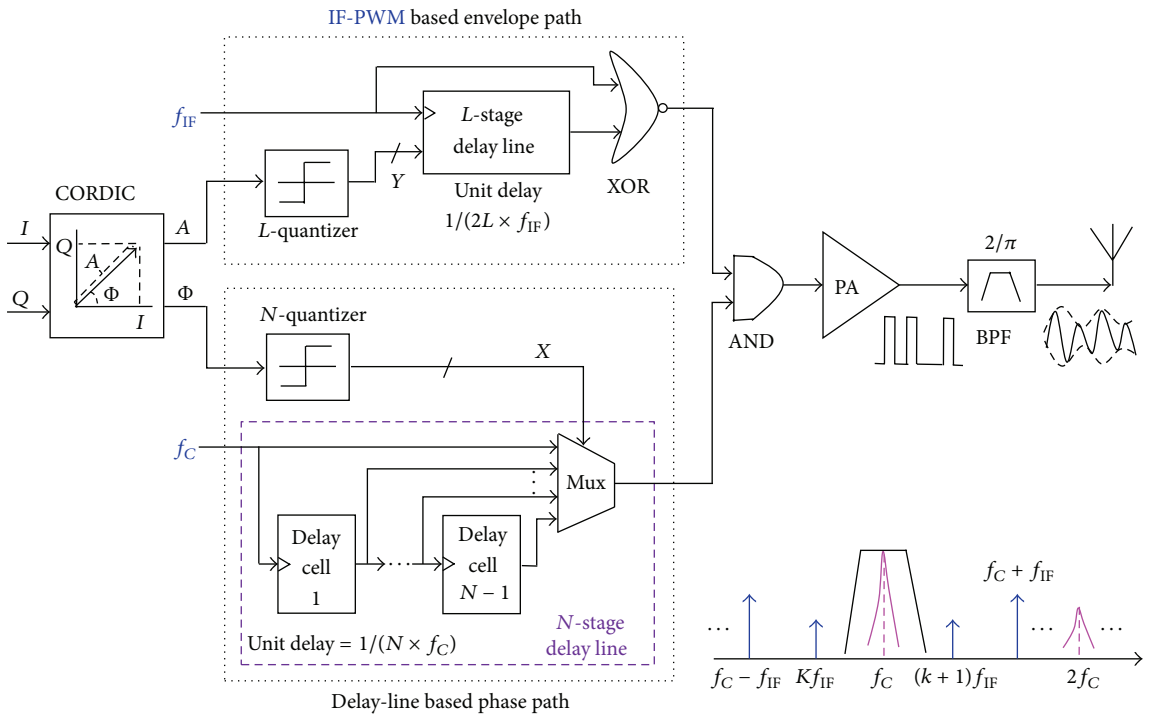


Figure 2: Delay-line based IF-PWM mode for proposed fully digital transmitter.

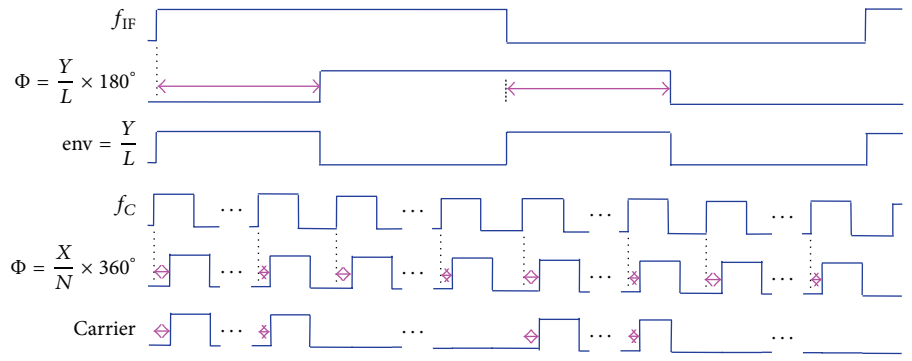


Figure 3: Function diagram of IF-PWM architecture.

linearity strongly depends on the quantization resolutions or levels.

The function diagram of the IF-PWM mode is shown in Figure 3. For a certain carrier frequency f_C, the N-stage delay line with a unit delay of $1/(N \times f_C)$ converts the quantized phase X to the rising-edge lag Φ of the carrier clock. The L-stage delay line with a unit delay of $1/(2L \times f_{IF})$ maps the quantized envelope Y into the rising-edge lag Φ of the IF clock. The pulse-width env generated by Φ shapes the pulse density of the carrier clock to represent the envelope component, and the rising-edge lag Φ of the carrier clock reflects the phase component, respectively.

Assuming baseband envelope $A(t)$, phase $\Phi(t)$, and envelope normalized value A_{std}, the modulated carrier clock $c(t)$ is shown in (3), where square() is the function of periodic square wave and ω_C is the carrier angular frequency. One has

$$c(t) = \frac{A(t)}{A_{std}} \times \text{square}\left[\omega_c t + \Phi(t)\right]. \tag{3}$$

After filtered smoothly by the sequent BPF, the modulated sinusoidal carrier $y(t)$ is shown in (4). Continuous baseband envelope A and phase Φ are transmitted:

$$\begin{aligned} y(t) &= \frac{A(t)}{A_{std}} \times \frac{2}{\pi} \times \sin\left[\omega_c t + \Phi(t)\right] \\ &= \frac{2}{\pi \times A_{std}} \left[A(t) \times \sin\left(\omega_c t + \Phi(t)\right)\right]. \end{aligned} \tag{4}$$

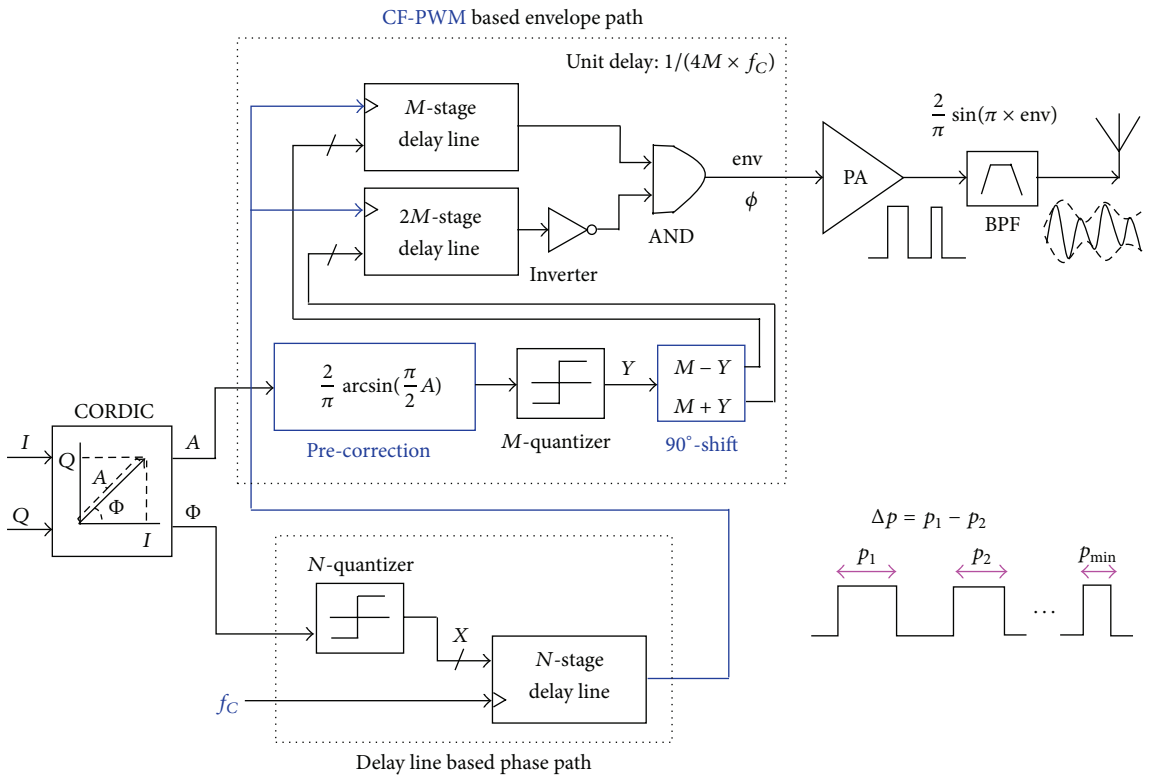


Figure 4: Proposed delay-line based CF-PWM mode for fully digital transmitter.

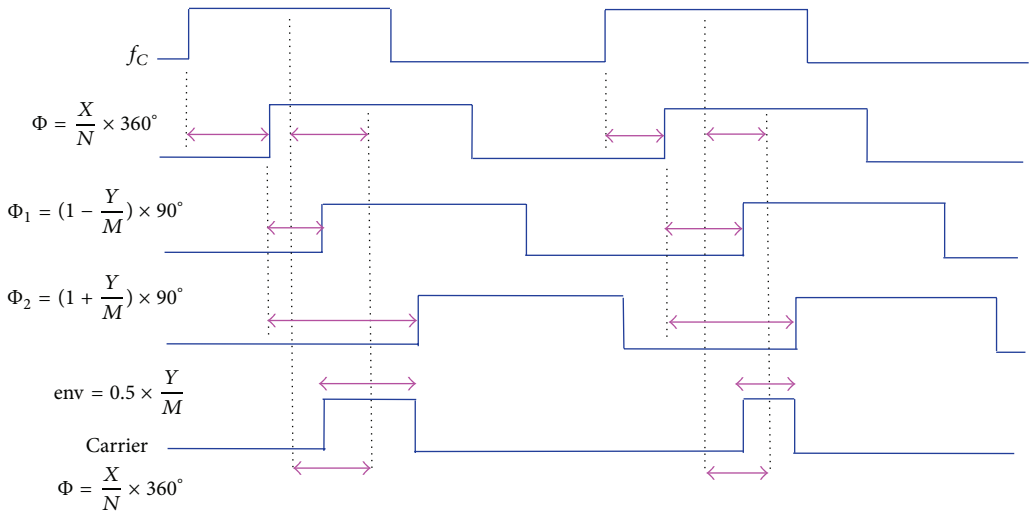


Figure 5: Function diagram of proposed CF-PWM architecture.

3.2. Proposed CF-PWM Mode. Figure 4 shows the proposed delay-line based CF-PWM mode for fully digital transmitter. Multibit phase components are mapped to the rising-edge positions of the carrier clock with a fixed duty cycle of 0.5 by employing an N-level quantizer and an N-stage delay line. Multibit envelope components are converted to the pulse widths of the position-modulated carrier clock through the delay differences between the M- and $2M$-stage delay lines and subsequent logic operations. Unlike IF-PWM mode, it is pulse widths rather than densities of the carrier clock that represent baseband envelopes. For ensuring the modulation linearity, both envelope precorrection module with antitrigonometric function and 90° phase-shifted operation are added to compensate for the distortions caused by the BPF with variable pulse-width inputs, as discussed above.

The function diagram of the proposed CF-PWM architecture is shown in Figure 5. For a certain carrier clock, the N-stage delay line with a unit delay of $1/(N \times f_C)$ converts

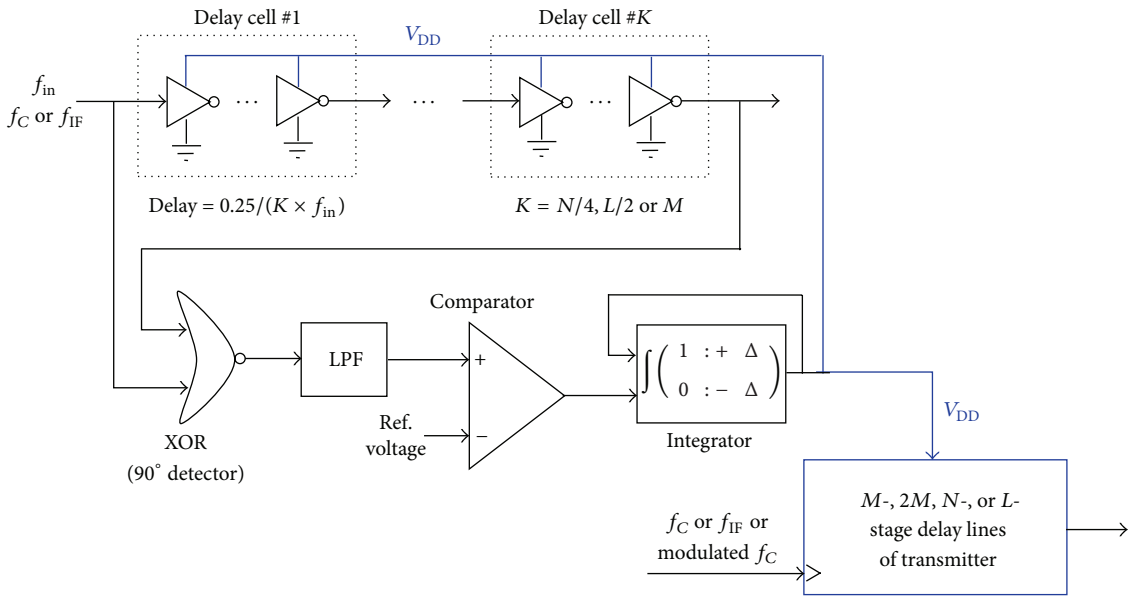


Figure 6: Proposed unit-delay autocalibration loop with reconfigurable f_C.

the quantized phase X to the rising-edge lag of the carrier clock. The M- and $2M$-stage delay lines with a unit delay of $1/(4M \times f_C)$ subsequently map the precorrected quantization envelope Y into two different rising-edge lags Φ_1 and Φ_2 on the symmetry of 90° phase-shifted points. The pulse-width env generated by $\Phi_{1\text{-}2}$ represents the precorrected envelope component, and the lag Φ of the 90° phase-shifted points reflects the phase component, respectively. That is, both pulse-widths and 1/4-period positions of the carrier clock convey baseband signals. Similarly, quantization resolutions or levels determine linearity. The modulated carrier clock $c(t)$ is shown in the following equation:

$$\begin{aligned} c(t) &= 0.5 \times \frac{Y}{M} \times \text{square}\left[\omega_c t - 90^\circ + \Phi(t)\right] \\ &= 0.5 \times \left[\frac{2}{\pi} \arcsin\left(\frac{\pi}{2} \times \frac{A(t)}{A_{\text{std}}}\right)\right] \\ &\quad \times \text{square}\left[\omega_c t - 90^\circ + \Phi(t)\right]. \end{aligned} \tag{5}$$

The modulated sinusoidal carrier $y(t)$ is shown in (6). Continuous baseband envelope A and phase Φ are transmitted. Consider

$$\begin{aligned} y(t) &= \frac{2}{\pi} \times \sin\left[\pi \times \left(0.5 \times \left[\frac{2}{\pi} \arcsin\left(\frac{\pi}{2} \times \frac{A(t)}{A_{\text{std}}}\right)\right]\right)\right] \\ &\quad \times \sin\left(\omega_c t - 90^\circ + \Phi(t)\right) \\ &= \frac{1}{A_{\text{std}}}\left[A(t) \times \sin\left(\omega_c t - 90^\circ + \Phi(t)\right)\right]. \end{aligned} \tag{6}$$

The minimum pulse width p_{min} of the modulated carrier clock, shown in (7), is determined by the maximum CF $f_{C,\text{max}}$ and the minimum normalized envelope $A_{\text{std,min}}$. The pulse width resolution Δp, shown in (8), depends on f_C and envelope quantization level M and needs to be recognized by the sequent PA. Clearly, the ability of the PA conducting narrow pulses is a critical parameter for the proposed implementation. With finite signal rise and fall time, ultra narrow pulses going through the class-D PA are prone to be trapezoidal or triangular rather than being square, considering the limited working frequency or conducting capability of the present PA. That is why the proposed CF-PWM architecture only aims for low CF range of 2 M–100 MHz. Consider the following equations:

$$p_{\text{min}} = \frac{0.5}{f_{C,\text{max}}} A_{\text{std,min}}, \tag{7}$$

$$\Delta p = \frac{0.5}{M \times f_C}. \tag{8}$$

3.3. Unit-Delay Autocalibration. To ensure modulation performances, the unit delay of delay lines needs to be accurate. To meet wide f_C range, the unit delay also needs to be reconfigurable. In addition to D flip-flops apt for large unit delay, in most cases the unit delay is small and is implemented by inverters without or with resistive interpolation [5, 11]. However, inverters require accurate delay calibration for high robustness over process and temperature variations. Figure 6 shows the proposed unit-delay calibration loop with wide and reconfigurable f_C.

The phase difference between the periodic clock input and 90°-shifted clock corresponding to K unit delays is measured and converted to an error voltage by an XOR gate followed by a low-pass filter (LPF) and a sequent comparator. The error voltage sent to an integrator with driver buffer is accumulated and fed to the power supply V_{DD} of delay cells, which inversely modifies the unit delay. Under the negative feedback operation with closed-loop V_{DD} calibration, for

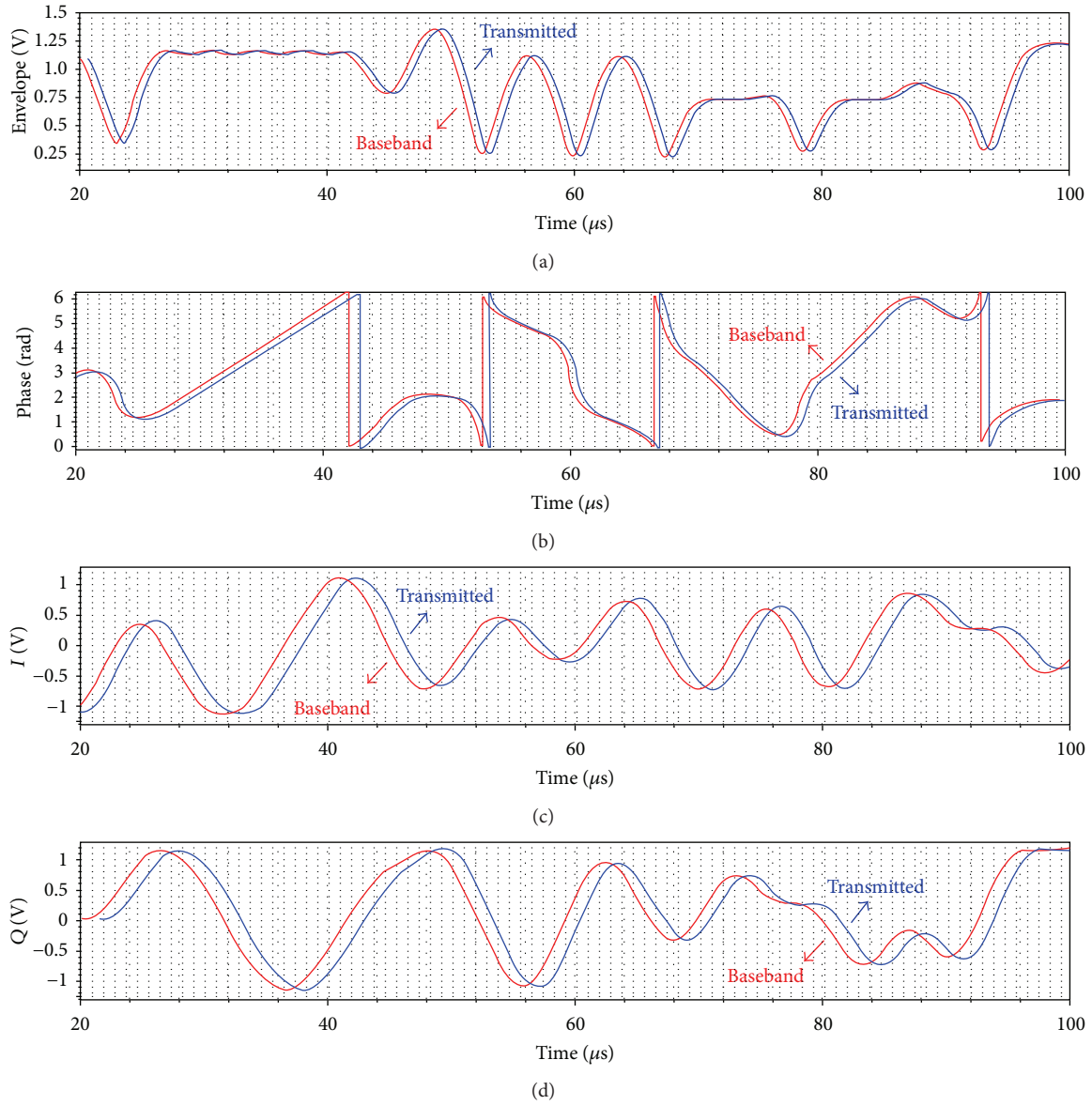


FIGURE 7: Simulated transmitter components conveyed by proposed architecture with comparison to baseband ones.

a certain clock f_{in} (f_C or f_{IF}), the unit delays of open-loop delay lines are accurately achieved by strict match designs and conform to (9), respectively, for different delay lines of the phase path and IF- and CF-PWMs. By setting matched inverter number in each delay cell and perfect V_{DD} range of delay cells, reconfigurable f_C and corresponding unit delays are accomplished as follows:

$$\tau = \frac{0.25}{K \times f_{in}} = \begin{cases} \dfrac{1}{N \times f_C}, & \text{Phase-Path } \left(K = \dfrac{N}{4}, f_{in} = f_C\right), \\ \dfrac{1}{2L \times f_{IF}}, & \text{IF-PWM } \left(K = \dfrac{L}{2}, f_{in} = f_{IF}\right), \\ \dfrac{1}{4M \times f_C}, & \text{CF-PWM } \left(K = M, f_{in} = f_C\right). \end{cases} \quad (9)$$

4. Experimental Results

The proposed fully digital transmitter is designed in 180 nm CMOS with external class-D PA and BPF. Excluding the PA, the proposed implementation only dissipates ultra low power of 100 μW from 1.8 V power supply. The transmitter achieves a power efficiency of 70%, according to circuit-level simulations. The quantization levels are 256 and 128 for the phase and envelope paths, respectively.

The supply voltage of delay cells can be changed from 1.4 to 2.2 V, which corresponds to the minimum unit delays of 7.8–3.9 ps for the phase path, 120.3–60.1 ps for the IF-PWM, and 39.0–19.5 ps for the CF-PWM, according to circuit-level simulations of three groups of different delay lines in the nominal case. As a result, the CF ranges of 50–100 MHz for the CF-PWM mode and 0.5–1 GHz for the IF-PWM one are

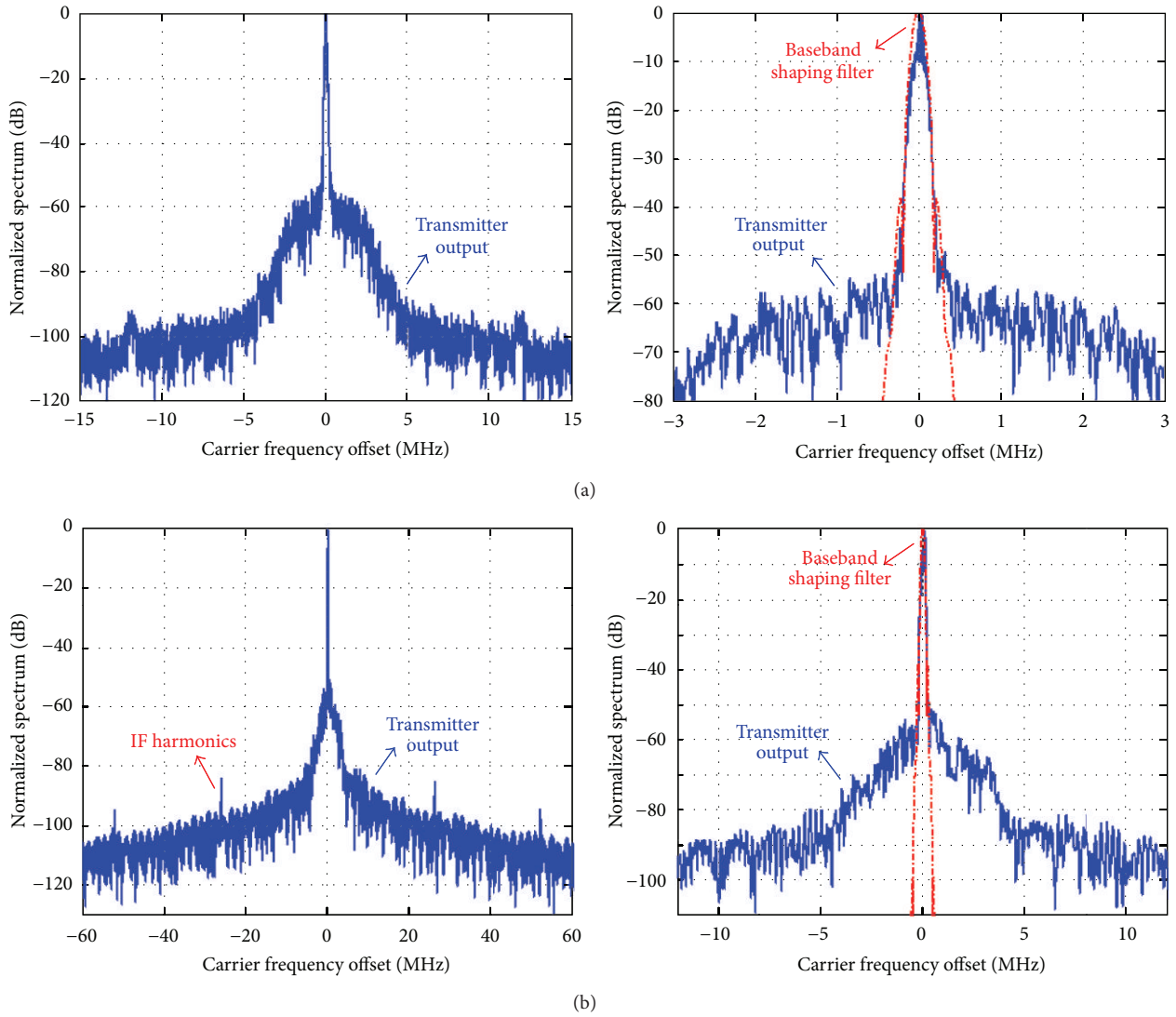


FIGURE 8: Simulated transmitter normalized far and near spectrums: (a) CF-PWM centered at 50 MHz; and (b) IF-PWM centered at 200 MHz.

gotten. By adding matched inverters in each group of delay cells, the lower CF range is also covered and the wide CF range of 2 M–1 GHz is achieved. For a certain baseband signal with normalized envelope range of 0.15–1.0, with f_C less than 100 MHz, the $p_{\min}$ and Δp of the CF-PWM mode are 0.75 ns and 0.04 ns, respectively, which could be recognized by the present PA.

Figure 7 shows the simulated transmitter components conveyed by the proposed architecture with comparison to the baseband ones for 8PSK signal with an envelope range of 0.22~1.45 V. The proposed transmitter conveys the baseband components very well with the simulated error vector magnitude (EVM) of 3%. Little distortions result from limited quantization resolutions and slight PA push-pull asymmetry. An ideal receiver reconstructing the transmitted components is implemented in Matlab.

Figure 8 shows the simulated transmitter normalized far and near spectrums centered at 50 MHz for CF-PWM mode and at 200 MHz for IF-PWM one. The roll-off feature of spectrum side lobes is determined by the baseband shaping filter. The noise floor less than 60 dB is observed below the carrier, and 20 dB spectrum optimization is achieved when compared to the existing designs [4, 5] with the noise floor at 40 dB below the carrier. For CF-PWM mode, no any other frequency components including spurs and harmonics exist, except for the carrier. For IF-PWM mode, IF spurs located at even multiples of f_{IF} from f_C are observed and less than −80 dB. Hence, the proposed transmitter achieves high spectrum purity.

5. Conclusions

By combining delay-line based IF-PWM for high f_C band and proposed CF-PWM with precorrection for low f_C band, a fully digital transmitter is implemented in 180 nm CMOS, with wide CF range of 2 M–1 GHz and high power efficiency of 70%. A unit-delay autocalibration circuit with closed-loop

detection and open-loop adjustment is presented to support f_C reconfiguration. The experimental results show that the proposed architecture transmits baseband components well with high spectrum purity and low EVM of 3%. Compared to the existing designs, 20 dB spectrum optimization is achieved. Chip prototype will be considered as a future work to further verify the proposed transmitter architecture.

Acknowledgments

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