

Research Article

50 MHz–10 GHz Low-Power Resistive Feedback Current-Reuse Mixer with Inductive Peaking for Cognitive Radio Receiver

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A low-power wideband mixer is designed and implemented in 0.13 μm standard CMOS technology based on resistive feedback current-reuse (RFCR) configuration for the application of cognitive radio receiver. The proposed RFCR architecture incorporates an inductive peaking technique to compensate for gain roll-off at high frequency while enhancing the bandwidth. A complementary current-reuse technique is used between transconductance and IF stages to boost the conversion gain without additional power consumption by reusing the DC bias current of the LO stage. This downconversion double-balanced mixer exhibits a high and flat conversion gain (CG) of 14.9 ± 1.4 dB and a noise figure (NF) better than 12.8 dB. The maximum input 1-dB compression point (P1dB) and maximum input third-order intercept point (IIP3) are -13.6 dBm and -4.5 dBm, respectively, over the desired frequency ranging from 50 MHz to 10 GHz. The proposed circuit operates down to a supply headroom of 1 V with a low-power consumption of 3.5 mW.

1. Introduction

As the number of new wireless applications advents tremendously, the demand for additional frequency spectrum allocation has been growing rapidly. However, the former practice of fixed spectrum allocation policy suffers from the low spectrum utilization setback and this sets a limitation in the available spectrum of accommodating the next generation wireless applications and services [1]. The inefficiency in spectrum usage and the shortage in spectrum have motivated the evolution of CRs. CR was deemed to be an innovative approach due to its versatility in the context of sensing local spectrum reliably and utilizing unoccupied frequency spectrum in the targeted spectral range, while abstaining interference for licensed user by favourably altering its receiving and transmitting parameters [2]. The first international regulation which establishes CRs based system is IEEE 802.22, where the access of unlicensed CR devices on (TV) frequency spectrum (54 MHz–862 MHz) is permitted [3].

Due to excessive demand and technology advancement, the CRs have a greater potential to be expanded further from the constraint of TV band [4].

In the realization of CRs function, a wideband receiver is required to encapsulate the entire aspired frequency band instead of the conventional practice where multiple receivers are envisioned to cover different frequency bands. This highlights the importance of wideband mixer in RF front-end receiver circuit to perform frequency translation. This paper focuses on the design of low-power wideband mixer with a flat and high CG frequency response, along with a flat and low NF frequency response and an adequate linearity over a wide frequency range for CR receiver application. On the platform of CMOS technology, several state-of-the-art architectures for wideband mixer have been reported [5–15]. The double-balanced Gilbert cell mixer has been the mainstay of development in wideband mixer due to its inherent characteristics of high CG and high port-to-port isolation [16, 17]. However, a high CG is inherited at the penalty of

high bias current which concurrently contributes towards the flicker noise problem and voltage headroom limitation. In the advantage of minimizing the load resistance in addressing the limitation of voltage headroom, the CG of the mixer is adversely affected. In [18], current-bleeding technique is used to mitigate the output voltage headroom problem by steering the DC current flow through the load resistance. However, this approach is not a preferred solution as the total power consumption remains the same as in conventional Gilbert cell architecture. In addition, the parasitic capacitance introduced by the bleeding transistors not only limits the operating bandwidth, but also degrades the CG by channelling a signal leakage path to the substrate ground.

The well-defined folded-cascode mixer is envisaged to surmount the drawbacks that exist in the Gilbert cell mixer. Instead of stacking the switching stage above the transconductance stage, the folded-switching stage is a promising solution to overcome the voltage headroom limitation. The folded-cascode mixer presented in [19] exhibits a narrow band response and it is not suitable for CR application. Hence, a wideband matching network is integrated at the input mixer to achieve a wideband operating frequency [15]. The mixer input matching circuit not only is crucial as an interstage matching in cascaded systems, but also is essential to ensure the wide bandwidth performance by providing a low input reflection loss across the frequency range.

The RFCR mixer [7, 20] with folded-cascode structure is widely adapted in recent reported work due to the inherent wideband input matching characteristic with low NF and high gain. Although the RFCR architecture had shown good inherent performance but there is severe contradiction in improving wideband input matching and noise due to the large gate-source parasitic capacitance of the input stage transistors. Therefore, a π -match LC network is introduced in [21] to enhance the input matching by creating an extra zero while reducing gate noise by series resonance of L_g - C_{in} at high frequencies. The reported low-voltage, low-power RFCR mixer architecture in [7] achieves a high CG over wide range of frequency bandwidth in 65 nm CMOS technology. As the DC current-reuse is not feasible in a folded architecture, the cost of this implementation would be in increased power consumption relative to the technology of implementation.

The effect of even-order distortion in CRs is more critical than narrow band receivers [4]. This distortion is heavily attributed to the presence of asymmetric mismatch in the downconversion mixer and it causes disturbance to the desired channel. To alleviate this distortion effect, a balanced circuit with differential architecture and symmetrical physical layout is preferred. In this work, a low-voltage, low-power and double-balanced wideband mixer integrates a π -match LC network at the input mixer to meet wideband input matching performance. The complementary current-reuse topology [22] improves the power consumption of mixer while enhancing the RF input transconductance. In addition, an inductive peaking is also employed to improve the mixer noise and conversion gain flatness. The proposed mixer is extracted, simulated, and verified on 0.13 μm standard CMOS platform. This paper is organized as follows. Section 2 reviews

and highlights the design limitations and performance trade-offs in conventional RFCR mixer. In Section 3, the circuit topology and operation principles of the proposed mixer are presented. An insight into RFCR mixer operation is given by analyzing the innovative techniques that are adapted to overcome the limitations in confirming the stringent requirements for CR application. Section 4 reports the RC-extracted postlayout simulation results and Section 5 presents the conclusion.

2. Design Challenges

Several publications were reported on RFCR architecture [7, 20, 23] which can be amenable to both narrow and wideband applications. The RFCR architecture is more viable design for wideband system due to its inherent wideband input matching, low-power consumption, and high gain characteristics. In typical wide bandwidth application, a flat frequency response of gain and NF is preferred across the operating frequency. However, the conventional RFCR architecture tends to suffer from poor NF performance although the CG can be flattened across the range of wide bandwidth due to intrinsic conflict between flat gain and flat NF [21, 24, 25]. Therefore, the conventional RFCR architecture is reviewed in order to analyse the performance parameter trade-offs, which limit the extension of the operational bandwidth. The architecture of Figure 1(a) illustrates the common single-balanced RFCR mixer with the simplified equivalent small signal representation of the transconductance stage given in Figure 1(b). Transistor $M_{1,2}$ represents the RF input transistor; transistor $M_{3,4}$ is LO switching pair; capacitor C_{ac} is the DC-decoupling capacitor; capacitor C_p is the emulation of the parasitic capacitance at node V_y while resistors R_s , R_{fb} , and $R_{L(1,2)}$ represent the input source resistance, feedback resistor, and load resistor, respectively.

At low frequency, the frequency-dependent component is negligible. From Figure 1(b), the input impedance, Z_{in} can be defined as follows:

$$Z_{in} \approx \frac{R_{fb} + r_o}{1 + |A_{vo}|}, \quad (1)$$

where A_{vo} is the open-loop gain, computed as $g_m r_o$, in which g_m is the RF input transconductance represented as $g_{m1} + g_{m2}$ and r_o is $r_{o1} \parallel r_{o2}$. Equation (1) reveals that input impedance of the RFCR circuit is mainly determined by resistor R_{fb} and transconductance g_m . In order to achieve an input reflection coefficient, $|\Gamma| \leq -10$ dB, with respect to a source impedance of $R_s = 50 \Omega$, yields Z_{in} in a range of 25 Ω to 100 Ω [7, 21].

The voltage gain and noise factor of the transconductance stage can be derived as

$$A_v = \frac{r_o (1 - g_m R_{fb})}{R_{fb} + r_o}, \quad (2)$$

$$F \approx 1 + \frac{R_{fb}}{R_s} \left(\frac{1 + g_m R_s}{1 - g_m R_{fb}} \right)^2 + \frac{\gamma g_m}{\alpha R_s} \left(\frac{R_{fb} + R_s}{1 - g_m R_{fb}} \right)^2, \quad (3)$$

where α is the ratio between the device transconductance and the zero-bias drain conductance, while γ is the channel

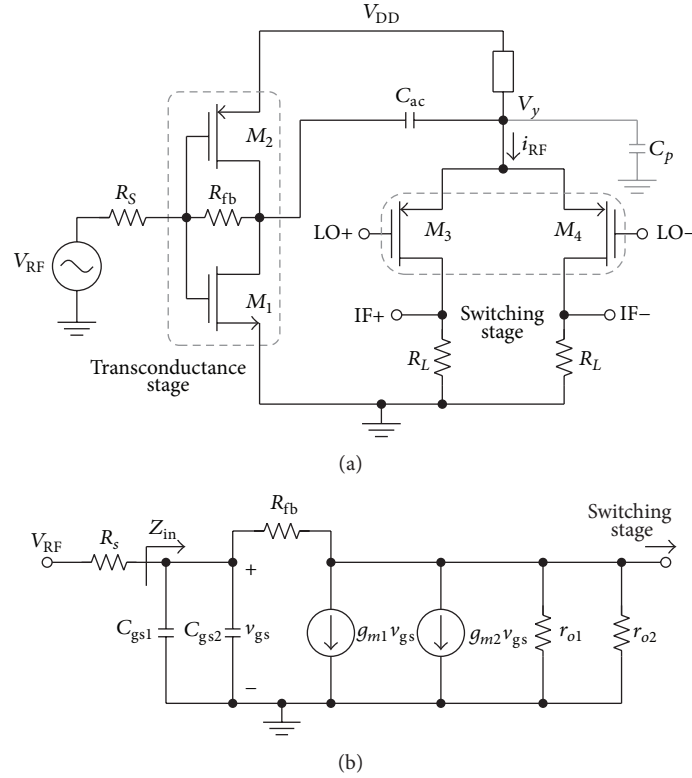


FIGURE 1: (a) Simplified single-balanced RFCR mixer and (b) small signal equivalent circuit of RFCR transconductance stage.

thermal noise coefficient. From (1) and (3), it can be observed that there is a close relationship between input impedance matching and NF. The NF can be significantly improved by increasing the RF input transconductance and the value of resistor R_{fb} at the expense of the input impedance matching performance.

However in practical circuit implementation, the parasitic capacitances introduced by the gate of input transistors further exacerbate the input matching especially at high frequencies. The frequency dependent component is taken into account to finalize the limitation of wideband operating bandwidth; thus (1) can be rewritten as follows:

$$Z_{in}(s) = \frac{R_{fb} + r_o}{1 + g_m r_o} \left(\frac{1}{1 + s(C_{gs}(R_{fb} + r_o)/(1 + g_m r_o))} \right), \quad (4)$$

where $C_{gs} = C_{gs1} + C_{gs2}$. From (4), as $Z_{in} = R_s = 50 \Omega$ for the perfect matching condition, the maximum gate-source parasitic capacitance can be expressed as follows:

$$C_{gs,max} = \frac{1}{\pi R_s f} \sqrt{\frac{|\Gamma|^2}{|\Gamma|^2 - 1}}, \quad (5)$$

where R_s represents the input port impedance and f is the cut-off frequency. Based on (5), at the targeted input matching of -10 dB with an upper corner frequency of 10 GHz respective to a source impedance of $R_s = 50 \Omega$, the maximum capacitance $C_{gs,max}$ which is contributed from both NMOS

and PMOS input transistors equals 200 fF. Evidently, a comparative small parasitic capacitance reflects to a small aspect ratio of RF input transistors which concurrently creates limitation in boosting the RF input transconductance and achieving low noise performance.

In addition to this trade-off, the investigation of noise contribution from switching stage reveals more setbacks which further degrade the mixer's performance. The total output noise of a mixer consists of thermal noise and flicker noise. The thermal noise which is mainly dominated by the transconductance stage can be easily reduced by increasing the bias current. The switches in an active mixer predominately contribute towards the growth of flicker noise at the mixer's output. The flicker noise articulated by the LO switches exists at the output of the mixer via direct and indirect mechanism [26]. The flicker noise in effect through the direct mechanism is due to random modulation of the duty cycle of the output current, whereas through the indirect mechanism it is caused by charging and discharging of the parasitic capacitances between transconductance and LO stages. The output noise current generated by the direct mechanism and indirect mechanism is given as in the following [26, 27]:

$$i_{o,n(direct)} = \frac{4I_{tail,sw}V_n}{ST}, \quad (6)$$

$$i_{o,n(indirect)} = \frac{2C_p}{T} V_n \frac{(C_p \omega_{LO})^2}{(g_{m,sw})^2 + (C_p \omega_{LO})^2}, \quad (7)$$

where $I_{\text{tail,sw}}$ is the DC tail current in switching stage, V_n is the equivalent flicker noise of the switching pair, S is the slope of LO signal, T is the LO period, C_p is the parasitic capacitance at switching tail, ω_{LO} is the frequency of LO signal, and $g_{m,\text{sw}}$ is the transconductance of switching transistor. In reference to (6) and (7), the direct and indirect noise currents are evidently proportional to the flicker noise voltage, V_n of LO transistor which is expressed as in the following:

$$V_n = \sqrt{\frac{2K_f}{W_{\text{eff}}L_{\text{eff}}C_{\text{ox}}f}}, \quad (8)$$

where K_f is the technology parameter, W_{eff} and L_{eff} are the effective width and length of LO transistor, respectively, C_{ox} is the oxide capacitance of LO transistor, and f is the operating frequency. Apparently, in order to minimize the flicker noise effect caused by the direct mechanism, low DC current at the switching stage and large size of LO transistor are preferred. On the contrary, the larger size of LO switching transistor yields to a larger parasitic capacitance, C_p at node V_y as referred to in Figure 1(a). This results in an increase of noise current from indirect mechanism as can be observed from (7). In addition, the capacitance C_p also creates detrimental effect at high frequency by introducing a low impedance path for RF signal which shunts the RF signal to the ground, thus reducing the CG and adversely limiting the operational bandwidth. This effect can be mathematically proven by deriving the pole frequency of the effective transconductance of the mixer in Figure 1(a) as in the following:

$$\frac{i_{\text{RF}}(s_{\text{RF}})}{v_{\text{gs}}(s_{\text{RF}})} = \frac{1 - g_m R_{\text{fb}}}{R_{\text{fb}} + R_{\text{eq}}} \left(\frac{1}{s_{\text{RF}} C_p (R_{\text{eq}} \parallel R_{\text{fb}}) + 1} \right), \quad (9)$$

where R_{eq} is total resistance at the node V_y . Hence, the pole frequency of the mixer which plays a crucial role in determining the operating bandwidth of the mixer core can be derived as

$$\omega_{\text{RF}} = \frac{1}{C_p (R_{\text{eq}} \parallel R_{\text{fb}})}. \quad (10)$$

It is noted that the capacitor C_p forms as a low-pass filter at the tail of switching quad, where the gain response rolls off beyond the cut-off frequency. Therefore, it can be concluded that obtaining a large operation bandwidth with relatively large capacitor C_p at node V_y is not feasible. This has driven the need for the exploration of new design technique to achieve large bandwidth performance.

3. Proposed Mixer

The proposed RFCR mixer illustrated in Figure 2 consists of RF input transistors $M_{1,2}$, current-reuse PMOS bias transistors $M_{3,4}$, feedback resistor $R_{\text{fb}(1,2)}$, DC-decoupling capacitor $C_{\text{ac}(1,2)}$, switching transistors M_7 – M_{10} , peaking inductor $L_{p(1,2)}$, and passive load of $R_{L(1,2)}$ and $C_{L(1,2)}$. The folded architecture is preferred over the conventional series stacking topology due to its merit in low voltage headroom

realization. The minimum voltage headroom that can be applied to the designed circuit is approximated as

$$V_{\text{DD,min}} = V_{\text{ds1,2(sat)}} + V_{\text{ds3,4(sat)}} + V_{\text{th},n} + V_{\text{th},p}, \quad (11)$$

where $V_{\text{ds1,2(sat)}}$ and $V_{\text{ds3,4(sat)}}$ are the overdrive voltage of transistors $M_{1,2}$ and $M_{3,4}$, respectively, while $V_{\text{th},n}$ and $V_{\text{th},p}$ are the respective threshold voltage of the transistors $M_{1,2}$ and $M_{3,4}$.

The transconductance stage is realized through the integration of inverter with feedback resistor, $R_{\text{fb}(1,2)}$. At the transconductance stage, PMOS transistor $M_{3,4}$ is stacked at the top of NMOS transistor $M_{1,2}$ to form a current-reuse topology. Therefore, the transistor $M_{3,4}$ enhances the RF input transconductance $g_{m,\text{RF}}$ to $g_{m(1,2)} + g_{m(3,4)}$ without additional power consumption compared to a single N-type common source amplifier associated with an RF input transconductance, $g_{m,\text{RF}} = g_{m(1,2)}$. In addition, the PMOS transistor $M_{3,4}$ also provides high intrinsic output impedance to prevent RF signal leakage to the power supply. The resistor $R_{\text{fb}(1,2)}$ is used not only to meet the aspired input impedance matching criterion, but also to reduce the power consumption in line to the elimination of additional biasing circuitry for transistors M_1 – M_4 in the context of self-biased principle. By adapting the complementary current-reuse technique, the DC current from the switching stage is fed into transistor $M_{1,2}$ instead of being routed into silicon ground as in a typical folded topology apparently in a quest to boost the gain without additional power consumption. As a result, the NMOS transistor $M_{1,2}$ contributes more transconductance than PMOS transistor $M_{3,4}$ due to an increased current flow through the transistor $M_{1,2}$; thus the aspect ratio of transistors $M_{1,2}$ and $M_{3,4}$ along with feedback resistor $R_{\text{fb}(1,2)}$ is optimized diligently according to (1) and (3).

As mentioned before, a large aspect ratio of RF input transistors contributes to a respective large gate-source parasitic capacitance at the input stage of the conventional RFCR topology and thus adversely affects the input matching and concurrently reduces the operating bandwidth. Hence, an inductor $L_{g(1,2)}$ is placed in series with the gate of the transconductance stage transistors while the input capacitor $C_{\text{in}(1,2)}$ is placed in parallel to the transconductance stage to extend the input bandwidth of the frequency response in achieving a good matching over the operating frequency range. The capacitor $C_{\text{in}(1,2)}$ and inductor $L_{g(1,2)}$ integrated with the total gate-source capacitance, C_{gst} of input transistors, form a third-order LC ladder low-pass filter. In this approach, the inductor $L_{g(1,2)}$ coupled with the capacitor $C_{\text{in}(1,2)}$ to eliminate the effect of C_{gst} and to resonate out the reactive component of Z_{in} at the desired frequency. Through this technique, the constraints of gate-source parasitic capacitance as described in (5) are relaxed. In preference the transconductance can be increased to achieve higher gain and low noise performance simultaneously by increasing the size of RF input transistor while retaining the operating bandwidth as there is an additional degree of freedom in increasing C_{gst} .

Figure 3 depicts the corresponding half circuit small signal representation of the proposed wideband mixer which

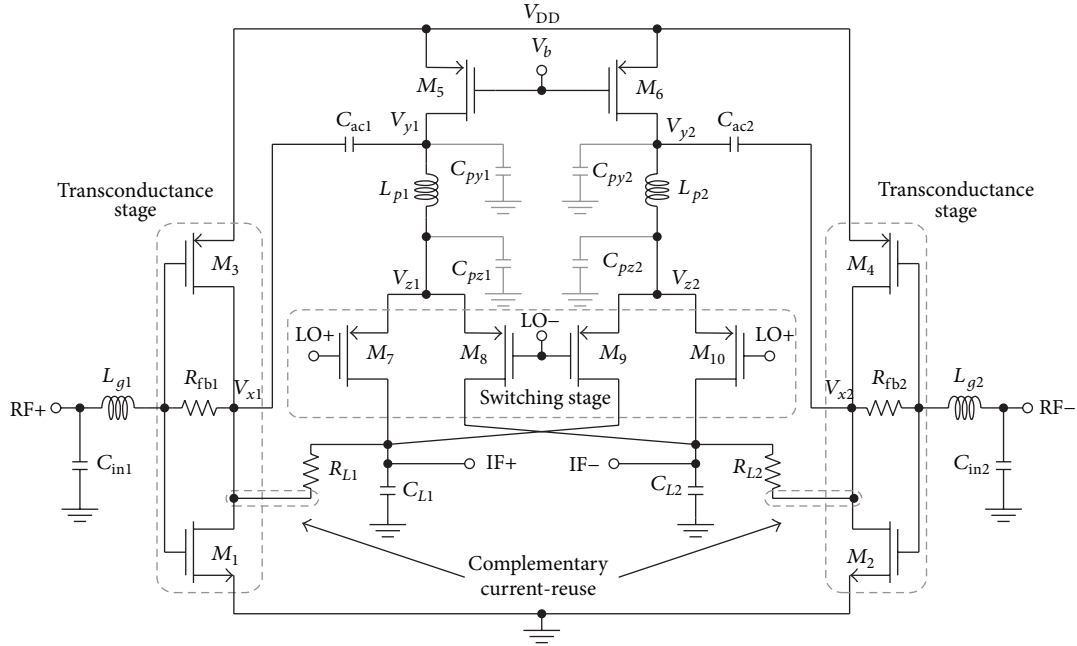


FIGURE 2: Proposed wideband mixer.

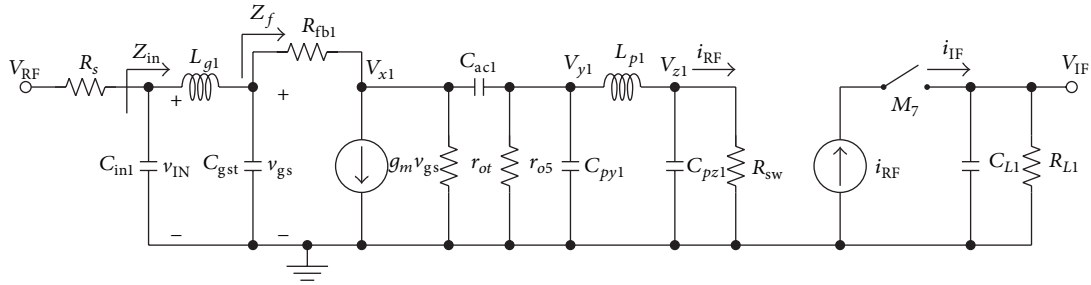


FIGURE 3: Half circuit small signal representation of the proposed wideband mixer.

is illustrated in Figure 2. The capacitors $C_{py(1,2)}$ and $C_{pz(1,2)}$ represent the parasitic capacitances at nodes $V_{y(1,2)}$ and $V_{z(1,2)}$, respectively. To simplify the analysis, the DC blocking capacitor $C_{ac(1,2)}$ between the transconductance and switching stage is neglected since the impedance in effect of $C_{ac(1,2)}$ is relatively small at the operating frequency range. The input impedance Z_{in} and the input return loss S_{11} of the proposed architecture can be derived and expressed as in (12) and (13), respectively,

$$Z_{in} = \frac{s^2 C_{gst} L_{g1} Z_f + s L_{g1} + Z_f}{s^3 C_{gst} C_{in1} L_{g1} Z_f + s^2 C_{in1} L_{g1} + s Z_f (C_{gst} + C_{in1}) + 1}, \quad (12)$$

$$|S_{11}| = \left| \frac{-s^3 C_{gst} C_{in1} L_{g1} Z_f R_s + s^2 C_{gst} L_{g1} Z_f - s^2 C_{in1} L_{g1} R_s + s L_{g1} - s Z_f R_s (C_{gst} + C_{in1}) + Z_f - R_s}{s^3 C_{gst} C_{in1} L_{g1} Z_f R_s + s^2 C_{gst} L_{g1} Z_f + s^2 C_{in1} L_{g1} R_s + s L_{g1} + s Z_f R_s (C_{gst} + C_{in1}) + Z_f + R_s} \right|, \quad (13)$$

where $C_{gst} = C_{gs1} + C_{gs3}$ is total gate-source capacitance of the input transistors and Z_f denotes the impedance looking into the resistor R_{fb1} . Assume that the π -match LC network is symmetrical for perfect input impedance matching by equating the capacitor $C_{in(1,2)}$ to capacitor C_{gst} and $Z_{in} = Z_f$ which is typically 50Ω . From (12), a good input matching for this circuit is obtained at frequencies

$$\begin{aligned} \omega_{o1} &= 0, \\ \omega_{o2} &= \sqrt{\frac{2}{C_{gst} L_{g1}} - \frac{1}{C_{gst}^2 Z_f^2}}. \end{aligned} \quad (14)$$

As can be seen from (14), the two frequencies, ω_{o1} and ω_{o2} , are adjusted to be located at DC and high frequency, respectively.

The frequency ω_{o2} is optimized to be in the vicinity of frequency ω_{o1} in order to maintain an input reflection of S_{11} below -10 dB across the entire operating frequency confirming a good input matching response inherited. At node $V_{x(1,2)}$ of Figure 2, the resistive load, $R_{L(1,2)}$, is designed to be relatively large compared to the impedance looking into the switching transistors; thus the RF signal is driven to subsequent stage through the AC coupling capacitor, $C_{ac(1,2)}$. In the worst case scenario, a small amount of RF signal leakage through the load resistor $R_{L(1,2)}$ can still be shorted out to ground through the load capacitor $C_{L(1,2)}$ instead of being routed to the IF output. Since the impedance looking into transistor $M_{5,6}$ at node $V_{y(1,2)}$ is also large, the RF signal is forced to enter the switching quad.

A PMOS based local oscillator (LO) switching stage is adopted in place of conventional NMOS transistor as PMOS transistor inherits an intrinsic characteristic of low flicker noise performance and less LO power sensitivity compared to NMOS transistor [23]. In reference to (6), large switching transistors with low LO current are applied to minimize the flicker noise in the direct mechanism. In contrast, a large switching transistor indirectly translates flicker noise to the mixer output due to the presence of large tail capacitance at the switches as described in the previous section. The inherited parasitic capacitance also limits the bandwidth, hence promoting the exploration of inductive peaking technique as illustrated in Figure 2.

The inductor $L_{p(1,2)}$ is placed at the tail of the switches to enhance the bandwidth through a peaking at high frequency without consuming additional power and voltage headroom. The aspect ratio of transistors $M_{5,6}$ and switching transistors are selected appropriately to form two suitable parasitic capacitors $C_{py(1,2)}$ and $C_{pz(1,2)}$ at nodes $V_{y(1,2)}$ and $V_{z(1,2)}$, respectively. These capacitors form a virtual π -network along with inductor $L_{p(1,2)}$, relaxing the requirement of integrating additional capacitors which degrade the CG and NF. From the perspective of transient analysis, the current charges the two capacitors $C_{p(y,z)}$ separately through the inductor $L_{p(1,2)}$, at different point of time, resulting in the charging time to be reduced leading to an enhancement in bandwidth. In further analyzing the operation of the peaking inductor $L_{p(1,2)}$, in reference to the frequency response, the LO transistor is modelled as an ON-OFF switch [28] while the resistor R_{sw} represents the resistance at the source terminal of switching transistor as illustrated in Figure 3. Based on this approximated model, the overall conversion gain of the mixer is computed by the following expression:

$$A_v = \frac{v_{IF}(s_{IF})}{v_{IN}(s_{RF})} = \frac{v_{IF}(s_{IF})}{i_{IF}(s_{IF})} \cdot \frac{i_{IF}(s_{IF})}{i_{RF}(s_{RF})} \cdot \frac{i_{RF}(s_{RF})}{v_{gs}(s_{RF})} \cdot \frac{v_{gs}(s_{RF})}{v_{IN}(s_{RF})}, \quad (15)$$

where $s_{RF} = j\omega_{RF}$ is the RF input frequency and $s_{IF} = j\omega_{IF}$ is the IF output frequency.

The transfer function of $[v_{gs}(s_{RF})/v_{IN}(s_{RF})]$ and $[v_{IF}(s_{IF})/i_{IF}(s_{IF})]$ can be solved by small signal analysis which are given by (16) and (17), respectively, while the transfer function of $[i_{IF}(s_{IF})/i_{RF}(s_{RF})]$ can be derived

adapting Fourier series analysis by approximating the LO signal as an ideal square wave, which is given by (18)

$$\frac{v_{gs}(s_{RF})}{v_{IN}(s_{RF})} = \frac{Z_f}{s_{RF}^2 C_{gst} L_{g1} Z_f + s_{RF} L_{g1} + Z_f}, \quad (16)$$

$$\frac{v_{IF}(s_{IF})}{i_{IF}(s_{IF})} = \frac{R_{L1}}{1 + s_{IF} C_{L1} R_{L1}}, \quad (17)$$

$$\frac{i_{IF}(s_{IF})}{i_{RF}(s_{RF})} = \frac{2}{\pi}. \quad (18)$$

Since the impedances looking through the transistors $M_{1,3}$ at node V_{x1} and transistor M_5 at node V_{y1} are relatively large, hence the intrinsic resistances $r_{ot} = r_{o1}/r_{o3}$ and r_{o5} in Figure 3 are neglected. With the integration of the peaking inductor, the frequency response of the RF signal in (9) is computed as in (19). The transfer function in (19) can be rewritten in expressing a single real pole and two complex poles as follows:

$$\begin{aligned} \frac{i_{RF}(s_{RF})}{v_{gs}(s_{RF})} &= \left(\frac{1 - g_m R_{fb1}}{R_{fb1} + R_{sw}} \right) \\ &\times \left(s_{RF}^3 \left[\frac{C_{py1} C_{pz1} L_{p1} R_{fb1} R_{sw}}{R_{fb1} + R_{sw}} \right] \right. \\ &\quad \left. + s_{RF}^2 \left[\frac{L_{p1} (C_{py1} R_{fb1} + C_{pz1} R_{sw})}{R_{fb1} + R_{sw}} \right] \right. \\ &\quad \left. + s_{RF} \left[\frac{R_{fb1} R_{sw} (C_{py1} + C_{pz1}) + L_{p1}}{R_{fb1} + R_{sw}} \right] + 1 \right)^{-1}, \end{aligned} \quad (19)$$

$$\frac{i_{RF}(s_{RF})}{v_{gs}(s_{RF})} = \frac{((1 - g_m R_{fb1}) / (R_{fb1} + R_{sw}))}{(1 + s_{RF}/\omega_0) (1 + s_{RF}/Q\omega_1 + s_{RF}^2/\omega_1^2)}. \quad (20)$$

Comparing (19) and (20), the pole factor Q , the real pole frequency ω_0 , and the complex pole frequencies ω_1 can be expressed as follows:

$$Q = 1 \times \left(\omega_1 \left((R_{fb1} \parallel R_{sw}) (C_{py1} + C_{pz1}) + \frac{L_{p1}}{R_{fb1} + R_{sw}} - \frac{1}{\omega_0} \right) \right)^{-1}, \quad (21)$$

$$\omega_0 = \frac{1}{\omega_1^2 C_{py1} C_{pz1} L_{p1} (R_{fb1} \parallel R_{sw})}, \quad (22)$$

$$\begin{aligned} \omega_1 &\approx \frac{R_{fb1} + R_{sw}}{2Q\omega_0 L_{p1} (C_{py1} R_{fb1} + C_{pz1} R_{sw})} \\ &\cdot \left(1 + \sqrt{1 + \frac{4Q^2 \omega_0^2 L_{p1} (C_{py1} R_{fb1} + C_{pz1} R_{sw})}{R_{fb1} + R_{sw}}} \right). \end{aligned} \quad (23)$$

Notably, the bandwidth extension is heavily dependent on the value of parasitic capacitances $C_{py(1,2)}$ and $C_{pz(1,2)}$, inductor $L_{p(1,2)}$, and resistors R_{sw} and $R_{fb(1,2)}$. The real pole results in gain and bandwidth reduction at the frequency higher than its value, whereas the complex poles can be adjusted to provide a peaking in frequency response which compensates this adverse effect. Since the real pole is the dominant parameter in achieving a high bandwidth and gain, it should be peaked at the highest frequency as possible, while the location of complex poles are adjusted accordingly to compensate for the gain drop at high frequencies by introducing a peaking and further extending the bandwidth. However, bandwidth enhancement using this approach introduces in-band ripples. Increasing the Q potentially enhances the gain at the peaking; however increasing Q excessively would result in bandwidth reduction. Similarly increasing ω_1 shifts the peaking to higher frequencies; however when ω_1 is increased excessively, it results in the reduction of gain in reference to (21) and (22). Therefore, ω_1 and Q are optimized appropriately to obtain relatively flat and high gain response over the wide bandwidth of operation.

The mixing point of RF and LO signals is located at the node $V_{z(1,2)}$. The switching quad M_7-M_{10} is biased in the vicinity of the threshold voltage at low bias current, thus reducing the DC offset and flicker noise while resulting in a substantial increase in switching efficiency. The low bias current allows the integration of larger load resistance, thus increasing the CG of the mixer and relaxing the constraint of voltage headroom consumption. Load capacitor $C_{L(1,2)}$ couples with the load resistor $R_{L(1,2)}$ presenting a low-pass filter at the IF output with the output real pole equal to $\omega_{IF} = 1/R_L C_L$ based on (17). This integration suppresses the feed components of $\sin(\omega_{LO})t$, $\sin(\omega_{RF})t$, and other unwanted harmonics including the higher-order mixing spurs such as $\sin(m\omega_{LO} \pm n\omega_{RF})t$, where m and n are integers. Ultimately, the overall conversion gain of the presented wideband mixer at the desired output spectrum is given by

$$\begin{aligned}
 CG = & \frac{2}{\pi} \cdot \frac{Z_f}{s_{RF}^2 C_{gst} L_{g1} Z_f + s_{RF} L_{g1} + Z_f} \\
 & \cdot (1 - g_m R_{fb1}) \\
 & \times \left(s_{RF}^3 C_{py1} C_{pz1} L_{p1} R_{fb1} R_{sw} \right. \\
 & \quad + s_{RF}^2 L_{p1} (C_{py1} R_{fb1} + C_{pz1} R_{sw}) \\
 & \quad + s_{RF} [R_{fb1} R_{sw} (C_{py1} + C_{pz1}) + L_{p1}] \\
 & \quad \left. + R_{fb1} + R_{sw} \right)^{-1} \\
 & \cdot \frac{R_{L1}}{1 + s_{IF} C_{L1} R_{L1}} \cdot [\sin(\omega_{LO} - \omega_{RF})t].
 \end{aligned} \tag{24}$$

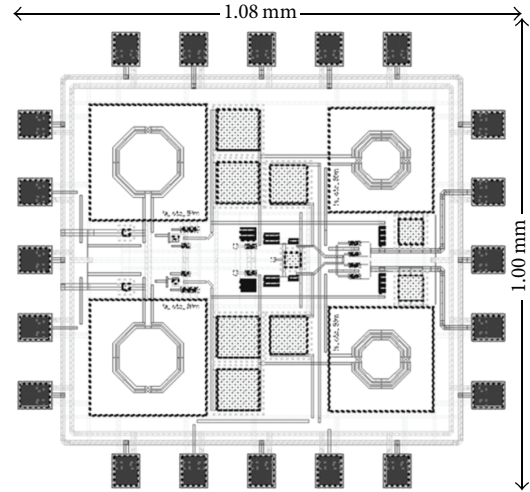


FIGURE 4: Physical layout of wideband mixer including RF ESD pads.

4. RC-Extracted Simulation Results

The proposed wideband mixer of Figure 2 has been designed and simulated using $0.13 \mu\text{m}$ CMOS standard process for regulated CR applications. The layout parasitic extraction (LPE) is executed and validated under Cadence Spectre-RF and Mentor Calibre platform. In an interest of perfect matching and the minimization of mismatch parasitic coupling effect, the components and metal paths in the designed mixer circuit were placed as symmetrical as possible. The physical layout of the circuit including the RF ESD pads is illustrated in Figure 4 with a total chip area consumption of $1.08 \times 1.00 \text{ mm}^2$.

The postlayout simulation results were carried out with a total power consumption of 3.5 mW at respective voltage headroom of 1 V. The RF input of the wideband mixer is matched to 50Ω termination and the respective simulated input return loss, S_{11} , is illustrated in Figure 5. The S_{11} of the optimized RFCR wideband mixer is achieved well below -12 dB across the operating frequency ranging from 50 MHz to 10 GHz.

Figure 6 shows the simulated NF versus RF frequency from 50 MHz to 10 GHz with a fixed IF output at 10 MHz while the LO power is set to be 0 dBm. The simulated minimum and maximum NF of the wideband mixer are 10.8 dB and 12.8 dB, respectively. This wideband mixer exhibits a flat NF with a variation of $\pm 1 \text{ dB}$ across the entire frequency range. Figure 7 shows the simulated CG versus RF frequency in a comparison plot with the presence of the peaking inductor and absence of the peaking inductor. At low frequency, the CG is observed to be around 16 dB. However, at high frequency range, the CG is achieved to about 8 dB without the peaking inductor in place and about 14 dB with the integration of peaking inductor, resulting in 6 dB of gain improvement. This plot reveals and confirms that the peaking inductor in RFCR mixer had improved the CG at high frequency range. The proposed wideband mixer achieves a high gain with a flatness variation of $\pm 1.4 \text{ dB}$ where

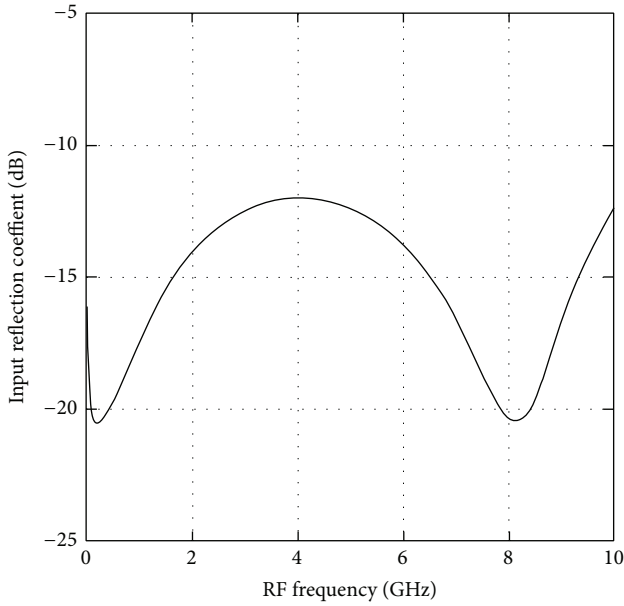
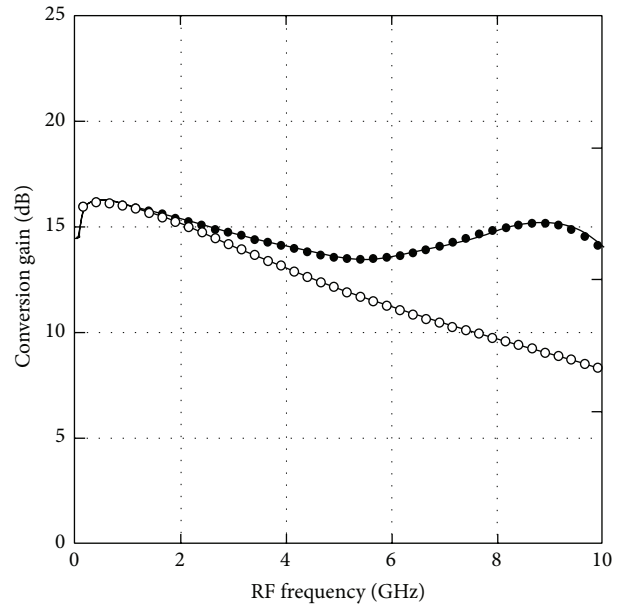


FIGURE 5: Simulated result of input return loss (S_{11}).



—●— With peaking inductor
 -○- Without peaking inductor

FIGURE 7: Simulated CG versus RF frequency.

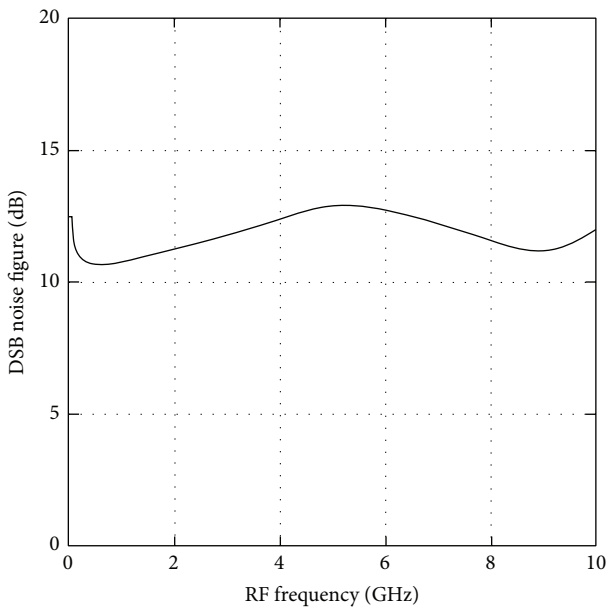
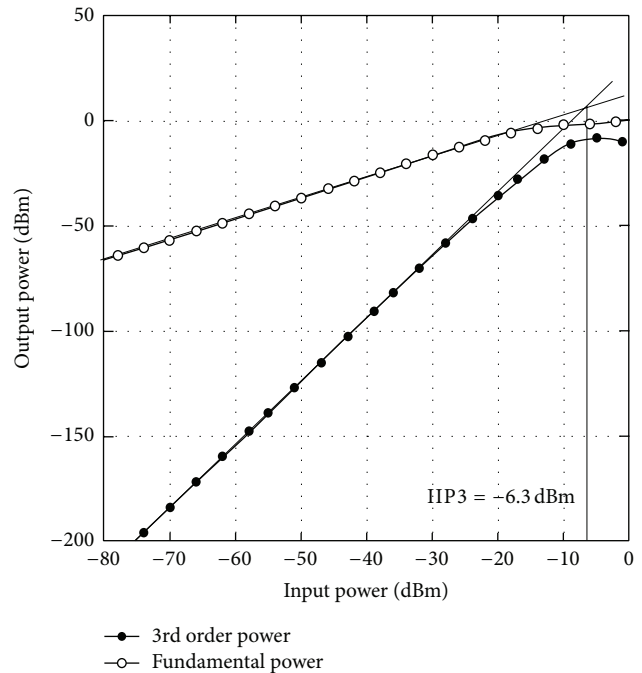


FIGURE 6: Simulated NF versus RF frequency.



—●— 3rd order power
 -○- Fundamental power

FIGURE 8: Two-tone IIP3 simulation at 5 GHz.

the maximum CG of 16.3 dB is observed at 500 MHz and a minimum of CG of 13.5 dB is observed at 5.5 GHz.

In observing the linearity response, the center frequency of 5 GHz from the operating bandwidth is selected. With an LO power of 0 dBm at $\omega_{LO} = \omega_{RF} + 10$ MHz, the P1dB is simulated to be -15.8 dBm. Applying two-tone test with 1 MHz frequency offset, the simulated IIP3 is -6.3 dBm as shown in Figure 8. Figure 9 depicts the overall performance of the simulated P1dB and IIP3 against RF frequency of the mixer over the range of 50 MHz to 10 GHz. The mixer

achieves a P1dB range of -17.0 dBm to -13.6 dBm while the IIP3 ranges from -8.1 dBm to -4.5 dBm.

The overall performance of the proposed mixer can be weighed comparatively with other reported works using a figure-of-merits (FOM). Generally, the mixer performance was compared in terms of CG, NF, linearity (IIP3 or input P1dB), and power consumption [29, 30]. However, a trade-off

TABLE 1: Summary of wideband mixer performance and comparison with prior published work.

Reference	Process (μm)	Freq. (GHz)	CG (dB)	NF (dB)	P1dB (dBm)	IIP3 (dBm)	V_{DD} (V)	P_{DC} (mW)	FOM (dB)
[5] ^a	0.18	3.4~6.8	5.75 ± 1.45	14.15 ± 0.25	—	2.5 ± 0.5	1.0	2.9	10.07
[6] ^a	0.13	0.87~3.7	13.75 ± 0.25	4.6 ± 1.9	—	-11.5 ± 1.5	1.2	16.8	14.03
[7] ^a	0.065	1~10.5	10.15 ± 2.65^c	9.8 ± 2.2^c	-12.7 ± 2.3^c	-3.5 ± 3.5^c	1.0	5.0	21.48
[8] ^a	0.13	3.1~10.6	11.9 ± 2.10	17.05 ± 2.55	-21.5 ± 2.5	-13.5 ± 2.5^c	1.2	1.85	10.5
[9] ^a	0.18	0.5~7.5	4.35 ± 1.35^c	15	-16	-11	0.77	0.48	18.77
[10] ^a	0.18	2~11	6.9 ± 1.5	17.75 ± 2.25^c	-6 ± 2.5^c	4.25 ± 2.25^c	1.8	25.7	5.68
[11] ^a	0.045	1~10	8.35 ± 1.05	21.2	-14.6 ± 1.4	—	1.1	1.46	—
[12] ^a	0.13	1~10	5.5 ± 2.5	13.15 ± 1.85	14.5 ± 1.5^c	-5.5 ± 1.5	1.2	8.4	11.0
[13] ^a	0.18	2.3~5.8	2.26 ± 1.48	20.5 ± 1.3	-17.5 ± 2.5	6.05 ± 1.35	1.8	8.3	2.0
[14] ^b	0.13	3.1~4.8	11.25 ± 1.25^c	12.75 ± 0.25^c	—	24	1.2	3.0	24.92
[15] ^a	0.18	0.2~16	7.0 ± 1.7^c	—	—	—	1.8	15	—
This work	0.13	0.05~10	14.9 ± 1.4	11.8 ± 1	-15.3 ± 1.7	-6.3 ± 1.8	1.0	3.5	26.14

^aMeasured results.

^bSimulated results.

^cEstimated value.

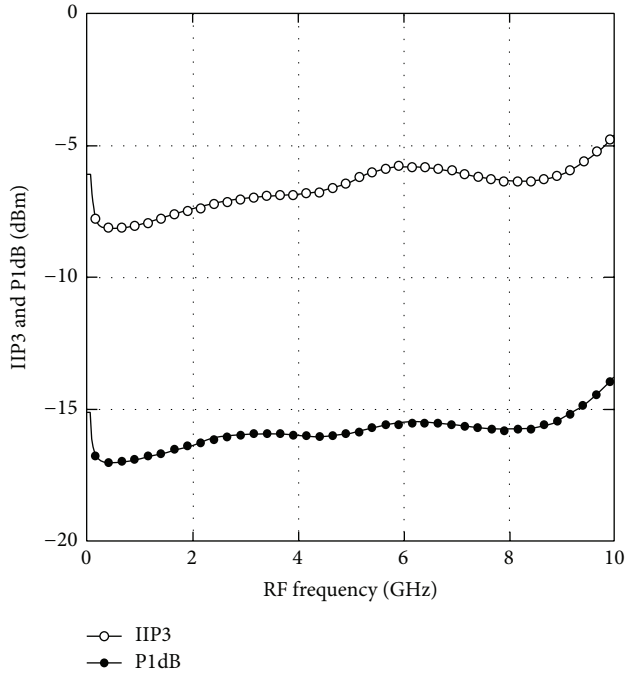


FIGURE 9: Simulated IIP3 and P1dB versus RF frequency.

exists between power dissipation and bandwidth in wideband mixer design. Hence, it is essential to include the operating bandwidth parameter into FOM calculation for the fair comparison with the reported works [31]. As a result, a modified FOM is introduced for wideband mixer, which is given as

$$\text{FOM} = 10 \log \left(\frac{10^{\text{CG}_{\text{max}}/20} \cdot 10^{(\text{IIP3}_{\text{max}}-10)/20}}{10^{\text{NF}_{\text{min}}/10} \cdot P_d} \cdot \frac{f_H - f_L}{\sqrt{f_H f_L}} \right), \quad (25)$$

where f_L and f_H represent lower cut-off frequency and upper cut-off frequency, respectively. P_d is the power consumption

in Watts. CG_{max} is the maximum conversion gain, IIP3_{max} is the maximum input third-order intercept point, and NF_{min} is the minimum noise figure. The simulated results of the proposed architecture along with other reported results of the recent works are tabulated in Table 1. The proposed mixer achieves 26.14 dB which is the highest FOM compared to other mixers.

5. Conclusion

In this work, a new wideband mixer for CR receiver has been successfully designed and simulated in 0.13 μm CMOS process. A π -match LC network is embedded at the input of RFCR architecture to simultaneously enhance the input impedance matching and NF while encapsulating an operating bandwidth as large as 10 GHz. The RFCR adaptation enables the proposed mixer to achieve high gain by summing up the transconductance of NMOS and PMOS in the transconductance stage. The peaking inductor achieves a flat CG response by compensating the gain degradation at high frequencies, while extending the bandwidth. Additionally, the complementary current-reuse technique is implemented at the output stage to further boost the CG without dissipating additional power. The proposed wideband mixer operates from 50 MHz to 10 GHz with an RF input return loss better than -12 dB, a high CG of 14.9 ± 1.4 dB, a flat NF of 11.8 ± 1 dB, an P1dB of -15.3 ± 1.7 dBm, and an IIP3 of -6.3 ± 1.8 dBm. This mixer operates at a low voltage headroom of 1.0 V while consuming only 3.5 mW of power. This characteristic of proposed wideband mixer serves to be a compatible architecture to meet the future growing demands in CR application.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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References

- [1] I. F. Akyildiz, W.-Y. Lee, M. C. Vuran, and S. Mohanty, "NeXt generation/dynamic spectrum access/cognitive radio wireless networks: a survey," *Computer Networks*, vol. 50, no. 13, pp. 2127–2159, 2006.
- [2] M. Kitsunezuka, H. Kodama, N. Oshima, K. Kunihiro, T. Maeda, and M. Fukaishi, "A 30-MHz-2.4-GHz CMOS receiver with integrated RF filter and dynamic-range-scalable energy detector for cognitive radio systems," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 5, pp. 1084–1093, 2012.
- [3] C. Cordeiro, K. Challapali, D. Birru, and N. Sai Shankar, "IEEE 802.22: the first worldwide wireless standard based on cognitive radios," in *Proceedings of the 1st IEEE International Symposium on New Frontiers in Dynamic Spectrum Access Networks (DySPAN '05)*, pp. 328–337, Baltimore, Md, USA, November 2005.
- [4] B. Razavi, "Cognitive radio design challenges and techniques," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 8, pp. 1542–1553, 2010.
- [5] J.-D. Chen, "A low-voltage high-linearity ultra-wideband down-conversion mixer in 0.18- μm CMOS technology," *Microelectronics Journal*, vol. 42, no. 1, pp. 113–126, 2011.
- [6] D. Na and T. W. Kim, "A 1.2 V, 0.87-3.7 GHz wideband low-noise mixer using a current mirror for multiband application," *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 2, pp. 91–93, 2012.
- [7] S. K. Hampel, O. Schmitz, M. Tiebout, and I. Rolfes, "Inductorless low-voltage and low-power wideband mixer for multistandard receivers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 5, pp. 1384–1390, 2010.
- [8] J.-B. Seo, J.-H. Kim, H. Sun, and T.-Y. Yun, "A low-power and high-gain mixer for UWB systems," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 12, pp. 803–805, 2008.
- [9] K.-H. Liang, H.-Y. Chang, and Y.-J. Chan, "A 0.5-7.5 GHz ultra low-voltage low-power mixer using bulk-injection method by 0.18- μm CMOS technology," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 7, pp. 531–533, 2007.
- [10] P.-Z. Rao, T.-Y. Chang, C.-P. Liang, and S.-J. Chung, "An ultra-wideband high-linearity CMOS mixer with new wideband active baluns," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 9, pp. 2184–2192, 2009.
- [11] O. Schmitz, S. K. Hampel, C. Orlob, M. Tiebout, and I. Rolfes, "Body effect up- and down-conversion mixer circuits for low-voltage ultra-wideband operation," *Analog Integrated Circuits and Signal Processing*, vol. 64, no. 3, pp. 233–240, 2010.
- [12] H. Zijie and K. Mouthaan, "A 1- to 10-GHz RF and wideband IF cross-coupled Gilbert mixer in 0.13- μm CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 11, pp. 726–730, 2013.
- [13] H. C. Wei, R. M. Weng, and S. Y. Li, "A Broadband high linearity and isolation down-conversion mixer for wimax applications," *Journal of Electromagnetic Waves and Applications*, vol. 23, no. 11-12, pp. 1555–1565, 2009.
- [14] M. Parvizi and A. Nabavi, "Low-power highly linear UWB CMOS mixer with simultaneous second- and third-order distortion cancellation," *Microelectronics Journal*, vol. 41, no. 1, pp. 1–8, 2010.
- [15] F.-C. Chang, P.-C. Huang, S.-F. Chao, and H. Wang, "A low power folded mixer for UWB system applications in 0.18- μm CMOS technology," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 5, pp. 367–369, 2007.
- [16] P. J. Sullivan, B. A. Xavier, and W. H. Ku, "Low voltage performance of a microwave CMOS Gilbert cell mixer," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 7, pp. 1151–1155, 1997.
- [17] Q. Z. Wan and C. H. Wang, "A wideband CMOS current-mode downconversion mixer for multi-standard receivers," *Progress in Electromagnetics Research*, vol. 129, pp. 421–437, 2012.
- [18] S. Douss, F. Touati, and M. Loulou, "An RF-LO current-bleeding doubly balanced mixer for IEEE 802.15.3a UWB MB-OFDM standard receivers," *AEU-International Journal of Electronics and Communications*, vol. 62, no. 7, pp. 490–495, 2008.
- [19] V. Vidojkovic, J. Tang, A. Leeuwenburgh, and A. H. M. Roermund, *Adaptive Multi-Standard RF Front-Ends*, Springer, Dordrecht, The Netherlands, 2008.
- [20] S. K. Hampel, O. Schmitz, M. Tiebout, K. Mertens, and I. Rolfes, "9-GHz wideband CMOS RX and TX front-ends for universal radio applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 4, pp. 1105–1116, 2012.
- [21] H.-K. Chen, Y.-S. Lin, and S.-S. Lu, "Analysis and design of a 1.628-GHz compact wideband LNA in 90-nm CMOS using a π -match input network," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 8, pp. 2092–2104, 2010.
- [22] W.-K. Chong, H. Ramiah, G.-H. Tan, N. Vitee, and J. Kanesan, "Design of ultra-low voltage integrated CMOS based LNA and mixer for ZigBee application," *AEU-International Journal of Electronics and Communications*, vol. 68, no. 2, pp. 138–142, 2013.
- [23] H.-K. Chiou, K.-C. Lin, W.-H. Chen, and Y.-Z. Juang, "A 1-V 5-GHz self-bias folded-switch mixer in 90-nm CMOS for WLAN receiver," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 6, pp. 1215–1227, 2012.
- [24] R. Gharpurey, "A broadband low-noise front-end amplifier for Ultra Wideband in 0.13- μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 9, pp. 1983–1986, 2005.
- [25] Q. Li and Y. P. Zhang, "A 1.5-V 2-9.6-GHz inductorless low-noise amplifier in 0.13- μm CMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 10, pp. 2015–2023, 2007.
- [26] H. Darabi and A. A. Abidi, "Noise in RF-CMOS mixers: a simple physical model," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 1, pp. 15–25, 2000.
- [27] T. Song, H.-S. Oh, E. Yoon, and S. Hong, "A low-power 2.4-GHz current-reused receiver front-end and frequency source for wireless sensor network," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 5, pp. 1012–1021, 2007.
- [28] M. El-Nozahi, E. Sánchez-Sinencio, and K. Entesari, "A 2032-GHz wideband mixer with 12-GHz if bandwidth in 0.18- μm SiGe process," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 11, pp. 2731–2740, 2010.
- [29] V. Vidojkovic, J. Van Der Tang, A. Leeuwenburgh, and A. H. M. Van Roermund, "A low-voltage folded-switching mixer in 0.18- μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 6, pp. 1259–1263, 2005.
- [30] K.-H. Liang and H.-Y. Chang, "0.5-6 GHz low-voltage low-power mixer using a modified cascode topology in 0.18 μm

CMOS technology,” *IET Microwaves, Antennas and Propagation*, vol. 5, no. 2, pp. 167–174, 2011.

- [31] H.-K. Chiou and H.-T. Chou, “An ultra-low power V-band source-driven down-conversion mixer with low-loss and broadband asymmetrical broadside-coupled balun in 90-nm CMOS technology,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 7, pp. 2620–2631, 2013.



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