Review Article

Photonic Integration on the Hybrid Silicon Evanescent Device Platform

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This paper reviews the recent progress of hybrid silicon evanescent devices. The hybrid silicon evanescent device structure consists of III-V epitaxial layers transferred to silicon waveguides through a low-temperature wafer bonding process to achieve optical gain, absorption, and modulation efficiently on a silicon photonics platform. The low-temperature wafer bonding process enables fusion of two different material systems without degradation of material quality and is scalable to wafer-level bonding. Lasers, amplifiers, photodetectors, and modulators have been demonstrated with this hybrid structure and integration of these individual components for improved optical functionality is also presented. This approach provides a unique way to build photonic active devices on silicon and should allow application of silicon photonic integrated circuits to optical telecommunication and optical interconnects.

1. INTRODUCTION

Recent research in silicon photonics has been driven by the motivation to realize silicon optoelectronic integrated devices using large scale, low-cost, and highly accurate CMOS technology. Silicon is transparent at the $1.5\,\mu$m and $1.3\,\mu$m telecommunication wavelengths and has demonstrated low loss waveguide with losses in the range of 0.2 dB/cm ~ 1 dB/cm. The large index contrast of silicon waveguides with silicon dioxide cladding results in highly confined optical modes and reduction of waveguide bend radii leading to dense photonic integration. This has resulted in advances in passive devices such as compact filters [1], optical buffers [2], photonic crystals [3], and wavelength multiplexer/demultiplexers [4, 5].

It was only recently that silicon has been demonstrated as a high-speed modulator. Silicon-based modulators have been reported using free carrier plasma dispersion in Mach-Zehnder interferometer structure [6, 7], photonic crystals [8], and ring resonator structures [9]. Strained silicon has been shown to break the inversion symmetry of silicon allowing silicon to exhibit linear electro-optic refractive index modulation [10]. Recently, an electroabsorption modulator on silicon has been demonstrated based on the quantum confined stark effect in strained silicon germanium [11].

Light detection is another major research topic in silicon photonics. Strained germanium and silicon germanium push the absorption out to $1.55\,\mu$m wavelength and are attractive since it is compatible with CMOS processing capabilities [12, 13]. Integration of the photodetector with the receiver is critical for lower capacitance and higher sensitivity [14].

The indirect bandgap of silicon has been a key hurdle for achieving optical gain elements. Although Raman lasers and amplifiers [15–17], and optical gain in nanopatterned silicon have been observed [18], an electrically pumped silicon waveguide gain element has been an unsolved challenge.

An alternative to fabricating the gain element in silicon is to take prefabricated lasers and couple them to silicon waveguides. However, due to the tight alignment tolerances of the optical modes and the need to align each laser individually, this method has limited scalability, and it is difficult to envision die attaching more than a few lasers to each chip without prohibitive expense. Furthermore, the reflections at the chip interfaces limit the gain and spectral flatness that can be achieved.
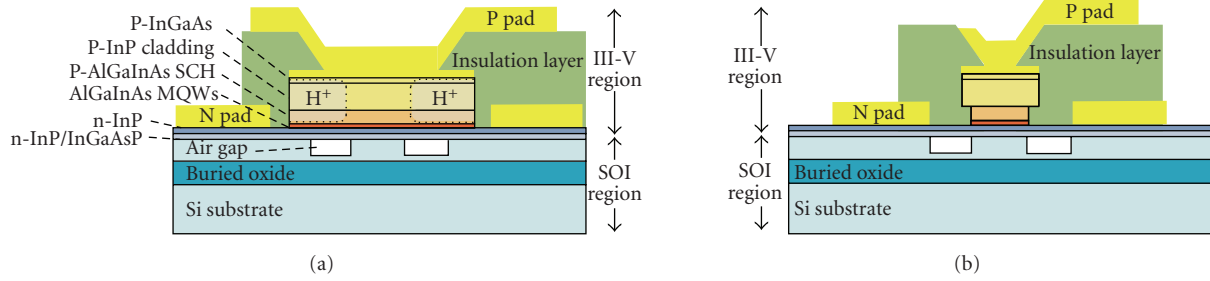
FIGURE 1: Hybrid silicon evanescent device cross-section structures: (a) a wide III-V mesa for amplifiers and lasers, (b) a narrow III-V mesa for detectors and modulators.

Epitaxial growth of III-V layers on silicon substrates has been investigated as well. The demonstrations include InGaAs quantum dot lasers [18] and InGaSb quantum well lasers [19] fabricated on silicon substrate. Those demonstrations have widened the possibility of building monolithically integrated on-chip laser sources on the silicon photonics platform. However, an efficient coupling scheme from the III-V lasers to the silicon waveguide needs to be developed since most of the lasing mode is in the III-V layers.

Recently, we have demonstrated a hybrid integration platform utilizing III-V epitaxial layers transferred to silicon to realize many types of photonic active devices through a single wafer bonding step. The wafer-bonded structure forms a hybrid waveguide, where its optical mode lies both in silicon and III-V layers. This structure enables the use of III-V layers for active light manipulation such as gain, absorption, and electro-optical effect for the amplifiers, lasers, detectors, and modulators. In this paper, we review the recent progress on hybrid silicon evanescent devices. In Section 2, the device structure and design issues are introduced. In Section 3, the device fabrication process is described. Section 4 presents the performance and characteristics of fabricated silicon evanescent devices. Finally, several potential future paths of this research are discussed in Section 5.

2. DEVICE PLATFORM

Figure 1 shows the general structure of hybrid silicon evanescent devices. The hybrid structure is comprised of a III-V region bonded to a silicon waveguide fabricated on a silicon-on-insulator wafer. The mesa structure formed on the III-V region enables the current flow through the multiple quantum well region. The general structure of III-V layers consists of a p-type contact layer, a p-type cladding, a p-type separated confinement heterostructure (SCH) layer, an undoped multiple quantum well layer, n-type contact layer, and n-type super lattices. Amplifiers and lasers have a wide III-V mesa ($12\,\mu m \sim 14\,\mu m$) for better heat conduction and mechanical strength (Figure 1(a)) while a narrow III-V mesa ($2\,\mu m \sim 4\,\mu m$) is chosen for detectors and modulators for high-speed operation with a reduced capacitance (Figure 1(b)). The optical mode in this hybrid waveguide lies both in the silicon waveguide and the multiple quantum well layers. The confinement factors in III-V and silicon regions of the hybrid waveguide can be manipulated by changing the silicon waveguide dimensions. The quantum well confinement factor is a critical design parameter in order to achieve enough optical gain and absorption while the silicon confinement factor is an important parameter determining coupling efficiency when the device is integrated with silicon passive devices. Figure 2 shows three different mode profiles with three different waveguide widths. In general, the silicon confinement factor increases as the height or width of the silicon waveguide increases while the quantum well confinement factor decreases. The epitaxial structures and confinement factors for each device set will be specified in Section 4.

3. FABRICATION

3.1. Plasma assisted low-temperature wafer bonding

The transfer of the indium phosphide (InP)-based epitaxial layer structure to the silicon-on-insulator (SOI) substrate is a key step in the fabrication of this hybrid platform and has direct impact on the device performance, yield, and reliability. Due to the mismatch between the thermal expansion coefficient of silicon and indium phosphide (α_{Si} = 2.6 $\times 10^{-6}/K$, α_{InP} = 4.8 $\times 10^{-6}/K$), high-temperature (>400°C) annealing steps are not desirable. Figure 3(a) shows a Nomarski photograph of the top surface of an InP die transferred to a silicon-on-insulator substrate at 600°C. Crosshatching can be seen for this high-temperature direct wafer bonding which can lead to degradation of material quality and scalability issues due to the accumulation of stress over larger sample sizes. In order to resolve this issue, low-temperature annealing is used with an oxygen plasma surface treatment to enable strong bonding [20]. An annealing temperature of 300°C is chosen to minimize bonding stress while still being able to convert the weak Hydrogen bonds formed by the room temperature bonding to strong covalent Si–O–In and Si–O–P bonds. Figure 3(b) shows a successful transfer of InP epitaxial layers to SOI with smooth device quality surface morphology and no interfacial voids.

Figure 4 is the schematic process flow of the oxygen plasma assisted low-temperature (300°C) wafer bonding. After rigorous sample cleaning and close microscopic inspection with 200x magnification, the native oxide on SOI and InP are removed in standard buffer HF solution (1HF : 7
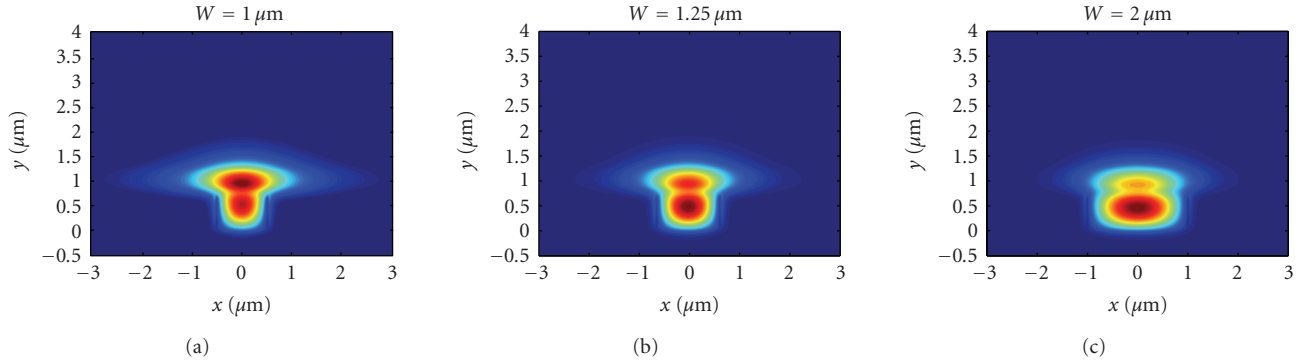
$W = 1\,\mu m$ $W = 1.25\,\mu m$ $W = 2\,\mu m$

FIGURE 2: Mode profiles with different waveguide widths. Height of the silicon waveguide is fixed at $0.7\,\mu m$.

(a) (b)

FIGURE 3: Nomarski microscope images of the transferred III-V surface at bonding temperatures of (a) 600°C and (b) 300°C.

H_2O) and NH_4OH (39%), respectively, resulting in clean, hydrophobic surfaces. The samples then undergo an oxygen plasma surface treatment to grow an ultrathin layer of oxide (<5 nm) [21] which leads to very smooth (rms roughness <0.5 nm) hydrophilic surfaces, which is less sensitive to the microroughness as compared to hydrophobic bonding. The Si–O–Si bonds of the oxide (SOI side) are also found to be more strained than conventional oxides formed in standard RCA-1 cleaning process or other hydrophilic wet-chemical treatment, and have a higher readiness to break and form new bonds. O_2 energetic ion bombardment also acts as a final cleaning step to remove hydrocarbons and water-related species on the sample surface efficiently. The following deionized water dip further terminates the oxide surface by polar hydroxyl groups OH^-, forming bridging bonds between the mating surfaces to result in spontaneous bonding at room temperature [22]. To strengthen the bond, the bonded sample is placed in a conventional wafer bonding machine (Suss Bonder SB6E), where the samples are held together at a pressure of 1.5 MPa and a temperature of 300°C, under vacuum (<4×10^{-4} Torr) from 1 to 12 hours. The 300°C annealing process enhances out diffusion of molecules trapped at the interface and desorption of chemisorbed surface atoms, such as hydrogen, while activating the formation of covalent bonds to achieve higher bonding energy [20]. After annealing and cooling, the InP substrate is selectively removed in a 3HCl : $1H_2O$ solution at room temperature.

Figure 5 shows a 2-inch InP-based expitaxial wafer bonded on a SOI sample cleaved from a 6 inch SOI wafer. Smooth III-V morphology with no interfacial void is achieved in the bonded area. The two defects on the left-hand side of the figure are due to wafer handling with tweezers and InP epitaxial surface defects that are $29\,\mu m$ in diameter. Successful epitaxial transfer on 2 inch wafer demonstrates the scalability of this oxygen plasma-assisted low-temperature bonding process, which subsequently paves the way for mass production of the hybrid devices.

3.2. Silicon waveguide and III-V back-end processing

The general procedure of silicon waveguide formation on an SOI wafer and III-V back-end processing after wafer bonding process is as follows. The silicon waveguide is formed on the (100) surface of an undoped silicon-on-insulator (SOI) substrate using Cl_2/Ar/HBr-based plasma reactive ion etching. The thickness of the buried oxide (BOX) is $1\,\mu m$ for the devices reported in this paper. The III-V epitaxial layer is then transferred to the patterned silicon wafer through low-temperature oxygen plasma-assisted wafer bonding, which was described in Section 3.1. After removal of the InP substrate, mesa structures on III-V layers are formed by dry-etching the p-type layers using a CH_4/H/Ar-based plasma reactive ion etch. Subsequent wet-etching of the quantum well layers to the n-type layers is performed using H_3PO_4/H_2O_2. Ni/AuGe/Ni/Au alloy contacts are deposited onto the exposed n-type InP layer. Pd/Ti/Pd/Au p-contacts are then deposited on the center of the mesas. For lasers and amplifiers, protons (H^+) are implanted on the two sides of the p-type mesa to create a $4\,\mu m$ wide current channel and to prevent lateral current spreading, ensuring a large overlap between the carriers and the optical mode. Ti/Au probe pads are then deposited on the top of the mesa. Then, if necessary, the sample is diced into bars and each bar is polished.

4. DEVICE RESULTS

4.1. Silicon evanescent lasers

4.1.1. 1550 nm Fabry Perot lasers

The first demonstrated device using the silicon evanescent device platform was the Fabry-Perot (FP) hybrid silicon evanescent laser [23]. The cavity for these lasers was made by dicing the ends of the hybrid waveguide and polishing
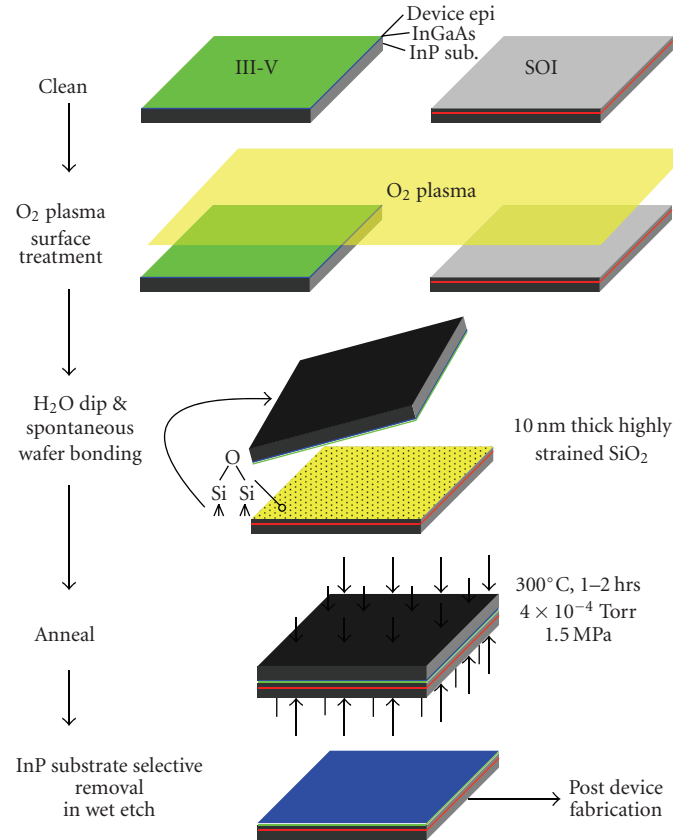
FIGURE 4: Oxygen plasma-assisted low-temperature wafer bonding process flow.
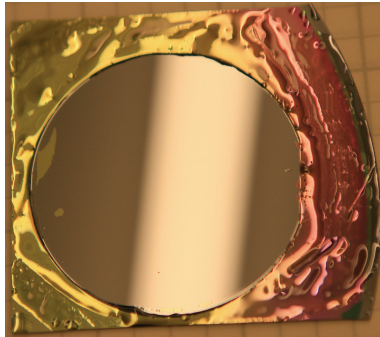

FIGURE 5: Photograph of a 2 inch III-V epitaxial transferred to an SOI sample after 300°C anneal for 2 hours and selective removal of the InP substrate. InP wafer sidewall is surrounded by Crystalbond™ wax to protect InP device layer from being etched laterally during the substrate removal step. The white region in the middle of the wafer is a reflection of the illuminator.

them to a mirror finish. The device presented here has two major changes from the first reported devices. First, the buried oxide thickness is reduced to 1 μm in order to reduce the thermal impedance of the device. Second, the III-V mesa was reduced to 12 μm in order to reduce the device series resistance as shown in Figure 1(a). The waveguide height, width, rib etch depth, and cavity length were 0.7 μm,

2 μm, 0.5 μm, and 850 μm, respectively. The calculated confinement factors in the silicon and the quantum well region are 63% and 4%, respectively. The epitaxial structure of the lasers is specified in Table 1.

The continuous wave (CW) LI curve for this device is collected on one side with an integrating sphere as shown in Figure 6(a). In order to account for light exiting both sides of the cavity, the data is multiplied by two. It can be seen that the maximum laser output power, threshold, and differential efficiency at 15°C are 24 mW, 70 mA, and 16%, respectively. The device shows improvement in output power and differential efficiency while maintaining a similar threshold when compared to the first generation device. The maximum operating temperature is 45°C.

Figure 6(b) shows a set of pulsed single-sided output power as a function of applied current (1 kHz repetition rate, 0.1% duty cycle) for stage temperatures ranging from 15 to 50°C. The characteristic temperature (T_0) and an above threshold characteristic temperature (T_1) [24] are 60 K and 120 K, respectively. The thermal impedance of the laser is measured using a combination of two experiments. The first set of measurements is used to establish a baseline for the shift in lasing wavelength as a function of active region (stage) temperature ($d\lambda/dT$) as shown in Figure 7(a). Similar to the characteristic temperature measurement above, this experiment is performed pulsed to ensure that there is minimal device heating other than what is provided by
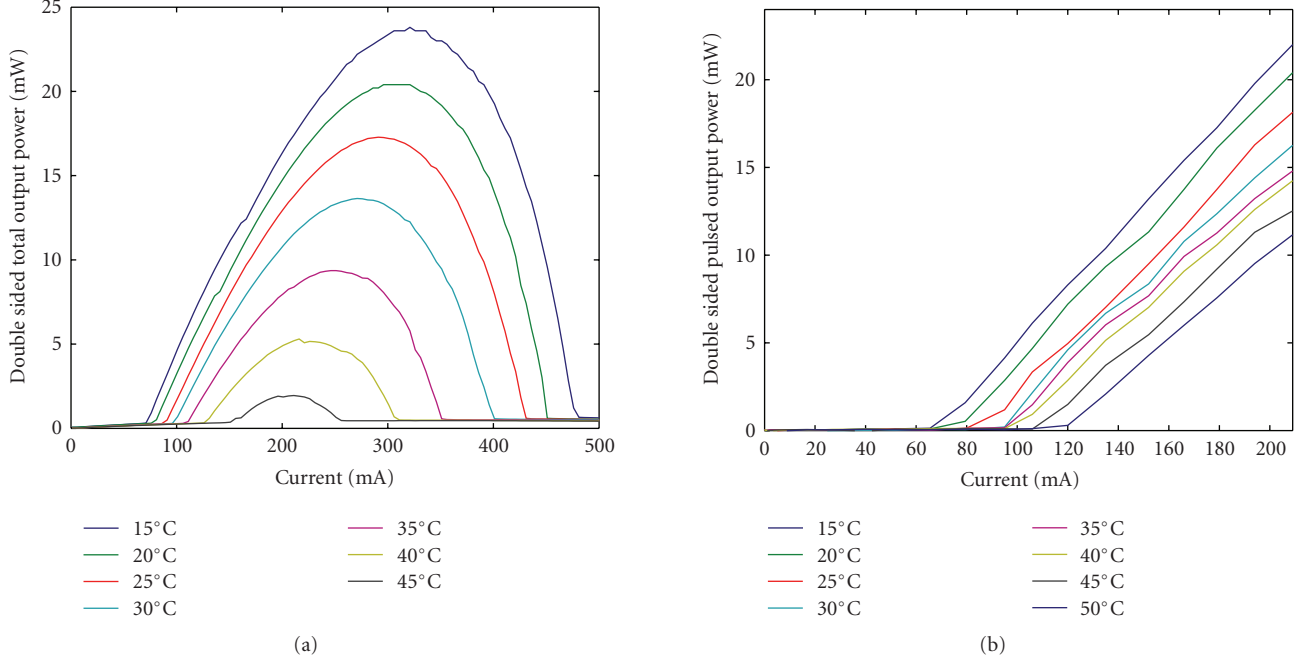
FIGURE 6: LI curves for a 1550 nm FP silicon evanescent laser (a) double-sided continuous wave output power, (b) double-sided pulsed output power.

TABLE 1: III-V epitaxial layer structure with a 1550 nm photoluminescence peak.

Name	Composition	Doping concentration	Thickness
P contact layer	P-type $In_{0.53}Ga_{0.47}As$	1×10^{19} cm^{-3}	0.1 μm
Cladding	P-type InP	1×10^{18} cm^{-3}	1.5 μm
SCH	P-type $Al_{0.131}Ga_{0.34}In_{0.528}$ As, 1.3Q	1×10^{17} cm^{-3}	0.25 μm
Quantum wells	$Al_{0.089}Ga_{0.461}In_{0.45}As$, 1.3Q(9x)	undoped	10 nm
	$Al_{0.055}Ga_{0.292}In_{0.653}As$, 1.7Q(8x)	undoped	7 nm
N layer	N-type InP	1×10^{18} cm^{-3}	110 nm
Super lattice	N-type $In_{0.85}Ga_{0.15}As_{0.327}P_{0.673}$, 1.1Q(2x)	1×10^{18} cm^{-3}	7.5 nm
	N-type InP (2x)	1×10^{18} cm^{-3}	7.5 nm
N bonding layer	N-type InP	1×10^{18} cm^{-3}	10 nm

the temperature-controlled stage. The second measurement is performed CW, and is used to measure the shift in wavelength as a function of applied electrical power to the laser ($d\lambda/dP$) as shown in Figure 7(b). The thermal impedance Z_T is then given by (1)

$$Z_T = \left(\frac{d\lambda}{dT}\right)^{-1}\left(\frac{d\lambda}{dP}\right). \tag{1}$$

In both the $d\lambda/dT$ and $d\lambda/dP$ experiments, a single longitudinal mode in the laser spectrum is monitored. Combining the results from Figures 7(a) and 7(b), the laser thermal impedance is measured to be 42°C/W.

The thermal performance of the hybrid laser depends on several factors. These include the amount and location of heat that is generated, the thermal conductivity of the layers surrounding the heat sources, and the operating temperature of the laser active region. To model the temperature rise as a function of applied bias, we have employed a two-

dimensional finite element modeling technique. For the hybrid laser cross-section shown in Figure 1(a), there are six major sources of thermal energy. These include resistive heating in the p-cladding, the n-contact layer, the active region, and the p and n contacts, along with heat generated by the diode drop associated with the active region. More detailed information about the values used in the simulation can be found in [25].

A two dimensional temperature profile of the hybrid laser operating at 500 mA is shown in Figure 8(a). The dissipated electrical power and the predicted temperature rise in the laser active region are plotted as a function of applied current in Figure 8(b). The contribution of each layer to the total electrical power dissipation is also shown in the same figure. Combining the simulated temperature rise, the dissipated electrical power, and the output optical power, the thermal impedance of the laser is 43.5°C/W, which is within 5% of our initial experimental results.
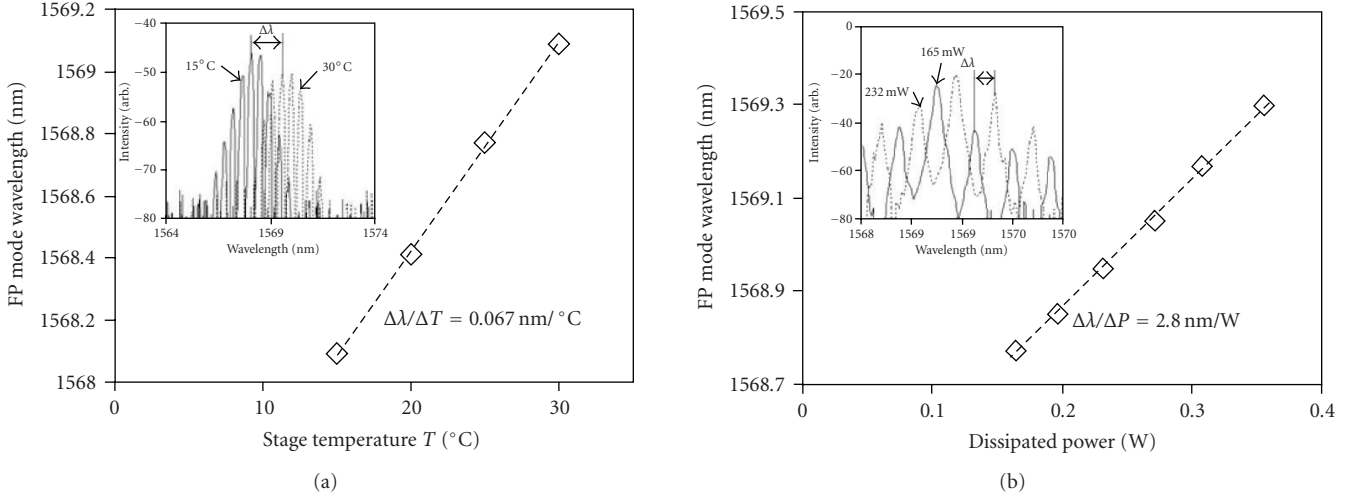
(a)

(b)

FIGURE 7: (a) Pulsed measurement results for the shift in lasing wavelength (single FP mode) as a function of stage temperature. The inset contains a laser output spectrum at 15°C and 30°C. (b) Results for the shift in lasing wavelength (single FP mode) as a function of dissipated power.
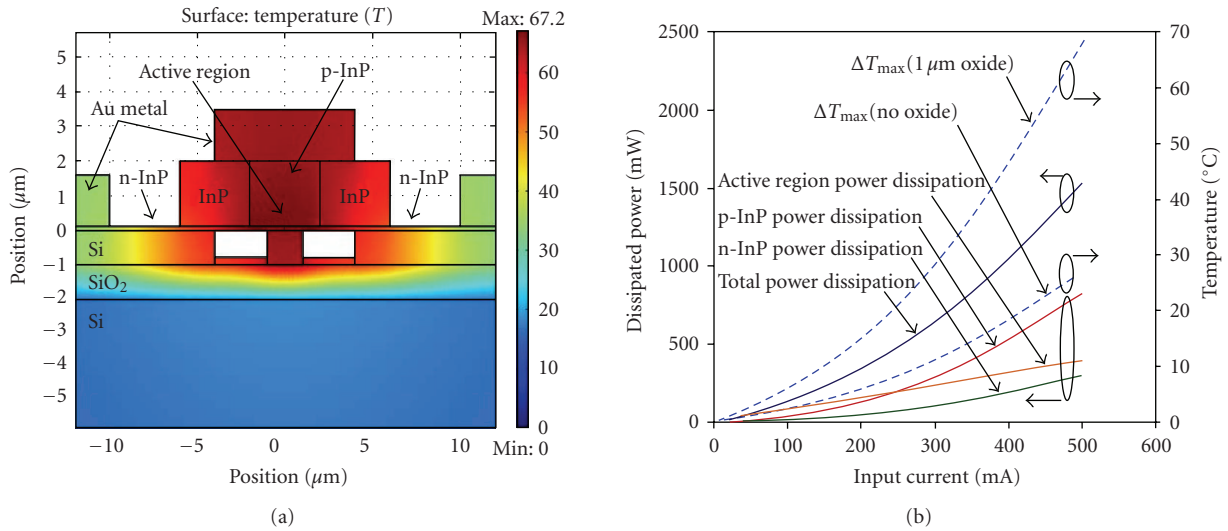

(a)

(b)

FIGURE 8: (a) Two-dimensional temperature profile in the hybrid laser at a bias current of 500 mA. (b) Theoretical predictions for the dissipated electrical power in the various laser sections along with the predicted temperature rise in the active region as a function of contact current.

To show the effect of the buried oxide on the thermal impedance, Figure 8(b) also includes a simulation of the temperature rise in the device when the buried oxide has been removed. Reducing the thickness of the BOX layer results in lowering the thermal impedance to 18°C/W. This illustrates how the high thermal conductivity of silicon should result in the very low thermal resistances of silicon photonic devices.

4.1.2. 1310 nm Fabry Perot lasers

1310 nm hybrid silicon lasers are also important for many data and telecommunication applications [26]. The epitaxial layer structure used here (Table 2) contains an electron

blocking layer between the quantum wells and the SCH layer for better injection efficiency [27]. The layer is designed to provide a high conduction band offset between the barrier and the SCH layer to prevent electrons from leaking out of the quantum well region while a valence band offset is kept low not to alter the hole flow into the quantum wells.

Lasers with fundamental transverse mode or with second-order transverse mode can be designed and fabricated. Figure 9(a) shows the simulated quantum well confinement factor as a function of silicon waveguide height while keeping the waveguide width and slab thickness at $2.5\,\mu$m and $0.2\,\mu$m, respectively. Quantum well confinement represents the mode overlap to the $4\,\mu$m wide quantum well at the center, where electrons and holes are injected. In the

TABLE 2: III-V epitaxial layer structure with a 1303 nm photoluminescence peak.

Name	Composition	Doping Concentration	Thickness
P contact layer	P-type $In_{0.53}Ga_{0.47}As$	$1 \times 10^{19} \ cm^{-3}$	$0.1 \ \mu m$
Cladding	P-type InP	$1 \times 10^{18} \ cm^{-3}$	$1.5 \ \mu m$
SCH	P-type $Al_{0.4055}Ga_{0.064}In_{0.5305}$ As, 0.9Q	$1 \times 10^{17} \ cm^{-3}$	$0.25 \ \mu m$
Electron blocking layer	$Al_{0.4764}Ga_{0.0189}In_{0.5047}As$	undoped	10 nm
Quantum wells	$Al_{0.055}Ga_{0.292}In_{0.653}As$, 1.0Q(9x)	undoped	10 nm
	$Al_{0.178}Ga_{0.1234}In_{0.0986}As$, 1.5Q(8x)	undoped	7 nm
N layer	N-type InP	$1 \times 10^{18} \ cm^{-3}$	110 nm
Super lattice	N-type $In_{0.85}Ga_{0.15}As_{0.327}P_{0.673}$, 1.1Q(2x)	$1 \times 10^{18} \ cm^{-3}$	7.5 nm
	N-type InP (2x)	$1 \times 10^{18} \ cm^{-3}$	7.5 nm
N bonding layer	N-type InP	$1 \times 10^{18} \ cm^{-3}$	10 nm

(a)

Fundamental mode
Second transverse mode

(a)

Fundamental   Second transverse

$H = 0.7 \ \mu m$
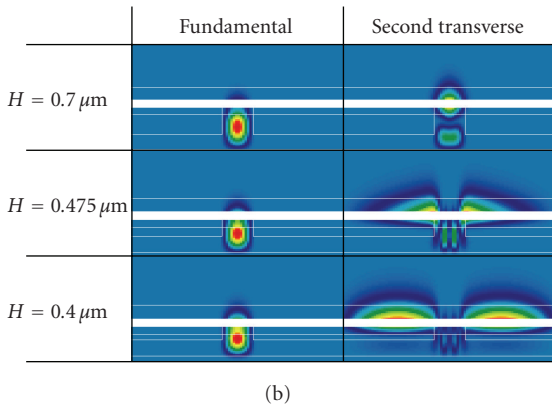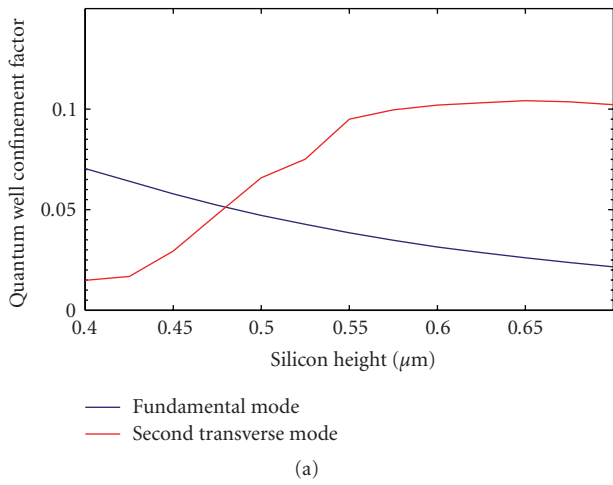
$H = 0.475 \ \mu m$

$H = 0.4 \ \mu m$

(b)

FIGURE 9: The confinement factor in III-V region simulation for different silicon waveguide height (a) confinement factor calculations for the fundamental mode and second transverse mode as a function of waveguide height (b) fundamental and second transverse modes for waveguide heights of 0.7, 0.475, and 0.4 μm. The image aspect ratio (Height:Width) is 4 : 1.

(a)   (b)

(c)   (d)

FIGURE 10: The simulated and measured lasing optical mode profiles (a) simulated optical mode for a waveguide height of 0.4 μm, (b) simulated optical mode for a waveguide height of 0.7 μm, (c) measured optical mode for a waveguide height of 0.4 μm, and (d) measured optical mode for a waveguide height of 0.7 μm.

tall silicon height regime (right hand part in Figure 9(a)), a higher quantum well confinement factor for the second transverse mode exists. In the short silicon height regime (left-hand part in Figure 9(a)), the fundamental mode has a
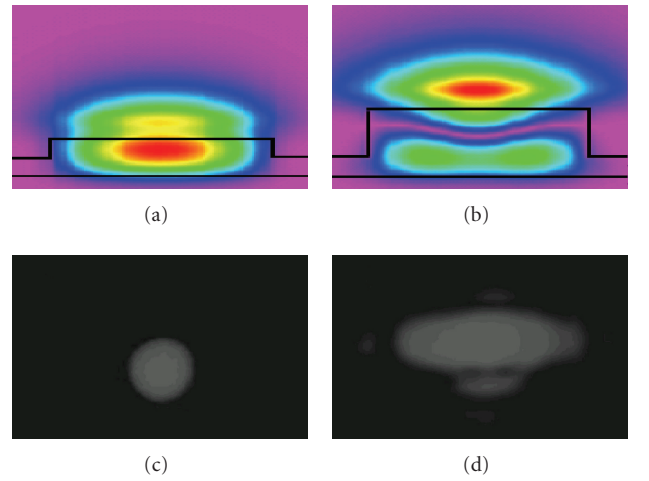
higher quantum well confinement factor. Figure 9(b) shows the fundamental mode and second transverse mode with different waveguide heights illustrating the fundamental mode increasingly lies more in the III-V region as the silicon height decreases. The second transverse mode also undergoes an increase in III-V confinement factor but splits into two lateral lobes at lower silicon heights. This splitting reduces the modal overlap with the 4 μm wide excited quantum well region at the center.

Two different silicon waveguide heights of 0.4 μm and 0.7 μm have been chosen to study the lasing mode selection depending on different quantum well confinement factors. The width and slab height of the silicon waveguide is 2.5 μm and 0.2 μm, respectively. The device length is ~850 μm. Figures 10(a) and 10(b) show the simulated mode profiles with the largest quantum well confinement factor for waveguide heights of 0.4 μm and 0.7 μm, respectively. The measured lasing mode profiles in Figures 10(c) and 10(d) agree with the simulation results, indicating the quantum well confinement
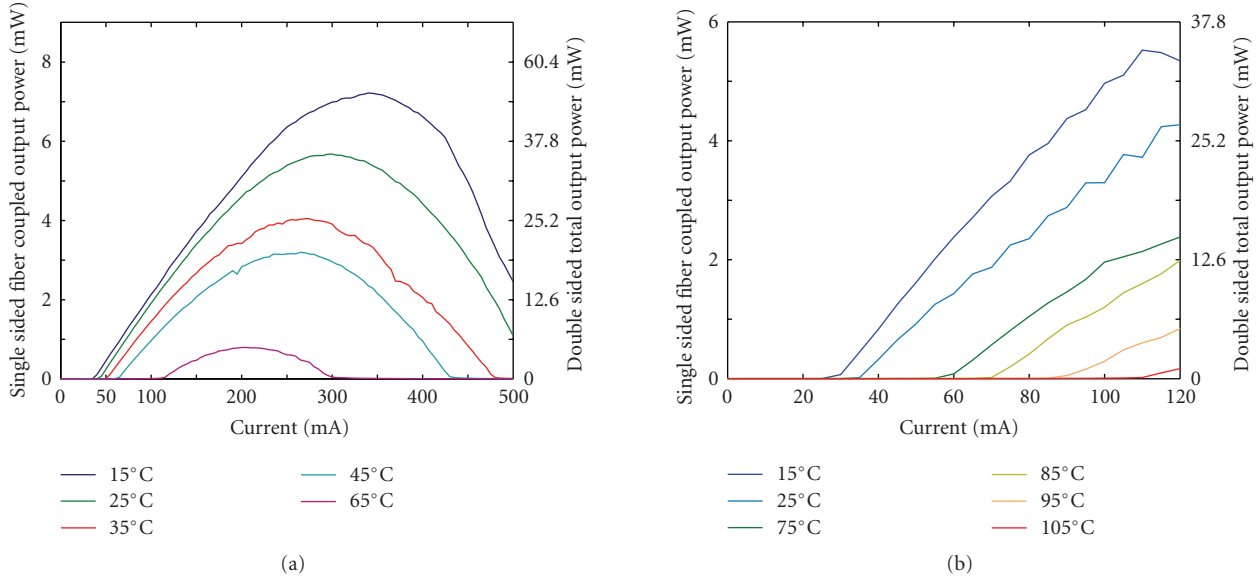
FIGURE 11: LI curves for 1310 nm FP silicon evanescent lasers (a) fundamental mode lasing device, (b) second transverse mode lasing device. The secondary y-axis represents the estimated total laser output power.

factor primarily determines the lasing mode and can be engineered by changing the silicon waveguide dimensions.

Figure 11 shows the measured single-sided fiber-coupled CW output power as a function of the injected current at different temperatures for two different lasers (0.4 μm and 0.7 μm waveguide heights). The threshold current for both devices at 15°C is 30 mA. The output power at 100 mA is 2.9 mW and 5 mW and its corresponding differential quantum efficiency is 2.5% and 8% for the fundamental mode and second transverse mode lasing devices, respectively. The estimated double-sided total output power is shown in the secondary y-axis taking account for the output power from the both facets and a coupling loss of 5 dB between the device and the lensed fiber. The double sided total output power at 100 mA is estimated to be 18 mW and 31 mW, and its total differential quantum efficiency is 15% and 50% for the fundamental mode and second transverse mode lasing devices, respectively. The device lasing with second transverse mode (0.7 μm waveguide height) operates up to 105°C and has better performance than the device lasing with a fundamental mode primarily due to the higher quantum well confinement factor (10% versus 7%). Moreover, the overall performance of 1.3 μm lasers is superior to 1.5 μm lasers previously described because the carrier blocking layer is incorporated and because of the reduced intravalence band absorption and Auger scattering.

4.1.3. 1550 nm integrated racetrack laser and photodetectors

Figure 12(a) shows the layout of an integrated hybrid silicon evanescent racetrack laser and two photodetectors operating at 1550 nm [28]. The same epitaxial structure described in Table 1 is used both for the laser and the detector. This laser

does not rely on facet dicing or polishing and can be tested on-chip with simple probing of the laser and photodetectors.

The waveguide height, width, and rib etch depth were 0.69 μm, 1.5 μm, and 0.5 μm, respectively. The scanning electron microscope (SEM) image of the fabricated devices is shown in Figure 12(b). It consists of a racetrack ring resonator with a straight waveguide length of 700 μm and ring radii of 200 and 100 μm. A directional coupler is formed on the bottom arm by placing a bus waveguide 0.5 micron away from the racetrack. Since clockwise and counterclockwise propagating modes of ring lasers are only weakly coupled, two 440 μm long photodetectors are used to collect the laser power; the clockwise being collected at the left detector, and the counterclockwise being collected at the right detector. These photodetectors have the same waveguide structure as the hybrid laser, and the only difference being that they are reverse biased to collect photogenerated carriers.

To estimate the laser output power from the measured photocurrent, the responsivity of the detector is first measured by dicing and polishing a discrete detector in the same chip and launching laser light into the detector through a lensed fiber. The fiber coupled responsivity was measured to be 0.25 A/W at 1580 nm. Taking into consideration the ∼30% reflection off the waveguide facet and an estimated 5.25 +/− .25 dB coupling loss, the photodetector responsivity is estimated to be in the range of 1.25–1.11 A/W. This corresponds to an internal quantum efficiency of around 92%. A responsivity of 1.25 A/W is used for laser power estimation such that the laser power values are on the conservative side. These measurement results are also consistent with the measured responsivity from stand alone photodetectors [29].

The total laser output power collected at both detectors as a function of current and temperature is shown in Figure 12(c) for a laser with a ring radius of 200 μm and a coupler interaction length of 400 μm. The laser has a total
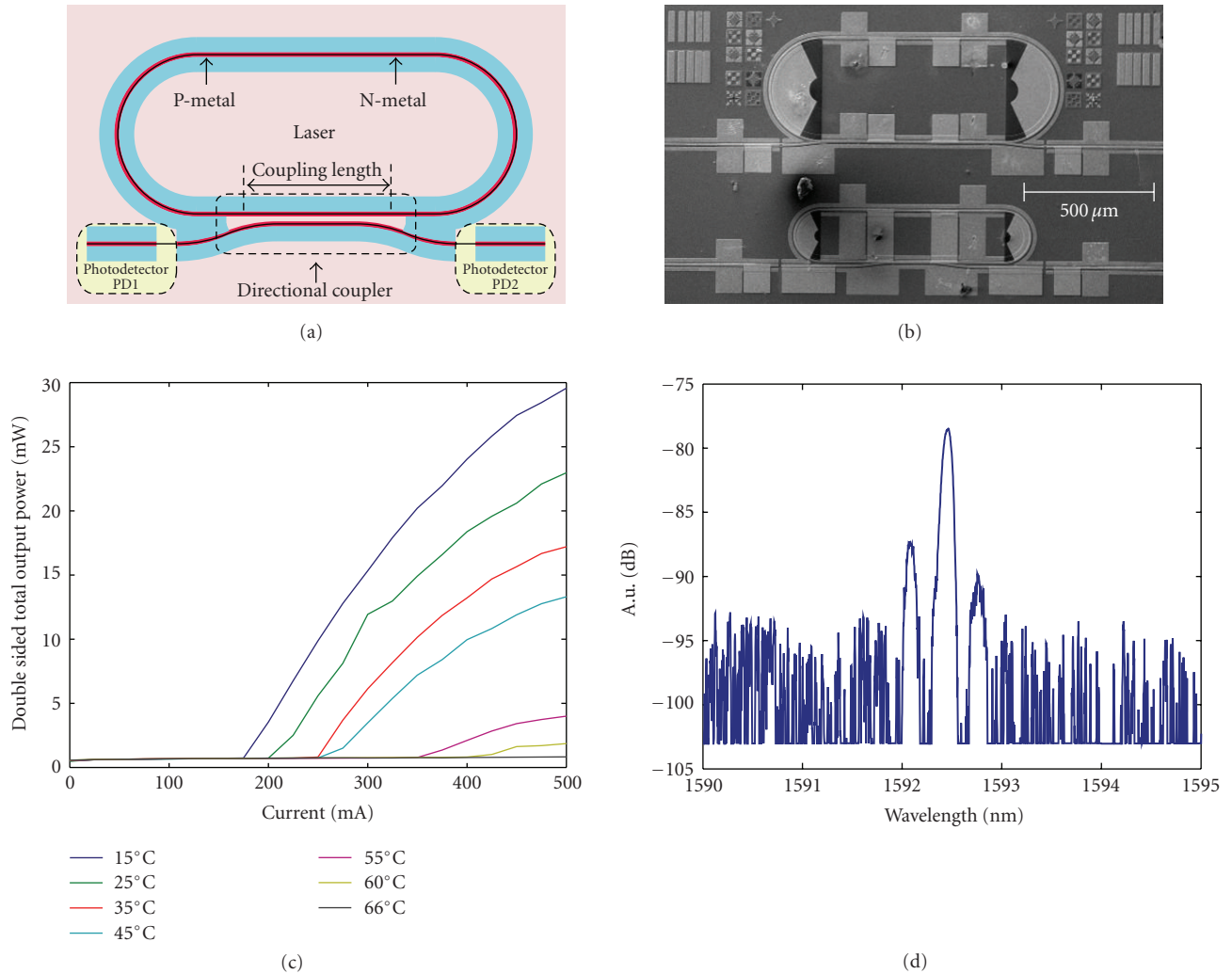
(a)

(b)

(c)

(d)

FIGURE 12: (a) The layout of the racetrack resonator and the photodetectors. (b) A top view SEM micrograph of two racetrack resonator lasers. The racetrack resonator lasers on the top and bottom have radii of 200 and 100 μm, respectively. (c) The LI curve for a laser with a bend radius, R, of 200 μm, and directional coupler coupling length, $L_{\text{interaction}}$, of 400 μm for various temperatures. (d) The spectrum for a laser with $R = 100$ μm and $L_{\text{interaction}} = 400$ μm.

output power of 29 mW with a maximum lasing temperature of 60°C. The differential efficiency is 17% and the laser threshold is 175 mA at 15°C. The laser spectrum is shown in Figure 12(d) with its lasing peak in the range of 1592.5 nm.

Since the two modes of propagation are not coupled and are degenerate, mode competition is typical in such lasers with a ring cavity structure. Figure 13(a) shows the photocurrent measured separately from the left (PD1) and the right (PD2) detectors as a function of the laser drive current for a laser with a ring radius of 100 μm and a coupler interaction length of 100 μm. There are two distinct regions of operation above threshold: (1) unidirectional bistable (low-bias current), and (2) alternating oscillation (high-bias current). In the unidirectional bistable region, the laser is lasing in either one direction or the other and the laser output switches from one direction to the other direction as the laser diode current increase. At higher bias (>360 mA), the laser enter the alternating oscillation region, the output power

exhibit oscillatory behavior. The unidirectional bistability of the racetrack laser can be alleviated if one of the detectors is forward biased to inject light into the cavity (Figure 13(b)). The forward-biased photodetector acts as an ASE source, which increases the photon density of the clockwise mode, leading to greater simulated emission and mode selection. This shows that the lasing direction can be controlled by forward biasing one of the photodiodes; that is, lasing either clockwise or counterclockwise.

4.1.4. 1550 nm mode locked lasers

Silicon hybrid lasers can be mode locked at a variety of frequencies from 10 GHz to 40 GHz [30], for potential applications in optical pulse generation, OTDM, WDM, and regenerative all-optical clock recovery [31].

An FP ML-SEL is shown in Figure 14(a) and its test setup is shown in Figure 14(b). The 39.4 GHz FP ML-SEL had
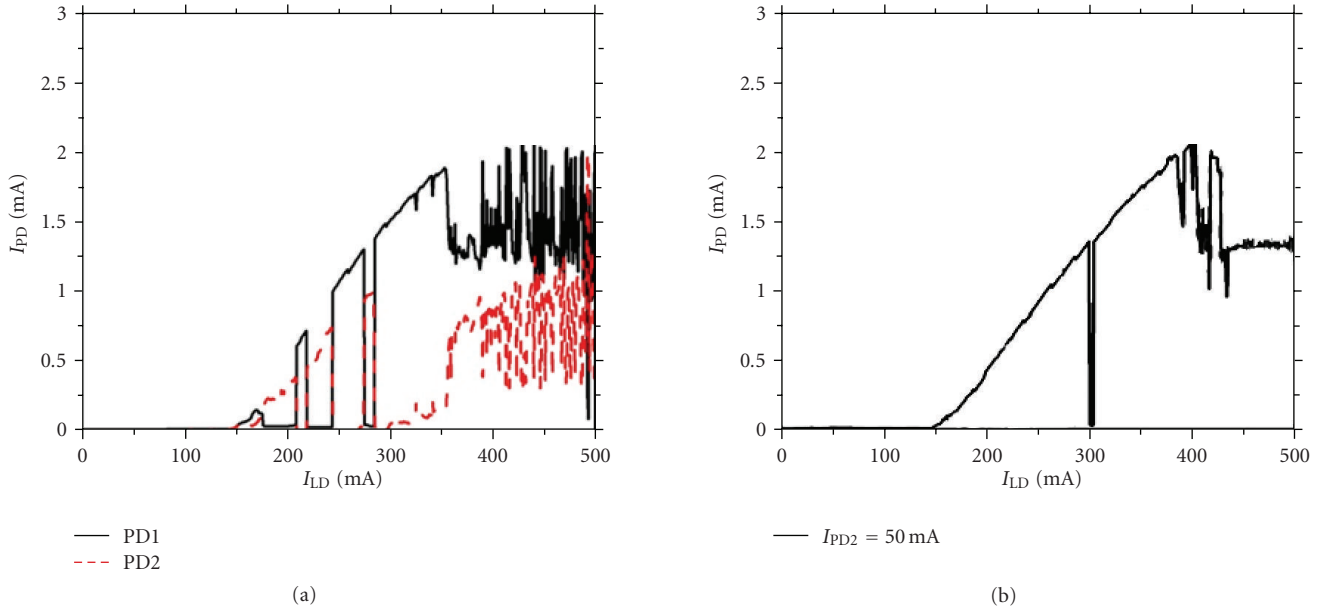
Figure 13: (a) L-I curves of CW and CCW direction, (b) L-I curve of CW direction when the PD2 is forward bias with 50 mA.

a total cavity length of 1060 μm and a saturable absorber (SA) length of 70 μm. For all devices presented here, separate gain and SA sections were electrically isolated using proton implantation. Passive mode locking was achieved for a range of gain currents between 195 mA and 245 mA with similar output characteristics. For a gain current of 206 mA and a saturable absorber reverse bias voltage of 0.4 V, the pulse has a sech^2 shape with 4.2 picoseconds full width at half maximum (FWHM) pulsewidth, extinction ratio (ER) over 18 dB between the peak and null, peak power of 4.5 dBm in fiber, and FWHM optical spectral width of 0.9 nm. The time bandwidth product is 0.4, close to the transform limited value of 0.32 for sech^2 pulses, indicating minimal chirp. The laser was capable of stable mode locking for a range of gain currents between 195 mA and 245 mA with similar output characteristics.

By applying an RF signal to the saturable absorber section, hybrid mode locking occurs and the jitter of the pulses can be considerably reduced [32] without changing the pulsewidth or spectral width. To achieve subharmonic hybrid mode locking, a 20 GHz RF source with 17 dBm of RF input power is used. For these conditions, the absolute jitter of this laser is 1 picosecond and the locking range was 5 MHz. For all measurements in this paper, the jitter was evaluated by integrating two times the single-sideband noise from 1 kHz to 100 MHz offset from the carrier frequency.

Increasing the cavity length to 4.16 mm resulted in 10 GHz mode locking. The saturable absorber was 80 μm long and the cavity was divided into 4 equal length gain sections that can be biased differently depending on the application. The bias conditions used for pulse generation were as follows: Gain 1 and Gain 2 (adjacent to the saturable absorber) were biased together at 531 mA, Gain 3 was biased at 140 mA, Gain 4 at 149 mA, and the SA was biased with
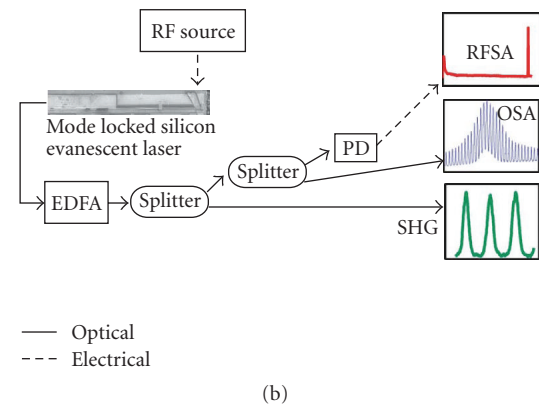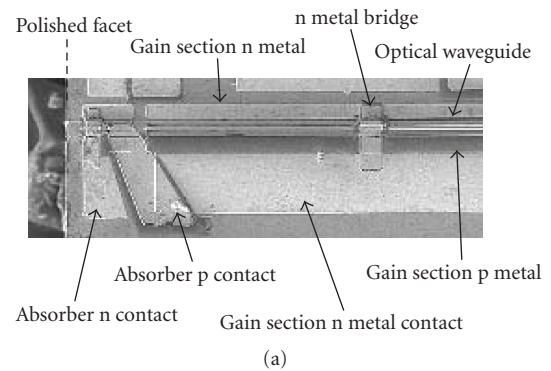

Figure 14: (a) Scanning electron micrograph of one end of an FP ML-SEL. (b) Schematic of the general experimental setup. For some measurements, more components were required as detailed in the references. EDFA = erbium doped fiber amplifier, SHG = second harmonic generation autocorrelator, OSA = optical spectrum analyzer, RFSA = 41 GHz radio frequency spectrum analyzer, PD = 40 GHz photodetector.
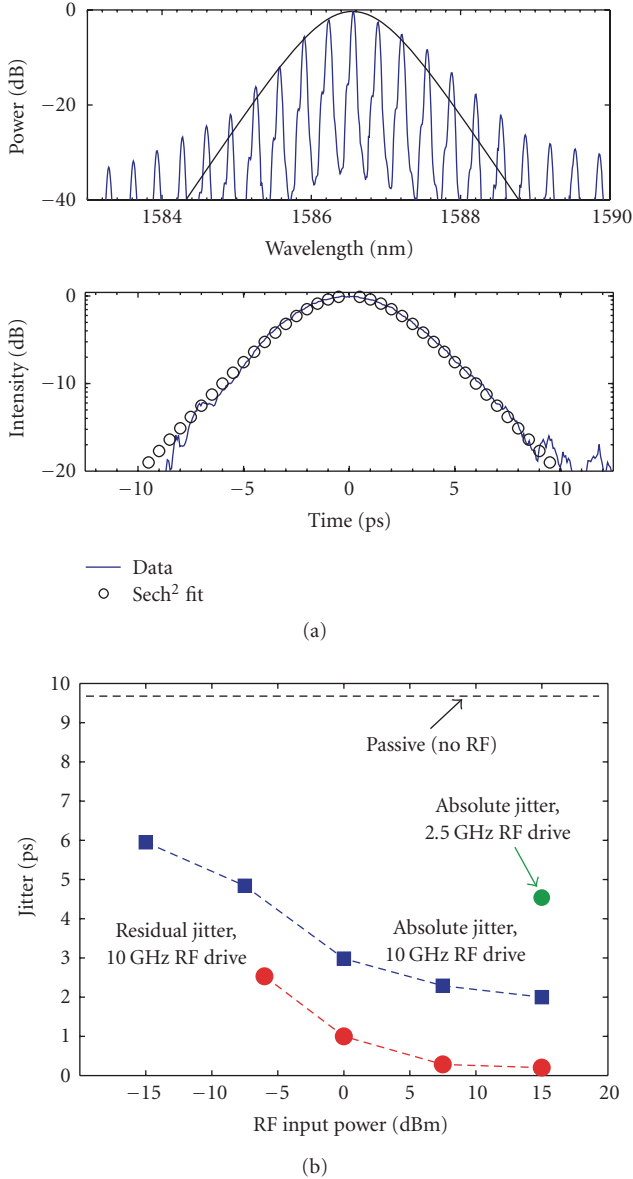
FIGURE 15: (a) Wavelength spectrum and autocorrelation trace of the 40 GHz FP ML-SEL output. The fit to the optical spectrum is the Fourier transform of the autocorrelation fit. (b) Jitter measurements for the 10 GHz FP ML-SEL versus the RF input power.

−2.3 V. The FWHM pulsewidth was 3.9 picoseconds with a sech^2 shape, the ER is over 18 dB, the peak power in fiber was 11.9 dBm, and the FWHM spectral width was 3.8 nm, containing 45 modes evenly spaced at 10.16 GHz. The time bandwidth product is 1.7, indicating significant chirping. Chirp can be reduced in future designs by incorporating passive silicon waveguide sections in the laser cavity with a shorter gain section [33]. This is fairly easy to do on this platform and is a potential advantage of the platform for lower repetition rate mode-locked lasers. Changing the SA bias between −0.5 and −2 V changes the output pulsewidth between 9 and 4 picoseconds, while the ER and output power

do not change significantly. Figure 15(b) shows results for passive and hybrid mode locking with different RF powers and RF injection frequencies. Also shown is the residual jitter, which is the jitter of the hybrid mode locked laser compared to that of the RF drive source. The minimum residual jitter is 199 femtoseconds with 15 dBm RF drive at 10.16 GHz. At this RF power, the locking range was 260 MHz.

Increasing the combined gain section bias currents to a total of 1 A generates over 100 optical modes with power levels within 10 dB of the peak mode power. If the modes have high enough quality, the single ML-SEL could be combined with an AWG and used as a multiple wavelength source for wavelength division multiplexing applications [34]. Across 100 modes, the linewidth was below 500 MHz and the OSNR was near 15 dB. The linewidths of these modes are too large for some applications, but for short reach applications the signal quality is sufficient. The mode quality can be improved by injecting a stable CW laser into the hybrid mode-locked laser, inducing optical injection locking [34]. In this case, the spectral width narrows to 30 modes within 10 dB, but the linewidth of each of these modes is reduced to that of the injected signal (<100 kHz). Also the OSNR is improved to over 25 dB for the majority of the modes. It is expected that better stabilization of the hybrid mode-locked laser through packaging would allow for a wider spectral width under optical injection locking, allowing for more high-quality modes to be generated.

A 30.4 GHz racetrack ML-SEL [31] is shown in Figure 16(a). A racetrack mode-locked laser has the advantage that its cavity is defined by lithography. Since the repetition rate is determined by the cavity length, this allows for the repetition rate to be precisely determined and repeated across different devices. Racetrack lasers can also be integrated monolithically with other components. This laser has a cavity length of 2.6 mm, an absorber length of 50 μm, and 2 separate gain sections. The gain sections were biased together at 410 mA and the absorber was biased with −0.66 V. This resulted in Gaussian-shaped output pulses with 7.1 picoseconds FWHM pulsewidth, 0.5 nm FWHM spectral width, and approximately 10 dB ER. The time bandwidth product was 0.43. The peak power was 6.8 dBm onchip, determined from onchip photocurrent measurements.

With a 30.4 GHz, 13 dBm RF signal applied to the SA section, this laser had 364 femtoseconds of absolute jitter and 50 MHz locking range. The laser could also be synchronized to 30 Gbps optical input signals with average powers below 0 dBm in the input waveguide meaning that it can perform all-optical clock recovery. To test this application, we intentionally degraded a 30.4 Gbps return to zero 2^{31}-1 pseudorandom bit stream by adding timing jitter and reducing the extinction ratio, and we used the racetrack ML-SEL to recover the clock all-optically [31]. The input ER was 3.8 dB and the input jitter was 14 picoseconds. The recovered clock had an ER of 10.4 dB and jitter of 1.7 picoseconds. The input data and output clock eye diagrams are shown in Figure 16(b). The device's extreme regenerative capabilities and potential for integration with other components indicate that it could be used as part of a silicon integrated optical 3R regenerator.
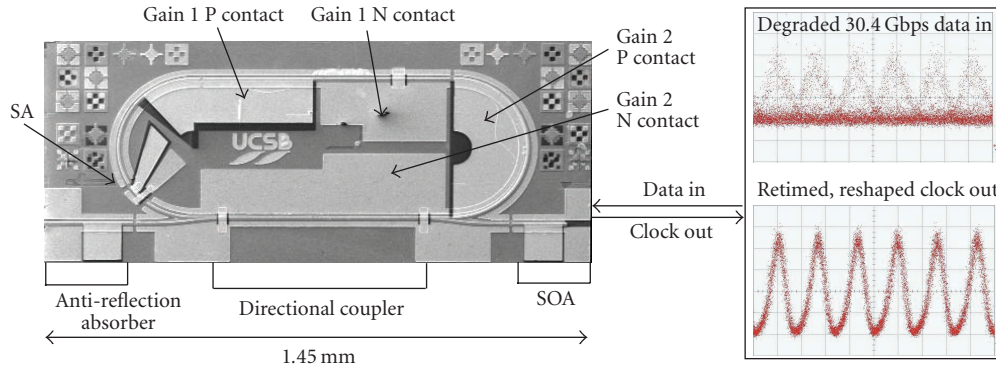
FIGURE 16: (a) SEM image of the 30.4 GHz racetrack ML-SEL. (b) Eye diagrams of the input data sent to the device and the regenerated, all-optically recovered clock.
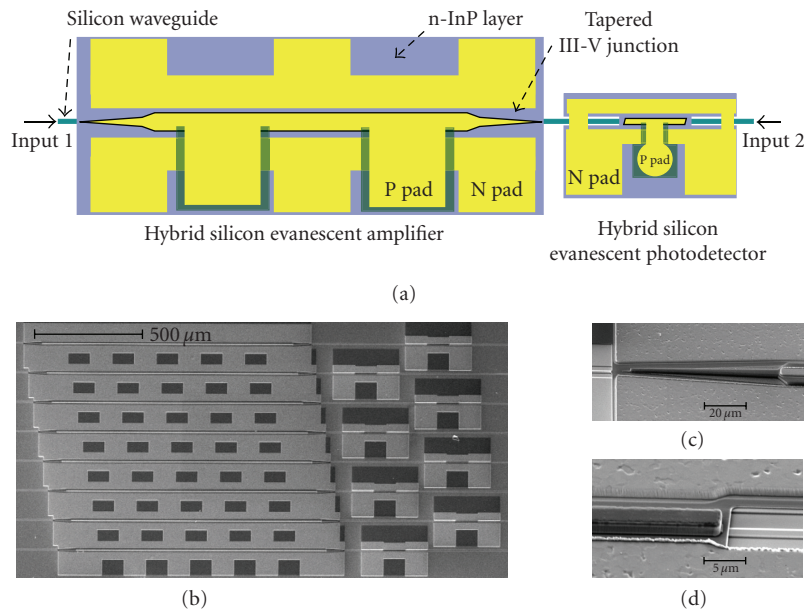

FIGURE 17: (a) Top view of the integrated device. (b) SEM image of eight fabricated devices. (c) Close view of the III-V taper of the amplifier. (d) Close view of the narrow III-V mesa of the detector.

4.2. Silicon evanescent amplifiers and photodetectors

Optical amplifiers are key components in realizing high levels of photonic integration as they compensate for optical losses from individual photonic elements. The hybrid silicon evanescent amplifier structure is similar to the offset quantum well structure which has typical quantum well confinement factor in the range of 2% to 4% and it is suitable for preamplifiers [35]. In this section, the integration of an amplifier and a detector for improved receiver sensitivity is discussed [36].

Figure 17(a) shows a device structure of the integrated device with an amplifier and a detector. At the transition between the passive silicon waveguide and the hybrid waveguide of the amplifier, the width of the III-V mesa is tapered from $0\,\mu$m to $4\,\mu$m over a length of $70\,\mu$m to increase the coupling efficiency and to minimize reflection. The width from $4\,\mu$m to $14\,\mu$m is tapered more abruptly over $5\,\mu$m

since III-V mesas wider than $4\,\mu$m do not laterally affect the optical mode. A 7° tilted abrupt junction is used between the passive silicon waveguide and the detector hybrid waveguide. The details of the epitaxial structure of the III-V layers are summarized in Table 1. The III-V mesa width of the amplifier is $14\,\mu$m. The III-V mesa width of the detector is $3\,\mu$m at the p cladding layer and $2\,\mu$m at the p SCH and the quantum well layers to reduce the capacitance of the device. The detector p and n pads are designed to be $100\,\mu$m apart from center to center to use a standard GSG RF probe for high-speed testing. The SEM image of the eight fabricated devices is shown in Figure 17(b), and the close view of the III-V amplifier taper and the III-V detector mesa are shown in Figures 17(c) and 17(d) respectively. The total length of the amplifier and the detector is 1.24 mm and $100\,\mu$m, respectively.

The internal quantum efficiency is measured to be around 50% at a reverse bias voltage of 2 V at 1550 nm as
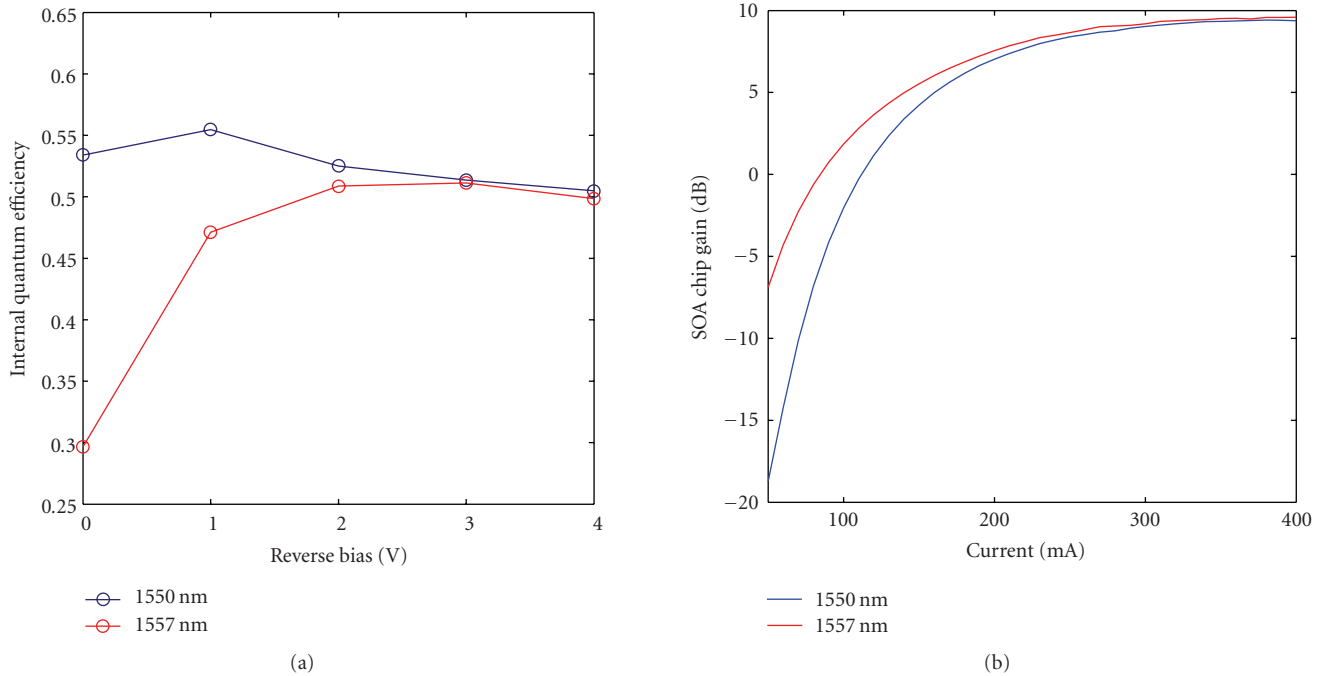
FIGURE 18: (a) Internal quantum efficiency of the detector. (b) Gain of the amplifier.
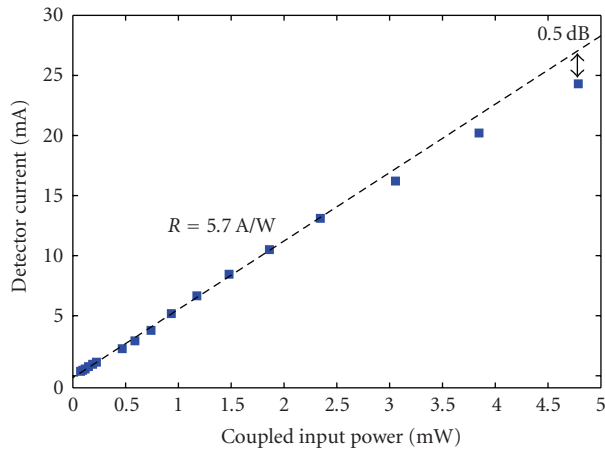

FIGURE 19: Saturation characteristics of the integrated optically preamplified receiver.

FIGURE 20: Optically preamplified receiver bit error rate curves measured with 2^{31}-1 NRZ 2.5 Gbps transmissions with different amplifier gains.

shown in Figure 18(a). The amplifier gain is also measured by taking photocurrent from the detector and the maximum gain is 9.5 dB at 300 mA as shown in Figure 18(b). The reflection from the III-V taper is estimated from the ripples at the ASE spectrum and it is less than 5×10^{-4}. The taper loss is estimated to be in the range of 0.6 dB to 1.2 dB by measuring the photocurrent from the reverse-biased amplifier [36]. Figure 19 shows the saturation characteristics of the integrated device. The overall responsivity is 5.7 A/W and the device is saturated by 0.5 dB at an output photocurrent of 25 mA. The device bandwidth is measured to be 3 GHz from the time domain impulse measurements even though the estimated RC limited bandwidth is 7.5 GHz.
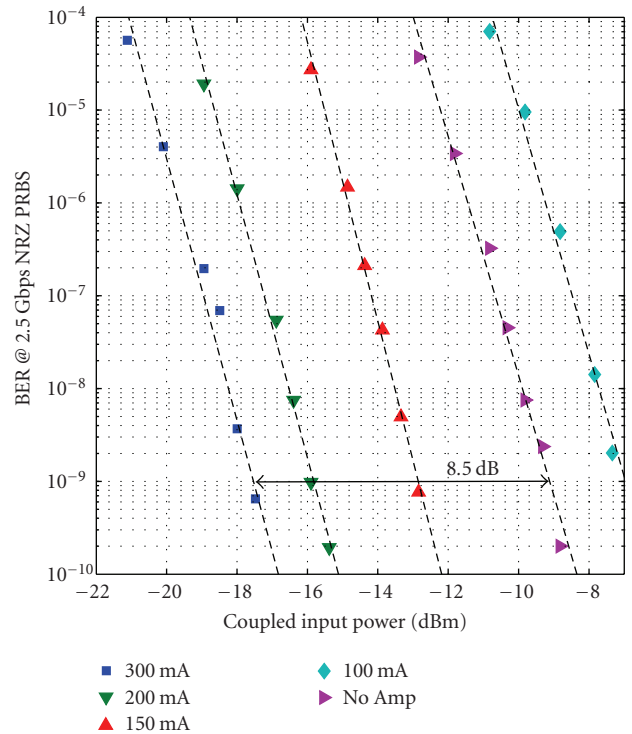
The current bandwidth is limited by carrier trapping in the quantum wells. Higher bandwidth can be achieved by incorporating a thinner SCH layer and a bulk absorbing
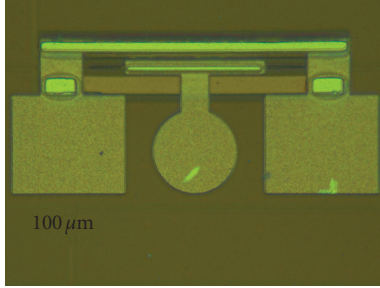
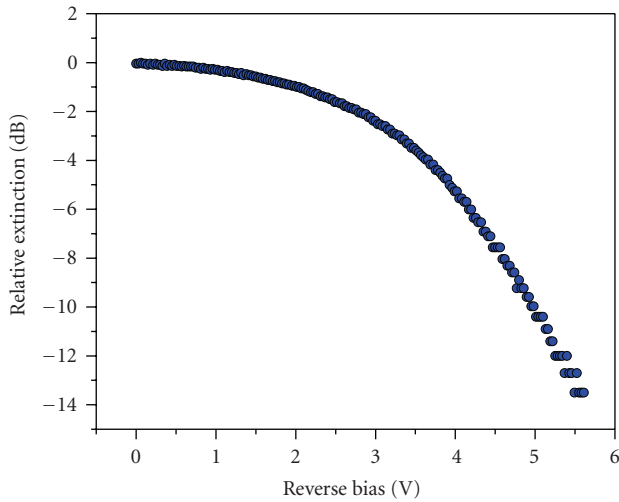FIGURE 21: Photograph of the fabricated EAM modulator.

FIGURE 22: EAM extinction versus bias.

FIGURE 23: Measured small signal response (solid). Calculated response using an RC model (dashed line).

region or new quantum wells with small valence band offset. The bit error rate (BER) was measured with 2.5 Gbps NRZ 2^{31}-1 pseudorandom bit sequence (PRBS) with different amplifier gains and the result is shown in Figure 20. The purple data points are baseline measurements without the amplification by launching the signal to input 2. The BER data at an amplifier current of 100 mA shows worse receiver sensitivity than the receiver sensitivity without amplification (baseline) because the amplifier is below transparency. Once the amplifier is driven beyond transparency, the power penalty becomes negative as shown in the three BER curves on the left side. At the maximum gain of 9.5 dB, the power penalty is −8.5 dB compared to the baseline and the receiver sensitivity at a BER of 10^{-9} is −17.5 dBm. The 1 dB difference between the gain and the measured power penalty is due to the ASE noise. Better sensitivities would be achievable with a good transimpedance amplifier and this device can be integrated with silicon passive wavelength demultiplexers for high-speed WDM receivers [37].

4.3. Silicon evanescent electroabsorption modulators

In this section, we review hybrid silicon evanescent electroabsorption modulators (EAMs). The modulator structure described here can be integrated with lasers, amplifiers, and photodetectors using quantum well intermixing [38]
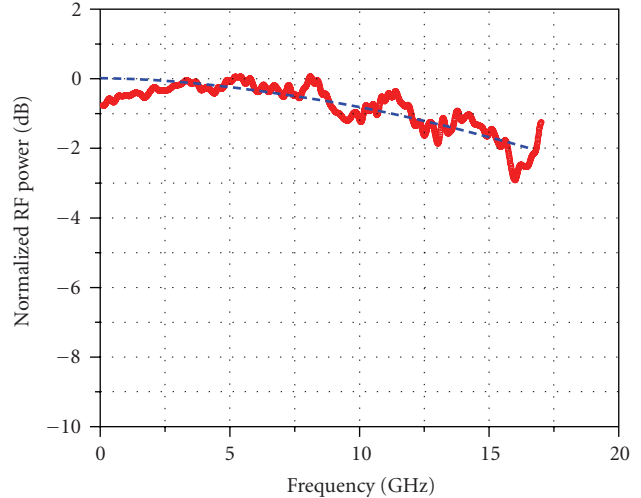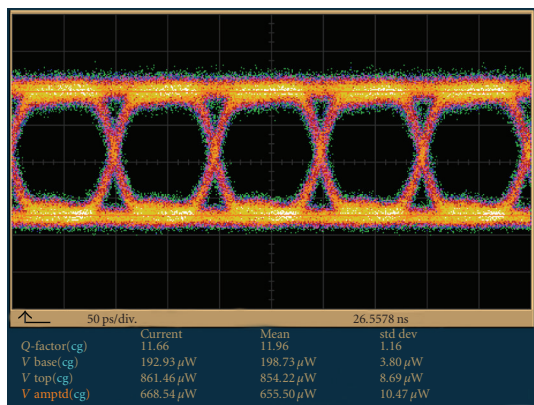
enabling integrated high-speed transmitters. The cross-sectional structure is shown in Figure 1(b) and the III-V epitaxial structure with photoluminescence at 1478 nm is summarized in Table 3. AlGaInAs is chosen as the multiple quantum well material because typically it has a large conduction band offset which provides a stronger carrier confinement and produces strong quantum confined Stark effect with higher extinction ratio [39, 40]. The silicon waveguide was fabricated with a height of 0.5 μm and a slab thickness of 0.3 μm. The silicon waveguide has a width of 1.5 μm for passive segments and is tapered to 0.8 μm in the hybrid modulator region for a larger quantum well confinement factor. The width of the III-V mesa is 4 μm at the top InP cladding layer and 2 μm at the SCH and quantum well layers to reduce the capacitance of the device [40, 41]. The overall layout of the device is the same as the detector describe in the previous section except for the width of the III-V mesa is tapered from 0 to 2 μm over a length of 60 μm to increase the coupling efficiency and to minimize reflection as in the amplifiers. The hybrid EAM has a total length around 220 μm with 100 μm absorber and two 60 μm long tapers. The photograph of the fabricated device is shown in Figure 21.

Figure 22 shows the relative extinction at wavelength of 1550 nm under various reverse biases. More than 10 dB extinction can be achieved with a reverse bias voltage of 5 V. The device has a series resistance around 30 Ω and capacitance of 0.1 pF measured from the impedance measurements resulting in a RC limited bandwidth of ~20 GHz. It matches with the measured small signal modulation response as shown in Figure 22.
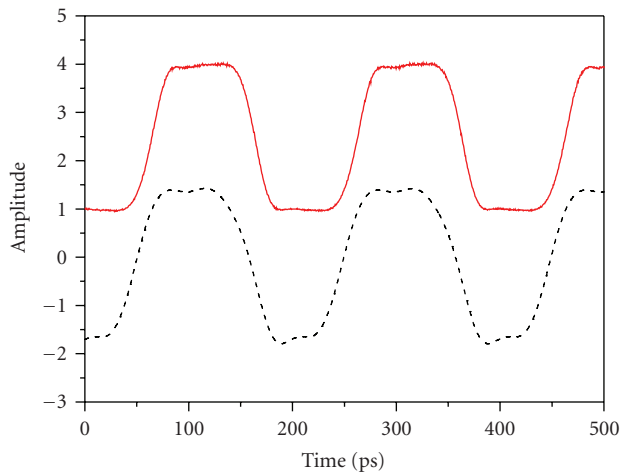
To investigate the performance of large signal modulation, the modulator is driven with a 2^{31}-1 pseudorandom bit sequence (PRBS). The device is biased at −3 V with a peak-to-peak drive voltage of 3.2 V. The modulated light is collected with a lensed fiber and amplified with an EDFA. Figure 24(a) shows eye diagrams measured at nonreturn-to-zero (NRZ) 10 Gbps. The 10 Gbps signal has an extinction

Table 3: III-V epitaxial layer structure with a 1478 nm photoluminescence peak.

Name	Composition	Doping concentration	Thickness
P contact layer	P-type $In_{0.53}Ga_{0.47}As$	1×10^{19} cm^{-3}	0.1 μm
Cladding	P-type InP	1×10^{18} cm^{-3}	1.5 μm
SCH	P-type $Al_{0.160}Ga_{0.320}In_{0.520}As$, 1.3Q	1×10^{17} cm^{-3}	0.15 μm
Quantum wells	$Al_{0200}Ga_{0.330}In_{0.470}As$, 1.19Q(11x)	Undoped	7 nm
	$Al_{0.080}Ga_{0.330}In_{0.590}As$, 1.55Q(10x)	Undoped	11 nm
SCH	$Al_{0.160}Ga_{0.320}In_{0.520}As$, 1.3Q	Undoped	0.1 μm
N layer	N-type InP	1×10^{18} cm^{-3}	110 nm
Super lattice	N-type $In_{0.85}Ga_{0.15}As_{0.327}P_{0.673}$, 1.1Q(2x)	1×10^{18} cm^{-3}	7.5 nm
	N-type InP (2x)	1×10^{18} cm^{-3}	7.5 nm
N bonding layer	N-type InP	1×10^{18} cm^{-3}	10 nm

(a)

(b)

Figure 24: (a) Measured 10G NRZ eye diagrams; (b) pulse train of drive signal (dashed) and optical modulated signal (solid). The drive signal has rise/fall time around 35 picosesonds. The modulated signal shows rising/falling times of about 27 picseconds.

ratio of 6.3 dB, which is slightly lower than the DC extinction due to additional microwave voltage drop at cladding and ohmic contacts. The eye is clearly open with quality factor (Q factor) close to 12. The rise and fall times of the signal are about 27 picoseconds, which is, as expected, faster than the driving signal as shown in Figure 24(b).

5. CONCLUSION

Recent progress of hybrid silicon evanescent devices has been reviewed in this paper. Discrete lasers, amplifiers, photodetectors, and electroabsorption modulators have been demonstrated. Racetrack lasers integrated with photodetectors, mode locked lasers, and photodetectors with preamplifiers have also been presented as examples of photonic integration with this hybrid device structure. These demonstrations show the potential for realizing active functionality on the silicon photonics platform. One of the important paths of this research is improving performance of individual devices, that is, device efficiency and thermal performance, in conjunction with studies on device reliability. Another path is the development of bonding of III-V materials to large size silicon wafers (>6 inch). The bonding process can be wafer scale or can be used for die attach. The optimum size of III-V material to use depends on the density of active devices required for the silicon wafer [42]. The hybrid silicon evanescent device platform provides a unique way to build photonic active devices on silicon, and those studies will expedite the applications of silicon photonic integrated circuits in optical telecommunications and optical interconnects.
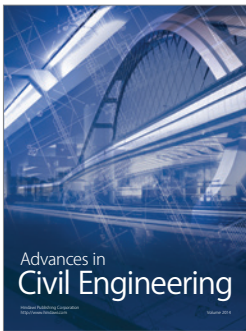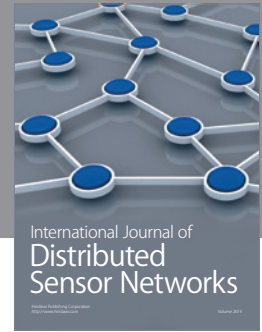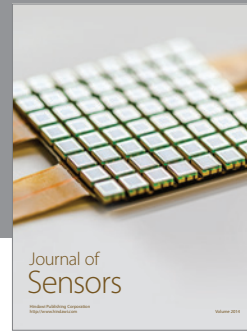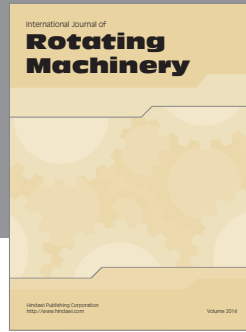
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