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Research Article

Analysis and Design of Transformer-Based mm-Wave Transmit/Receive Switches

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Transformer-based shunt single pole, double-throw (SPDT) switches are analyzed, and design equations are provided. A mm-wave transformer-based SPDT shunt switch prototype was designed and fabricated in 90 nm digital CMOS process. It has a minimum insertion loss of 3.4 dB at 50 GHz from the single pole to the ON-thru port and a leakage of 19 dB from the single pole to the OFF-thru port. The isolation is 13.7 dB between the two thru ports. Large signal measurements verify that the switch is capable of handling +14 dBm of input power at its 1 dB compression point. The fabricated SPDT switch has a minute active area size of $60\,\mu\text{m} \times 60\,\mu\text{m}$.

1. Introduction

Transmit/receives switches implemented in standard CMOS technologies are key mm-wave building blocks for demonstrating the ultimate goal of a mm-wave single chip solution. Previous works [1–5] have demonstrated the feasibility of many key mm-wave transceiver building blocks in standard digital CMOS processes. Operating at mm-wave frequencies has many advantages. One key advantage is due to small wavelengths, which allows antennas to be realized on chip or on the package, further reducing the cost of a system. Moreover, many antennas could be integrated with suitable phase shifters to create phased array systems that effectively increase the aperture size and directivity of transmit/receive antennas by a factor of N (number of antennas). Spatial filtering achieved by a phased antenna array system alleviates impairments such as delay spread and cochannel interference and further helps to extend the communication range and bandwidth. Without a transmit/receive (T/R) switch, two separate antennas should be employed for the receiver, and transmitter, which translates to half the transmit/receive antenna gain and aperture size for a given area. T/R switches with sufficient performance can allow a single antenna to be shared between the transmitter and receiver and thereby twice the number of antennas (antenna array gain) will be realizable out of the same die area. Hence T/R switches can save a great deal of area, and thus lower the total system cost, since antennas are relatively large, especially if implemented on chip. Therefore, designing CMOS T/R switches at mm-wave frequencies is an important goal toward the realization of a low-cost mm-wave system.

2. Antenna Array Reuse via T/R Switching

At mm-wave frequencies, antennas can be realized in the package or on chip due to the relatively small wavelength. Higher performance is realized from package antennas due to the smaller conductive and dielectric losses compared to a silicon substrate. Multilayer boards with high-quality metallization not only provide good design environments for the antenna array but they can also be employed to route signal, power, and ground lines and furthermore act as a heat sink to take the dissipated power off the chip.

Even when antennas are implemented on a package, having a smaller package makes the over-all solution more cost-effective and allows for easier adoption of the solution by WPAN applications such as smart phones and portable media players. But whenever the package size is a secondary

issue, then removing T/R switches should result in a better overall performance, since there is no extra component after the PA to harm the TX linearity and output power nor is there a component before the LNA which degrades the receiver noise figure and consequently sensitivity. However in practical cases, for solutions without the T/R switch, the bigger size of the package means longer on-package routings to connect front ends residing on the chip to the antennas implemented on the package (Figure 1). The routing loss is as important as the T/R switch loss, since it directly affects the transmit power and receive sensitivity. Depending on the array size and on-package transmission line loss characteristics, the resultant routing loss can offset the benefit of not including a T/R switch.

To have a quantitative comparison, we consider the scenarios described in Figure 1. In Figure 1(b), one antenna array is shared between TX and RX via T/R switches (where each switch incorporates 3 dB of insertion loss), and in Figure 1(c) two separate arrays are used for RX and TX portions of the transceiver. To compare these two scenarios, we compare the maximum communication range achievable by each case while assuming nominal values of transmitter $P_{\text{out}} = 10\,\text{dBm}$, receiver NF $= 10\,\text{dB}$ and a required SNR of 10 dB, for maintaining the communication link at the frequency band of 57–64 GHz.

As can be seen from Figure 2, for larger arrays (a 100 element array in this case) transmission line routing loss is more pronounced and unless very low loss routing is realizable on package, including the T/R switch will provide better overall performance. For smaller arrays (16 antenna elements in Figure 2) more routing loss is tolerable. However, for ultimate single-chip solutions where the antenna array is realized on chip, due to higher on-chip routing losses (~1 dB/mm), a solution with a shared array between TX and RX through a T/R switch looks more promising.

3. T/R Switching Configurations

3.1. Series versus Shunt Switching. By its nature, when the gate terminal of a MOS transistor is driven by a rail-to-rail voltage, it acts as a switch. In fact, this single transistor switch is sufficient for many digital and analog applications. When the switch is on, the transistor is in the triode region and a low resistive channel connects the MOS source and drain terminals. To the first order, the on resistance of a MOS switch (R_{ON}) is equal to $1/g_m$, where the transconductance is calculated at the edge of saturation. When the switch is off, there is no conducting channel between the source and drain terminals, and the resistive path that connects the source and drain nodes of the transistor exhibits a very large R_{OFF}. However, in the off mode there is a feedthrough path through parasitic capacitors between source and drain terminals. This path is through both C_{gd}-C_{gs} and C_{db}-C_{sb} networks. At low frequencies, when the transistor is operating at frequencies much lower than its f_t, the capacitive feedthrough path introduces a much higher off-mode reactance than the resistance of the channel in the on mode. But at mm-wave frequencies, when the device is operating close to the f_t limit, the impedance of the switch in the off state is comparable to when it is on. Figure 3 depicts the measured S_{21} of a 40 μm NMOS transistor acting as a switch in a 50 Ω environment. As can be seen in this figure, S_{21} for on and off states at 60 GHz is comparable.

There are techniques to diminish the feedthrough path by cascading multiple switches (decreasing the effective series capacitance) and adding a shunt switch in between two series switches with an inverted gate signal with respect to the series switches (shorting out the feedthrough signal). These techniques (Figures 4(a) and 4(b)) are mostly applicable to lower RF frequency systems, since at mm-wave frequencies having multiple transistors in the signal path introduces substantial insertion loss. Switches cannot be made too large due to parasitic capacitance limitations. In mm-wave regime, a switching structure with the least number of transistors is desirable to reduce parasitics. Furthermore, any transistors in series with the signal path can incur a noticeable loss, and a structure that removes series transistors is more suitable. This is the reason that in [6] an L-configuration with corresponding matching networks as depicted in Figure 4(c) is exploited with only one series transistor and two transistors in shunt with the signal path. An ultimate shunt SPDT switch at mm-wave frequencies has the capability to provide lower losses due to the elimination of transistors in series with the signal path.

The shunt SPDT switch configuration is demonstrated in Figure 5. Traditionally shunt switches were realized with two quarter-wave transmission line sections (Figure 5(a)) and shunt switches at each end. When a switch is closed, the corresponding thru port is grounded, and all the incident power reflects with negligible amount coupling through. The $\lambda/4$ line converts this low impedance of the short from the off-thru port to a high impedance (open circuit) at the common input port which results in directing all the input power toward the on port. The impedance of the on-port load is matched to the quarter-wave line characteristic impedance which is in turn matched to the input impedance. The off-state switch at the on-thru port has a very high shunt loading resistance and its parasitic capacitance is absorbed into the quarter wavelength transmission line design.

Even at mm-wave frequencies, $\lambda/4$ lines are rather bulky and occupy too much area to be implemented on chip. Absorption of parasitic capacitances added by the interfacing building blocks helps to reduce the transmission line size. The other approach to reduce the footprint of a transmission line is employing slow-wave structures by placing floating metal filaments underneath the line [12]. These filaments act as a shield preventing electric fields from penetrating down to the substrate and by confining the electric field to a small volume just underneath the transmission line, they increase the effective per unit length capacitance of the line, and as a result of that the wavenumber ($\beta = \omega\sqrt{LC}$) is increased at the price of having lower characteristic impedance ($Z_0 = \sqrt{L/C}$) which in turn requires higher power consumptions for interfacing blocks that drive such lines. Slow-wave techniques can enhance the capacitance of the line by up to four times which means that the length of the line can be halved for further area savings [13].

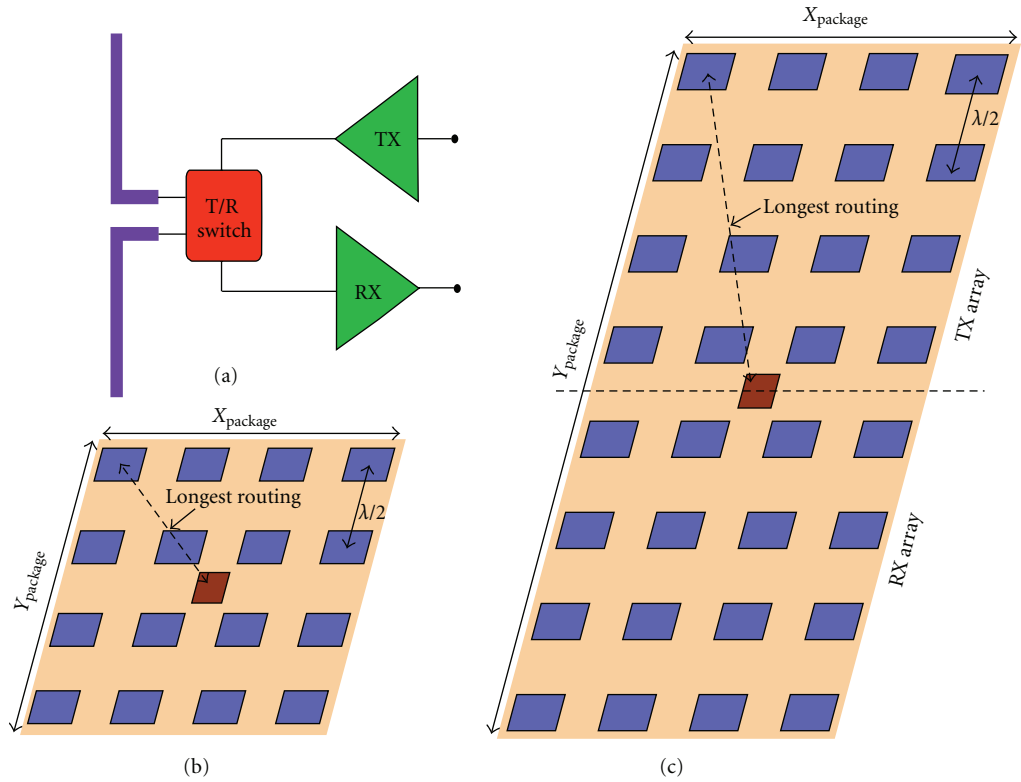


Figure 1: A T/R switch building block in a transceiver architecture (a). An antenna array which employs T/R switches (b) has half the footprint of the one without T/R switches (c).

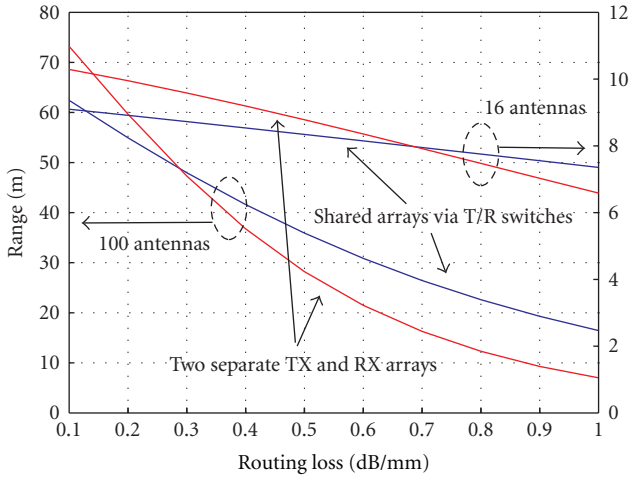


Figure 2: Graph of the maximum achievable communication range in two configurations of shared or separate arrays (for both small and large arrays). For larger arrays, the routing loss is more detrimental than the T/R switch loss and higher quality packaging should be employed (T/R switches were assumed to have 3 dB of insertion losses).

Even after absorbing the capacitance of the interfacing blocks and utilizing slow-wave techniques to reduce the transmission line footprint, they are still bulky and devising a lumped component counterpart for the shunt SPDT switch is highly valuable. In this work, we demonstrate and analyze a transformer based shunt switch employing a transformer and shunt NMOS switches as shown in Figure 5(b) [7].

3.2. The Transformer-Based Shunt Switching Structure. A transformer-based shunt switching structure is demonstrated in Figure 5(b). Comparing it with the traditional shunt SPDT structure, Figure 5(a) reveals that the two quarter-wavelength arms are replaced with a miniature transformer that saves a considerable amount of the die area. When a transistor is on, it introduces a low impedance at its port which quenches any voltage swing on it, and the induced voltage will majorly appear at the other end of the secondary winding. As shown in Figure 5(c), all parasitic capacitances in this structure are shunt capacitors to ground and do not provide a feedthrough path between the input and output terminals. Moreover, these capacitances will be resonated out with the equivalent inductance appearing at the transformer terminals at the desired frequency and will not be seen by load and source impedances.

Unlike the traditional distributed switch, this structure introduces a 180° phase difference between the two outputs. In a T/R switch, this 180° phase shift is of minor concern, since this corresponds to moving the transceiver a distance of $\lambda/2$, and most circuits that are sensitive to RF phase use carrier locking techniques. Shunt switches shown in Figure 5 are reflective type of switches which means that when the input is not connected to an output port, that port sees a

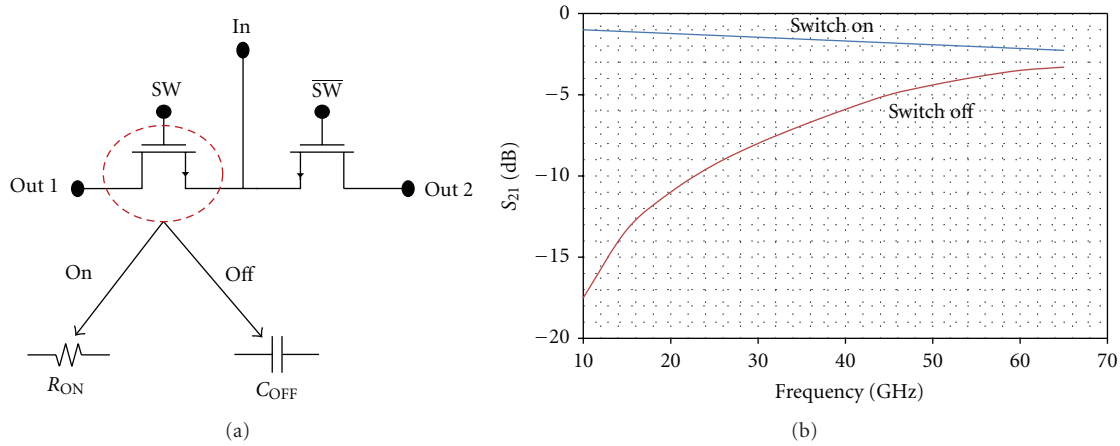


FIGURE 3: Measured S_{21} of an NMOS transistor acting as a series switch in a 50 Ω environment.

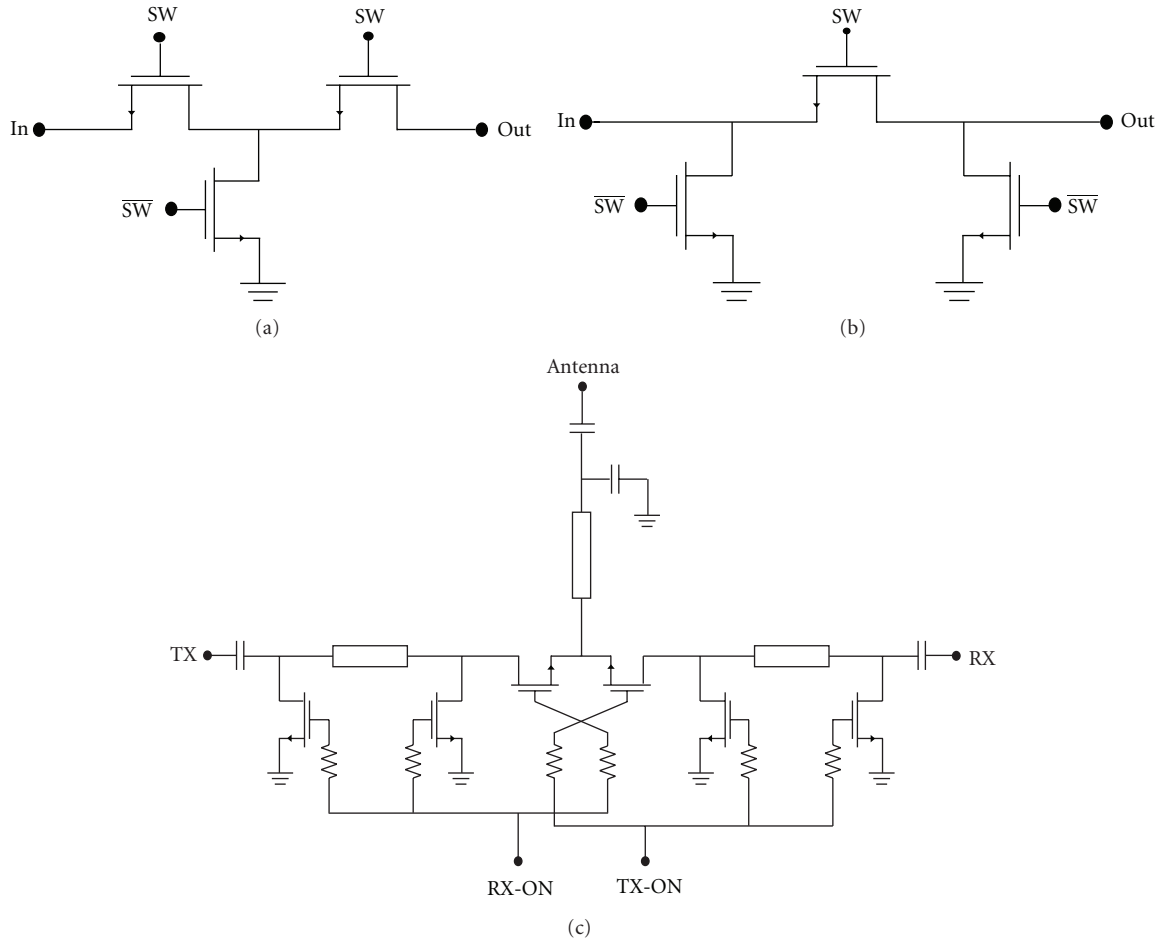
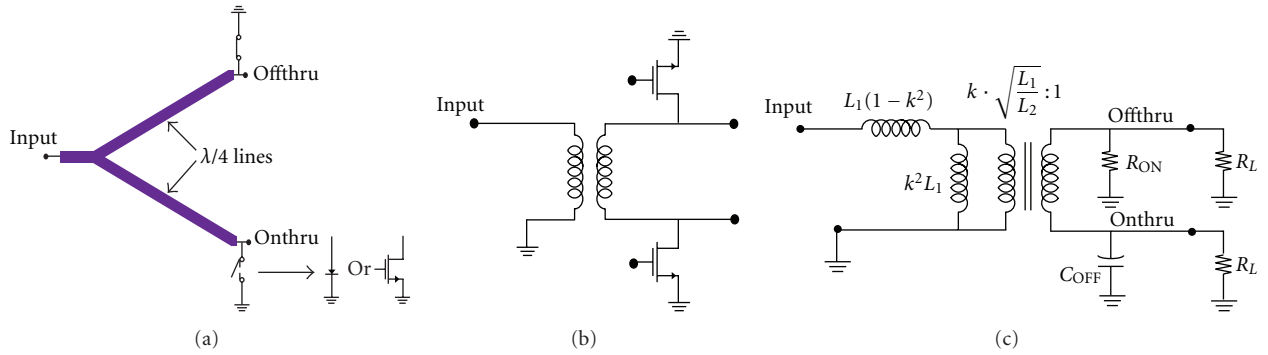


FIGURE 4: Combinations of series and shunt switches in a T (a) or π (b) or L-shape configuration (c). The technique in (c) [6] decreases the amount of off-state leakage at the price of degrading the on-state insertion loss.

short circuit and hence it is not matched. A mismatch at the input of LNA and output of PA can be problematic and cause oscillation. However, since these switches are used in a time division duplexing (TDD) scheme, whenever one output is disabled, the interfacing building block will be turned off in order to save some power dissipation. This eliminates the potential oscillation problems. Care must be taken to make sure that the recovery time of the interfacing building block to reach its steady state when it is turned on is within the overall system specification.



(a) (b) (c)

Figure 5: A traditional microwave shunt switch (a), the proposed miniature structure (b), and the equivalent circuit (c).

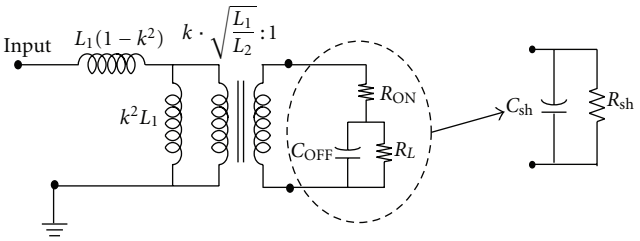
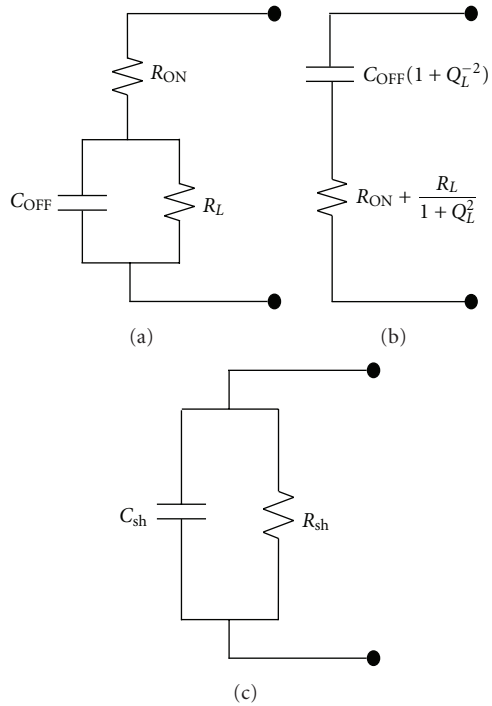


Figure 6: Simplified model of the SPDT network including loading effects.



(a) (b) (c)

Figure 7: Calculating the shunt equivalent loading network.

4. Design Equations of a Transformer-Based T/R Switch

The equivalent circuit model depicted in Figure 5(c) will be used to drive design equations for the center frequency, insertion loss, leakage, and isolation of the switch. Since the on-resistance of the transistor is much smaller than the load resistance ($R_{ON} \ll R_L = Z0$) and for operating frequencies (ω) adequately less than the technology's transit frequency (ω_t), the on resistance is much lower than the shunt reactance of parasitic capacitances of the transistor (C_{drain}), then, we can assume that the loading at the off-thru port is only R_{ON} of the transistor. At the on-thru port, the transistor is off and the total loading at that port will be the load resistance(R_L) in parallel with the drain capacitance of the transistor at the off mode (C_{OFF}) as depicted in Figure 6.

4.1. Equivalent Shunt Loading. To derive the transfer function, the loading network depicted in Figure 7(a) is transformed into its equivalent shunt impedance (Figure 7(c)). Two quality factors are defined in order to accomplish this. The first one is the quality factor of the shunt network of R_L and C_{OFF} which is the loading network quality factor and can be written as

$$Q_L = R_L C_{OFF} \omega. \tag{1}$$

And the second one is the quality factor for the series network of R_{ON} and C_{OFF} which is the transistor-only quality factor and is determined by the choice of the technology. It improves by CMOS technology scaling and can be written as

$$Q_0 = \frac{1}{R_{ON} C_{OFF} \omega}. \tag{2}$$

In order to reach to the shunt equivalent network, first the intermediate series network depicted in Figure 7(b) is calculated as

$$R_S = R_{ON} + \frac{R_L}{1+Q_L^2}, \qquad C_S = C_{OFF}\left(1+Q_L^{-2}\right). \tag{3}$$

To transform this intermediate series network to the equivalent shunt network we should calculate its quality factor (Q_{int}) as follows

$$\frac{1}{Q_{int}} = \omega\left(R_{ON} + \frac{R_L}{1+Q_L^2}\right) C_{OFF}\left(1+Q_L^{-2}\right). \tag{4}$$

Expanding and regrouping the above equation yields to

$$\frac{1}{Q_{\text{int}}} = \frac{1}{Q_0} + \frac{Q_L\left(1+Q_L^{-2}\right)}{1+Q_L^2}. \tag{5}$$

For large values of the load quality factor ($Q_L^2 \gg 1$) the intermediate quality factor can be simplified as:

$$\frac{1}{Q_{\text{int}}} = \frac{1}{Q_0} + \frac{1}{Q_L} \Longrightarrow Q_{\text{int}} = Q_0 \| Q_L. \tag{6}$$

Finally with the aid of the intermediate quality factor (Q_{int}), the series network depicted in Figure 7(b) can be transformed into its shunt equivalent network (Figure 7(c)). This shunt-loading impedance can be characterized as a resistance in parallel with a capacitance with values of

$$R_{\text{sh}} = R_{\text{ON}}\left(1+(Q_0\|Q_L)^2\right) + R_L\frac{1+(Q_L\|Q_0)^2}{1+Q_L^2}, \tag{7}$$

$$C_{\text{sh}} = C_{\text{OFF}}\frac{1+Q_L^{-2}}{1+(Q_L\|Q_0)^{-2}}. \tag{8}$$

This equivalent-loading network is used in the next section to calculate the center frequency.

4.2. Center Frequency and Matching. Since a lower desired loss requires a lower on resistance and consequently a larger transistor with more capacitive loading to operate at mm-wave frequencies, the smallest realizable inductance is preferred. So from now on we assume that the transformer is a 1 : 1 structure with self-inductance of L for each loop. As depicted in Figure 6, there is one remaining series structure. When this is transformed to its parallel equivalent network, the structure will resemble a parallel tank allowing the calculation of the center frequency. The series network of the source impedance (R_S) and the leakage inductance ($L(1-k^2)$) have a quality factor of $Q_S = L(1-k^2)\omega/R_S$. For a good transformer (tight coupling), the leakage inductance is small and the reactance associated with it at mm-wave frequencies is still much smaller than the source impedance ($Q_S \ll 1$). This small Q makes the equivalent shunt impedance of R_S stay at roughly the same value after the transformation ($R_S(1+Q_S^2) \sim R_S$), and the shunt equivalent of leakage inductance ($L(1-k^2)(1+Q_S^{-2})$) be much larger than the already existing shunt-magnetization inductance (k^2L) and be neglected in the parallel configuration. As the loading network ($R_{\text{sh}}\|C_{\text{sh}}$) is moved to the source side by multiplication by the factor k^2 (k being the coupling factor of the 1 : 1 transformer), the equivalent circuit looks like the one shown in Figure 8.

Neglecting the transformed shunt equivalent of the leakage inductance with respect to the magnetization inductance reduces the parallel tank depicted in Figure 8 to an inductance of k^2L in parallel with a capacitance of C_{sh}/k^2 with the resonance frequency of

$$\omega_0 \sim \frac{1}{\sqrt{(k^2L)\cdot(C_{\text{sh}}/k^2)}} = \frac{1}{\sqrt{LC_{\text{sh}}}}, \tag{9}$$

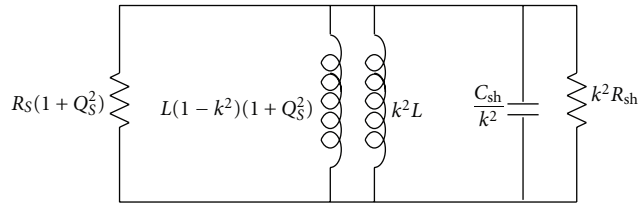


Figure 8: Parallel tank equivalent network of the switch for calculating the center frequency.

where L is the self-inductance of each loop of the transformer and C_{sh} was derived in (8). At the resonance frequency, the apparent load impedance at the source side is k^2R_{sh}, where R_{sh} is described in (7). For an ideal case where coupling factor is unity and the transistor-only quality factor (Q_0) is infinity, the load impedance is transformed to the source side intact and the match is perfect. However, for practical cases of $k \sim$ 0.7-0.9, $Q_L \sim$ 2-3, and $Q_0 \sim$ 5-7 getting a -10 dB of return loss (which is sufficient to meet the requirement for most communication systems) is fairly feasible.

4.3. Insertion Loss. The insertion loss due to the finite on resistance of the switch (R_{ON}) will be the ratio of the power delivered to the effective on-thru load impedance and the power transferred to the total effective impedance. Since we already have these two impedances in the series format (Figure 7(b)), the insertion loss is a resistance ratio and can be written as

$$\text{I.L.} = \frac{R_L\left(1+(Q_L\|Q_0)^2\right)/(1+Q_L^2)}{R_{\text{ON}}\left(1+(Q_0\|Q_L)^2\right) + R_L\left(1+(Q_L\|Q_0)^2\right)/(1+Q_L^2)}. \tag{10}$$

In practice, Q_0 is significantly larger than Q_L and as the design is moved to a more advanced technology in the future, Q_0 will be even higher with respect to Q_L and can be neglected in a parallel configuration ($Q_0\|Q_L \sim Q_L$), and hence the insertion loss can be simplified as

$$\text{I.L.} = \frac{RL}{RL + R_{\text{ON}}Q_L^2}. \tag{11}$$

The transformer is assumed to be lossless in (10) and (11), which means that the insertion loss of the transformer itself should be added to above equations to get the overall insertion loss of the switch. In practice, a typical transformer insertion loss is less than 1 dB at mm-wave frequencies.

4.4. Leakage. To calculate the leakage signal, we should consider that 1 − I.L. of the input power will be delivered to the network at the off-thru port. But since at that port R_L is in parallel with R_{ON}, most of the power will be dissipated in R_{ON} and only a portion of it $R_{\text{ON}}/(R_{\text{ON}}+R_L)$ will reach the off-thru output port. Therefore, the leakage can be formulated as

$$(1-\text{I.L.})\frac{R_{\text{ON}}}{R_{\text{ON}}+R_L} \sim \frac{R_{\text{ON}}}{R_L}\cdot\frac{R_{\text{ON}}Q_L^2}{R_L+R_{\text{ON}}Q_L^2}. \tag{12}$$

Again the transformer was assumed to be lossless here. Nonideal transformers help the leakage, number as the leakage signal will be attenuated by the insertion loss of the transformer as well.

4.5. Isolation. To calculate the isolation, the input signal is connected to the off-thru port, and the signal reaching to the on-thru port is calculated (or vice versa). The situation is depicted in Figure 9. The source impedance and the magnetization inductance can be moved to the secondary side as depicted in Figure 10. Assuming the shunt resistance of R_S/k^2 is large enough to be neglected in a parallel configuration with the reactance of $L\omega$ (which is not a very accurate assumption but can be thought of as an overestimation for the quality factor of the inductor and hence as an underestimation of the isolation value), the equivalent network can be simplified further which results in the inductance L being in series with the resistance $R_{ON} \| R_L$. Converting this series network to its shunt equivalent circuit (and taking into account that in this transformation the output voltage gets multiplied by the quality factor which is in fact the Q_L), we arrive at the parallel tank network described in Figure 10(b). At the center frequency L and C_{OFF} will resonate out each other and the equation for the isolation can be written as

$$\frac{1}{Q_0} \cdot \frac{Q_0^2 \cdot R_{ON}}{Q_0^2 \cdot R_{ON} + R_L} = \frac{Q_o R_{ON}}{R_L + Q_0^2 R_{ON}}. \tag{13}$$

Impact of the transistor on-resistance R_{ON} is noticeable again in the performance of the switch and as more advanced technologies are employed, better isolation is also achievable in the transformer-based T/R switches. These switches are reflective type of switches being used in TDD schemes, and as described earlier, the building block interfacing the off-thru port will be turned off, and hence low isolations are somewhat tolerable in such switches.

4.6. Effect of Interwinding Capacitances. The parasitic interwinding capacitances between the two loops of the transformer were not included in this analysis in order to have the order of the network low enough, and as a result of that to reach at some design equations that can be used as a guidance for obtaining close-to-optimum transistor and transformer sizes before plugging them in to the simulators for further optimizations.

However, if there are non-negligible feed-through capacitances between the two loops, the frequency response of the network would be down shifted, and there would be asymmetries between the frequency response from the single pole to the two different thru ports. As the polarity of the signal is inverted by choosing a different thru port, the voltage appearing on the feed-through capacitance changes and due to the Miller effect, it creates two different networks that the insertion loss through them can be different whether the operation is inverting or noninverting. The inverting configuration would have a higher insertion loss compared to the noninverting scenario [14].

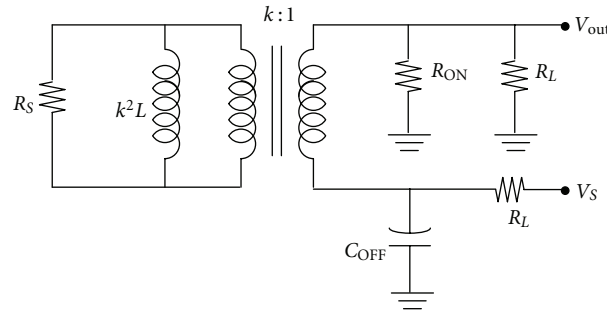


Figure 9: Equivalent circuit for calculating the isolation between the two thru ports.

5. Transformer-Based Switch Design Example in 90 nm CMOS Technology

After deriving design equations of a transformer-based shunt T/R switch presented in Section 4, a prototype is designed, fabricated, and tested to verify the validity of proposed equations. In upcoming subsections, MOS transistor performance in the switch mode is investigated, and an optimum transistor layout to be used in the T/R switch design is investigated. Chosen sizes and design parameters for the transformer and shunt transistors are presented and measurement results are shown at the end.

5.1. MOS Transistor's Performance in the Switching Mode. Layout concerns of a MOS transistor when it is used as a high frequency switch is different from when it is expected to function as a high frequency amplifier. When a MOS transistor is laid out to be used in a mm-wave amplifier, smaller finger widths are used to decrease the series resistance of the gate terminal and as a result of that, lower losses and higher f_{max} are achieved. To decrease the loss through the back-gate effect, bulk resistance should be either close to zero (the case with a solid substrate ring surrounding the device) or approaching infinity (which means very few contacts are placed relatively distant from the transistor or in case of having the deep n-well option, a bulk resonant network is employed). For high frequency amplifier design, the former option of having a well-defined substrate ring is preferred due to its compactness, more predictable modeling of the device, and less vulnerability to substrate noise and coupling issues. However, when a MOS transistor is laid out for switching purposes, especially transmit/receive switching, linearity is a major concern since any degradation to the output power will be extremely costly.

For MOS transistors acting as a shunt switch, the input signal is supposed to be directed to the output port that its corresponding shunt transistor is in the OFF mode ($V_{GS} = 0$). In case of having a small impedance at the gate, that terminal becomes an AC short which means that the gate voltage remains at the provided bias voltage throughout the operation. Therefore, for positive swings of the output voltage, the terminal connected to the output acts as the drain terminal of the transistor, while the AC fluctuation of the V_{GS} remains at zero and the transistor stays completely

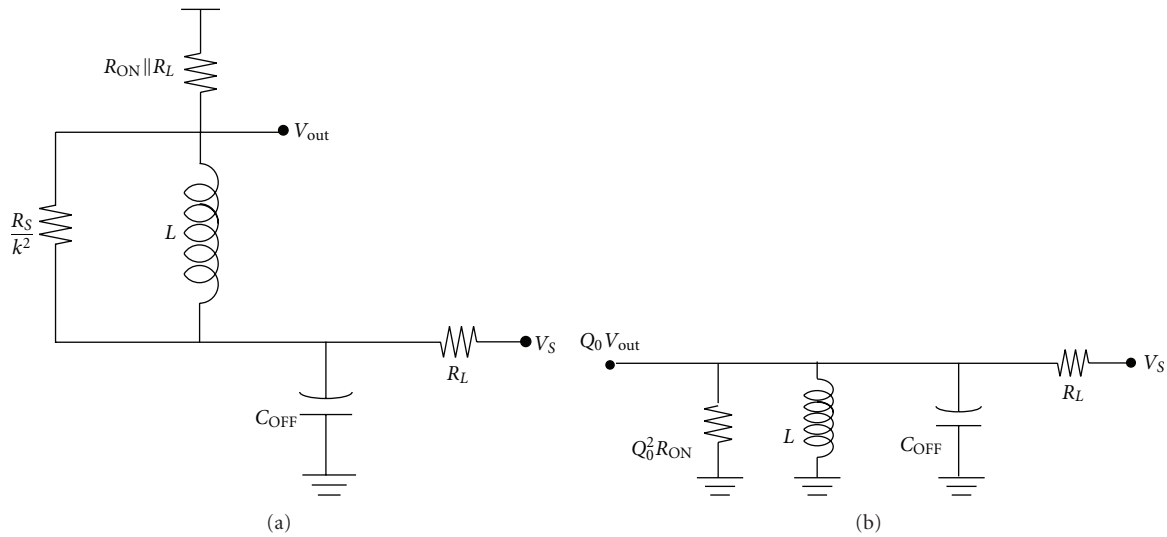


Figure 10: Source network is transferred to the load side (a) and then the structure is converted to a parallel tank configuration (b).

OFF at all times with no degradation to the output power linearity. However, in negative excursion of the swing the output node functions as the source of the transistor and if the output voltage goes below zero by a V_{TH}, the transistor will be turned on in the reverse direction which clamps the signal and produces severe distortion to the output voltage waveform (Figure 11).

On the other hand, if there is a large biasing impedance placed at the gate node, the gate terminal will be an AC floating node, and hence a feed through of output signal will appear at the gate terminal via parasitic paths provided by the transistor capacitances. As depicted in Figure 11, for positive swings of output signal that the output node becomes the drain of the transistor, the feedthrough signal appearing across gate-source terminal through the C_{GD}-C_{GS} network will be

$$V_{GS} = \frac{C_{GD}}{C_{GS} + C_{GD}} V_{out}. \tag{14}$$

For negative excursion of the output signal, the output node serves as the source of the transistor, and therefore, the voltage across gate-source terminal that modulates the channel can be written as

$$V_{GS} = \frac{C_{GS}}{C_{GS} + C_{GD}} V_{out} - V_{out} = \frac{-C_{GD}}{C_{GS} + C_{GD}} V_{out}. \tag{15}$$

Therefore, the gate-source voltage will be modulated by a fraction of the output voltage and the channel turns on when

$$|V_{out}| \geq \frac{C_{GS} + C_{GD}}{C_{GD}} V_{TH}, \tag{16}$$

which is a factor of $1 + (C_{GS}/C_{GD})$ larger than the turn-on voltage in the case of small biasing impedance being presented at the gate line ($|V_{out}| \geq V_{TH}$).

In conclusion, for the interest of linearity, large biasing resistors should be placed at the gate of MOS transistors intended for transmit/receive switching. Since that gate biasing resistance is in series with device's poly gate resistance and much larger than that, the value of intrinsic series gate resistance of the device loses significance, and therefore, larger finger widths are exploited in the layout to make the overall transistor structure more compact and the impact of parasitic inductances caused by long interconnections less effective.

The same argument applies to the bulk terminal through the back-gate effect which makes larger substrate resistances desirable. To do so one can use a deep n-well option and bias the bulk of the transistor through an inductor which makes the bulk node open at the operating frequency. However, having a triple-well transistor with a bulk resonant network is not appealing at mm-wave frequencies for the following reasons.

(1) The added deep n-well region increases parasitic capacitances of the MOS transistor and limits its operating frequency.

(2) Transformer-based switches at mm-wave frequencies are quite compact and adding two bulk resonating inductors (one for each shunt transistor) roughly triples the size of the SPDT structure. Ground shields should also be placed around inductors in order to diminish the inductive coupling among the loops.

The other method to increase the substrate resistance is by having fewer number of bulk contacts (with respect to a MOS transistor specialized for high frequency amplifier design) and place them at a relatively far distance. These few contacts will provide the correct bias voltage for the substrate. However, for latchup and substrate coupling purposes, it is still beneficial to have a well-defined ring at an outer area. The space between this ring and transistor's few bulk contacts can be filled with a p-well blocking layer in order to have a native substrate (as opposed to a highly doped surface) around the transistor to preserve the substrate resistance at a high desirable value (Figure 12).

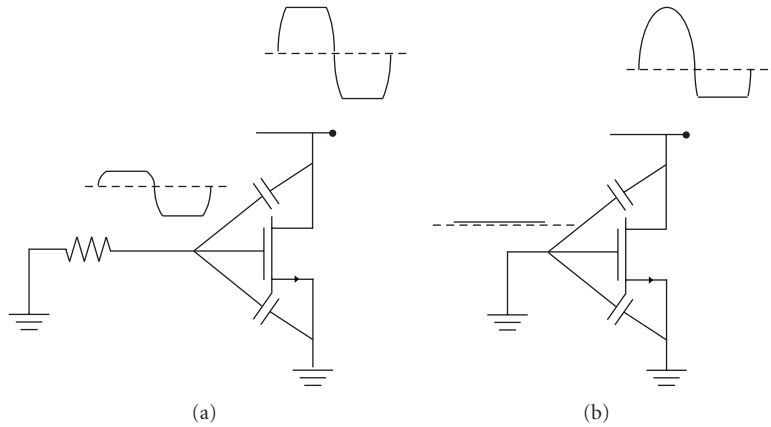


Figure 11: Higher biasing impedance at the gate not only improves the insertion loss but also results in less distortion to the output signal and a higher linearity number for the T/R switch.

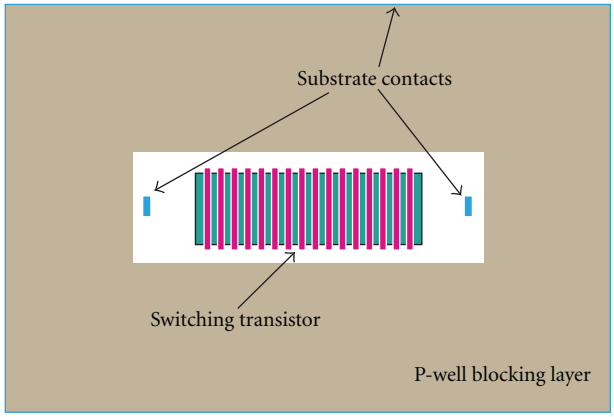


Figure 12: Layout example of a MOS transistor to be used as a switch.

Since this is a customized layout configuration and not included in standard libraries provided by the foundry, extraction tools will not be accurate in capturing all the device parasitic parameters. To have an accurate model of the transistor, a test structure is required to be fabricated and characterized so that a measured based custom model of that transistor is available for maximum accuracy of the design.

5.2. Prototype Design. In our design an overlay structure for a 1 : 1 transformer was used. Two equally thick top metal layers were employed. The diameter of the octagon loop is 42 μm and the width of the winding is $W = 8\,\mu$m. The two loops are identical in shape and have a self inductance of $L_1 \sim 90$ pH. Since the thickness and conductivity of the two top metal layers are equal, the quality factor numbers are similar for the loops ($Q \sim 12$). Although more parasitic capacitances is present at the bottom loop, its effect on the Q is not significant at 60 GHz. The coupling between the two loops is $k = 0.72$. These numbers for quality factors and mutual coupling at the operating frequency result in a minimum insertion loss of 0.85 dB.

The prototype uses 40 μm NMOS transistors in a 90 nm standard CMOS process. Channel lengths are set to the minimum for smallest R_{ON}. However, since higher R_{Gate} is beneficial for the switch insertion loss (less power will be dissipated in the gate network) and improves the linearity (by making the gate terminal a floating node), as previously discussed, finger widths that result in maximum f_{max} were not used. To further increase the impedance at the gate, a large biasing resistor of $R_G = 1$ KΩ was inserted at the gate of each transistor in series. This large added R_G also alleviates the effect of any gate line inductance. Inductance at the gate line is detrimental to the linearity as it resonates out some part of parasitic gate capacitance to the ground (this is a capacitance that helps linearity as described in Section 5.1). This 1 KΩ of gate biasing resistance is high enough to have negligible effects on the insertion loss and linearity of the T/R switch. However it is low enough in order to provide a fast switching time—less than 250 pS—to turn the switch OFF and ON when 0 and 1.2 V are applied as gate switching voltages respectively. To eliminate the detrimental effect of the bulk network on linearity and insertion loss, a layout as described in Figure 12 with few close by bulk contacts is devised.

6. Prototype Measurement Results

A prototype SPDT T/R switch has been fabricated in a 90 nm CMOS process. The die photo is shown in Figure 13. As can be seen in Figure 13, employing a transformer and designing on a lumped component basis miniaturized the structure, and the active area of the switch is only 60 $\times$ 60 μm^2. On-wafer measurement results are shown in Figures 14 and 15. The input and output GSG pads have been deembedded from the measurements using on-chip open and short deembedding structures of the pad. As depicted in Figure 14, the switch has its minimum insertion loss of 3.4 dB at 50 GHz, and its 3 dB bandwidth extends beyond the range of 40 GHz–60 GHz. In simulation, the T/R switch was designed to have a center frequency at the 60 GHz band with a 2.5 dB of insertion loss. However since a custom transistor

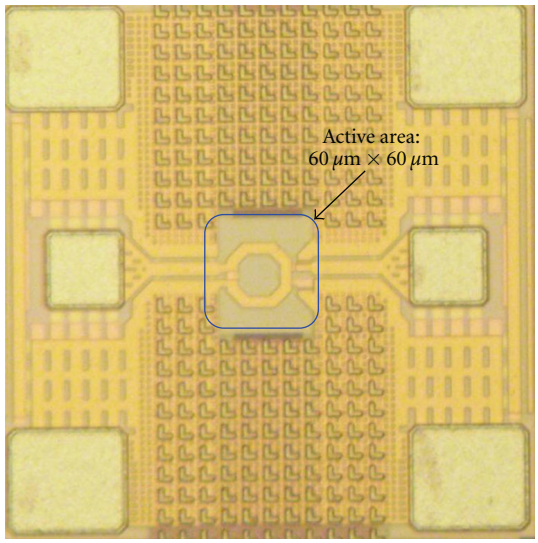


Figure 13: Die microphotograph of the miniaturized shunt switch employing a transformer.

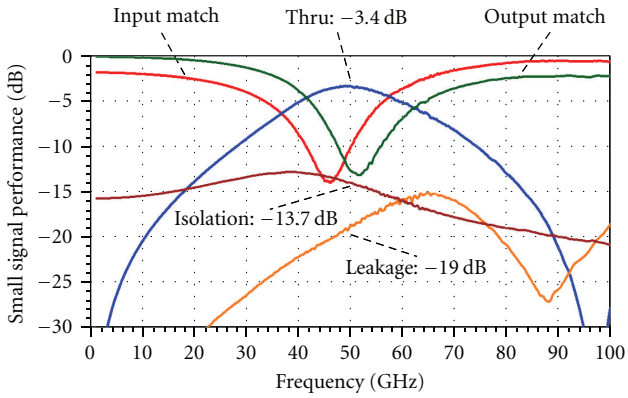


Figure 14: Measured insertion loss, leakage (input to the off-thru port), isolation (between the on-thru and off-thru ports), and return loss performance of the switch.

as described in Section 5.1 was used for switching, where its exact layout was not fabricated beforehand and characterized for the mm-wave library, a 0.9 dB difference in the insertion loss and a 10 GHz downshift in the frequency response can be observed.

When the input is connected to an on-thru output, there is 19 dB of leakage in the off-thru port. The isolation between two output ports is 13.7 dB. Input and output return loss numbers are better than −10 dB (Figure 14). The large-signal power measurement depicted in Figure 15 shows an input referred 1 dB compression point of +14 dBm, which is adequate for most CMOS mm-wave applications. Due to this high input power required and power handling limitations of the VNA, an external power amplifier module was used to bring up the power provided at the probe tips to a range that $P_{-1\,\mathrm{dB}}$ curves could be captured. Table 1 summarizes the overall measured performance of the switch

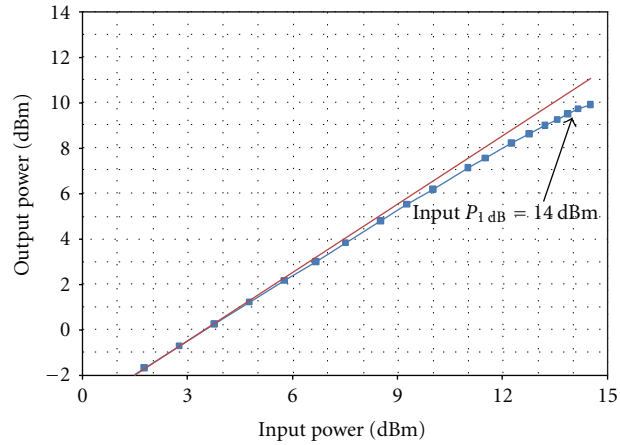


Figure 15: Large signal measurement ($P_{-1\,\mathrm{dB}} = 14$ dBm).

and compares them to recently published results for mm-wave T/R switches. This work has the best performance in terms of the die area. Linearity is comparable to other mm-wave switches, and the insertion loss will benefit from technology scaling in future demonstrations as suggested by [13].

This transformer-based shunt switch was implemented in a 90 nm MOS process with an f_t of ~100 GHz. According to equations derived in Section 4, insertion loss, leakage, and isolation numbers get better as the R_{ON} of transistor improves. More advanced CMOS technologies with improved f_t numbers directly enhance the performance of the switch by providing more g_m at a constant transistor size (and hence a constant capacitive loading). This makes the future deployment of transformer-based shunt switches in mm-wave systems promising. In addition to transmit/receive (T/R) switching, single pole double throw (SPDT) switches have many other useful applications. Examples include modulators, stepped attenuators, and phase shifters.

7. Conclusion

A miniature lumped-element switch topology employing only a transformer and two shunt NMOS switches has been demonstrated. Shunt-only transistors make it more suitable for mm-wave frequencies. Design equations for the operating frequency, insertion loss, leakage, and isolation were derived in terms of the transformer inductance and coupling factor as well as transistors ON resistance and parasitic capacitances. A transformer-based single pole, double throw (SPDT) shunt switch prototype was designed and fabricated in 90 nm digital CMOS process. It has a minimum insertion loss of 3.4 dB at 50 GHz from the single pole to the ON-thru port and a leakage of 19 dB from the single pole to the OFF-thru port. The isolation is 13.7 dB between the two ports and the switch is capable of handling 14 dBm of power at its 1 dB compression point. The fabricated chip has a small active area of 60 μm × 60 μm.

Table 1: Comparison to recently published mm-wave T/R switches.

Process	This work/[7]	[6]	[8]	[9]	[10]	[11]
	90 nm CMOS	130 nm CMOS	90 nm CMOS	90 nm CMOS	65 nm CMOS	90 nm CMOS
	Ref.					
Frequency (GHz)	50	60	24	72	82	60
Insertion loss (dB)	3.4	4.5	3.5	2.7	4.2	1.5
Tx-RX isolation (dB)	13.7	24	16	27	25	25
Supply voltage (V)	1	1.2	1.2	1	1.2	1.2
$IP_{-1\,dB}$ (dBm)	14	4.1	28.7	15	N/A	13.5
Area (mm^2)	0.004	0.221	0.018	0.14	N/A	0.27
Switching time (nS)	0.25	0.4	10	N/A	N/A	3.1

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