RF Front-End for Autonomous Low Power Wireless Sensor Nodes

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Contents

List of Figures

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Abstract

This work focusses on the design of a low power RF receiver front-end circuit for use in wireless sensor nodes. Wireless sensor nodes must generally be maintenance proof and thus they must be energy autonomous. This imposes a requirement for them to be able to scavenge energy from energy harvesters like solar panels and piezo-generators. Therefore, the RF transceiver, which is the largest consumer of the available power, must be a low power system. This is the impetus behind this project and the study undertaken herein.

The report summarizes the state-of-the-art topologies in RF receiver front-ends targeted at sensor nodes or similar applications, comparing them on various performance parameters, especially power consumption. Of these, a particularly attractive topology, *the LMV Cell (LNA, Mixer and VCO)* is analyzed further.

The design of the LNA and the oscillator are studied separately with respect to optimizing them as constituents of the LMV cell. Consequently, a unified design methodology for co-designing the LNA and the oscillator is chalked out.

Chapter 1

Introduction

1.1 Wireless Sensor Nodes

These days wireless sensor networks are being deployed in a multitude of applications like vital-health sign monitoring in hospital environments, monitoring of stresses and strains in buildings and bridges, monitoring of ocean resources, plant monitoring in agricultural environments, rainfall monitoring in tropical rainforests, etc. As the name implies, a *Wireless Sensor Network* is a collection of sensor nodes that are deployed over an area to monitor the sensors' local environment. The sensor nodes communicate amongst each other as well as with a base station for relaying the data wirelessly.

In typical applications of sensor networks as listed above, the sensors are deployed in hard to reach areas. This dictates the requirement for the nodes to be maintenance-free. They should be able to last their expected lifetime without any need for a battery replacement, i.e., they should be energetically autonomous [1]. Since the radio transceivers are the biggest consumers of power in a given application, the requirement for the sensor nodes to be energetically autonomous provides an impetus to design low-power circuit architectures.

1.2 Low-Power Design for Wireless Sensors

Wireless sensor applications are low data rate (less than 2 Mbps), low power and short range(10-50m). Power-conscious design for such applications must necessarily involve optimization at all layers of from the transaction layer to the MAC and ultimately the physical layer. Designers have to adopt a hardware software co-design approach, optimizing the communication protocols while at the same time designing and optimizing low-power radio circuits. However, in the present context we will discuss only the issues pertaining to circuit design.

In general, RF circuit design involves tradeoffs between various conflicting performance requirements like low power, low noise, high linearity, high gain etc. These are summarized in the "RF design hexagon" shown in figure 1.1. The fundamental limits on power dissipation in a wireless receiver are imposed by the following:

- Noise

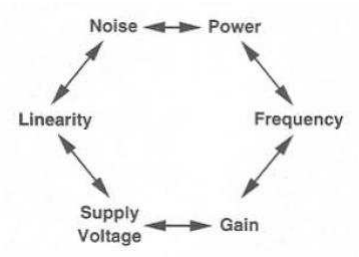

Figure 1.1: RF design tradeoffs [2]

- Gain
- Linearity
- Spurious Free Dynamic Range- The *spurious free dynamic range*(SFDR) is a measure of the limits on allowable signal amplitudes set by noise and linearity. Thus it governs the sensitivity of the receiver. A system employing very low-power receivers must relax requirements on dynamic range or must operate at low data rates [5].
- Q of passive components

Because of these tradeoffs between higher performance and low power consumption certain choices must be made regarding the kind of architecture to be used, the operating frequency within the limitations imposed by the process technology to achieve a reasonable performance. For example, with Direct Conversion architectures reduced component count can be achieved, that too without the need for high-Q components. However, at the same time they suffer from higher 1/f noise and DC offset problem. Low-IF architectures overcome these problems but require higher order filters, thus increasing power consumption. A careful frequency selection should be done to ensure reasonably low power operation.

1.3 State-Of-The-Art

In this section a summary of the state-of-the-art in low-power RF transciver circuit design is presented. It must be remarked here that it is difficult to compare the various circuits because due to the lack of a standard way of specifying performance under same operating conditions.

Out of the topologies presented in Table 1.1 the one presented in the first column [6] has been selected a subject of further study in this project. This topology distinguishes itself in that it presents a current reuse methodology in a novel architecture that combines LNA, Mixer and VCO in a single stacked structure. This seems attractive from the power consumption point of view and a suitable candidate for further analysis.

Table 1.1: Comparison of State-Of-The-Art Front-Ends

	[6]	[7]	[1]	[8]	[9]
Type	Low-IF	Direct Conversion	Direct Conversion	No-Phase detection	Superhet
Power Consumption [mW]	11	0.8	1.8	0.5-2.5	1.8
Supply Voltage [V]	1.2	1.0	0.9	NA	1.8
Process [μm]	0.13	0.18	0.18	0.18	0.18
Sensitivity [dBm]	NA	-95	-105	-65 to -37	NA
Frequency	2.4 GHz	434 MHz	433/868 MHz	916.5 MHz	2.4 GHz

Chapter 2

Receiver Architecture

In this chapter we discuss the architecture of the LMV. Our discussion here will mostly follow [6]. The LMV cell is a new RF front-end receiver topology which shares the same bias current and the same devices among by merging LNA, mixer and VCO into a single stage. Thus a single structure performs amplification, mixing and LO generation.

A cross coupled LC tank oscillator intrinsically performs mixing functionality since the cross coupled transistors downconvert the RF signal in the bias current. Sensing the downconverted signal at the VCO output degrades the oscillator phase noise [6]; the bias current generator is thus split into two transistors substituting the short at sources of the oscillator transistors with a capacitor that acts as a short at RF but as a high impedance at IF/DC (figure 2.1). This enables the downconverted output to be sensed at the sources of the oscillator transistors. Since the capacitor between the sources of these transistors degenerates them, its value must satisfy

$$2\pi f_{LO} C_{diff} >> G_{m1,2} \tag{2.1}$$

so as not to reduce the loop gain significantly.

This structure is called the **Bias Splitting Self Oscillating Mixer**. The operation can be easily understood by considering half LO period in which the signal coming from M_{0a} flows through the bias transistor M_{0a} and through M_1, while the signal through M_{0b} flows through the load and M_1. Similarly, in the second half of the LO cycle the current through M_{0a} flows through the load. Thus, the RF current is effectively multiplied by a square wave and sensed at the load.

The ideal conversion gain of the bias splitting SOM is only $1/\pi$, since only half of the total RF current flows through the load. This gain can be doubled by introducing an additional switching pair between the input trasnconductor and cross coupled pair, as shown in Figure 2.2. The additional transistors M_3 and M_4 are driven by the LO in opposite phase than M_1, M_2. This causes all the RF current to flow through the load thereby increasing the conversion gain to $2/\pi$. The input trasnconductor can be modified into an LNA (inductively degenerated common-source) so that the complete structure works as single stage LNA, mixer and VCO, thus the structure is called **LMV cell**.

We will study the design on the individual constituents of the receiver in the subsequent chapters with an aim of designing an optimum receiver for use in the wireless sensor applications.

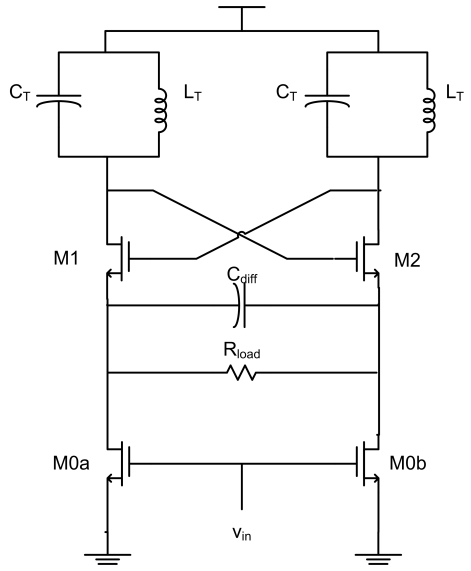

Figure 2.1: Bias splitting self oscillating mixer

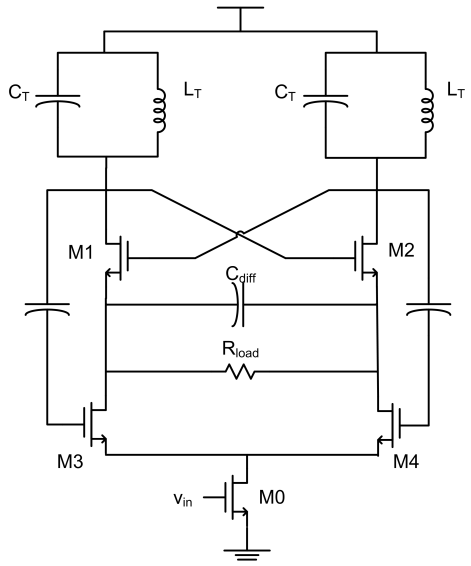

Figure 2.2: The LMV cell

Chapter 3

Receiver Design

In this chapter we will study the design of the two constituents of the receiver- the LNA and the oscillator. We will analyze the designs with respect to optimizing various parameters with an aim of coming up with a design methodology.

3.1 LNA Analysis and Design

3.1.1 Design Considerations

The low-noise amplifier (LNA) is typically the first stage in a receiver. As its name suggests the LNA provides the gain while adding minimum noise and distortion itself. Generally, it must also present a specific input impedance (typically 50Ω) for maximum power transfer from the previous stage which would be an antenna or a passive filter.

Impedance Matching Impedance Matching is essential in RF front-end circuit design to maximize the power transfer between the source and the load. Since, the received signal levels are quite small, it is imperative that the maximum power be delivered to the subsequent stages in the receiver chain. The input impedance of a MOS transistor is inherently capacitive and hence it difficult to provide a 50Ω resistive match. Several topologies are possible to achieve the same [3]. These include

1. using a resistive termination across the input terminals of a common-source amplifier,
2. shunt-series feedback amplifier,
3. using the $1/g_m$ resistance of a common-gate amplifier and
4. inductively degenerated common-source amplifier.

Of these, the first two suffer from degraded noise figures due to the additional noise introduced by the resistors in the signal path. The last two will be studied in 3.1.2 as possible alternatives for use in the receiver.

Noise Noise is one of the most important design parameters in RF design since it imposes the limits on the receiver sensitivity. Depending on the origin of noise, it can be classified into various types:

Thermal: Random voltage generated due to thermally agitated carriers. It is characterized by Temperature T and noise bandwidth B.

Flicker: This is also called the 1/f noise because its power spectral density is an inverse function of the frequency. The origin of this type of noise is still not well defined.

Shot: This type of noise arises when there is a charge flow across a potential barrier. It is characterized by the DC current I_DC through a device and the noise bandwidth B.

A more detailed theory about these types of noise can be found in [3]. We will discuss more about the Thermal noise in MOS transistors in the context of LNA Design in section 3.1.3. An important figure of merit to characterize the noise performance of a system is called Noise Factor, F.

$$F \triangleq \frac{total\ output\ noise\ power}{output\ noise\ due\ to\ input\ source} \tag{3.1}$$

Gain The LNA needs to provide sufficient gain not only to amplify the feeble input signal but also to reduce the input referred noise of the subsequent stages of the receiver. This follows from the Friis formula:

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots \tag{3.2}$$

where,
F_n = Noise Factor of the n^{th} stage and
G_n = Gain of the n^{th} stage.

Linearity Linearity is another important consideration in LNA design because of the consequences like harmonic distortion, gain compression, intermodulation etc. The system must remain linear while receiving large input signals as well as weak signals in the presence of strong interferers. Nonlinearity of systems is generally characterized by its third-order Input Intercept Point (IIP_3). IIP_3 is proportional to the ratio of the fundamental and the 3^{rd} order components of the transfer characteristic of the system.

3.1.2 Impedance Analysis

In this section we derive the impedance matching conditions for the Common-Gate and source degenerated Common-Source LNAs.

Common Gate LNA

Figure 3.1 shows the common-gate LNA without any impedance matching network. The input impedance is

$$Z_{in} = \frac{1}{G_{ms}} \tag{3.3a}$$

where,

$$G_{ms} = \frac{2I_D/U_T}{\sqrt{4IC + 1} + 1} \tag{3.3b}$$

where, I_D is the MOS drain current, IC is the inversion factor of the transistor and U_T is thermal voltage = 25.8 mV.

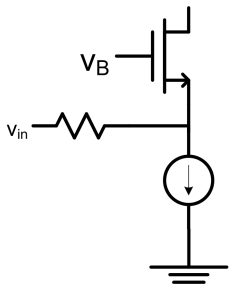

Figure 3.1: Common Gate LNA without matching network

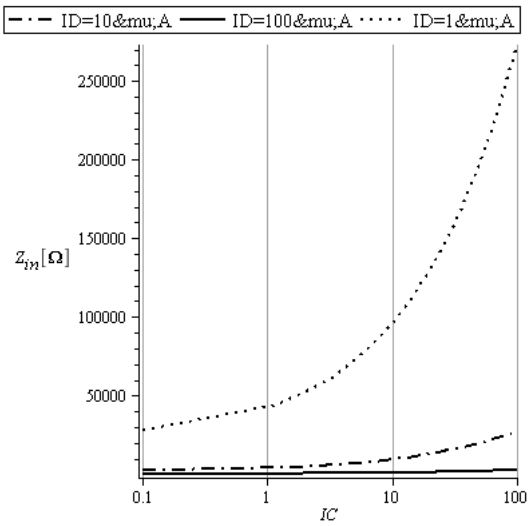

Figure 3.2: Common Gate input impedance as a function of IC

In figure 3.2 the input impedance is plotted as a function of the inversion factor for multiple values of drain current. It can be clearly seen that the required value of 50Ω cannot be reached even when working in weak-inversion or with currents as high as 100μA. This implies that for a small impedance matching with small source impedances leads to a high power consumption. Thus, the use of an impedance matching network becomes imperative.

Figure 3.3 shows the common-gate LNA now with the impedance matching network introduced. The impedance matching network consists of capacitor C_S and inductor L_S.

Now, the input impedance is given by,

$$Z_{in} = \frac{1}{sC_S} + \frac{sL_S}{1 + sL_sG_{ms}}. \tag{3.4}$$

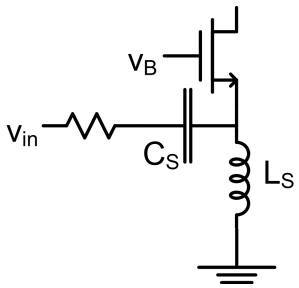

Figure 3.3: Common Gate LNA with matching network

Let,

$$\begin{aligned} Q &= \frac{X_S}{R_S} \\ &= \frac{R_P}{X_P} \\ &= \sqrt{\frac{R_P}{R_S} - 1} \end{aligned} \tag{3.5}$$

where,

$$X_P = \omega_0 L_S = \frac{1}{QG_{ms}} \tag{3.6a}$$

$$X_S = \frac{1}{\omega_0 C_S} = QR_S. \tag{3.6b}$$

Therefore,

$$G_{ms} = \frac{1}{(1+Q^2)R_S} \tag{3.7}$$

From the above equations, we get the conditions for impedance matching in common-gate LNA.

$$G_{ms} = \frac{1}{(1+Q^2)Z_{in}} \tag{3.8a}$$

$$L_S = \frac{1}{\omega_0 Q G_{ms}} \tag{3.8b}$$

$$C_S = \frac{1}{\omega_0 Q Z_{in}}. \tag{3.8c}$$

Here, we see that by introducing the matching network the required G_{ms} of the MOS is now reduced by a factor of $1+Q^2$. Thus, by choosing a sufficiently high Q we can reduce the power consumption required to have an impedance match in a common-gate LNA.

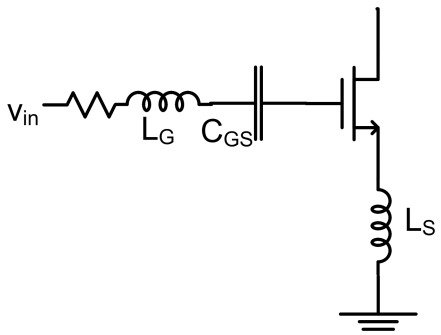

Figure 3.4: Inductively Degenerated Common Source LNA

Common Source LNA

Figure 3.4 shows the inductively degenerated LNA. Referring to the small signal model the input impedance is

$$\begin{aligned} Z_{in} &= \frac{G_m}{C_{GS}} + s(L_S + L_G) + \frac{1}{sC_{GS}} \\ &= \frac{G_m}{C_{GS}} + j\frac{\omega^2(L_S + L_G)C_{GS} - 1}{\omega C_{GS}}. \end{aligned} \tag{3.9}$$

At resonant frequency, the MOS capacitance C_GS will be tuned out by the L_S and L_G. It should be noted here that L_G is required to provide an additional degree of freedom to tune out C_GS because L_S is chosen to match the source resistance R_S and hence cannot be used to tune out C_GS. Thus, the impedance matching conditions for the common-source LNA are given by,

$$G_m = \frac{Z_{in}C_{GS}}{L_S} \tag{3.10a}$$

$$C_{GS} = \frac{1}{\omega^2(L_S + L_G)}. \tag{3.10b}$$

3.1.3 Noise Analysis

In this section we will do an analysis of the common-gate and common-source LNAs with an aim of determining their noise-factors as functions of inversion factor of the transistor. To simplify the analysis we will consider the effect of only thermal noise. Also, we will use simplified small-signal circuits neglecting induced gate noise and noise due to substrate resistances.

Common Gate LNA

Figure 3.5 shows the small-signal equivalent circuit of the common-gate LNA with the drain noise source and input voltage noise source also included. Following the standard two-port noise theory as

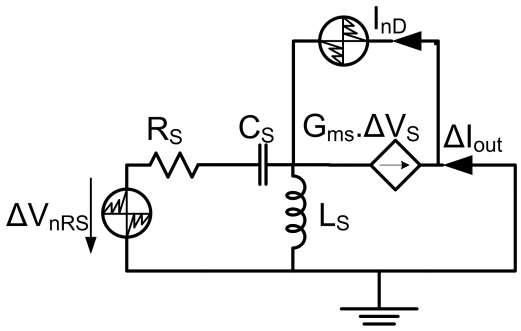

Figure 3.5: Common Gate LNA equivalent circuit including noise sources

applied to MOS [10], the noise factor F can be defined as,

$$\begin{aligned} F &\triangleq \frac{G_{neq}}{G_s} \\ &= \frac{R_{neq}}{R_s}. \end{aligned} \tag{3.11}$$

(3.12)

where, G_{neq} is the total input referred noise conductance and G_s is the conductance of the signal source.

From the small-signal circuit, the short circuit output noise current is given by

$$I_{nout} = \Delta I_{nD} - G_{ms}\Delta V_S. \tag{3.13}$$

The total input referred noise voltage is then

$$V_{neq} = \frac{\Delta I_{nD}}{G_{ms}} - \Delta V_S. \tag{3.14}$$

The mean square value of V_{neq} is thus given by

$$\overline{|V_{neq}|^2} = \frac{\overline{|\Delta I_{nD}|^2}}{G_m s^2} + \overline{|\Delta V_S|^2}. \tag{3.15}$$

Replacing $\overline{|\Delta I_{nD}|^2}$ with 4kTBG_{nD}, ΔV_S by $G_{ms}R_sV_{ns}$ and dividing the expression by 4kTB, we get total input referred noise resistance R_{neq}

$$R_{neq} = \frac{G_{nD}}{G_{ms}}R_s + R_s. \tag{3.16}$$

Now,

$$G_{nD} = \delta_{nD} \cdot G_{ms} \tag{3.17}$$

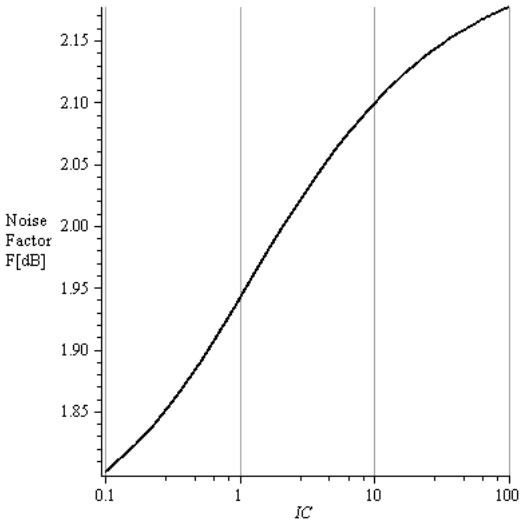

Figure 3.6: Common Gate LNA noise figure as a function of IC

where δ_{nD} is the **drain thermal noise excess factor**.

Therefore, noise factor

$$F = \frac{R_{neq}}{R_s} = 1 + \delta_{nD}. \tag{3.18}$$

δ_{nD} is a bias dependent according to [11]

$$\delta_{nD} = \frac{2}{3} - \frac{1}{6} \cdot \frac{G_{ms}/G_{spec}}{IC} \tag{3.19}$$

Expressing G_{ms} as a function of inversion factor IC and substituting for δ_{nD} in 3.18, we get

$$F = \frac{1}{3} \cdot \left(5 - \frac{1}{\sqrt{4IC+1}+1}\right) \tag{3.20}$$

Figure 3.6 shows the variation of the Noise Figure (10· log F) as a function of the MOS inversion factor. As can be clearly seen that the noise performance is best while operating in weak-inversion.

Common Source LNA

Figure 3.7 shows the small-signal equivalent circuit of the inductively degenerated LNA with the noise sources included. Following an approach similar to that of common-source LNA we can find the noise factor of the common-source LNA. Here, we directly present the result. A detailed derivation can be referred in [10]. The noise factor is given by

$$F = 1 + \frac{\gamma_{nD}\omega_0}{Q_L\omega_t} \tag{3.21a}$$

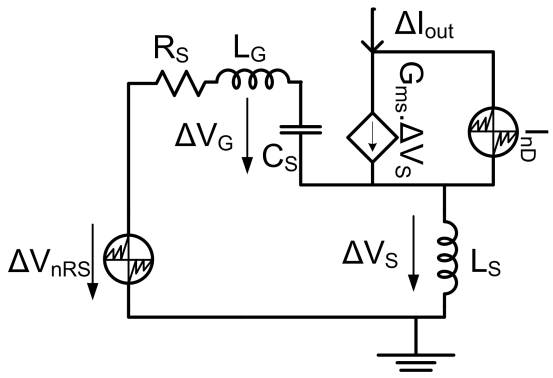

Figure 3.7: Common Source LNA equivalent circuit including noise sources

where,

$$Q_L = \frac{1}{\omega_0 R_S C_{GS}} \tag{3.21b}$$

and

$$\gamma_{nD} = n \cdot \delta_{nD} \tag{3.21c}$$

From the above expression for noise factor it is easy to see that it will give a similar variation with respect to the inversion factor IC as that of the common-gate LNA. However, it must be remarked here that lower limit of noise figure for common-source LNA is 0 dB vis-a-vis 1.8 dB for common-gate LNA.

In the due course of this work, power constrained noise optimization (simultaneously with impedance matching), following the approach in [3] was also attempted. The analysis was done with an aim to obtain an expression for noise factor and conditions for impedance matching as functions of inversion factor, given a power constraint. However, the algebraically involved analysis failed to provide a set of simultaneous equations which could be easily solved to obtain the optimum parameters. Another attempt was made to derive a continuous expression from weak to strong inversion for noise factor, considering all thermal, shot and flicker noise sources. However, this analysis too yielded unwieldy expressions that failed to provide any insight.

3.1.4 Linearity Analysis

As has already been emphasized linearity is an important aspect in LNA design. Linearity performance is characterized by the amplitudes fundamental and third order terms of the transfer characteristic of the LNA. In this section we will do a linearity analysis of the common-gate and common-source LNAs first considering the MOS in weak and strong inversion operations separately and finally using the continuous MOS model.

Common Gate LNA

MOS in weak inversion In the case of weak inversion, the nonlinearity is a simple exponential function.

$$I_D = I_{spec} \cdot exp\left(\frac{V_P - V_S}{U_T}\right) \tag{3.22}$$

Assuming a sinewave input is applied to the source and the transistor is in saturation, with V_G being constant, we get,

$$\begin{aligned} V_S &= V_{Sq} + A\cos(\omega t) && (3.23)\\ I_D(t) &= I_{D0} \cdot exp\left(-\left(\frac{V_{Sq} + A\cos(\omega t)}{U_T}\right)\right) \\ &= I_q \cdot exp(x \cdot \cos(\omega t)) && (3.24)\\ & && (3.25) \end{aligned}$$

with

$$I_q = I_{D0} \cdot exp\left(\frac{-V_{Sq}}{U_T}\right)$$

and

$$x = \frac{-A}{U_T}$$

Normalizing the output current to the dc value,

$$i_d(t) = \frac{I_D(t)}{I_q} = exp(x \cdot \cos(\omega t)) \tag{3.26}$$

Comparing to the Taylor series expansion of e^x, we get the different harmonics as

$$\alpha_1 = 1 \tag{3.27a}$$

$$\alpha_2 = \frac{1}{2} \tag{3.27b}$$

$$\alpha_3 = \frac{1}{6} \tag{3.27c}$$

MOS in strong inversion The strong inversion nonlinearity function for a MOS is simply a quadratic function if no short channel effects are considered. This would imply that there would be no third order terms and the IIP_3 would be infinite. To have a more realistic picture, we need to consider the short channel effects of the MOS. Here, we consider the MOS model accounting only for velocity saturation effect for the sake of simple analysis.

$$I_D = \frac{{q_s}^2}{1 + \lambda_c/, q_s} \tag{3.28}$$

where,

$$q_s \approxeq \frac{V_P - V_S}{2U_T}$$

and

$$\lambda_c \triangleq \frac{2\mu_0 U_T}{v_{sat} \cdot L}$$

λ_c represents the velocity saturation coefficient and is dependent on carrier mobility μ_0, carrier saturation velocity v_{sat} and transistor channel length L.

Thus, normalized drain current

$$i_d = \frac{\left(\frac{V_P - V_S}{2U_T}\right)^2}{1 + \lambda_c \cdot \left(\frac{V_P - V_S}{2U_T}\right)} \tag{3.29}$$

Adding sine wave at the source input, such that

$$V_S = V_{Sq} + A\cos(\omega t)$$

we can write

$$i_d = i_q \cdot \frac{(1 - x/v_{gt})^2}{1 - \lambda_c{}' \cdot x/v_{gt}} \tag{3.30}$$

with

$$x = \frac{A}{2U_T},$$

$$v_{gt} = \frac{V_P - V_{Sq}}{2U_T}$$

and

$$\lambda_c{}' = \frac{\lambda_c \cdot v_{gt}}{1 + \lambda_c \cdot v_{gt}} \tag{3.31a}$$

Defining f(x)=$\frac{i_d(t)}{i_q}$ and developing as a Taylor series,

$$\begin{aligned} f(x) &= 1 + \alpha_1{}' \frac{x}{v_{gt}} + \alpha_2{}' \frac{x}{v_{gt}}^2 + \alpha_3{}' \frac{x}{v_{gt}}^3 + \cdots \\ &= 1 + \alpha_1 x + \alpha_2 x^2 + \alpha_3 x^3 + \cdots \end{aligned} \tag{3.32}$$

Thus,

$$\alpha_1 = \frac{\lambda_c{}' - 2}{v_{gt}} \tag{3.33a}$$

$$\alpha_3 = \frac{\lambda_c{}'(1-\lambda_c{}')^2}{{v_{gt}}^3} \tag{3.33b}$$

Substituting for $\lambda_c{}'$ in terms of λ_c and taking $\lambda_c << 1$ for devices with $L > 0.1\mu m$ [4], we obtain

$$\alpha_1 \cong \frac{-2}{\sqrt{IC}} \tag{3.34a}$$

$$\alpha_3 \cong \frac{\lambda_c}{IC} \tag{3.34b}$$

where,

$$IC = {v_{gt}}^2$$

Common Source LNA

Following an approach similar to that of common-gate LNA we can do the linearity analysis of the common-gate LNA. In case of the common source LNA, for the stron inversion operation, the transistor model accounting for mobility reduction due to vertical field is used to account for the third order nonlinearity. Here, we directly present the results. A detailed derivation can be referred in [10].

In **weak inversion**

$$\alpha_1 = 1 \tag{3.35a}$$

$$\alpha_2 = \frac{1}{2} \tag{3.35b}$$

$$\alpha_3 = \frac{1}{6} \tag{3.35c}$$

In **strong inversion**

$$\alpha_1 \cong \frac{1}{\sqrt{IC}} \tag{3.36a}$$

$$\alpha_3 \cong \frac{-\theta}{8 \cdot IC} \tag{3.36b}$$

where, θ is the normalized mobility reduction coefficient.

Linearity Analysis Using The Continuous MOS Model

The normalized current from weak to strong inversion (using continuous EKV MOS model [4], accounting for both velocity saturation and mobility reduction due to vertical field is given by

$$\begin{aligned} i_d &= \frac{\ln^2\left(1+exp\left(\frac{v_P-v_S}{2}\right)\right)}{1+\Theta v_P+\lambda_c v_P/2} \\ &= \frac{\ln^2\left(1+exp\left(\frac{v_P-v_S}{2}\right)\right)}{1+\sigma v_P} \end{aligned} \tag{3.37}$$

where v_P is the normalized pinch-off voltage, Θ is the mobility reduction coefficient, λ_c is the velocity saturation coefficient and $\sigma = \Theta + \lambda_c/2$.

Taking $v_S = 0$ for **common source** and adding a sine wave at the gate, the normalized current becomes

$$i_d(t) = \frac{i_q}{\ln^2(1 + exp(v_P/2))} \cdot \frac{\ln^2\left(1 + exp\left(\frac{v_P + v_{in}}{2}\right)\right)}{1 + \sigma' v_P} \tag{3.38}$$

with

$$i_q = \frac{\ln^2(1 + exp(v_P/2))}{1 + \sigma v_P}$$

and

$$\sigma' = \frac{\sigma}{1 + \sigma v_P}$$

Defining $f(v_{in}) = \frac{i_d(t)}{i_q}$ and developing as a Taylor series we get the coefficients as

$$\alpha_1 = 2\left(\frac{\mathrm{e}^k}{\ln\left(1 + \mathrm{e}^k\right)\left(1 + \mathrm{e}^k\right)} - \sigma\right) \tag{3.39a}$$

$$\alpha_3 = 1/3\,\frac{-3\,\sigma' y^3\left(\ln\left(y\right)\right)^2 - 3\,\mathrm{e}^{2\,k}\left(\sigma' y - 1\right) + 6\,\mathrm{e}^k \ln\left(y\right)\left(\sigma'^2 y^2 + 1/6 - 1/6\,\mathrm{e}^k - 1/2\,\sigma'\,y\right)}{y^3\left(\ln\left(y\right)\right)^2} \tag{3.39b}$$

Here, $k = v_P/2$, $x = v_{in}/2$, $\sigma' = 2\sigma$ and $y = 1 + e^k$.

The above expressions for α_1 and α_3 fail to provide any sufficient insight into the linearity behavior. Thus, we need to study the asymptotes of α_1 and α_3 in weak and strong inversion. Not surprisingly, the asymptotes derived from these expressions are the same as the values of α_1 and α_3 obtained while considering only weak or strong inversion operation.

The values of α_1 and α_3 are plotted as functions of inversion factor in Figures 3.8 and 3.10. Alongside, the figures also show the plots of α_1 and α_3 obtained from Harmonic Balance simulations using the EKV MOS model [10]. The match between the expressions obtained using a continuous MOS equation and reported simulation results proves the validity of the derived expressions.

3.1.5 Design Example

Following the discussion of the preceding sections, we now come up with a design approach for the optimum design of the LNA. In the current context of front-end for wireless sensor node we will design a common-gate LNA with impedance matching network.

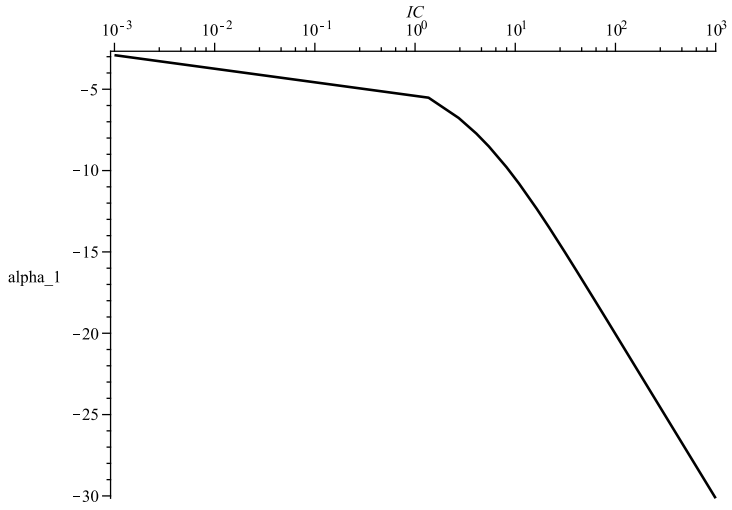

Figure 3.8: α_1 as a function of IC

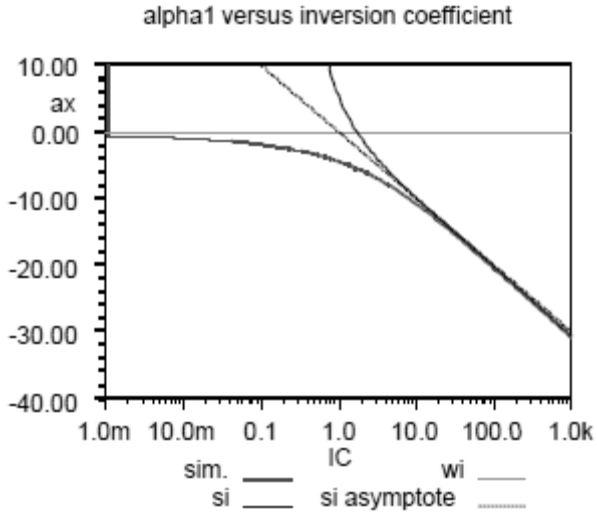

Figure 3.9: α_1 as a function of IC (simulated) [10]

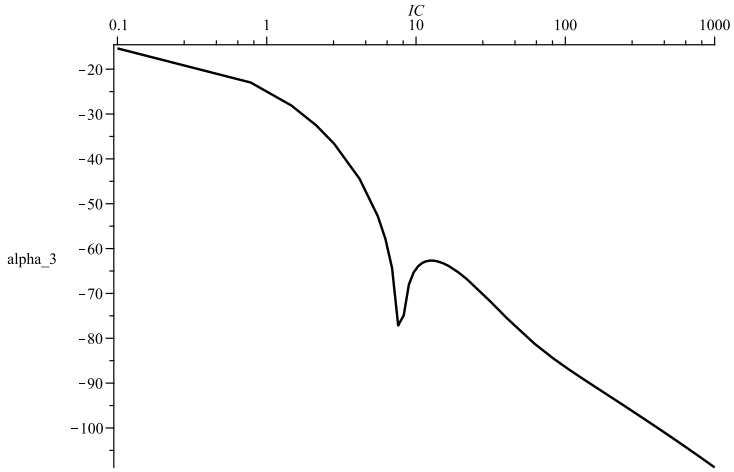

Figure 3.10: α_3 as a function of IC

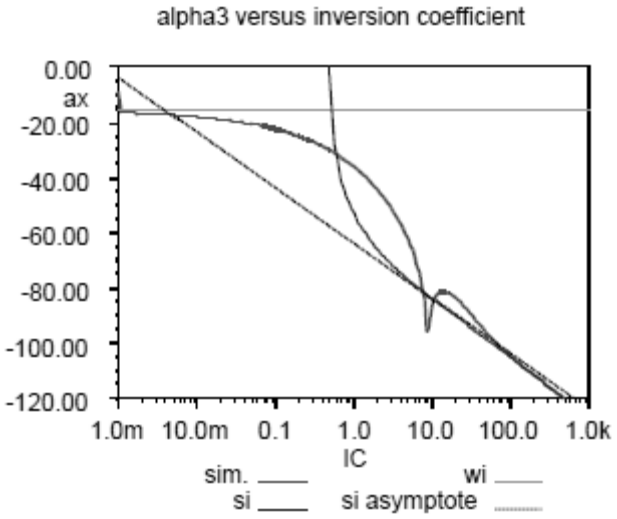

Figure 3.11: α_3 as a function of IC (simulated) [10]

Design Methodology

From the discussions in section 3.1.2 we find that the input impedance of the LNA is the least while operating in weak inversion. Thus for impedance matching with small source resistance values like 50Ω, it would be better to be working with low value of inversion factor IC. Similarly, in section 3.1.3 we find that the noise performance of the LNA is best in weak inversion with noise figure being the lowest there. However, the linearity analysis (section 3.1.4) shows that the better linearity is achieved in strong inversion. These results lead to the conclusion that the optimum operating point of the LNA (optimizing noise, linearity and impedance matching) would be somewhere in **moderate inversion**. Here follows the design procedure:

1. Given a load R_{load}, and targeting the design for a dc gain A_v, calculate the required source transconductance G_{ms} using $A_v = G_{ms} \cdot R_{load}$.
2. Choose an appropriate inversion factor IC for achieving required noise figure and linearity (moderate inversion) and calculate the drain current I_D for the calculated G_{ms}.
3. Knowing I_D and IC, size the transistor.
4. For a given source resistance R_S (50Ω) determine the Q of the matching network using eqn. 3.8.
5. Determine the values of impedance matching components L_S and C_S using 3.8.

Example

Using the above approach, here we design a common-source LNA for a gain $A_v = 20dB$, $R_load = 100k\Omega$ and assuming IC=1.

$$G_{ms} = \frac{A_v}{R_{load}} = 100\,\mu S$$

$$G_{ms} = \frac{2I_D/U_T}{\sqrt{4IC+1}+1}$$

$$\Rightarrow I_D = 4.2\,\mu A$$

$$\therefore \frac{W}{L} = 8.4$$

Using eqn. 3.8

$$Q \cong 14$$

$$L_S = 0.26\,\mu H$$

$$C_S = 0.5\,pF$$

3.2 Oscillator Design

The oscillator used in the LMV cell is a cross-coupled LC tank resonator. It is used as a local oscillator for RF down-conversion. Here we do not do adopt an analytical approach for the oscillator

and instead refer the results presented in [10]. The design equations for the cross coupled LC oscillator are given below: The critical transconductance of the diffential MOS pair for sustained oscillations

$$G_{mcrit} = \frac{2C\omega_0}{Q_L} \tag{3.40a}$$

where

$$\omega_0 = \frac{\omega_{LC}}{\sqrt{1 + \frac{1}{{Q_L}^2}}} \; with \; \omega_{LC} = \frac{1}{\sqrt{LC}} \tag{3.40b}$$

The transconductance for the fundamental component

$$G_{m(1)} = G_m \cdot \frac{a_1(x)}{x} \tag{3.40c}$$

where, x is the normalized amplitude of oscillation and $a_1(x)$ is the amplitude of the fundamental component of oscillation given by,

$$a_1(x) \cong \frac{2I_1(x)}{I_0(x) + I_2(x)} \tag{3.40d}$$

where $I_n(x)$ is the modified Bessel function of second type of order n.

Also,

$$\frac{G_{mcrit}}{G_m} = \frac{I_{crit}}{I_b} \tag{3.40e}$$

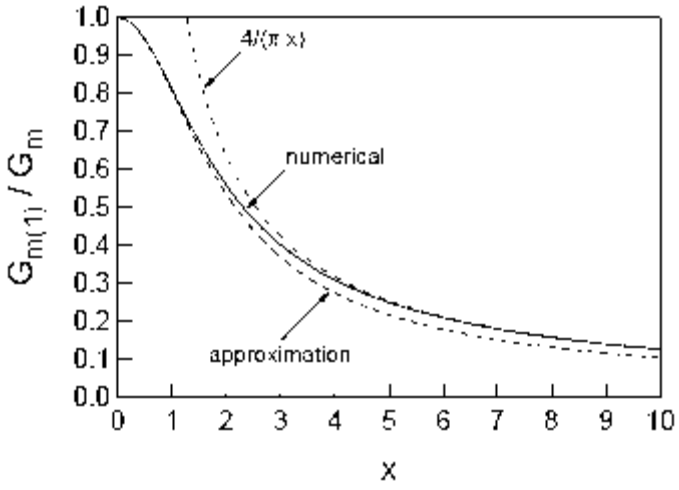

Figure 3.12: $G_{m(1)}/G_m$ vs. oscillation amplitude in cross coupled oscillator

Figure 3.12 shows the variation of $G_{m(1)}/G_m$ with respect to the normalized oscillation amplitude x in the cross coupled oscillator.

3.2.1 Design Example

We now present the design procedure for the cross coupled oscillator following it with an example.

Design Methodology

1. For the targeted technology choose a reasonable value of Q of the LC tank and a reasonable value of L.
2. Knowing the required frequency of oscillation, determine the capacitor C using 3.40.
3. With 3.40 determine G_{mcrit} knowing C and Q_L.
4. To design for a required amplitude of oscillation v_{in}, we first determine x=$\frac{v_{in}}{2nU_T}$.
5. Using figure 3.12 determine the ratio $G_{m(1)}/G_m$ for the value of x calculated in previous step.
6. With 3.40 determine the ratio I_{crit}/I_b.
7. Since $I_{crit} = 2nU_T G_{mcrit}$ obtain the tail current I_b.
8. With the current and choosing an inversion factor determine W/L.

Example

Using the above design approach we now design a cross coupled LC tank for getting an amplitude of 300 mV at 433 MHz (ISM band selected as the operating frequency for the sensor node). For the targeted 0.18 μm standard process $Q_L = 8.8$ and L=6.7 nH are reasonable values.

$$C = \frac{1}{2\pi {f_{LC}}^2 L} = 20\,pF$$

$$G_{mcrit} = \frac{2C\omega_0}{Q_L} = 6.18\,mS$$

$$\Rightarrow I_{crit} = 405\,\mu A$$

$$x = \frac{300\,mV}{2nU_T} \cong 5$$

Using figure 3.12

$$G_{m(1)}/G_m = I_{crit}/I_b = 0.3$$

$$\Rightarrow I_b = 1.35\,mA$$

$$\therefore W/L \cong 566$$

3.3 Self Oscillating Mixer with LNA

Having designed the LNA and the oscillator separately we now discuss the design of the LMV cell which would be the front-end of the receiver circuit for the wireless sensor node. However, instead of designing the LMV cell as presented in [6] and discussed in chapter 2, we will design only the *bias splitting self oscillating mixer* (see chapter 2) while replacing the bottom transistors with common gate LNA. The only foreseeable disadvantage of using this structure instead of the complete LMV cell is that the gain of this circuit is half that of the the full LMV cell.

3.3.1 Design Considerations

Figure 3.13 shows the LNA-self oscillating mixer (LSOM). In the LSOM the cross coupled LC oscillator is stacked up on the common gate LNA with the addition of the load resistance R_{load} and capacitor C_{diff} which acts a short for the LO frequency while acting as an open circuit at the down converted IF or DC. This requires a careful selection of the value of C_{diff} while also satisfying condition 2.1.

Referring back to the design examples for LNA and oscillator we see that the bias current requirement for the oscillator is much higher (1.35 mA) as compared to that of the LNA (4.2 μA). Since the two now share the current it is obvious that the current requirement of the oscillator dictates the current in the circuit and governs the design of the LNA too.

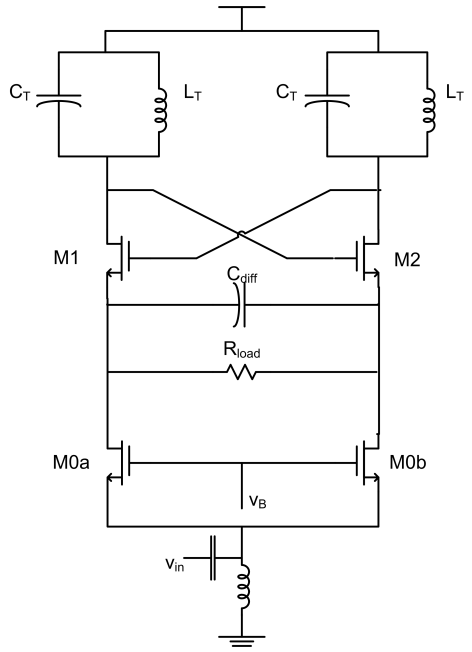

Figure 3.13: LNA-self oscillating mixer

3.3.2 Design Example

Based on the discussion and observations in the previous section, we now present a unified design procedure for the LSOM following it up with an example.

Design Methodology

1. For the targeted technology choose a reasonable value of Q of the LC tank and a reasonable value of L.
2. Knowing the required frequency of oscillation, determine the capacitor C using 3.40.
3. With 3.40 determine G_{mcrit} knowing C and Q_L.
4. To design for a required amplitude of oscillation v_{in}, we first determine x=$\frac{v_{in}}{2nU_T}$.
5. Using figure 3.12 determine the ratio $G_{m(1)}/G_m$ for the value of x calculated in previous step.
6. With 3.40 determine the ratio I_{crit}/I_b.
7. Since $I_{crit} = 2nU_TG_{mcrit}$ obtain the tail current I_b.
8. With the current and choosing an inversion factor determine W/L.
9. Choose an appropriate inversion factor IC for achieving required noise figure and linearity (moderate inversion) of the LNA and calculate G_{ms} for the the drain current $I_D = I_b/2$.
10. Knowing I_D and IC, size the LNA transistors.
11. For a given source resistance R_S (50Ω) determine the Q of the matching network using eqn. 3.8. Note that the G_{ms} will be twice the G_{ms} calculated in the previous step.
12. Determine the values of impedance matching components L_S and C_S using 3.8.
13. Targeting the design for a dc gain A_v, calculate the required load knowing the source transconductance G_{ms} by using $A_v = G_{ms} \cdot R_{load}$.
14. Choose an appropriate value of C_{diff} using 2.1.

Example

To design the LSOM we start with the design of the oscillator already presented in section 3.2.1 and using the results directly. From section 3.2.1 we have

$$f_0 = 433\,MHz$$

$$Q_L = 8.8$$

$$L = 6.7\,nH$$

$$C = 20\,pF$$

$$G_{mcrit} = 6.18\,mS$$

$$I_{crit} = 405\,\mu A$$
$$x = \frac{300\,mV}{2nU_T} \cong 5$$
$$G_{m(1)}/G_m = I_{crit}/I_b = 0.3$$
$$\Rightarrow I_b = 1.35\,mA$$
$$\Rightarrow W/L \cong 566$$

Using $L = 0.18\,\mu m$,

$$W \cong 102\,\mu m$$

Now, using $I_D = I_b/2 = 675\,\mu A$ and IC=1

$$G_{ms} = 16\,mS$$

Here, we observe that the two LNA transistors will present an input impedance of $1/2 \cdot G_{ms} = 31.25\,\Omega$. Thus, we can actually do away with the impedance matching network and choose IC appropriately so that the input impedance is $50\,\Omega$. Now,

$$G_{ms} = \frac{1}{50}\,\Omega = 20\,mS$$
$$\Rightarrow IC = 0.4$$
$$\Rightarrow W/L = 2375$$

Using $L = 0.18\,\mu m$,

$$W \cong 428\,\mu m$$

For gain $A_v = 20\,dB$, $R_{load} = 625\,\Omega$.
Using 2.1 we get

$$C_{diff}(min.) = 2.27\,pF$$

So, we choose $C_{diff} = 50\,pF$.

Figure 3.14 shows the simulation results for the LSOM circuit using LTSPICE. The results show the oscillator is self oscillating at an amplitude of 300 mV and at the same time is behaving as a mixer by down converting the 434 MHz input to 1 MHz.

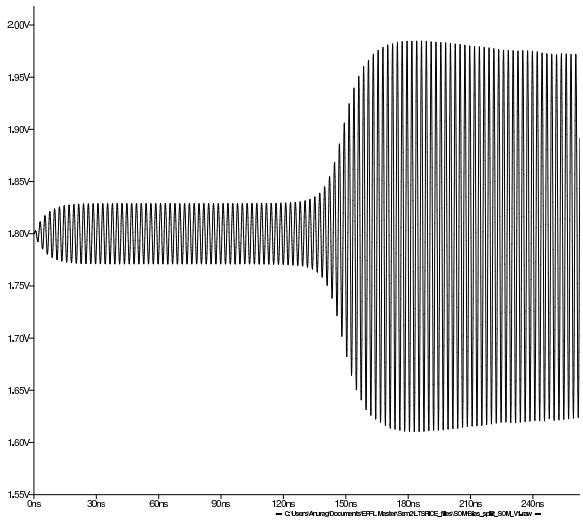

Figure 3.14: Simulation results for the LSOM showing oscillations

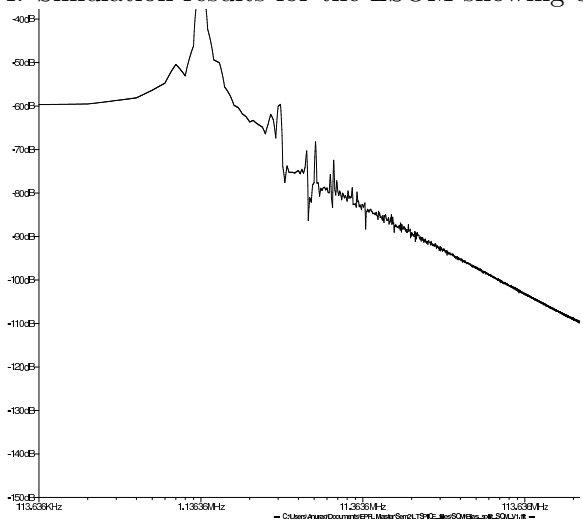

Figure 3.15: Simulation results for the LSOM showing downconversion

Chapter 4

Conclusions

4.1 Summary

In this work the design of a new topology for radio front ends has been discussed. The topology combines LNA, mixer and oscillator in a single stage by sharing current and devices among the three. The topology is thus attractive for low power applications like wireless sensor nodes which need to be energy autonomous, operating on energy scavengers like solar cells and piezo-generators.

The report presents a detailed analysis of the common-gate and common-source LNAs considering all aspects of LNA design- impedance matching, noise and linearity. All the three parameters have been expressed as functions of MOS inversion factor, with an aim of determining the optimum operating point optimizing all the parameters at the same time. Continuous expressions for the fundamental and third harmonic because of nonlinearity, valid from weak to strong inversion have been derived and have been found to agree with simulation results reported elsewhere. A brief discussion on the design of cross coupled oscillators has also been presented.

Finally, a unified design approach for the stacked topology has been developed and presented herein. The design approach has been supported with an example for the design of a 433 MHz receiver and verified with simulation.

4.2 Future Work To Be Done

Here we list down a few of the possible further analyses that could be done to enhance the understanding of the operation of the receiver front-end circuit and to optimize its performance.

- Study the behavior of the circuit by introducing separate current sources for the oscillator so that the current consumption and hence the size of the LNA is kept to the required minimum.
- Study of the complete LMV cell introducing the additional mixing transistors between the oscillator and the LNA.
- Study of the impact of load resistance on downconversion.

- Study the impact of the various types of the loads (voltage load and virtual ground load) as discussed in [6].

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