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Research Article

Isolation of III-V/Ge Multijunction Solar Cells by Wet Etching

A. Turala,[1,2] A. Jaouad,[1,2] D. P. Masson,[3] S. Fafard,[3] R. Arès,[1,2] and V. Aimez[1,2]

[1] *Institut Interdisciplinaire d'Innovation Technologique (3IT), Université de Sherbrooke, 3000 Boulevard Université, Sherbrooke, QC, Canada J1K OA5*
[2] *Laboratoire Nanotechnologies Nanosystèmes (LN2)-CNRS UMI-3463, Université de Sherbrooke, 3000 Boulevard Université, Sherbrooke, QC, Canada J1K OA5*
[3] *Cyrium Technologies Inc., 50 Hines Road, Suite 200, Ottawa, ON, Canada K2K 2M5*

Correspondence should be addressed to A. Jaouad; abdelatif.jaouad@usherbrooke.ca

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Microfabrication cycles of III-V multijunction solar cells include several technological steps and end with a wafer dicing step to separate individual cells. This step introduces damage at lateral facets of the junctions that act as charge trapping centers, potentially causing performance and reliability issues, which become even more important with today's trend of cell size reduction. In this paper we propose a process of wet etching of microtrenches that allows electrical isolation of individual solar cells with no damage to the sidewalls. Etching with bromine-methanol, the solution that is typically used for nonselective etching of III-V compounds, results in the formation of unwanted holes on the semiconductor surfaces. We investigate the origin of holes formation and discuss methods to overcome this effect. We present an implementation of the isolation step into a solar cell fabrication process flow. This improved fabrication process opens the way for improved die strength, yield, and reliability.

1. Introduction

The effective singulation of solar cells without performance and yield losses is an important issue for CPV manufacturers. Standard dicing techniques generate defects at the edges, like uncontrolled fragmentation, chipping, stress-induced cracks, debris, and heat-induced damage [1]. Such damage to the active layers may cause short-circuits or increase perimeter recombination. Stress-induced damages weaken the mechanical strength of dies and lead to structural integrity failures [1]. An alternative to avoid damages during dicing is to wet-etch trenches into the III-V layers to define the MJSC's perimeter. In the following, this is referred to as the isolation process. For single junction GaAs solar cells, an isolation process by mesa wet etching has already been demonstrated [2]. However, a single step wet-etch for MJSC has not been reported yet since the different etch selectivities of the various III-V layers building up the multijunction solar cell structure add complexity to this process. A typical multijunction solar cell (MJSC) with its subcells and tunnel junctions composed of different binary, ternary, and quaternary III-V layers is shown in Figure 1. Br_2-CH_2OH solution is a well-known nonselective etchant for nearly all III-V semiconductors [3]. This solution etches selectively III-V materials over Ge but attacks photoresist [4]. Therefore, a dielectric etching mask such as SiO_2 or Si_xN_y is necessary.

In this paper, we describe a bromine-based wet-etch isolation technique. First, we show that bromine-methanol solution causes the appearance of unwanted holes in the III-V structure underneath the dielectric mask that extend to the pn-junctions, thus reducing the solar cell performance. In a second step, we present a study on the origin of the holes and propose a method to overcome this problem. The latter was done by optimizing the dielectric mask and increasing the viscosity of the etchant. Finally, we demonstrate how this isolation process can be integrated into the MJSC fabrication and the die singulation processes.

2. Development of Isolation Process for MJSC

The simplified microfabrication process of MJSC shown in Figure 2 starts with isolating the mesa through trenches that

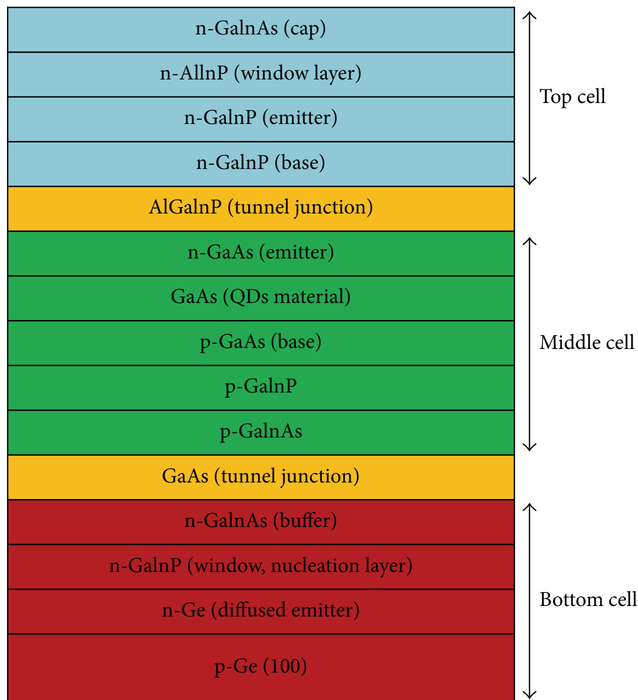
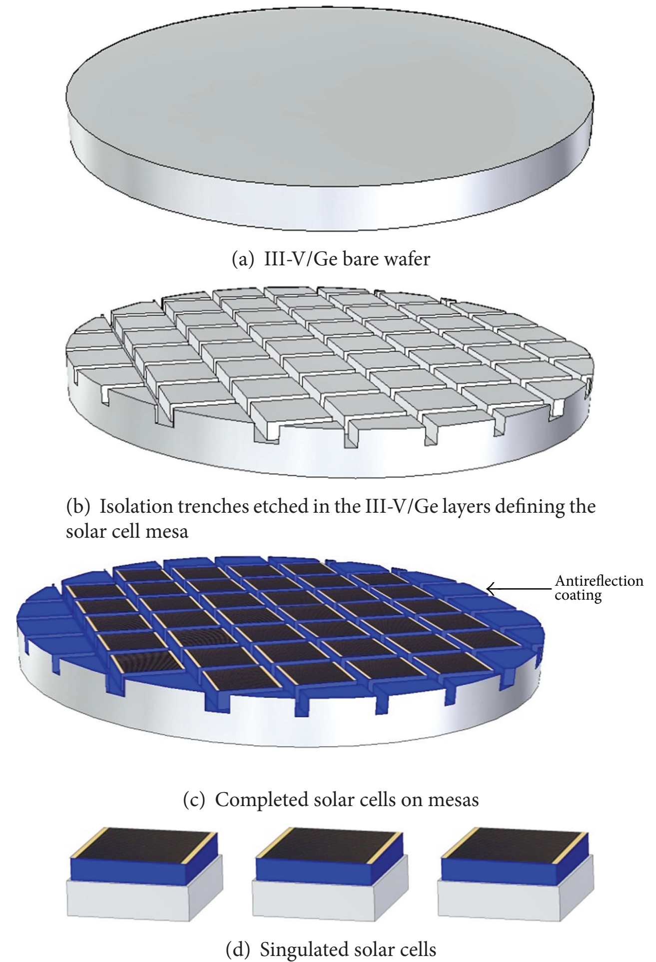


FIGURE 1: Structure of a triple junction solar cell with quantum dots (QDs) material.



(a) III-V/Ge bare wafer

(b) Isolation trenches etched in the III-V/Ge layers defining the solar cell mesa

(c) Completed solar cells on mesas

(d) Singulated solar cells

FIGURE 2: Simplified microfabrication process of isolated multijunction solar cells.

are etched down to the germanium substrate defining the perimeter of the solar cell (Figure 2(b)). Beyond this step, the solar cell microfabrication process continues with the front surface processing and electrical contact deposition (Figure 2(c)). The singulation of the cells is done by saw dicing at the end of the fabrication process (Figure 2(d)). Since the active junctions are already mesa-separated, the saw follows the paths inside the isolation trenches, cutting through the Ge substrate only. Therefore, any destructive physical contact of the saw with the sidewalls of the mesas is avoided and optimal electronic properties of the sidewalls are obtained. The isolation process involves an extra deposition, lithography, and etching steps. In order to define the isolation trenches, a 100 nm SiO_2 mask was deposited by plasma enhanced chemical vapor deposition (PECVD) on the front surface, which was then patterned by photolithography and subsequently etched with a buffered oxide etchant (BOE). After stripping the remaining photoresist, the samples were immersed in the chemical solution for deep trenches etching.

2.1. Formation of Small Holes during Bromine-Methanol Etching of III-V Layers. The samples were immersed in a bromine-methanol (Br_2-CH_2OH) solution having a bromine concentration of 1%. Etching was performed at 20°C. The solution was prepared by adding bromine to the alcohol and left for the time necessary for temperature stabilization. Due to the volatility of bromine, the solution mixture is covered during the etching and no agitation is used in order to minimize bromine evaporation. The scanning electron microscope (SEM) image in Figure 3 shows that the solution etched through the whole III-V structure of the MJSC with an average rate of 1 μm/min. A profile with multiple slopes was observed, indicating some residual crystallographic orientation dependence of this non-selective isotropic etch on the different layers. Further investigation by optical microscopy and cross-sectional SEM revealed randomly distributed small holes in the III-V layers, localized underneath the dielectric mask.

This is confirmed by Figure 4(a), where holes are observed through the transparent SiO_2 layer. As seen in this image, the holes may have different sizes. The microscopic and profilometric analysis of the SiO_2 mask let us conclude that no damage to the dielectric film was done due to the bromine-methanol etching. Figure 4(b) shows a cross-sectional view of a hole observed following the etching step. It can be seen that the SiO_2 film remains suspended as a membrane. The hole presented in this figure has a depth of few hundred nanometers and punches through the cap layer, the window layer, the emitter, the pn-junction, and the base of the top subcell of a MJSC presented in Figure 1. The holes depth varies randomly from several nanometers to a few micrometers and may reach through the entire III-V heterostructure down to the Ge substrate. The observed

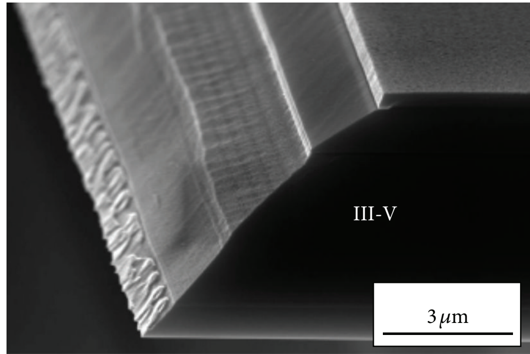
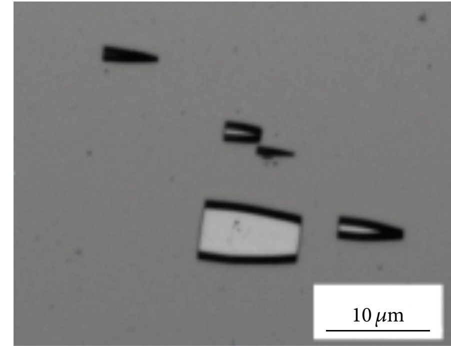
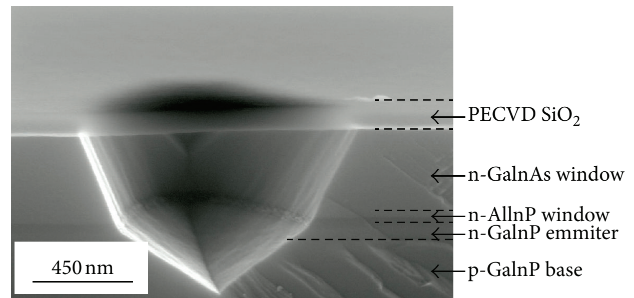


Figure 3: SEM image of solar cell sidewall after bromine-methanol etching.



(a) Top view image showing the holes through the transparent SiO_2 mask



(b) Cross-sectional SEM image of a heterostructure containing a hole

Figure 4: Holes in the III-V layers underneath the intact SiO_2 mask.

holes in the III-V layers could cause increased surface recombination and could lead to short-circuits across junctions if localized under the metallic contact electrode. Since these effects are likely to deteriorate the performance of solar cells or the yield of a production process, it was necessary to find the root cause and eliminate the issue of small holes.

2.2. Influence of the Substrate on Hole Formation. In order to determine the permeability to liquid etchants of as-deposited, PECVD SiO_2 films, a set of silicon (Si), indium phosphide (InP), and gallium arsenide (GaAs) substrates were coated with 100 nm of SiO_2, deposited under the same conditions as used in the previous experiment. These samples were then exposed to the suitable liquid etchant for each substrate: the SiO_2/Si sample to concentrated potassium hydroxide (KOH) and the SiO_2/GaAs and SiO_2/InP samples to a piranha solution ($H_2SO_4 : H_2O_2$ (3 : 1)). Subsequent to immersion, measurements by spectroscopic ellipsometry were carried out and confirmed that the thickness of the SiO_2 layer had not changed. Furthermore, microscopic observation showed no damage neither to the dielectric layer nor to the substrate's surface. This suggests that the SiO_2 layer deposited on GaAs, Si, and InP substrates acts as a good barrier for KOH and $H_2SO_4 : H_2O_2$.

In a further part of the experiment, series of GaAs, InP, and III-V/Ge triple-junction structure samples were coated with a 100 nm thick SiO_2 mask and then exposed to the Br_2-CH_2OH (1 : 100) for the duration necessary to complete mesa etching on a patterned III-V/Ge solar cell structure. Holes were not found in the SiO_2 mask nor in the GaAs or InP wafer, as determined by optical microscopy. The SiO_2 layer thickness remained unchanged as measured by ellipsometry. However, holes were visible in the III-V layers of the solar cell structure. It is therefore most likely that the holes in the III-V layers of the solar cell wafer are caused by diffusing etchant through pores or tiny cracks in the SiO_2 layer that cannot be seen under the microscope.

The results of this experiment lead us to conclude that the permeability of a SiO_2 mask to bromine-methanol solution is strongly affected by the intrinsic properties of the underlying substrate. Br_2 diffused only through the oxide deposited on solar cell structure, which suggests that the complex nature of III-V/Ge heterostructures reduces the diffusion resistance of the PECVD deposited film.

2.3. Influence of the SiO_2 Mask Layer Thickness on Hole Formation. In order to check if the permeability of the SiO_2 mask to Br_2-CH_2OH (1 : 100) is related to its thickness, III-V/Ge samples were coated with SiO_2 films with thicknesses ranging from 50 to 400 nm and then exposed to the bromine-methanol. Microscopic observations revealed that the density of holes in the III-V layers did not decrease with increasing SiO_2 mask thickness. Note that the 400 nm SiO_2 layer delaminated after its deposition, indicating strong intrinsic stress. Therefore, although no clear tendency in terms of hole density versus mask thickness could be distinguished, we conclude that stress could play an important role in the hole formation in the III-V layers of solar cell structures.

2.4. Influence of Stress in the Dielectric Mask on Hole Formation. Since the stress in the dielectric mask deposited on the III-V/Ge structure affects the formation of the small holes, the intrinsic stress of different dielectric layers was evaluated. It is known that this stress is influenced by PECVD parameters, such as the plasma frequency. A STS MESC Multiplex CVD reactor was used to deposit 100 nm of SiO_2 and silicon nitride (Si_xN_y), each at low (380 kHz) and high (13.56 MHz) frequency, on silicon wafers. Subsequently, the intrinsic stress of the four thin films was determined by the standard wafer bow

technique [5], which is based on the measurement of wafer curvature before and after film deposition. Wafer curvature was measured using a Veeco Dektak 150 profilometer. Table 1 lists the results. In the two SiO_2 layers the intrinsic stress is compressive and increases one order of magnitude when the deposition frequency is changed from 380 kHz to 13.56 MHz. Also Si_xN_y is compressively stressed when deposited at low frequency but tensile stressed if the layer is deposited at high frequency.

After the intrinsic stress of the different dielectric masks was characterized, III-V/Ge samples were coated with these layers and etched in the bromine-methanol solution. Holes were found underneath all four dielectric masks in the III-V layers, but the density varied as seen in Table 1.

Generally, samples coated with Si_xN_y show a lower hole density than SiO_2-coated ones, regardless of the stress nature and value. This is most likely due to its higher density compared to SiO_2. The largest hole density is found on the sample that was masked with the dielectric having the strongest compressive stress. The lowest value is achieved using a tensile-stressed layer. Note that this Si_xN_y layer, deposited at high frequency, is less dense than the one deposited at low frequency. This suggests that stress plays a more important role in the formation of holes during etching than the layer density. In order to understand how the intrinsic stress of the dielectric mask influences the formation of small holes in the III-V layers, a study of the bowing of MJSC wafers was done. The epitaxial MJSC wafers used had an Si_xN_y-coated back side. The bowing data obtained by profilometry is displayed in Figure 5. The curves were normalized with respect to the maximum deflection measured in the center of a MJSC (III-V/Ge) bare wafer, represented by the curve (c). A bare Ge wafer that served as a reference shows no bowing as seen from curve (a). A convex bowing for the III-V/Ge wafer is observed (curve (b)) which becomes more pronounced when the back side Si_xN_y layer is removed (curve (c)). From that, we conclude that the growth of the III-V materials on the Ge wafer introduces compressive stress resulting in a convex bowing of the wafer that is partially compensated by the Si_xN_y layer on the back side. Further reduction of this stress is achieved by depositing a tensile stressed Si_xN_y layer on top of the III-V/Ge structure as shown in curve (d). Due to the compressive stress of the III-V/Ge structure the deposition of an intrinsically compressively stressed SiO_2 on top of it leads to a large residual stress in SiO_2. This stress could cause small cracks and pinholes in the dielectric, providing diffusion paths for the bromine-methanol solution, and finally lead to the formation of small holes underneath the etching mask. This is in good agreement with the results of experiments presented in Section 2.2, which demonstrated that only the III-V/Ge substrates with high residual stress are affected by the problem of holes in contrast to nonstressed GaAs, InP, and Si substrates. Therefore, we conclude that an interaction of these factors—the compressively stressed III-V/Ge wafer, the compressively stressed SiO_2 mask, and the diffusion of etchants through the mask—is the root cause of the formation of the small holes in the III-V layers during a bromine-methanol linebreak etching.

2.5. Through-Mask Diffusion Minimization via Utilization of Stress-Compensating Dielectric Mask. According to the results above, the key for reducing the holes in the III-V layers during bromine-methanol etching is to avoid strong compressive stress in the dielectric mask. This can be done by depositing a compressively stressed layer on the back side of the wafer prior to the front side mask deposition. The wafer bowing will be reduced as well as the residual stress in the front mask, even if intrinsically compressively stressed. Indeed, a III-V/Ge structure coated with a compressively stressed layer on the back side and 100 nm thick SiO_2 mask (deposited at high frequency) on the front side showed a much lower hole density after exposure to the bromine-methanol solution. However, since the back side deposition occurs prior to the etch mask deposition on the front side, the latter could be contaminated with unwanted particles due to contact with the sample holder in the PECVD reactor. The presence of particles could lead to regions not protected by the mask causing etchant infiltration of the III-V layers.

A second approach to reduce the compressive stress in the dielectric mask is to deposit an intrinsically tensile-stressed layer on the front side of the bowed III-V/Ge wafer. As a result, the residual stress in the MJSC wafer is minimized and such stress-compensating layer can act as a dielectric mask for the etching. With increasing thickness of a tensile-stressed Si_xN_y mask on the front side of the wafer, its bowing decreases leading to a higher resistance to the diffusion of etchants. The samples with such a front side stress-compensating mask exhibited a minimal number of holes after etching in bromine-methanol solution.

2.6. Through-Mask Diffusion Suppression via Increased Viscosity of Etching Solution. The previous experiments demonstrated that the diffusion of the etchant through the mask can still occur even if residual stress in the dielectric mask is significantly reduced. Therefore, further optimization of the process was performed to reduce the diffusivity of the etching solution through the mask. Lower penetration depth can be achieved by replacing the bromine-methanol with the bromine-isopropanol. Due to the higher viscosity of isopropanol compared with the methanol (2.4 mPa·s and 0.59 mPa·s at 20°C, resp.), the penetration of the bromine etching solution through the dielectric mask is reduced. This etching process also seems to be more stable due to the lower volatility of isopropanol which improves the process reproducibility. However, in order to maintain the same high etch rate (1 μm/min) as for the methanol-based solution, the concentration of Br_2 was increased. Therefore, experiments were conducted with bromine concentration of 10% by volume. As previously, the solution was kept in covered vessels to maintain the bromine concentration and was left for temperature stabilization after preparation. The etching was performed at ambient temperature, without agitation.

To study the effect of using different solvent in etching solution, III-V/Ge structures were coated with a 100 nm compressively stressed SiO_2 layer, as used for the experiments in Sections 2.1 to 2.3, and immersed in the etching bath. Using

Table 1: Hole density for different thin dielectrics used as etching mask.

Dielectric material	Radio frequency	Nature of intrinsic stress (on Si)	Value of intrinsic stress (on Si) (dyn/cm^2)	Hole density (cm^{-2})
SiO_2	380 kHz	Compressive	-2×10^9	310
SiO_2	13.56 MHz	Compressive	-2×10^{10}	870
Si_xN_y	380 kHz	Compressive	-7.6×10^9	160
Si_xN_y	13.56 MHz	Tensile	$+5.2 \times 10^9$	60

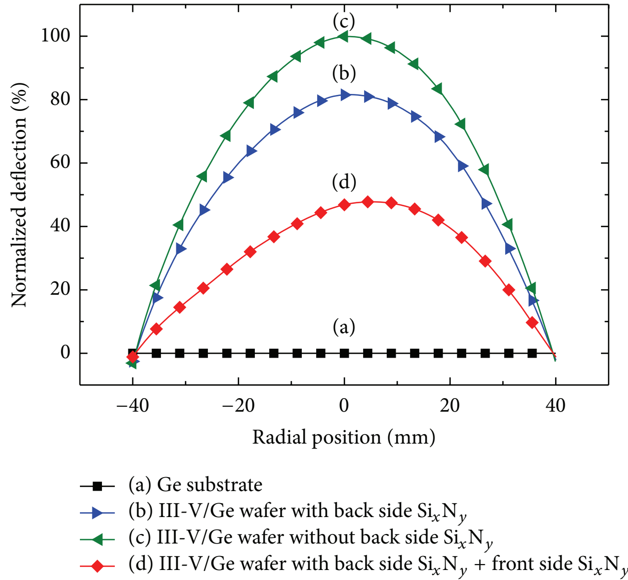


Figure 5: Normalized deflection measured by profilometry: (a) Ge substrate, (b) III-V/Ge wafer with Si_xN_y coating at the back side, (c) III-V/Ge wafer for which the Si_xN_y coating at the back side was removed and (d) III-V/Ge wafer with Si_xN_y coating at the back side and tensile Si_xN_y film on the front side.

bromine-isopropanol instead of bromine-methanol for the etching of the III-V layers resulted in a substantial decrease (two orders of magnitude) in hole density.

Finally, the optimization of the etching process was completed by combining the high-viscosity isopropanol-based solution with a stress-compensating Si_xN_y etching mask. Patterned test MJSC wafers did not show any etchant diffusion-related holes or other damage, confirming that this method can be used to wet-etch mesa-isolation trenches into the active III-V layers.

3. Implementation of the Developed Isolation Process into Microfabrication of MJSC

The proposed wet-etch isolation process for III-V/Ge solar cell structures can easily be implemented in the MJSC microfabrication. To demonstrate this, we fabricated solar cells using InGaP/GaAs/Ge wafers provided by Cyrium Technology Inc. [6]. The process is shown in Figures 6(a)–6(i). The III-V/Ge wafer (Figure 6(a)) is initially characterized by compressive stress. As shown earlier, the deposition of a stress-compensating Si_xN_y mask can reduce this stress. Therefore, 350 nm of Si_xN_y was deposited on the front side of the wafer (Figure 6(b)). Photolithography was used to define the isolation trenches that were etched into the Si_xN_y mask by buffered oxide etchant (BOE) (Figure 6(c)) and transferred into the III-V layers by etching with the optimized bromine-isopropanol solution.

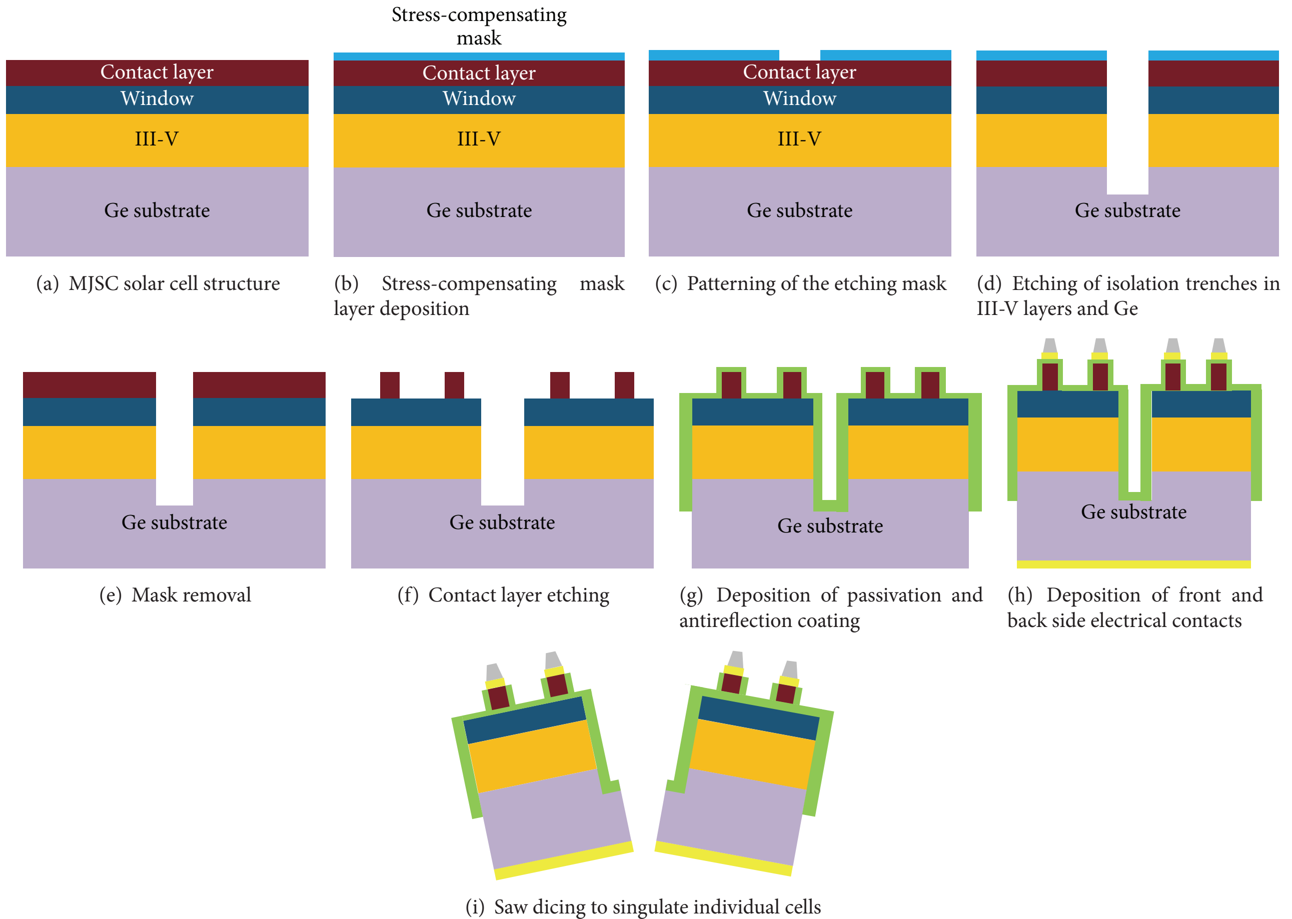
Supplementary etching by hydrogen peroxide into the Ge emitter (typically less than 1 μm) was necessary to isolate the Ge bottom cell and complete the isolation of the entire MJSC (Figure 6(d)). Afterwards, the Si_xN_y mask was removed by BOE (Figure 6(e)). Another photolithography step was carried out to align the cap layer used to make the ohmic contact with the front metal grid fingers to be deposited later. Nonprotected regions were etched away, exposing the AlInP window (Figure 6(f)). Subsequently, the front surface and the sidewalls of the etched trenches were coated with a SiO_2/Si_xN_y bilayer, which is optimized for its antireflective [7] and passivating [8] properties (Figure 6(g)). The micro-fabrication process was completed by depositing electrical contacts on the front and back side (Figure 6(h)). Finally, the isolated solar cells were separated by saw dicing along the isolation trenches through the Ge substrate (Figure 6(i)).

Figure 7 shows a SEM top view image of the edge of a singulated solar cell fabricated with a process with the isolation step included. As seen in this image, the damage induced by dicing is confined to the saw path in the passive region of the Ge substrate. This is due to the fact that saw passes in the middle of the trenches, never approaching the facets of III-V layers. The facets remain smooth and intact which suggests their good surface quality, as seen in Figure 7. The mechanical damage to the Ge substrate outside of active region does not affect the performance of the solar cell.

For validation, these solar cells were tested for their functionality with a solar simulator showing good electrical characteristics with no signs of abnormal behavior.

4. Isolation Process for Die Singulation and Packaging

Singulation of brittle and thin wafers such as III-V solar cells grown on Ge substrates remains a challenge. Commonly used scribe and break techniques involve a two-step process. A scribe line is created to establish a stress concentration factor for crack initiation in the following breaking step. Typical scribing methods exploit diamond scribing, diamond blade sawing, or laser scribing. Those techniques may have a negative impact on the die yield and performances of solar cells,



(a) MJSC solar cell structure

(b) Stress-compensating mask layer deposition

(c) Patterning of the etching mask

(d) Etching of isolation trenches in III-V layers and Ge

(e) Mask removal

(f) Contact layer etching

(g) Deposition of passivation and antireflection coating

(h) Deposition of front and back side electrical contacts

(i) Saw dicing to singulate individual cells

FIGURE 6: Process flow of III-V/Ge solar cell fabrication including the developed isolation step.

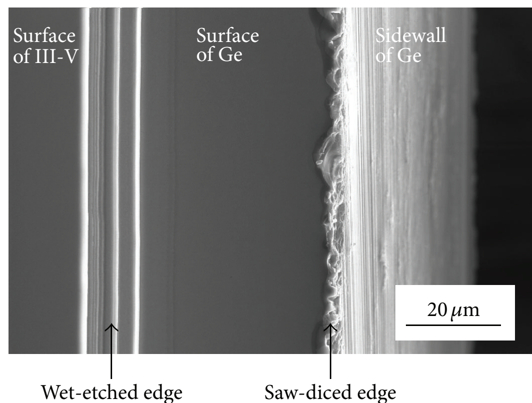


FIGURE 7: Top view SEM image of a sidewall of an isolated solar cell after singulation.

due to thermal or mechanical stress concentration introduced locally to the dies. The proposed technique of isolation by wet etching has a number of advantages. When included in the fabrication process, wet etching minimizes microcracks and fractures leaving smooth sidewalls for passivation with a hard dielectric coating. This provides added protection from environmental conditions and also from accidental short-circuits of the junctions with the solder during the die attach step. In contrary to typical scribing techniques, the proposed chemical isolation does not introduce local stress (neither mechanical nor thermal), increasing therefore the mechanical strength of the die. No damage is done to the surface during this process, no debris is generated, no hazardous materials like V group elements from III-V compounds are emitted in the air, and consequently, no special post-dicing treatment is necessary. This process shows also potential for "dicing by substrate thinning" that could eliminate the necessity of saw dicing. Finally, isolation as in-parallel processing could have a positive economic impact on solar cell wafer manufacturing if the added cost of processing due to supplementary lithography, PECVD deposition, and etching is compensated by higher yield and potentially higher performance and reliability.

5. Conclusion

We reported on a single step wet-etch isolation process for III-V/Ge wafers with a bromine solution. MJSC were fabricated incorporating the isolation step into their microfabrication process. It was demonstrated that etching with the standard,

bromine-methanol solution results in the formation of holes in the III-V layers due to the diffusion of bromine through the dielectric mask. We have demonstrated that this diffusion is related to the defects induced in the dielectric mask during plasma deposition by the high compressive stress in the III-V/Ge structure. These defects, which act as a diffusion path for bromine during wet etching, could be suppressed using a stress-compensating thin film as etching mask and a high-viscosity bromine-isopropanol solution.

The demonstrated isolation technique opens the way for improved performance and reliability of individual solar cells due to its capability of producing damage-free, smooth side-walls and possibility of passivation with a dielectric PECVD film. Work is in progress to quantify the enhancement in solar cells performance, fabricated with this process.

Acknowledgments

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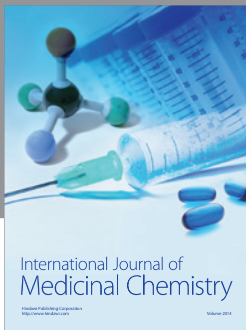
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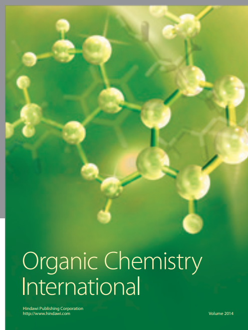
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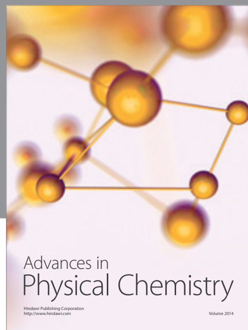
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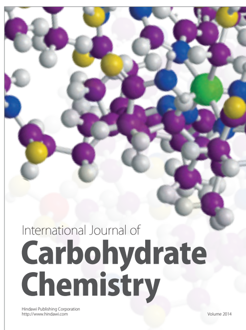
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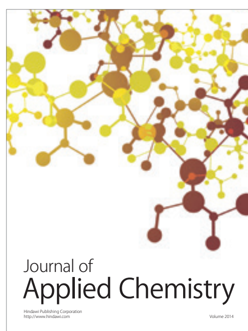
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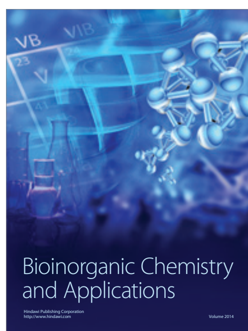
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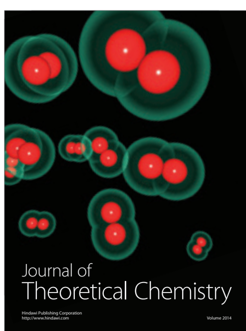
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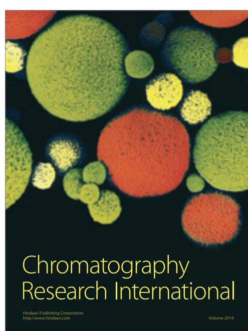
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