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DIODE PARAMETER DETERMINATION APPLIED TO LDD-MOSFETs FOR DEVICE CHARACTERIZATION

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The electrical properties of the drain-substrate diode of MOSFETs are shown to be related to the device geometrical structure. The two dimensional analysis takes into account the edge effects of the length and width of the gate. Intrinsic parameters are extracted from current-voltage characteristics and obtained dependent on these dimensions.

Keywords: drain-substrate diode; intrinsic parameters; current-voltage characteristics

1. INTRODUCTION

The general mode of operation of Metal-Oxide-Semiconductor Field Effect Transistors has been discussed extensively in the literature [1]. Power MOSFETs using double-diffused metal-oxide-semiconductor (D-MOS) technology have higher switching speeds than bipolar transistors [2], a negative temperature coefficient of carrier mobility which reduces the potential for thermal runaway and in addition they have simpler input drive requirements than bipolar transistors. They have overtaken bipolar transistors in overall performance.

With the continuous scaling down of MOSFETs devices for very large scale integration, a degradation of their electrical properties

appears under normal operating conditions. Published works [3, 4] have discussed this degradation in terms of interface-states and of oxide trapping sites. They are based on the presence of very high fields in micronic MOS structures which increase carrier injection into the thermally grown silicon dioxide layer (SiO_2) used as the gate isolator. The high electric field causes the generation of states at the silicon-oxide interface and of trapping sites in the oxide layer.

The aim of this work is to show modifications of the structural properties of the devices which are enhanced by the decrease of its size. The electrical parameters of the substrate-drain junction of MOSFETs are obtained related to the layer dimensions and the analysis of the junction current-voltage characteristics enables us to discuss the contributions of diffusion and recombination currents to the total current. These results introduce a new method for micronic device characterization.

2. METHOD

This study has been performed with *n*-channel LDD MOSFETs, *n*-doping regions are introduced between channel and *n*+ source and drain diffusions (Fig. 1).

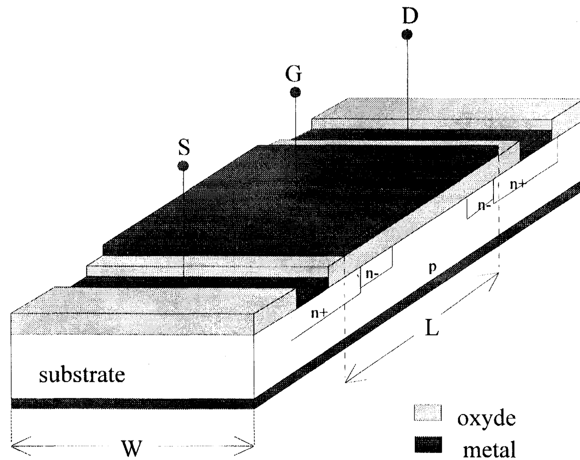

FIGURE 1 3D structure of a *n*-channel LDD-MOSFET (not to scale).

The same wafer contains transistors with different gate sizes referred to their length (25 µm and 0.8 µm) and to their width (25 µm and 1.4 µm) for each length value. All gates and drains can be individually accessed.

When a sufficiently large positive voltage, V_G, is applied to the gate ($V_G > V_T$ where V_T represents the threshold voltage), the conduction band at the oxide-semiconductor interface is brought close to the Fermi level and the surface of the *p* substrat region becomes inverted. An inversion layer is formed and constitutes a region of high conductivity called the channel. Hence, when the drain is positively biased, a current can flow from drain to source. For the direct bias transistor, the substrate-drain is reversed biased and the thermally dependent saturation current flows through it.

The method we used is based on extraction of device parameters from the substrate-drain junction experimental current-voltage curves. For these experiments, the transistor is reversed biased i.e. the source terminal is made positive with respect to the drain. The substrate is connected to the source. The substrate-drain diode is forward biased. Figure 2 shows the experimental setup and the applied bias used to characterize the substrate-drain junction. Current-voltage characteri-

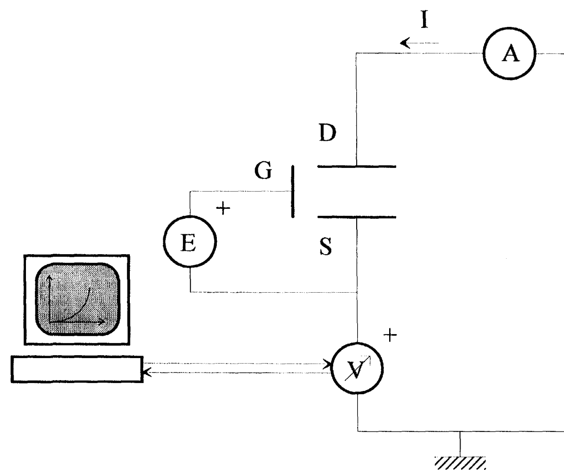

FIGURE 2 Diagram of a transistor biased for substrate-drain junction characterization.

tics of the diode are obtained by a computer driven acquisition system. Current (I) and voltage (V) values of one hundred points of I-V characteristics are used for the modeling analysis of the diode. Physical and electrical parameters are extracted from a theoretical description of the current-voltage characteristics for each substrate-drain diode of all transistors. This procedure has been used [5] to study radiation induced defects in field effect transistors.

The characterization of the substrate-drain junction is performed under low voltage operating conditions with a gate voltage lower than the threshold voltage value V_T. This is to insure the characterization of recombination phenomena in the junction since when the channel turns on, the diode effect disappears and the drain-to-source current flows via the channel.

Models of the silicon p-n junctions are reasonably well developed. I-V characteristics of the junction can be described by a first order single exponential model (SEM) or a second order double exponential model (DEM) with the equation [6]:

$$I = \frac{V + R_s I}{R_{sh}} + I_{01}\left[e^{\frac{q}{kT}(V+R_s I)} - 1\right] + I_{02}\left[e^{\frac{q}{nkT}(V+R_s I)} - 1\right] \qquad (1)$$

These models introduce the series resistance R_s to take into account the power losses, the shunt resistance R_{sh} for the leakage currents and the diode ideality factor n. currents I_{01} and I_{02} are the two components of the diode reverse currents.

The SEM model (where $I_{01} = 0$) gives a global description of the physical processes in the operating diode. For an ideal junction $n = 1$ and the reverse diffusion-recombination current I_{02} is low (its area-normed value is of the order of $10^{-14}\,\mathrm{Acm}^{-2}$) which implies a predominant diffusion process. Values of the ideality factor n greater than unity [7] are related to carrier recombination via traps. The increase of n is correlated with an increase of the reverse I_{02} current.

The DEM model ($I_{01} \neq 0$ and $I_{02} \neq 0$) separates electronic diffusion-recombination phenomena (I_{01}) in the quasi-neutral regions of the junction from recombination in the space-charge region (I_{02}).

3. RESULTS AND DISCUSSION

Figure 3 shows the characteristics of the substrate-drain junction for transistors with different structures where the gate length (L) and width (W) are indicated. For large values (25 µm) of W, the evolution is sensitive to a decrease of the channel length from 25 µm to 0.8 µm but that is not so much the case when the channel width is of the order of a 1 µm. This and since the length of the channel is only related to the modification of the depleted part of the substrate-drain junction near the drain, and so acts only to a second order on this junction structure. This result is observed with the diffusion-recombination current values which are increased by a factor of 10 for large W values but has no significant change for the case of the smaller width.

The ideality factor increases when the gate width decreases from 25 µm to about 1.4 µm (Fig. 4). A comparative lower influence of L values is again observed. This increase of the ideality factor reflects an increase of carrier recombination in the diode space charge region and

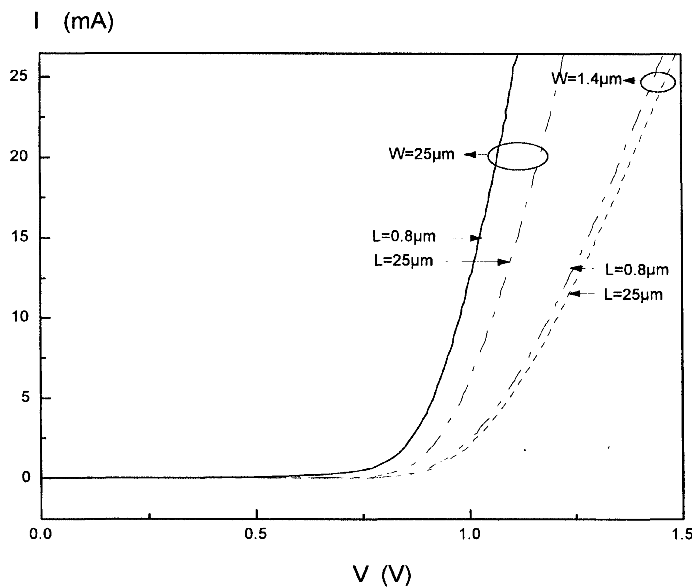

FIGURE 3 I-V characteristic of the substrate-drain junction for different gate lengths (L) and widths (W) and for $V_G = 0$ Volts.

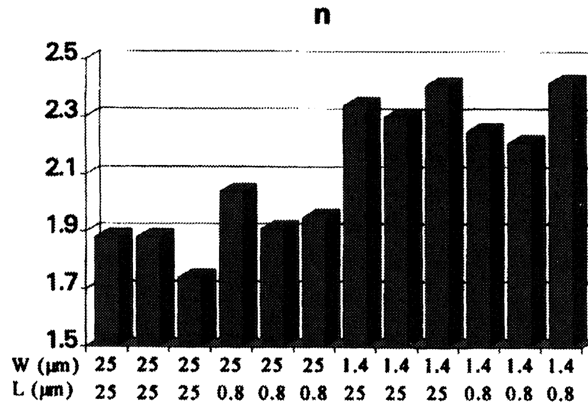

FIGURE 4 The ideality factor of the substrate-drain junction for different gate lengths (L) and widths (W).

at the oxide-semiconductor interface. For very small surfaces, the technological doping process leads to less uniform levels than for larger surfaces, and the edge effects, which are related to high default (broken bonds) concentrations, are more sensitive for the former than for the later. These effects lead to a high contribution of the recombination current to the reverse diode current. This is confirmed by an increase of I_{02} reverse current. A lower quality junction is then

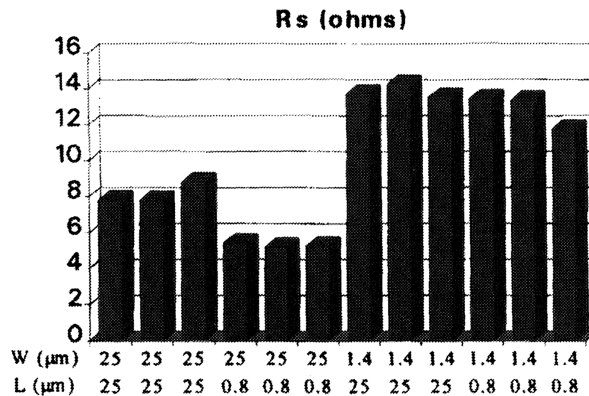

FIGURE 5 The series resistance of the substrate-drain junction for different gate lengths (L) and widths (W).

obtained. The electrical field has an influence on recombination processes since high electrical field values in the oxide layer make the oxide traps to move and exchange charges with the silicon. This implies a decrease of oxide-silicon interface trapped charges with an increase of carrier recombination.

The two geometrical parameters W and L have an influence of the series resistance R_s as it is shown in Figure 5. This result could be expected because of the modifications of the drain current flow surface as a consequence of the device gate dimensions.

4. CONCLUSION

An experimental method for studies of MOSFETs junctions has been described. The effect, on the substrate-drain junction properties, of a decrease of both the channel length and the channel width for micronic devices, has been pointed out. Structural parameters have been extracted and a two dimensional analysis has shown that the method is powerful for the device characterization.

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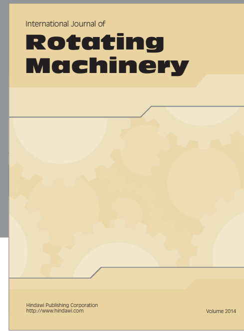
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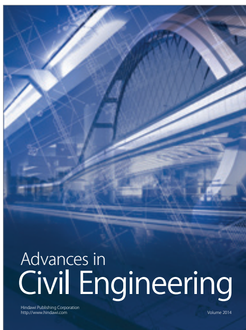
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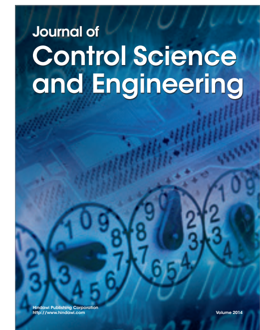
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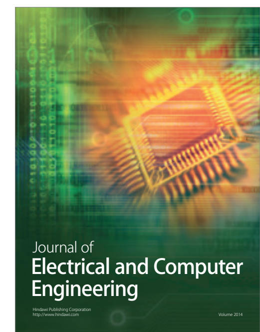
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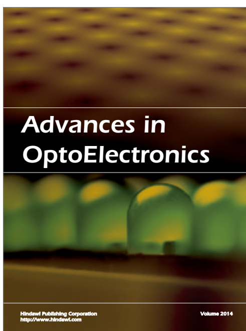
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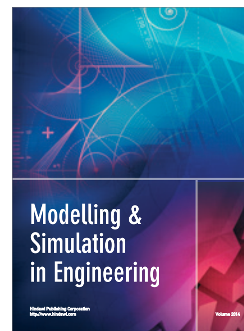
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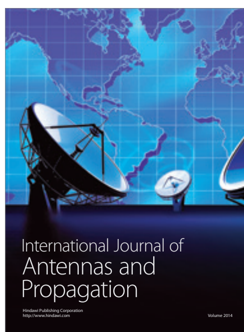
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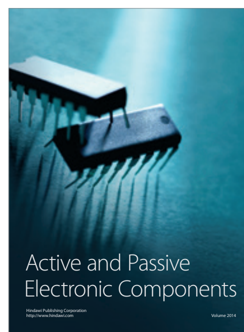
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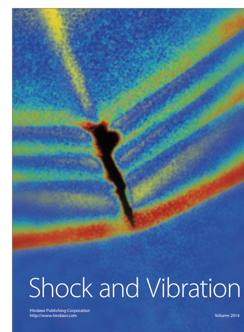
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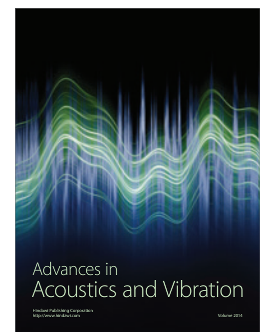
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