Folded-Cascode Transimpedance Amplifiers Employing a CMOS Inverter as Input Stage

Elton N. Lima[2], José Luís Cura[1,2], Luís Nero Alves[1,2]
[1]Dpt. Eletrónica, Telecomunicações e Informática, Universidade de Aveiro, Campus de Santiago, Aveiro, Portugal
[2]Instituto de Telecomunicações, Campus de Santiago, Aveiro, Portugal
picassokil@hotmail.com, jlc@ua.pt, nero@av.it.pt

***Abstract*— This paper presents the design and comparison of two shunt feedback transimpedance amplifiers (TIAs) implemented in standard 350nm CMOS technology from Austria Microsystems. These transimpedance amplifiers are based on a folded cascode topology. The first one is a conventional folded-cascode (CFC-TIA) and the second is a modified version folded-cascod (MFC-TIA) employing a CMOS inverter at the input stage. The proposed MFC-TIA achieves a gain of 80dBΩ, 370MHz bandwidth and minimum input current noise of 1,6pA√Hz with 0.5pF total input capacitance. The achieved results show that MFC-TIAs can match the performance of CFC-TIAs with reduced implementation area, thus being a suitable solution for photo-detector array receivers.**

I. INTRODUCTION

Transimpedance amplifiers are widely used in optical communications systems where the detected signal needs to be converted from current to voltage domains. With the growing demand for higher data rates in optical communications networks, transimpedance amplifiers (TIAs) are usually recognized as the critical building block at the optical receiver side. This is due to the fact that the front-end amplifier needs to comply with stringent requirements demanding high gain, high bandwidth, low input equivalent noise and high dynamic range [1]. Gain and bandwidth are constrained by the gain-bandwidth product of the technology, implying that, there is a necessary tradeoff between gain and bandwidth. For these amplifiers, the situation is even more dramatic, since, the photo-detector generally impairs the bandwidth at the input of the amplifier. PIN photodiodes (PDs) are usually selected as photo-detector devices. These PDs are operated under reverse bias conditions, implying that their intrinsic capacitance varies with the reverse voltage applied. The association of the PDs capacitance and the amplifiers input impedance acts as an input pole, usually impairing bandwidth. TIA configurations employing shunt-shunt feedback topologies are usually selected due to their relatively low input impedance, which is able to mitigate the effect of the PDs intrinsic capacitance [1].

Several methods have been proposed to extend the bandwidth in these amplifiers. Inductive peaking [2] is probably the most common used technique in which the inductors are placed in strategic circuit locations, resulting in resonance phenomena with parasitic capacitances and larger bandwidths. The use of inductors to extend amplifiers bandwidth has some drawbacks: i) it occupies a large chip area, making inappropriate for high density designs; ii) substrate coupling increases through the inductors, resulting in higher crosstalk; iii) integrated inductors are difficult to design, usually demanding high efforts on modeling and parasitic extraction; and iv) design kits provide a reduced number of inductance values. Another method consists of capacitive peaking [3] that resorts to capacitive effects able to extend the bandwidth. Capacitive peaking implies the usage of feedback, where the added capacitance acts as an auxiliary pole which can be explored to improve bandwidth.

Other solutions resort to circuit level techniques [4, 5]. These techniques are suitable for both gain and bandwidth improvement. Circuit level techniques are able to produce interesting bandwidth enhancement effects. For example, the common-gate configuration has low input impedance which is desirable to mitigate the effect of the large input parasitic capacitance on the bandwidth. Common gate stages are also useful when combined with a common source input stage. This is the basis of the well-known cascode configuration [4-6]. Variations of cascode configuration, aiming for enhanced performance under low voltage bias, resort to folded-cascode (FC) [6], and regulated cascode (RGC) configurations [4, 5].

This paper presents a variation on FC configuration with a CMOS inverter as input stage. This modification allows matching the performance of conventional FC circuits with reduced implementation area, a feature suited for photo-detector array receivers, where each detector needs an amplifying stage [7]. Power consumption increase due to the operation of the CMOS input stage. Performance comparison is addressed using two TIAs, one employing a conventional FC stage as active amplifier (CFC-TIA) and the other introducing a modified version (MFC-TIA).

The paper is divided into 4 sections. Section II, presents the proposed MFC-TIA configuration and addresses a circuit analysis comparison with the conventional CFC-TIA. Section III discusses simulation results. Finally, section IV, presents the major conclusions.

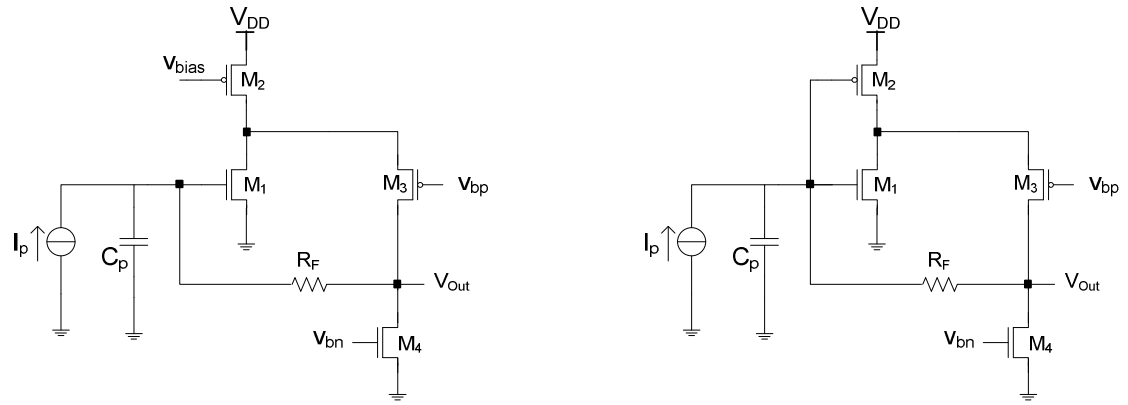

Fig. 1: a) Conventional Folded-Cascode transimpedance amplifier; b) Proposed CMOS Folded-Cascode transimpedance amplifier.

II. TRANSIMPEDANCE AMPLIFIER DESIGN

Figure 1 depicts the two topologies under consideration, the CFC-TIA and the MFC-TIA. The conventional FC based TIA in figure 1a) uses M_1 as the common source input stage and M_3 as the common gate output stage. Due to the low impedance at the input of M_3, the effect of the intrinsic capacitance c_{gd} of M_1 is effectively removed, thus improving bandwidth. M_2 and M_4 are biasing current sources for both M_1 and M_3. The modified topology, replaces M_1 and M_2 by a CMOS inverter stage. As it will be demonstrated, the major improvement is a net reduction on the required area to achieve similar performance as in CFC-TIA. The major drawback is a reduce control over the input stage biasing.

A. CFC-TIA Circuit Analysis

The closed-loop gain and input impedance present a suitable ground for performance comparison between these two circuit topologies. Starting with the CFC-TIA of figure 1a), Circuit analysis reveals that the closed-loop transimpedance gain is approximated by:

$$Z_T \approx -R_F \frac{g_{m1} g_{m3} r_o R_F}{1 + g_{m3} r_o + g_{m1} g_{m3} r_o R_F} \tag{1}$$

where, g_{mk} and r_{ok} represent the transconductance and output resistance of transistor M_k. In (1) it was assumed that $r_{o4} >> R_F$, r_o is the parallel association of r_{o1} and r_{o2} and that r_{o3} as negligible effect on circuit performance. The closed-loop input impedance can be approximated by:

$$Z_i \approx \frac{R_F(1 + g_{m3} r_o)}{1 + g_{m3} r_o + g_{m1} g_{m3} r_o R_F} \tag{2}$$

where the same simplifying assumptions still hold. It is instructive to see that if $g_{m1} g_{m3} r_o R_F >> 1 + g_{m3} r_o$ and $g_{m3} r_o >> 1$, the closed-loop input impedance is dominated by $1/g_{m1}$.

The frequency response of CFC-TIAs has three important pole contributions: i) one due to the photodiode capacitance, which is usually the dominant one; ii) a second one due to the interstage between M_1 and M_3, normally placed at a high frequency due to the effect of M_3 that reduces the interstage load resistance; and iii) a third contribution due to the output circuitry. Assuming dominant pole behavior the input pole frequency, ω_{p1}, can be approximated by:

$$\omega_{p1} \approx \frac{1 + g_{m3} r_o + g_{m1} g_{m3} r_o R_F}{R_F(1 + g_{m3} r_o)(C_p + c_{gs1})} \tag{3}$$

Under the same previous conditions, the input pole is dominated by the $g_{m1}/(C_p+c_{gs})$, which reveal that bandwidth improvement can be achieved increasing g_{m1}, which also improves the closed-loop gain (becoming near $-R_F$). Increasing g_{m1} can be accomplished either by increasing the W/L ratio of M_1 or controlling its biasing current (with M_2). The first method implies a tradeoff, since increasing W/L has effects on c_{gs1}.

B. MFC-TIA Circuit Analysis

For the proposed MFC-TIA circuit topology of figure 1b), equations (1), (2) and (3) still hold, taking $g_{meff} = g_{m1} + g_{m2}$ instead of g_{m1}. In terms of both gain and bandwidth, the same targeted performance can be achieved by both circuits. In MFC-TIAs, bandwidth improvements resort only to the optimized selection of the W/L ratios of M_1 and M_2. In this configuration, the quiescent current of M_1 and M_2 is constrained by the desired DC voltages at both the input and the interstage. Matching similar bandwidth as in the previous case must comply with the optimization of $(g_{m1}+g_{m2})/(C_p+c_{gs1}+c_{gs2})$. Achieving the same performance in terms of bandwidth has different circuit design implications, since now, the W/L ratios of M_1 and M_2 are imposed by biasing considerations. For the circuit of figure 1b), M_2 has to provide biasing for both M_1 and M_3. Furthermore, all these transistors are operated under saturation conditions. Assuming that $I_{D3} = \alpha I_{D2}$, whit $0 < \alpha < 1$, representing the portion of I_{D2} diverted trough M_3. Then the quiescent voltage V_Q, common to both input and output nodes is given by:

$$V_Q = \frac{V_{Tn} + \xi\left(V_{DD} - |V_{Tp}|\right)}{1 + \xi} \tag{4}$$

$$\xi = \sqrt{(1 - \alpha)\frac{k_p}{k_n}\frac{S_2}{S_1}} \tag{5}$$

where, V_{Tn} and V_{Tp}, k_n and k_p represent the threshold voltage and the transconductance parameter of N and P type devices, respectively; S_2 and S_1 are the W/L ratios of M_2 and M_1. The current through M_2 is given by:

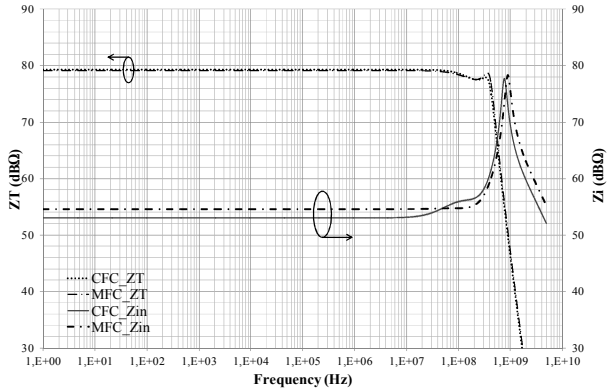

Fig. 2 - AC performance of MFC-TIA and CFC-TIA.

$$I_{D2} = k_p S_2 \left(\frac{V_{DD} - V_{Tn} - |V_{Tp}|}{1 + \xi} \right)^2 \quad (6)$$

Using (6), it is possible to show that the input pole can be approximated by,

$$\omega_{p1} \approx \frac{g_{m2}}{C_p + c_{gs2}\left(1 + \frac{W_1}{W_2}\right)} \left(1 + \frac{1 - \alpha}{\xi}\right) \quad (7)$$

In (7), W_1 and W_2 are the channel widths of M_1 and M_2 respectively. Equations (4) to (7) show that in MFC-TIAs bandwidth and biasing must be established carefully in order to achieve the targeted performance. Equation (7) shows that MFC-TIA can achieve higher bandwidths than those of CFC-TIA for the same transistors dimensions (M_1) and same biasing considerations. This is a natural consequence of the reduced input impedance presented by the CMOS input stage.

C. Input Equivalent Noise

Typically transimpedance amplifiers are used to sense very small currents. Thus, the input current noise has to be very low in order to comply with signal to noise ratio optimization. The main input noise contribution of shunt-feedback TIAs are the thermal noise generated by a feedback resistance and the input referred noise of the core amplifier. With slight modifications, the input referred noise is similar for both CFC-TIA and MFC-TIA configurations. For the CFC-TIA depicted if figure 1a), the main source of noise is thermal noise currents of transistors M_1, M_2 and M_3 and feedback resistor R_F. The input referred noise is modeled with two equivalent noise sources, a noise current source in parallel with the input of the amplifier and a noise voltage source in series with the input of the amplifier. The spectral noise densities are:

$$\overline{v_n^2} = \frac{\overline{\iota_{M1}^2} + \overline{\iota_{M2}^2} + \overline{\iota_{M3}^2}}{g_{m1}^2} \quad (8)$$

$$\overline{\iota_n^2} = \overline{\iota_f^2} + \frac{\overline{v_n^2}}{R_F^2} \quad (9)$$

$$\overline{\iota_{Mk}^2} = 4kT\gamma g_{mk} \quad (10)$$

where, i_{Mk} are the noise sources of transistors M_1, M_2 and M_3 respectively, i_f is the noise source due to the feedback resistance, k is the Boltzmann constant, T the absolute temperature in Kelvin and γ the transistors noise factor.

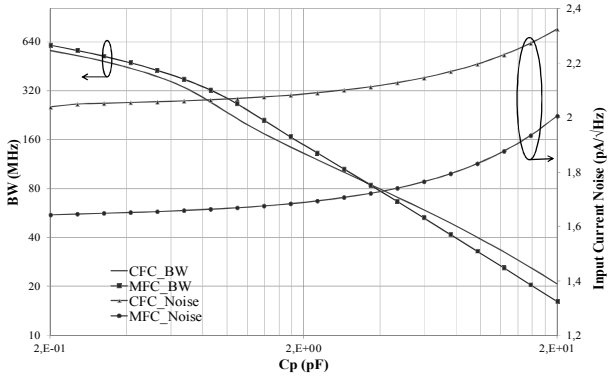

Fig. 3 - Input noise and bandwidth of MFC-TIA and CFC-TIA.

Equations (8), (9) remain valid for MFC-TIA configuration. The noise contributions remain the same, but the term g_{m1} in the denominator of (8) must be replaced by the equivalent transconductance of M_1 and M_2, that is, $g_{m1}+g_{m2}$.

MFC-TIA configuration can display better noise performance when compared to CFC-TIA configurations. This is patent on equation (8), which includes the noise contribution arising from the core amplifier. In MFC-TIAs, the dividing term depends on both M_1 and M_2, which allows the reduction of the input referred noise.

D. Simulations Results

CFC-TIA and MFC-TIA circuits were designed in the standard 350nm CMOS process from Austria Microsystems. Both circuits were optimized for a transimpedance gain of about *80dB*Ω, having a photodiode with parasitic capacitance (C_p), of *0.5pF* and a feedback resistance R_F=*10k*Ω. Table 1 displays the configurations achieved *W/L* transistors ratios. The biasing voltages were: V_{DD}=*3.3V*, V_{bias}=*2.5V* and V_{bp}=*0.9V*. The quiescent voltage at both input and output was V_Q=*1.47V*. Folded-cascode configurations have high output impedance, which increases susceptibility to loading conditions. Therefore, the test circuits include a source follower stage to promote load isolation. The same circuit was used for both configurations thus allowing direct comparison. The load consisted of a *0.5pF* capacitance to ground.

Figure 2 depicts the transfer function of MFC-TIA and CFC-TIA for C_p=*0.5pF*. The results were measured at the output of the source follower stage. The measured bandwidth of MFC-TIA was *370MHz* while for CFC-TIA reached to *320MHz*. As it can be observed, the transimpedance gain was closed to the targeted value of *80dB*Ω for both configurations. The measured input impedance was near *50dB*Ω for both

Table 1: Transistor dimensions.

Device	CFC-TIA	MFC-TIA
M_1	40/0.5	10/0.5
M_2	80/0.5	20/0.5
M_3	10/0.5	10/0.5
M_4	10/1.5	10/1.5

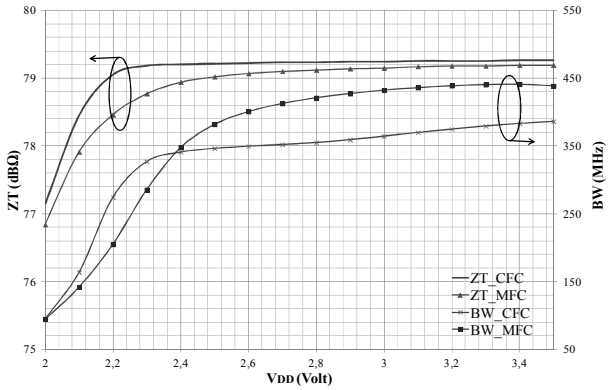

Fig. 4 - Transimpedance gain and bandwidth versus V_{DD} (C_p=*0.5pF*).

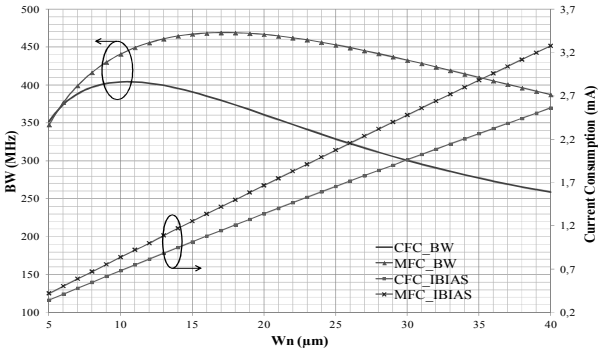

Fig. 5 - Bandwidth and current consumption versus W_n (C_p=*0.5pF*).

cases. These results show that circuit performance in terms of gain and input impedance is nearly the same, with the MFC-TIA configuration achieving a higher cut-off frequency.

Figure 3 illustrates the input current noise and the bandwidth of both configurations against input capacitance, C_p. In terms of noise, MFC-TIA presents better performance as predicted earlier. Although the size of the input transistor M_1 of CFC-TIA is four times larger than that of MFC-TIA, its input current noise is higher. This is a consequence of M_2, which injects higher noise currents in CFC-TIAs due to its large *W/L*. Nevertheless, it is possible to reduce the input equivalent noise current in CFC-TIA increasing the width of M_1, as stated in (8). The bandwidth decreases with the increase of the input capacitance on both topologies. Revealing that, MFC-TIAs have slightly better performance for low values of C_p.

Several parametric simulations were undertaken in order to fully compare the performance of both configurations. For these cases, the comparison metrics consider the core amplifiers without the source follower stage and loading. Figure 4 shows the transimpedance gain and the bandwidth of the proposed transimpedance amplifier against V_{DD}. As it can be seen, both configurations are able to operate under low voltage conditions. Severe performance degradation occurs for V_{DD} values below *2V*.

Figure 5 shows that the aspect ratio of M_1 can be adjusted to improve bandwidth. For the same W_n, MFC-TIA exhibit larger bandwidths than CFC-TIA at the expense of higher power consumption. Nevertheless, for the same power

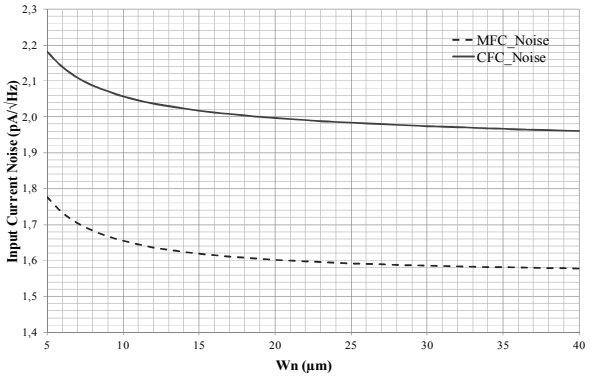

Fig. 6 - Input current noise versus W_n (C_p=*0.5pF*).

consumption, MFC-TIA can even achieve higher bandwidths with reduced W_n when compared with CFC-TIAs. This implies that, for the same power consumption, the input transistors of MFC-TIA are smaller and occupies less implementation area, an important aspect when high integration is required.

The input current noise is also dependent on the aspect W_n as depicted on figure 6. When the input transistors width increases, the noise decreases. As predicted in (8), the input noise of MFC-TIA is smaller than in CFC-TIA configurations.

III. CONCLUSION

A new transimpedance amplifier configuration based on a folded-cascode topology with a CMOS inverter as input stage has been presented. The achieved results show that this configuration provides a wide variation of the supply voltage at a constant transimpedance gain. It has a good performance in terms of input impedance, input current noise, bandwidth and gain. This amplifier topology, due to its reduced implementation area, is particularly suited for optical receivers employing photo-detectors arrays.

REFERENCES

[1] M. Nakamura, N. Ishihara, Y. Akazawa, and H. Kimura, "An Instantaneous Response CMOS Optical Receiver IC with With Dynamic Range and Extremely High Sensitivity Using Feed-Forward Auto-Bias Adu," stmentIEEE J. Solid-state Circuits, September 1995.

[2] C. Y. Wang, C.S. Wang and C.K. Wang, "An 18mW Two-stage CMOS Transimpedance Amplifier for 10Gb/s Optical Application," IEEE Asian Solid-state Circuits Conference, A-SSCC, pp.412–415, 2007.

[3] Z. Lu, K. S. Yeo, J. Ma, M. A. Do, W. M. Lim and X. Chen, "Broad-band Design Techniques for Transimpedance Amplifiers," IEEE Trans. on Circuits and Systems I: Regular Papers, vol. 54, no. 3, 2007.

[4] S. M. Park and H. J. Yoo, "1.25-Gb/s Regulated Cascode CMOS Transimpedance amplifier for Gigabit Ethernet Applications," IEEE Journal of Solid-State Circuits, vol. 39, no. 1, pp. 112-121, 2004.

[5] C.T. Chan and O.T.C. Chen, "Inductorless 10Gb/s CMOS Transimpedance Amplifier using Source-Follower Regulated Cascode and Double Three-order Active Feedback," in Proc. of the IEEE Inter. Symposium on Circuits and Systems, pp. 5487-5490, 2006.

[6] K. Schneider and H. Zimmermann, "Folded-Cascode Transimpedance Amplifier for Burst-Mode Applications," 10th IEEE International Symposium on EDMO, pp. 294-299, 2002.

[7] B. Huang, H. Chen, "A monolithic optical receiver chip for free space visible light communication system", IEEE Intern. Conf. on Solid-State and Integrated Circ.Tech., 2012, Xi'an, China, October 2012.