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Verify level control criteria for multi-level cell flash memories and their applications

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Abstract

In *M*-bit/cell multi-level cell (MLC) flash memories, it is more difficult to guarantee the reliability of data as *M* increases. The reason is that an *M*-bit/cell MLC has 2^M states whereas a single-level cell (SLC) has only two states. Hence, compared to SLC, the margin of MLC is reduced, thereby making it sensitive to a number of degradation mechanisms such as cell-to-cell interference and charge leakage. In flash memories, distances between 2^M states can be controlled by adjusting verify levels during incremental step pulse programming (ISPP). For high data reliability, the control of verify levels in ISPP is important because the bit error rate (BER) will be affected significantly by verify levels. As *M* increases, the verify level control will be more important and complex. In this article, we investigate two verify level control criteria for MLC flash memories. The first criterion is to minimize the overall BER and the second criterion is to make page BERs equal. The choice between these criteria relates to flash memory architecture, bits per cell, reliability, and speed performance. Considering these factors, we will discuss the strategy of verify level control in the hybrid solid state drives (SSD) which are composed of flash memories with different number of bits per cell.

Introduction

Flash memory is now the fastest growing memory segment, driven by the rapid growth of mobile devices and solid state drives (SSD). To satisfy the market demand for lower cost per bit and higher density of nonvolatile memory, there are two approaches: (1) technology scaling, (2) multi-level cell (MLC) [1-4].

As the technology continues to scale down, flash memories suffer from more severe physical degradation mechanisms such as cell-to-cell interference (coupling) and charge leakage [5,6]. In addition, *M*-bit/cell MLC flash memories have 2^M states within the threshold voltage window whereas the single-level cell (SLC) has only two states. Therefore, the reliability of stored data is an important challenge for high density flash memories.

In order to cope with this reliability problem, many approaches have been proposed. The incremental step pulse programming (ISPP), which is the most widely used programming scheme, was proposed to maintain a tight cell threshold voltage distribution for high reliability [7,8].

ISPP is a program and verify strategy with a stair case program voltage V_{pp} as illustrated in Figure 1, where ΔV_{pp} is the incremental step size. During each program and verify cycle, the floating gate threshold voltage is first boosted by up to ΔV_{pp} and then compared with the corresponding verify level. If the threshold voltage of the memory cell is still lower than the verify level, the program and verify iteration continues. Otherwise, further programming of this cell is disabled [7-10].

Therefore, positions of program states (except the erase state) are determined by verify levels and the tightness of each program state depends on the incremental step size ΔV_{pp}. By reducing ΔV_{pp}, the cell threshold voltage distribution can be made tighter, but the programming time will increase [7,8]. In brief, ISPP can control both the distances between states by verify levels and the tightness of program states by the incremental step size.

For SLC, determining the verify level of the programming state is a simple problem because there is only one program state and the margin between the erase state and the program state is sufficiently large so that small changes in the margin will not change the error rates noticeably. However, the verify level control issue for *M*-bit/cell flash memories is more important and complex than that for SLC. This is because 2^M states have to be crammed within

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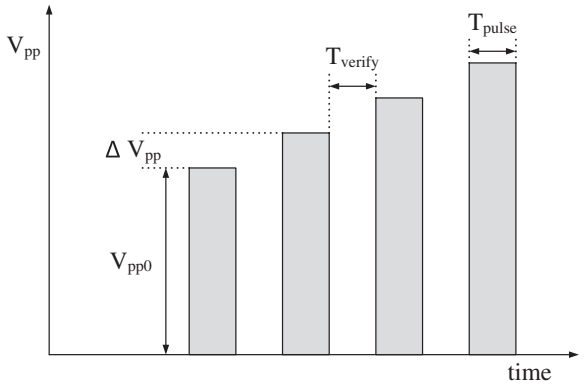

Figure 1 Program pulses in ISPP. A verify operation is carried out after each pulse. ΔV_{pp} is the incremental step size of the program pulse. V_{pp0} is the initial value of the program pulse. T_{verify} is the verify read time. T_{pulse} is the program pulse width [10].

the given constrained threshold voltage window W. More states will significantly reduce the margin between states and bit error rates (BER) will vary in response to small changes in verify levels. Furthermore, the number of verify levels which ISPP has to control increases from 1 (for SLC) to $2^M - 1$ (for M-bit/cell MLC). In addition, as explained in the following, the multipage architecture of MLC flash memories makes verify level control more complex than SLC.

Most MLC flash memories adopt the multipage architecture. The important property of the multipage architecture is that different bits of a single cell are assigned into different pages [10-15]. Therefore, BERs of each page can be different. As a page is the unit of data that is programmed and read at one time, the error control coding (ECC) should be applied within the same page. It means that each page is composed of one or several codewords. Therefore, ECC has to be designed for the worst page BER and this leads to wasted redundancy for the other (i.e., better) pages. This uneven page BER problem is an important and practical issue and there have been several attempts to deal with it [11-15].

To deal with this different page BERs issue, we investigate two verify level control criteria for MLC flash memories. The first criterion is to minimize the overall BER. The second criterion is to make all page BERs equal [14]. These two criteria will be formulated as convex optimization problems. After solving these optimization problems, we will compare the numerical results from two criteria. In addition, the advantages and disadvantages of the two criteria will be discussed based on reliability, speed performance, and architecture of MLC flash memories. To the best of authors' knowledge, the convex optimization approach for verify levels of ISPP has not been addressed in the open literature though experimental approaches could be investigated in industry.

An interesting way to combine the speed advantage of SLC and the cost advantage of MLC is to use a hybrid solid state drive (SSD) that judiciously uses both SLC and MLC flash memories. The basic idea of hybrid SSD is to complement the drawbacks of SLC and MLC with each other's advantages [16-19]. Based on the architecture of the hybrid SSD and properties of the proposed verify level control criteria, we propose a strategy to apply the proper verify level control criterion for the hybrid SSD. This strategy is aimed at both reliability and speed performance.

The rest of this article is organized as follows: Section "Cell threshold voltage distribution" discusses the cell threshold voltage distribution under the assumption of a Gaussian mixture model (GMM). Based on this statistical model, the overall BER and the page BER are derived. Sections "Criteria for verify level control" and "ECC and flash memories of multipage architecture" address verify level control criteria and discuss their advantages and disadvantages for various MLCs ($M = 2 \sim 4$) considering multipage architecture and ECC. Section "Hybrid SSD and strategy for verify level control" proposes a method to choose these criteria for the hybrid SSD based on reliability and speed performance. Finally, Section "Conclusion" concludes this article.

Cell threshold voltage distribution

In M-bit/cell flash memory, the cell threshold voltage distribution is composed of 2^M states from S_0 (the erase state) to S_{2^M-1} (the highest state). Even though there are tail cells and asymmetry in cell distributions, the cell threshold voltage distribution of flash memories could be approximated as a sum of Gaussian distributions [6,20,21]. Therefore, we will model the cell threshold voltage distribution $f(x)$ by the following GMM.

$$\begin{aligned} f(x) &= \sum_{i=0}^{2^M-1} P(S_i) f_i(x) \\ &= \frac{1}{2^M} \sum_{i=0}^{2^M-1} \frac{1}{\sqrt{2\pi}\sigma_i} \exp\left\{ \frac{-(x-\mu_i)^2}{2\sigma_i^2} \right\} \end{aligned} \tag{1}$$

where x refers to the threshold voltage and $f_i(x)$ is a Gaussian pdf with mean μ_i and standard deviation σ_i corresponding to the state S_i. $P(S_i)$ is the probability of the state S_i. If data size is sufficiently large and a scrambler is used, then we can assume that $P(S_0) \approx \cdots \approx P(S_{2^M-1}) \approx \frac{1}{2^M}$ with high probability.

Figure 2 shows the cell distribution of 2-bit/cell flash memories. There are four states from S_0 (the erase state) to S_3 (the highest state) within the constrained voltage window W. The constrained voltage window W is the dis-

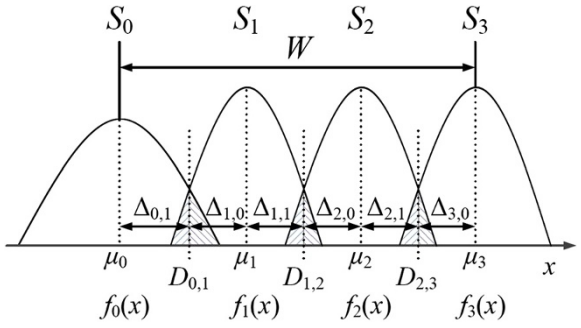

Figure 2 Cell threshold voltage distribution for 2-bit/cell flash memories. There are four states from S_0 to S_3. Each state S_i can be modeled by the distribution f_i.

tance between the mean of the erase state and the mean of the highest state, which is given by

$$W = \mu_{2^M-1} - \mu_0. \tag{2}$$

The overall BER (i.e., $\text{BER}_{\text{overall}}$) is the total number of erroneous bits divided by the total number of data bits which contains data of all pages. If the Gray mapping is used, there is only one bit difference between S_i and S_{i+1}. For example, in 2-bit/cell MLC, states S_0, S_1, S_2, and S_3 denote bit patterns 11, 10, 00, and 01. Probabilities that cells are misread as states which are more than two states away from the original state are much smaller than probabilities of cells being misread as adjacent states and thus are negligible. Therefore, the overall BER can be expressed as

$$\text{BER}_{\text{overall}} = \frac{1}{M2^M} \sum_{i=0}^{2^M-2} \left\{ Q\left(\frac{\Delta_{i,1}}{\sigma_{i,1}}\right) + Q\left(\frac{\Delta_{i+1,0}}{\sigma_{i+1,0}}\right) \right\} \tag{3}$$

where $\Delta_{i,1}$ is the distance from μ_i to $D_{i,i+1}$ and $\Delta_{i+1,0}$ is the distance from μ_{i+1} to $D_{i,i+1}$. $D_{i,i+1}$ is the optimal decision level between S_i and S_{i+1}, which satisfies the condition of $f_i(D_{i,i+1}) = f_{i+1}(D_{i,i+1})$ [22-24]. In addition, $\sigma_{i,0}$ and $\sigma_{i,1}$ are used separately for convenience although $\sigma_{i,0} = \sigma_{i,1} = \sigma_i$. The tail probability function $Q(x)$ is defined as

$$Q(x) = \int_x^\infty \frac{1}{\sqrt{2\pi}} \exp\left(-\frac{t^2}{2}\right) dt. \tag{4}$$

If we change the index of $\Delta_{i,j}$ into Δ_k and $\sigma_{i,j}$ into ρ_k by $k = 2i + j$, (3) can be rewritten as

$$\text{BER}_{\text{overall}} = \frac{1}{M2^M} \sum_{k=1}^{2(2^M-1)} Q\left(\frac{\Delta_k}{\rho_k}\right) \tag{5}$$

where all Δ_ks are positive since it is natural that $\mu_{i+1} > \mu_i$.

Most MLC flash memories adopt multipage architectures [10]. In this multipage architecture, ECC encoding and decoding are performed within each page. This means that pages with higher BERs will suffer from worse decoding failure rate. Therefore, the BER of each page could be more important than the overall BER in terms of ECC [11,13-15].

The page BER (i.e., the BER of each page) depends on the mapping scheme that converts a state level to corresponding bit representation. We will define $\text{BER}_{\text{page } m}$ as the BER of page m. For example, if the 2-bit/cell flash memory adopts the Gray mapping of Table 1, the data of page 1 are obtained by one read operation between S_1 and S_2. Therefore, the BER of page 1 is determined by $f_1(x)$ and $f_2(x)$. In order to read the data of page 2, two read operations (one between S_0 and S_1, and another between S_2 and S_3) are required. Then the BER of page 2 is determined by $f_0(x)$ and $f_1(x)$, $f_2(x)$, and $f_3(x)$. Therefore, page BERs for 2-bit/cell are given by

$$\begin{aligned}
\text{BER}_{\text{page 1}} &= \frac{1}{4}\left\{ Q\left(\frac{\Delta_{1,1}}{\sigma_{1,1}}\right) + Q\left(\frac{\Delta_{2,0}}{\sigma_{2,0}}\right) \right\}, \\
\text{BER}_{\text{page 2}} &= \frac{1}{4}\left\{ Q\left(\frac{\Delta_{0,1}}{\sigma_{0,1}}\right) + Q\left(\frac{\Delta_{1,0}}{\sigma_{1,0}}\right) + Q\left(\frac{\Delta_{2,1}}{\sigma_{2,1}}\right) \right. \\
&\quad \left. + Q\left(\frac{\Delta_{3,0}}{\sigma_{3,0}}\right) \right\}.
\end{aligned} \tag{6}$$

By the same method, page BERs for 3-bit/cell adopting the Gray mapping of Table 2 are given by

$$\begin{aligned}
\text{BER}_{\text{page 1}} &= \frac{1}{8}\left\{ Q\left(\frac{\Delta_{3,1}}{\sigma_{3,1}}\right) + Q\left(\frac{\Delta_{4,0}}{\sigma_{4,0}}\right) \right\}, \\
\text{BER}_{\text{page 2}} &= \frac{1}{8}\left\{ Q\left(\frac{\Delta_{1,1}}{\sigma_{1,1}}\right) + Q\left(\frac{\Delta_{2,0}}{\sigma_{2,0}}\right) + Q\left(\frac{\Delta_{5,1}}{\sigma_{5,1}}\right) \right. \\
&\quad \left. + Q\left(\frac{\Delta_{6,0}}{\sigma_{6,0}}\right) \right\}, \\
\text{BER}_{\text{page 3}} &= \frac{1}{8}\left\{ Q\left(\frac{\Delta_{0,1}}{\sigma_{0,1}}\right) + Q\left(\frac{\Delta_{1,0}}{\sigma_{1,0}}\right) + Q\left(\frac{\Delta_{2,1}}{\sigma_{2,1}}\right) \right. \\
&\quad + Q\left(\frac{\Delta_{3,0}}{\sigma_{3,0}}\right) + Q\left(\frac{\Delta_{4,1}}{\sigma_{4,1}}\right) + Q\left(\frac{\Delta_{5,0}}{\sigma_{5,0}}\right) \\
&\quad \left. + Q\left(\frac{\Delta_{6,1}}{\sigma_{6,1}}\right) + Q\left(\frac{\Delta_{7,0}}{\sigma_{7,0}}\right) \right\}.
\end{aligned} \tag{7}$$

Similarly, page BERs for 4-bit/cell or more could be derived from the mapping scheme provided.

Table 1 Gray mapping for 2-bit/cell flash memories

State	S_0	S_1	S_2	S_3
page 1	1	1	0	0
page 2	1	0	0	1

Table 2 Gray mapping for 3-bit/cell flash memories

State	S_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7
page 1	1	1	1	1	0	0	0	0
page 2	1	1	0	0	0	0	1	1
page 3	1	0	0	1	1	0	0	1

The overall BER of (3) can be expressed as the mean of page BERs, which is given by

$$\mathrm{BER}_{\mathrm{overall}} = \frac{1}{M}\sum_{m=1}^{M} \mathrm{BER}_{\mathrm{page}\,m}. \tag{8}$$

The distance between the means of S_i and S_{i+1} is $\mu_{i+1} - \mu_i = \Delta_{i,1} + \Delta_{i+1,0}$. We will term $\mu_{i+1} - \mu_i$ as the distance from S_i to S_{i+1}, and the distance from S_i to S_{i+1} will be determined by $\Delta_{i,1}$ and $\Delta_{i+1,0}$. For all states, we will define two parameters as follows.

$$\overrightarrow{\Delta} = \left(\Delta_1, \ldots, \Delta_{2(2^M-1)}\right) \tag{9}$$

$$\overrightarrow{\rho} = \left(\rho_1, \ldots, \rho_{2(2^M-1)}\right) \tag{10}$$

where $\Delta_k = \Delta_{i,j}$ and $\rho_k = \sigma_{i,j}$ by $k = 2i + j$. Therefore, $\overrightarrow{\Delta}$ and $\overrightarrow{\rho}$ will represent the all distances between states and the tightness of program states, respectively, and they will determine the overall BER and the page BERs. In the ISPP scheme, $\overrightarrow{\Delta}$ can be controlled by verify levels and $\overrightarrow{\rho}$ by the incremental step size. In the following section, we will propose criteria for verify level control, which means how to determine $\overrightarrow{\Delta}$ at the given $\overrightarrow{\rho}$.

Criteria for verify level control

We investigate two verify level control criteria. The first criterion is to minimize the overall BER, which is aimed at only reliability. The second criterion is to make page BERs equal considering both the reliability and the multipage architecture. These two criteria will be formulated as optimization problems. If the parameters of $W(= \mu_{2^M-1} - \mu_0)$ and $\overrightarrow{\rho}$ are given, $\overrightarrow{\Delta} = \left(\Delta_1, \ldots, \Delta_{2(2^M-1)}\right)$ will be the variables of optimization problems.

We will show that the proposed criteria for verify level control are convex optimization problems. Therefore, the (globally) optimal solution can be efficiently found using numerical optimization techniques and the interior-point method was used to obtain the numerical results [25]. Also, mathematical conditions for the optimal solutions of these criteria are derived.

Criterion 1: minimize overall BER

The first criterion is to minimize the overall BER. This criterion 1 for M-bit/cell flash memories can be formulated as follows.

$$\begin{aligned} \underset{\overrightarrow{\Delta}}{\text{minimize}} \quad & g_1\left(\overrightarrow{\Delta}\right) = \sum_{k=1}^{2(2^M-1)} Q\left(\frac{\Delta_k}{\rho_k}\right) \\ \text{subject to} \quad & \sum_{k=1}^{2(2^M-1)} \Delta_k = W \\ & \Delta_k \geq 0, \quad k = 1, \ldots, 2\left(2^M - 1\right) \end{aligned} \tag{11}$$

where $g_1\left(\overrightarrow{\Delta}\right) = M2^M \cdot \mathrm{BER}_{\mathrm{overall}}$ by (5).

The cost function $g_1(\cdot)$ is a nonnegative weighted sum of $Q(\cdot)$. From (4), the second derivative of $Q(\cdot)$ is given by

$$\frac{d^2Q(x)}{dx^2} = \frac{x}{\sqrt{2\pi}} \exp\left(-\frac{x^2}{2}\right) \geq 0 \quad \text{for } x \geq 0. \tag{12}$$

Since Δ_k is the distance and ρ_k is the standard deviation, all Δ_ks and ρ_ks are always positive. Therefore, (11) is a *convex* optimization problem and can be solved by several numerical methods [25].

We will define the Lagrangian G_1 as follows.

$$G_1(\overrightarrow{\Delta}, \lambda, \overrightarrow{\eta}) = g_1 + \lambda\left(\sum_{k=0}^{2(2^M-1)} \Delta_k - W\right) + \sum_{k=1}^{2(2^M-1)} \eta_k(-\Delta_k) \tag{13}$$

where $\overrightarrow{\eta} = \left(\eta_1, \ldots, \eta_{2(2^M-1)}\right)$. The optimal solution of (11) has to satisfy the following Karush-Kuhn-Tucker (KKT) conditions [25].

$$\begin{aligned} \eta_k &\geq 0, \quad k = 1, \ldots, 2\left(2^M - 1\right) \\ \eta_k(-\Delta_k) &= 0, \quad k = 1, \ldots, 2\left(2^M - 1\right) \\ \nabla G_1 &= 0 \end{aligned} \tag{14}$$

Since all Δ_ks are positive, $\eta_k = 0$ for all k by (14), which results from *complementary slackness*. Therefore, the optimal solution will satisfy the following condition from (13) and (14).

$$\begin{aligned} &\frac{\partial G_1}{\partial \Delta_k} = -\frac{1}{\sqrt{2\pi}\rho_k} \exp\left(-\frac{\Delta_k^2}{2\rho_k^2}\right) + \lambda = 0, \\ &\quad k = 1, \ldots, 2\left(2^M - 1\right). \end{aligned} \tag{15}$$

From (15), the optimal solution has to satisfy the following condition in order to minimize the overall BER.

$$\begin{aligned} f_0\left(\mu_0 + \Delta_{0,1}\right) &= f_1\left(\mu_1 - \Delta_{1,0}\right) = \cdots \\ &= f_{2^M-1}\left(\mu_{2^M-1} - \Delta_{2^M-1,0}\right) = \lambda \end{aligned} \tag{16}$$

Figure 3 illustrates the condition of (16) for minimizing the overall BER. In addition, Figure 3 shows that the decision level $D_{i,i+1}$ satisfies the condition $f_i\left(D_{i,i+1}\right) =$

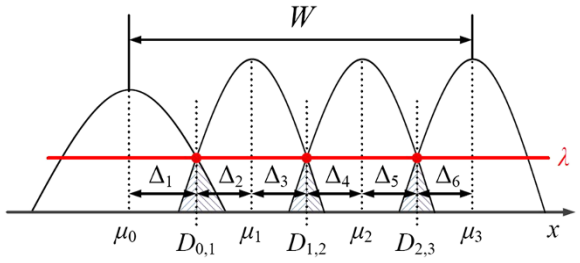

Figure 3 Example of criterion 1 for 2-bit/cell. This example illustrates the condition which minimizes the overall BER.

$f_{i+1}\left(D_{i,i+1}\right)$ which corresponds to the definition of the optimal decision level [22-24].

If variances for all states are equal (i.e., $\sigma_k^2 = \sigma^2$), then all Δ_ks become $\Delta = \frac{W}{2(2^M-1)}$ from (11) and (15). In this case, the BER of page m ($1 \le m \le M$) is given by

$$\mathrm{BER}_{\mathrm{page}\ m} = \frac{1}{2^{M-m}} \cdot Q\left(\frac{\Delta}{\sigma}\right). \tag{17}$$

(17) shows that $\mathrm{BER}_{\mathrm{page}\ m+1}$ will be twice $\mathrm{BER}_{\mathrm{page}\ m}$ if variances for all states are same. When $M = 2$, $\mathrm{BER}_{\mathrm{page}\ 1} = \frac{1}{2} \cdot Q\left(\frac{\Delta}{\sigma}\right)$ and $\mathrm{BER}_{\mathrm{page}\ 2} = Q\left(\frac{\Delta}{\sigma}\right)$. From (8), $\mathrm{BER}_{\mathrm{overall}} = \frac{3}{4} \cdot Q\left(\frac{\Delta}{\sigma}\right)$. Figure 4 shows $\mathrm{BER}_{\mathrm{page}\ 1}$, $\mathrm{BER}_{\mathrm{page}\ 2}$, and $\mathrm{BER}_{\mathrm{overall}}$ as a function of σ for 2-bit/cell flash memories. From (17), it is seen that the ratio of page BERs for 3-bit/cell is 1:2:4. For 4-bit/cell flash memories, the ratio of page BERs will be 1:2:4:8 [11-15]. Therefore, using criterion 1 makes the difference between page BERs larger as M increases.

In addition, the difference between page BERs from criterion 1 could increase if variances for states are not equal. For example, it is possible that the erase state S_0 has wider distribution than other program states since the cell threshold voltage distribution of the erase state is not controlled as tightly as other program states by ISPP [8]. In this case, more errors will occur between S_0 and S_1, which results in the increase of the last page BER ($\mathrm{BER}_{\mathrm{page}\ M}$) in the Gray mapping schemes of Tables 1 ∼ 3. Table 4 shows the increase of the difference between page BERs. In Table 4, we assumed that the standard deviation of the erase state (S_0) is σ_0 and standard deviations of other program states ($S_1 \sim S_3$) are same as σ. As the erase state distribution becomes broader, criterion 1 will lead to more difference between page BERs.

Criterion 2: make page BERs equal

The second criterion is to make the page BERs equal [14]. In addition, the overall BER has to be made as small as possible. Therefore, this criterion 2 for M-bit/cell flash memories can be formulated as follows.

$$\begin{aligned} \underset{\vec{\Delta},\varepsilon}{\text{minimize}} \quad & g_2 = \varepsilon \\ \text{subject to} \quad & \sum_{k=1}^{2(2^M-1)} \Delta_k = W \\ & h_m\left(\vec{\Delta}\right) \le \varepsilon, \quad m = 1, \ldots, M \\ & \Delta_k \ge 0, \quad k = 1, \ldots, 2\left(2^M - 1\right) \end{aligned} \tag{18}$$

where $h_m\left(\vec{\Delta}\right) = 2^M \cdot \mathrm{BER}_{\mathrm{page}\ m}$. Therefore, from the constraints of this optimization problem, ε will represent the maximum value among all page BERs. While trying to minimize ε, we can find the optimal solution which minimizes the overall BER among candidates satisfying the following condition.

$$\begin{aligned} \mathrm{BER}_{\mathrm{page}\ 1} \approx \mathrm{BER}_{\mathrm{page}\ 2} \approx \cdots \approx \mathrm{BER}_{\mathrm{page}\ M} \approx \mathrm{BER}_{\mathrm{overall}} \\ \approx \frac{\varepsilon}{2^M} \end{aligned} \tag{19}$$

In other words, even though the formulation in (18) does not explicitly set the page BERs to be identical, it implicitly minimizes the difference between all page BERs. Intuitively, if $\mathrm{BER}_{\mathrm{page}\ m}$ is higher than other page BERs, the optimization in (18) will try to reduce $\mathrm{BER}_{\mathrm{page}\ m}$ and make it as close to other page BERs as possible.

(18) is a *convex* optimization problem since $h_m\left(\vec{\Delta}\right)$ is a nonnegative weighted sum of convex function $Q(\cdot)$. The convex property of $Q(\cdot)$ was shown in (12). Therefore, the optimal solution can be obtained by several numerical methods.

The Lagrangian G_2 associated with (18) is given by

$$\begin{aligned} G_2\left(\vec{\Delta}, \vec{\lambda}, \vec{\eta}\right) = g_2 + \lambda_0 \cdot \left(\sum \Delta_k - W\right) + \sum_{m=1}^{M} \lambda_m \left(h_m - \varepsilon\right) \\ + \sum_{k=1}^{2(2^M-1)} \eta_k(-\Delta_k) \end{aligned} \tag{20}$$

Table 3 Gray mapping for 4-bit/cell flash memories

State	S_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}
page 1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
page 2	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
page 3	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
page 4	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1

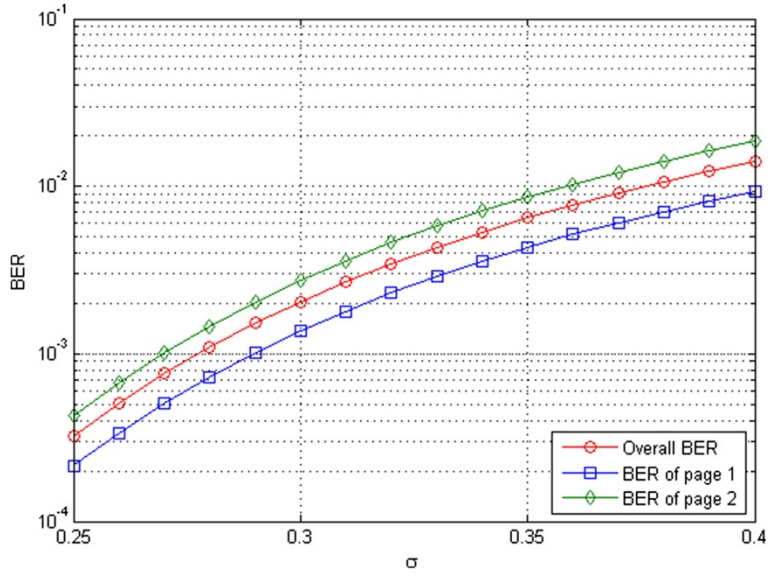

Figure 4 BER of 2-bit/cell flash memories using Criterion 1. The constrained voltage window W is assumed to be 5.

where $\vec{\lambda} = \left(\lambda_0, \ldots, \lambda_{2(2^M-1)}\right)$ and $\vec{\eta} = \left(\eta_1, \ldots, \eta_{2(2^M-1)}\right)$. The optimal solution of (18) has to satisfy the following KKT conditions.

$$\begin{aligned} \lambda_m &\geq 0, \quad m = 1, \ldots, M \\ \lambda_m (h_m - \varepsilon) &= 0, \quad m = 1, \ldots, M \\ \eta_k &\geq 0, \quad k = 1, \ldots, 2\left(2^M - 1\right) \\ \eta_k(-\Delta_k) &= 0, \quad k = 1, \ldots, 2\left(2^M - 1\right) \\ \nabla G_2 &= 0 \end{aligned} \tag{21}$$

As discussed in criterion 1, all η_ks will be zero due to *complementary slackness* of (21).

Figure 5 shows how criterion 2 works for 2-bit/cell flash memories. In order to make page BERs equal, $|\mu_2 - \mu_1| = \Delta_3 + \Delta_4$ of criterion 2 has to be reduced compared to that of criterion 1. Meanwhile, $|\mu_1 - \mu_0| = \Delta_1 + \Delta_2$ and $|\mu_3 - \mu_2| = \Delta_5 + \Delta_6$ will be larger than those of criterion 1.

Table 4 $\mathrm{BER}_{\mathrm{page\,2}}/\mathrm{BER}_{\mathrm{page\,1}}$ for 2-bit/cell flash memories ($W = 5$)

σ	$\sigma_0 = \sigma$	$\sigma_0 = 2\sigma$	$\sigma_0 = 3\sigma$	$\sigma_0 = 4\sigma$
0.20	2.00	2.55	3.16	3.83
0.22	2.00	2.56	3.19	3.89
0.24	2.00	2.57	3.22	3.97
0.26	2.00	2.58	3.26	4.04
0.28	2.00	2.59	3.30	4.12
0.30	2.00	2.61	3.34	4.21

From (21), we can obtain following conditions for the optimal solution of 2-bit/cell flash memories.

$$\begin{aligned} \frac{\partial G_2}{\partial \varepsilon} &= 1 - \lambda_1 - \lambda_2 = 0, \\ \frac{\partial G_2}{\partial \Delta_i} &= \lambda_0 + \lambda_1 \cdot \frac{1}{\sqrt{2\pi}\,\rho_i} \exp\left(-\frac{\Delta_i^2}{2\rho_i^2}\right) = 0, \quad i = 3, 4, \\ \frac{\partial G_2}{\partial \Delta_j} &= \lambda_0 + \lambda_2 \cdot \frac{1}{\sqrt{2\pi}\,\rho_j} \exp\left(-\frac{\Delta_j^2}{2\rho_j^2}\right) = 0, \quad j = 1, 2, 5, 6 \end{aligned} \tag{22}$$

If one of λ_ms (for $m = 0, \ldots, M$) is zero, then all λ_ms should be zero since $\frac{\partial G_2}{\partial \Delta_k} = 0$ and $\frac{1}{\sqrt{2\pi}\,\rho_k} \exp\left(-\frac{\Delta_k^2}{2\rho_k^2}\right) > 0$ for all k. However, if all λ_ms are zero, the condition of $1 - \lambda_1 - \lambda_2 = 0$ in (22) cannot hold. Therefore, we can see that $\lambda_m \neq 0$, which results in $h_m - \varepsilon = 0$ by KKT conditions

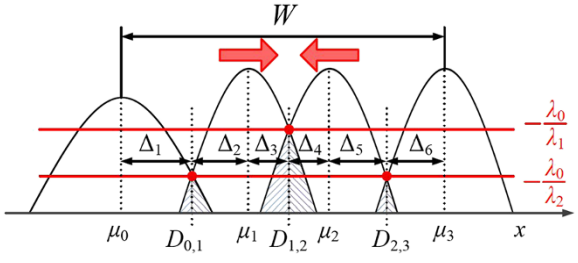

Figure 5 Example of criterion 2 for 2-bit/cell. This example illustrates the condition which makes page BERs equal and minimizes the overall BER as far as possible.

of (21). It means that all page BERs will be equal for the optimal solution of (18) $\left(\because h_m\left(\overrightarrow{\Delta}\right) = 2^M \cdot \mathrm{BER}_{\mathrm{page}\ m}\right)$.

Taking into account the aforementioned discussions, the conditions of (22) can be modified by

$$\begin{aligned} \lambda_1 + \lambda_2 &= 1, \\ \frac{1}{\sqrt{2\pi}\,\rho_i} \exp\left(-\frac{\Delta_i^2}{2\rho_i^2}\right) &= -\frac{\lambda_0}{\lambda_1}, \quad i = 3, 4, \\ \frac{1}{\sqrt{2\pi}\,\rho_j} \exp\left(-\frac{\Delta_j^2}{2\rho_j^2}\right) &= -\frac{\lambda_0}{\lambda_2}, \quad j = 1, 2, 5, 6 \end{aligned} \tag{23}$$

which are illustrated in Figure 5.

Figure 6 shows the numerical results of criterion 2 for 2-bit/cell flash memories when variances for all states are equal to σ. All page BERs and the overall BER are made equal by criterion 2. Even if variances for all states are not equal, the optimal solution can be obtained by the same method.

It is worth mentioning that the overall BER from criterion 2 is worse than that from criterion 1. The reason is that the overall BER increases when we try to make page BERs equal. Figure 7 shows the degradation of the overall BER from criterion 2 compared to criterion 1 for 2-bit/cell flash memories. In order to measure this degradation, we will define the degradation ratio γ given by

$$\gamma = \frac{\mathrm{BER}_{\mathrm{overall}} \text{ from criterion 2}}{\mathrm{BER}_{\mathrm{overall}} \text{ from criterion 1}}. \tag{24}$$

Figure 8 shows the degradation ratio γ for 2-bit/cell, 3-bit/cell and 4-bit/cell flash memories where we assume that variances for all states are same. For 2-bit/cell, γ is about 1.05, which means that the degradation of the overall BER is 5 %. Meanwhile, the degradation of 3-bit/cell is about 14 % ($\gamma \approx 1.14$) and the degradation of 4-bit/cell is about 25 % ($\gamma \approx 1.25$). These results reveal that equalizing page BERs causes an increase of the overall BER.

Verify level control criteria and charge leakage

After programming data into flash memories, the cell threshold voltage distribution can change because of charge leakage. The cell threshold voltage distribution change due to charge leakage can be modeled as a change in the mean and the variance of the distributions, i.e., [6]

$$\begin{aligned} \mu_{\mathrm{post}} &= \mu_{\mathrm{pre}} + \mu_{\mathrm{shift}}, \\ \sigma^2_{\mathrm{post}} &= \sigma^2_{\mathrm{pre}} + \sigma^2_{\mathrm{shift}}, \end{aligned} \tag{25}$$

where μ_{pre} and σ^2_{pre} are the mean and the variance before charge leakage. μ_{post} and σ^2_{post} are the mean and the variance after charge leakage. μ_{shift} and $\sigma^2_{\mathrm{shift}}$ are the mean and the variance of threshold voltage shift by charge leakage. μ_{shift} and $\sigma^2_{\mathrm{shift}}$ depend on the program and erase (P/E) cycle count, retention time and temperature [6].

The proposed verify level control criteria should be applied based on μ_{post} and σ^2_{post} because μ_{post} and σ^2_{post} will determine the BER of flash memories. Therefore, we have to control μ_{pre} and σ^2_{pre} considering the amount of μ_{shift} and $\sigma^2_{\mathrm{shift}}$. Basically, μ_{pre} and σ^2_{pre} can be controlled by verify levels and the incremental step size ΔV_{pp} of ISPP though physical mechanisms such as cell-to-cell interference, program disturbance, and background pattern dependency also affect μ_{pre} and σ^2_{pre} [5,7,8].

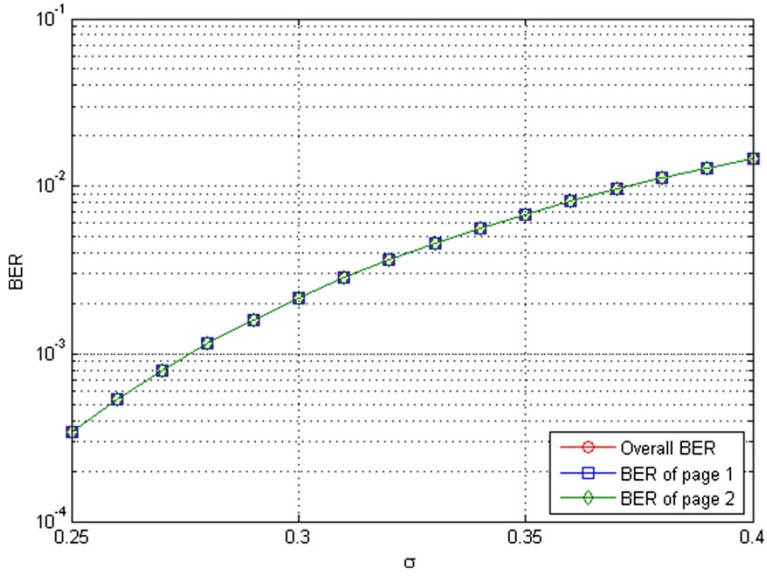

Figure 6 BER of 2-bit/cell flash memories using Criterion 2. The constrained voltage window *W* is assumed to be 5.

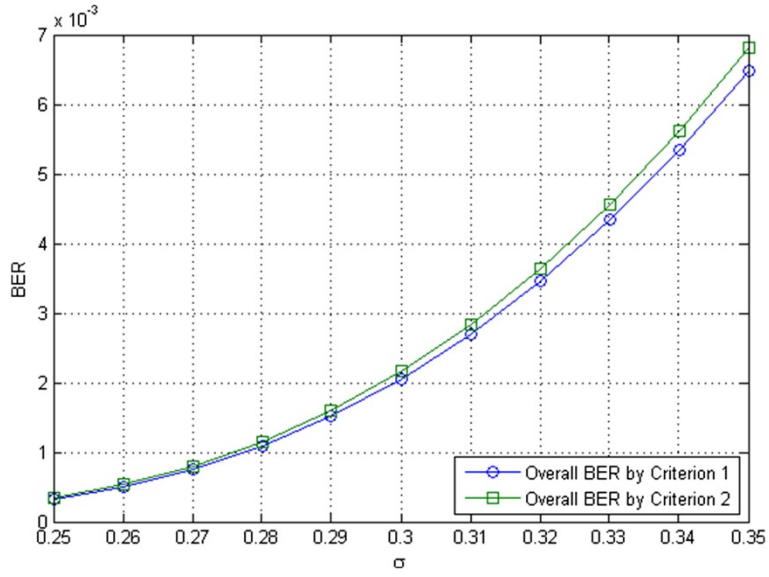

Figure 7 Comparison between the overall BER from the two criteria. The constrained voltage window *W* is assumed to be 5.

Via chip testing, we can measure the amount of μ_{shift} and σ^2_{shift} as a function of P/E cycle count and retention time [6]. However, the allowable maximum values of μ_{shift} and σ^2_{shift} are generally used because ECC has to be designed to guarantee the reliability even in the worst case, which is also called end-of-life (EOL). EOL assumes the allowable maximum P/E cycle count and the allowable maximum retention time. Therefore, it is a practical method to apply the proposed verify level control criteria based on μ_{post} and σ^2_{post} of EOL. In this case, μ_{post} and σ^2_{post} should be used to formulate the convex optimization problems shown in (11) and (18). Other than this minor modification, no additional change is required for our proposed mathematical formulations.

Verify level control criteria and other statistical distributions

We will extend these proposed verify level control criteria for other distributions. Suppose that the threshold voltage distribution of each state S_i can be approximated as an

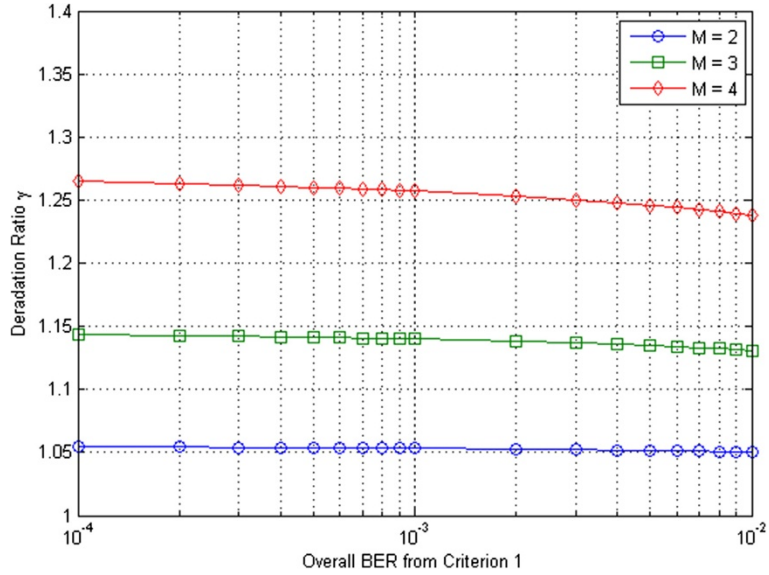

Figure 8 Degradation ratio γ for 2∼4-bit/cell flash memories. The constrained voltage window *W* is assumed to be 5.

arbitrary distribution $\phi_i(x)$ which has a maximum value at $x = v_i$ (i.e., v_i is the mode of $\phi_i(x)$). Instead of (2), the constrained voltage window W will be defined by

$$W = v_{2^M-1} - v_0. \tag{26}$$

The distance between S_i and S_{i+1} will be defined as $v_{i+1} - v_i$ instead of $\mu_{i+1} - \mu_i$ and it is assumed that $v_{i+1} > v_i$ for all i. In the case of Gaussian distributions, μ_i and v_i are same.

Then, the error probability between S_i and S_{i+1} (i.e., $E_{i,i+1}$) is given by

$$E_{i,i+1} = P(S_i) \cdot \int_{v_i+\Delta_{i,1}}^{\infty} \phi_i(t)dt + P(S_{i+1}) \cdot \int_{-\infty}^{v_{i+1}-\Delta_{i+1,0}} \phi_{i+1}(t)dt \tag{27}$$

where $P(S_i)$ is the probability of S_i. In addition, $\Delta_{i,1}$ is the distance from v_i to $D_{i,i+1}$ and $\Delta_{i+1,0}$ is the distance from v_{i+1} to $D_{i,i+1}$. $D_{i,i+1}$ is the decision level between S_i and S_{i+1}.

Since v_i and v_{i+1} of (27) are also variables which are determined by $\overrightarrow{\Delta} = \left(\Delta_1, \ldots, \Delta_{2(2^M-1)}\right)$, we will modify (27) as follows.

$$E_{i,i+1} = P(S_i) \cdot \int_{v_0+\Delta_{i,1}}^{\infty} \phi_{i,-}(t)dt + P(S_{i+1}) \cdot \int_{-\infty}^{v_{2^M-1}-\Delta_{i+1,0}} \phi_{i+1,+}(t)dt \tag{28}$$

where $\phi_{i,-}(t) = \phi_i\left(t + (v_i - v_0)\right)$ and $\phi_{i+1,+}(t) = \phi_{i+1}\left(t - \left(v_{2^M-1} - v_{i+1}\right)\right)$. v_0 and v_{2^M-1} are fixed value by (26).

The overall BER and the page BERs of M-bit/cell MLC flash memories are nonnegative weighted sums of $E_{i,i+1}$ for $i = 0, \ldots, 2^M - 2$. Therefore, if $E_{i,i+1}$ is a convex function of $\Delta_{i,1}$ and $\Delta_{i+1,0}$, the proposed verify level control criteria will be convex optimization problems.

The Hessian matrix of $E_{i,i+1}$ is given by

$$\begin{aligned}\nabla^2 E_{i,i+1} &= \begin{bmatrix} \frac{\partial^2 E_{i,i+1}}{\partial \Delta_{i,1}^2} & \frac{\partial^2 E_{i,i+1}}{\partial \Delta_{i,1}\partial \Delta_{i+1,0}} \\ \frac{\partial^2 E_{i,i+1}}{\partial \Delta_{i+1,0}\partial \Delta_{i,1}} & \frac{\partial^2 E_{i,i+1}}{\partial \Delta_{i+1,0}^2} \end{bmatrix} \\ &= \begin{bmatrix} -P(S_i)\cdot\frac{d\phi_{i,-}(v_0+\Delta_{i,1})}{d\Delta_{i,1}} & 0 \\ 0 & -P(S_{i+1})\cdot\frac{d\phi_{i+1,+}(v_{2^M-1}-\Delta_{i+1,0})}{d\Delta_{i+1,0}} \end{bmatrix} \\ &= \begin{bmatrix} -P(S_i)\cdot\phi_{i,-}{}'(v_0+\Delta_{i,1}) & 0 \\ 0 & P(S_{i+1})\cdot\phi_{i+1,+}{}'(v_{2^M-1}-\Delta_{i+1,0}) \end{bmatrix}. \end{aligned} \tag{29}$$

If $\phi_{i,-}{}'(v_0 + \Delta_{i,1}) = \phi_i'(v_i + \Delta_{i,1}) \le 0$ and $\phi_{i+1,+}{}'(v_{2^M-1} - \Delta_{i+1,0}) = \phi_{i+1}'(v_{i+1} - \Delta_{i+1,0}) \ge 0$ (i.e., $\nabla^2 E_{i,i+1}$ is positive semidefinite), $E_{i,i+1}$ is a *convex* function. Therefore, the conditions of $\phi_i(x)$ for convex optimization problems are given by

$$\begin{aligned} &\phi_0'(x) \le 0 \quad \text{for } x > v_0, \\ &\phi_i'(x) \ge 0 \quad \text{for } x < v_i \quad \text{and} \quad \phi_i'(x) \le 0 \quad \text{for } x > v_i, \\ &\qquad i = 1, \ldots, 2^M - 2 \\ &\phi_{2^M-1}'(x) \ge 0 \quad \text{for } x < v_{2^M-1}, \end{aligned} \tag{30}$$

which mean that $\phi_i(x)$ should be a *unimodal* distribution for convex optimization.

Since the measured threshold voltage distributions of recent flash memory products [2-4] are unimodal, the proposed verify level control criteria can be effectively applied to flash memories. In addition, the proposed verify level control criteria can be applied to other memories such as phase change memory (PCM) because the measured distributions of PCM in literature seem to be unimodal [26-28]. Especially, [26] claims that the distributions of PCM could be approximated by the log-normal distribution in spite of the anomalous tail. Therefore, our proposed verify level control criteria are expected to be useful in PCM.

ECC and flash memories of multipage architecture

When algebraic ECC such as Bose, Chaudhuri, and Hocquenghem (BCH) codes are used in a binary symmetric channel (BSC) with bit error probability p, the word error rate (WER) is given by

$$\mathrm{WER}(p) \le \sum_{i=t+1}^{n} \binom{n}{i} p^i (1-p)^{n-i} \tag{31}$$

where n is the codeword length and t is the error correcting capability. The bound becomes an equality when the decoder corrects all combinations of errors up to and including t errors, but no combinations of errors greater

than t (i.e., bounded distance decoder) [29,30]. In this article, the bounded distance decoder will be considered. Once ECC parameters such as n and t are selected, the WER is a function of only p.

Though errors in flash memories are generally not symmetric, the asymmetric component of errors could be minimized if the decision level are selected appropriately [22-24]. For example, for 2-bit/cell flash memories, the errors of page 1 will be symmetric if we select the decision level $\widehat{D}_{1,2}$ between S_1 and S_2 which makes $Q\left(\frac{\Delta_{1,1}}{\sigma_{1,1}}\right) = Q\left(\frac{\Delta_{2,0}}{\sigma_{2,0}}\right)$ in (6). Similarly, the errors of page 2 can be symmetric if we choose the decision levels $\widehat{D}_{0,1}$ and $\widehat{D}_{2,3}$ which make $Q\left(\frac{\Delta_{0,1}}{\sigma_{0,1}}\right) = Q\left(\frac{\Delta_{1,0}}{\sigma_{1,0}}\right)$ and $Q\left(\frac{\Delta_{2,1}}{\sigma_{2,1}}\right) = Q\left(\frac{\Delta_{3,0}}{\sigma_{3,0}}\right)$ in (6).

In the case of $\sigma_i = \sigma_{i+1}$, the decision level $\widehat{D}_{i,i+1}$ which makes the errors symmetric is equal to the optimal decision level $D_{i,i+1}$ as follows.

$$D_{i,i+1} = \widehat{D}_{i,i+1} = \frac{1}{2}(\mu_i + \mu_{i+1}) \tag{32}$$

Although $\sigma_i \neq \sigma_{i+1}$, if σ_i is not substantially different from σ_{i+1}, the difference between $D_{i,i+1}$ and $\widehat{D}_{i,i+1}$ is almost negligible [22]. Therefore, the BER based on $\widehat{D}_{i,i+1}$ is similar to that based on $D_{i,i+1}$. Considering these, we will use (31) to calculate the WER of flash memories [31].

In most of flash memories, program and read operations are performed in page units [10]. Therefore, ECC encoding and decoding are also performed in page units [13-15]. It means that the WER of each page depends on each page BER which corresponds to p in (31). Therefore, the overall WER is given by

$$\mathrm{WER}_{\mathrm{overall}} = \frac{1}{M}\sum_{m=1}^{M} \mathrm{WER}\left(\mathrm{BER}_{\mathrm{page}\ m}\right) \tag{33}$$

where $\mathrm{WER}\left(\mathrm{BER}_{\mathrm{page}\ m}\right)$ is the WER of page m.

Theorem 1. *If* $0 <= p <= \frac{t}{n-1}$, *then WER*(p) *of (31) is a convex function of p.*

Proof. WER(p) of (31) can be computed from the incomplete beta function $I_x(a,b)$ [32].

$$\begin{aligned}\mathrm{WER}(p) &= I_p(t+1, n-t)\\ &= (n-t)\binom{n}{t}\int_0^p x^t (1-x)^{n-t-1}\,dx\end{aligned}$$

□

The second derivative of WER(p) is given by

$$\frac{d^2\mathrm{WER}(p)}{dp^2} = (n-t)\binom{n}{t}p^{t-1}(1-p)^{n-t-2}\{t-p(n-1)\}.$$

Therefore, $\frac{d^2\mathrm{WER}(p)}{dp^2} >= 0$ when $0 <= p <= \frac{t}{n-1}$. □

Generally, the operation range of ECC satisfies the condition of $0 <= p <= \frac{t}{n-1}$. By the convex property of WER(p) and (33), the following equation holds.

$$\mathrm{WER}\left(\frac{1}{M}\sum_{m=1}^{M}\mathrm{BER}_{\mathrm{page}\ m}\right) \leq \frac{1}{M}\sum_{m=1}^{M}\mathrm{WER}\left(\mathrm{BER}_{\mathrm{page}\ m}\right) \tag{34}$$

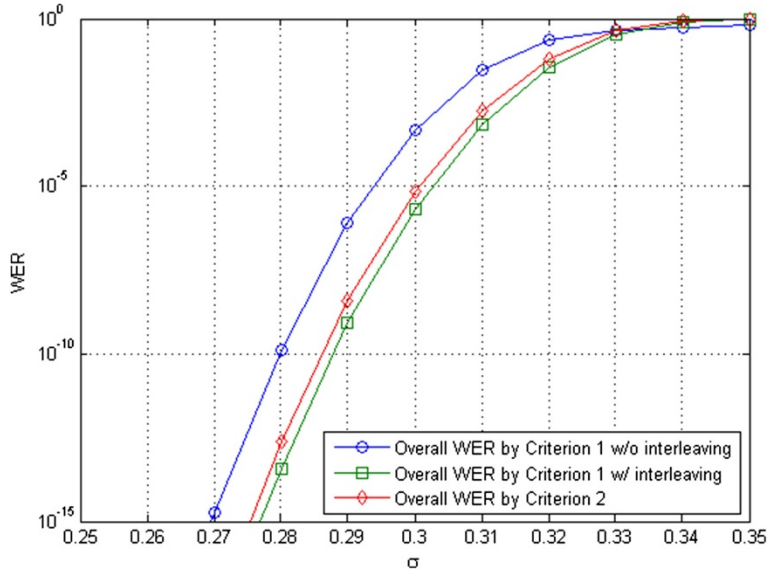

Figure 9 Comparison between the overall WER from criterion1 and from criterion 2 for 2-bit/cell. The BCH code ($n = 8752$, $k = 8192$, $t = 40$) is applied. The constrained voltage window W is assumed to be 5.

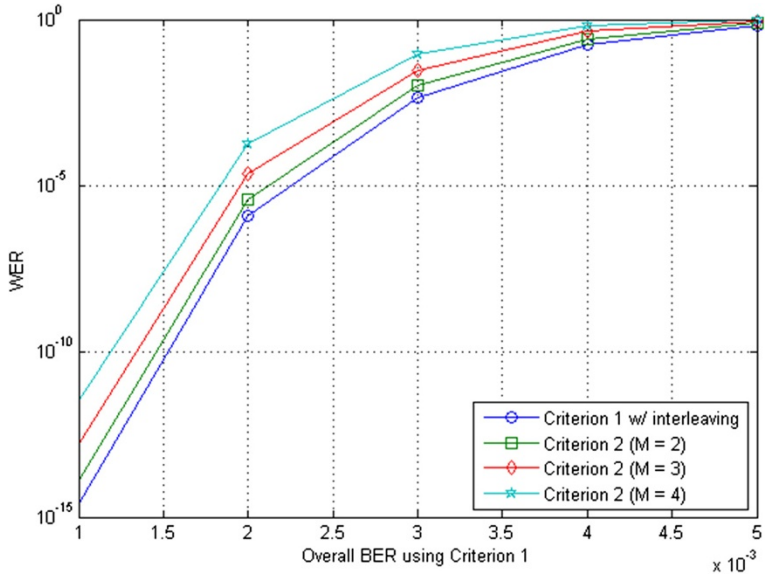

Figure 10 Comparison between the overall WER from criterion1 and from criterion 2 for 2-bit/cell, 3-bit/cell and 4-bit/cell. The BCH code ($n = 8752$, $k = 8192$, $t = 40$) is applied. The constrained voltage window W is assumed to be 5.

(34) reveals that the overall WER would be improved by interleaving. If the interleaver is applied for the whole data from page 1 to page M, all page BERs will be averaged into the overall BER of (8) and the overall WER would be improved according to (34). In other words, minimizing the overall BER (i.e., criterion 1) is preferred over achieving identical page BERs (i.e., criterion 2), if interleaving is applied.

Actually, the application of interleaving and similar ideas have been proposed in order to resolve the uneven page BER problem and improve the reliability [11,12]. However, the adoption of interleaving will slow down the program and read speed performance because the interleaver should wait to collect at least M pages data before program and read operation in the multipage architecture. Especially, random speed performance would be more degraded than sequential speed performance when employing an interleaver (see Section "Hybrid SSD and strategy for verify level control").

Therefore, criterion 2 could be a practical alternative for flash memories because it does not degrade the speed performance and exhibits only slight degradation of the overall BER as shown in Figure 8. In addition, criterion 2 does not require large memory buffer for interleaving. Figure 9 shows that the overall WER from criterion 2 is much better than that of criterion 1 without interleaving and only slightly worse than that of criterion 1 with interleaving for 2-bit/cell flash memories.

However, the WER degradation of criterion 2 will increase as M increases as shown in Figure 10. The reason is that the overall BER from criterion 2 will be much worse than that from criterion 1 for large M as shown in Figure 8. Therefore, criterion 2 would not be appropriate for large M in terms of the reliability.

Hybrid SSD and strategy for verify level control

In order to reduce the cost of SSD and maintain the speed performance and the durability, the hybrid SSD has been proposed [16,17]. The basic idea is to use both SLC flash memories and MLC (usually 2-bit/cell) flash memories. The SLC flash memory has an edge over the MLC flash memory in terms of the speed performance and the durability. However, the MLC flash memory is cheaper than the SLC flash memory. Therefore, combining them can allow both types of flash memories to complement each other [16-19].

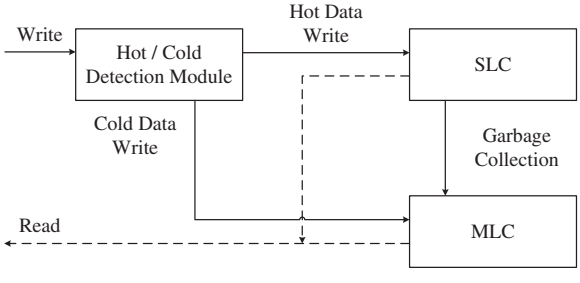

Figure 11 The architecture of the hybrid SSD [18]. The hot and cold detection module separates hot data from cold ones dynamically.

Recently, many flash translation layer (FTL) mapping schemes classify incoming data into *hot* and *cold* based on the access frequency and size. If a data is updated frequently, it is referred to as hot, and otherwise cold. Generally, small data are accessed more often, and they are classified as hot data. Meanwhile, cold data correspond to bulk writes at low frequencies [16,18]. The speed performance of SSD is classified into random speed performance and sequential speed performance. The random speed performance is measured in input/output operations per second (IOPS) and the sequential speed performance is measured by transfer rate or throughput such as MB/sec [33]. Considering the characteristics of hot and cold data, we see that the random speed performance is a pivotal factor for hot data and the sequential speed performance is important for cold data.

Figure 11 illustrates the architecture of the hybrid SSD. In this architecture, the hot and cold detection module separates hot data from cold ones dynamically and directs them either to SLC or MLC based on the decision. Before SLC flash memories run out of free blocks, the hybrid SSD performs garbage collection to merge valid cold data of SLC and move them into MLC [18].

Based on this architecture of the hybrid SSD, we propose that criterion 1 with interleaving is suitable for storing cold data in MLC because the interleaving would have only a small impact on the sequential speed performance for the cold data access and the garbage collection. Of course, we do not need to consider the verify level control criterion for SLC.

In addition, we can anticipate a lower cost and high density hybrid SSD which combines two types of MLC flash memories. For example, 2-bit/cell may replace SLC and 4-bit/cell may be used in place of 2-bit/cell. Unlike the conventional hybrid SSD which combines SLC and MLC of 2-bit/cell, we have to consider the verify level control criterion for both hot and cold data. We propose that criterion 2 will be appropriate for 2-bit/cell flash memories which mainly deal with hot data. For 4-bit/cell which usually stores cold data, criterion 1 with interleaving will be suitable considering the sequential speed performance and the reliability.

Conclusion

In this article, we investigated the verify level control criteria of ISPP for MLC flash memories. These criteria are formulated and solved by convex optimization. Criterion 1 can minimize the overall BER, however it requires interleaving in multipage architecture which reduces the speed performance. Criterion 2 is suitable for multipage architecture especially for 2-bit/cell flash memories. The problem of criterion 2 is that the error rate degradation will increase for more bits per cell.

Based on these advantages and disadvantages of verify level criteria, we investigated the application of verify level control criteria for the hybrid SSD. By selecting the proper criterion considering the architecture of the hybrid SSD, we can achieve both reliability and speed performance.

The verify level control criteria and the proposed formulation of optimization problems can be extended to other emerging memories such as PCM which are modeled by unimodal distributions.

Competing interests

The authors declare that they have no competing interests.

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