

Poster presentation

## Verifying the biological relevance of a neuromorphic hardware device

Daniel Brüderle\*, Karlheinz Meier, Eilif Mueller and Johannes Schemmel

Address: Kirchhoff Institute for Physics, University of Heidelberg, Germany

Email: Daniel Brüderle\* - [bruederle@kip.uni-heidelberg.de](mailto:bruederle@kip.uni-heidelberg.de)

\* Corresponding author

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### Background

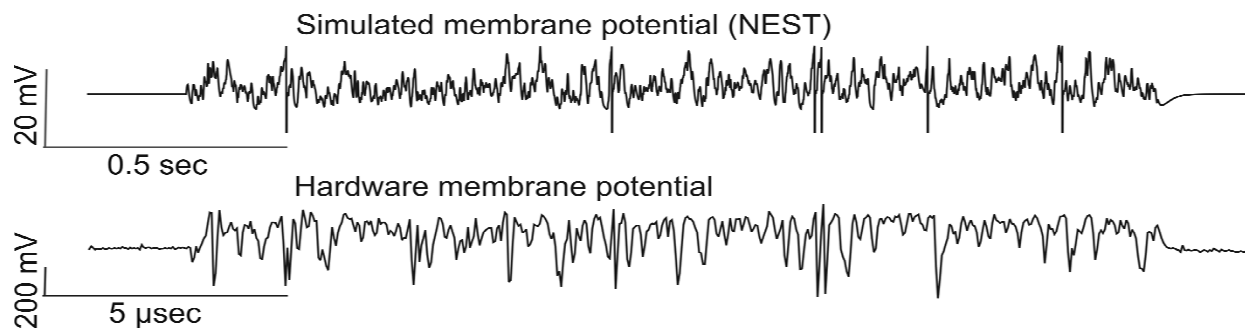
Within the FACETS research project, a neuromorphic mixed-signal VLSI device was created [1]. It was designed to exhibit a linear correspondence with an I&F neuron model, including synaptic plasticity and short-term synaptic dynamics. It operates with a speedup factor of around  $10^5$  compared to biological real time. Utilizing the existing prototype, networks of up to 384 neurons and the temporal evolution of the weights of  $10^5$  synapses under STDP can be modeled.

### Methods

We developed a software framework which allows a unified access to both the hardware system and the pure software neuro-simulator NEST, providing the possibility to verify that the chip can be operated in a biologically realistic regime. From within a single software scope, we can compare and post-process results obtained from both systems, based on identical input and network setups.

### Results

We present experiments that illustrate the status of hardware neuron model verification by comparing its dynamics to NEST simulations. Exemplarily, Figure 1 shows the

**Figure 1**

The membrane potentials of a single neuron under Poisson process input. The upper one has been simulated using NEST, the lower one is a digitization of the analog voltage trace of the neuromorphic hardware.

linear correspondence between the hardware and the software neuron model.

### Conclusion

To establish neuromorphic hardware as a valuable tool for neuroscience, its biological correctness has to be proven. We provide a tool for the direct comparison of a specific hardware system and a simulation software. Our experimental data illustrates the functionality of the hardware and shows its biological relevance. The resulting uniform software interface will allow modelers to port existing network models to the hardware system with minimal effort.

### Acknowledgements

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### References

1. Schemmel J, Brüderle D, Meier K, Ostendorf B: **Modeling synaptic plasticity within networks of highly accelerated I&F neurons.** In *Proceedings of the 2007 IEEE International Symposium on Circuits and Systems (ISCAS'07)* IEEE Press; 2007.

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