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Research Article

Low Power Data Acquisition System for Bioimplantable Devices

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Signal acquisition represents the most important block in biomedical devices, because of its responsibilities to retrieve precise data from the biological tissues. In this paper an energy efficient data acquisition unit is presented which includes low power high bandwidth front-end amplifier and a 10-bit fully differential successive approximation ADC. The proposed system is designed with 0.18 μm CMOS technology and the simulation results show that the bioamplifier maintains a wide bandwidth versus low noise trade-off and the proposed SAR-ADC consumes 450 nW power under 1.8 V supply and retain the effective number of bit 9.55 in 100 KS/s sampling rate.

1. Introduction

In the past few years, the rapid developments in the field of microelectronics and VLSI have driven forward the advent of implantable medical sensors and devices. Multichannel devices are emerging due to the fact of recording numerous number of biological tissue activities collectively [1]. Such multichannel sensors first collect the extracellular signals from a micromachined array including several electrodes and process them through embedded microelectronic circuits for conditioning, multiplexing, and digitization. A fully implantable recording device would then wirelessly transfer the digital data through an inductive link to an external controller. As the capability to integrate more recording channels is growing, suitable data acquisition systems are needed to meet smaller silicon area and lower power dissipation requirements [2].

Biopotential signals, such as electrooculogram (EOG), electroencephalogram (EEG), electromyogram (EMG), and electrocardiogram (ECG), cover a wide range of spectrum and signal bandwidth ranging from few hertz to 10 kHz [3] and the acquired signals through dense microelectrode arrays are very low in amplitude and susceptible to environment noises [4]. Proper processing of these signals requires amplification and noise cancellation, digitization, and digital signal processing before being considered for analysis. Figure 1 shows the block diagram of the proposed system architecture.

Bioamplifiers are the primary building blocks in biomedical sensing devices [5]. The most common characteristics of bioamplifiers are band pass characteristics, DC offset, low noise or noise reduction, and reduced power consumption. For designing bioamplifiers the power dissipation should be restricted to several orders of below 80 mWcm^{-2} [6] in order not to harm the tissues. Implantable bioamplifiers must dissipate little power so that surrounding tissues are not damaged by heating. For a 1000-electrode system the maximum power dissipation should be limited to some few microwatt per amplifier. Noise elimination is another primary concern of such amplifiers which brings out the band pass feature of these front-end amplifiers. The resulting amplifier in this paper passes signals from 2.52 Hz to 8.07 kHz with an input referred noise of 2.83 μV_{rms} and a power dissipation of 18 μW.

Among the signal processing blocks within a bioimplant, analog to digital converter is a critical interface to convert the amplified signal coming from the front-end amplifier for further backend processing. The SAR ADC architecture suits well the biomedical applications due to its moderate speed, moderate resolution, and very low power consumption characteristics [7]. The primary sources of power consumption in a SAR ADC are the comparator and charge/discharge of the capacitor arrays. This paper describes a fully differential asynchronous SAR ADC in 1.8 μm CMOS technology that

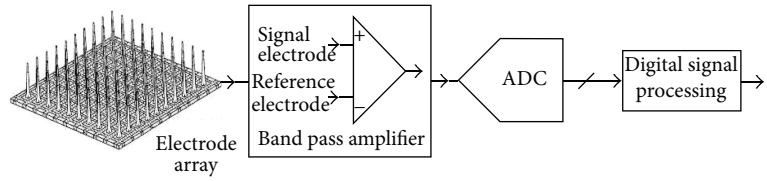

Figure 1: System overview.

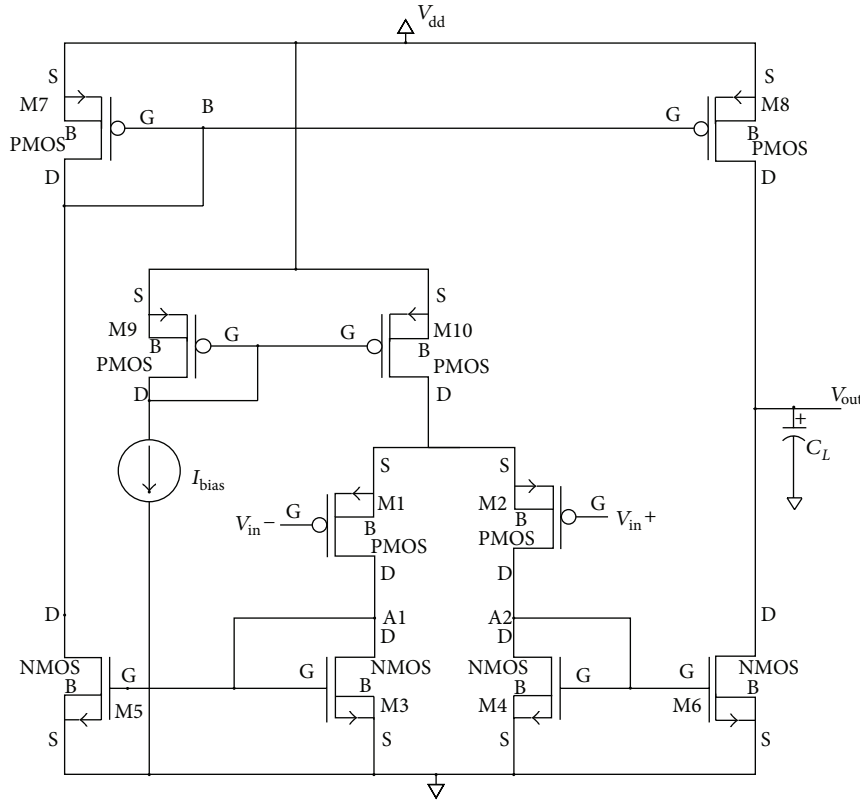

Figure 2: Three-mirror OTA.

uses a charge distribution differential DAC with monotonic capacitor switching architecture designed for energy efficient application. The proposed architecture occupies sample rate of 100 KS/s and a supply voltage of 1.8 V; the 10-bit SAR achieves an ENOB of 9.55 and consumes 450 nW power.

2. Front-End Amplifier

The necessity of front-end bioamplifiers in biomedical signal acquisition system is increasing for applications such as electroencephalogram (EEG), electrocardiogram (ECG), and electromyogram (EMG). A low noise amplifier is required for direct recording of signals from the dense microelectrode arrays as these signals are very weak in amplitude (typically 10–500 μV) and have a wide range (1–10 Khz) [13]. Due to electrochemical effects at the electrode-tissue interface DC offsets are common across differential electrodes. It is necessary to reject the DC offset [14] as the electrode electrolyte interface may reach few hundreds of millivolts sometimes. Amplifier required for the purpose of bioimplantable data acquisition system must pursue high gain, acceptable bandwidth, and good stability with low power consumption and low noise. For this purpose symmetric operational transconductance amplifier (OTA) or three-current-mirror OTA [15] is used, as shown in Figure 2.

This symmetric OTA has a large transconductance, slew rate, and gain bandwidth compared to the other basic OTA's. In the given architecture input stage is a differential pair where M1, M3 and M2, M4 pairs are self-biased inverters.

Transistors M3, M5; M4, M6; M7, M8; and M9, M10 are simple current mirrors. In this symmetric OTA a dominant pole (P1) is present at the output node and two nondominant poles are present at nodes A (P2) and B (P3). Due to symmetric behavior at the input stage, the amplifier has a RHP (right hand plane) zero (Z) which can reduce the phase margin and cause instability of the system. To ensure stability P2, P3 $\gg$ P1 and Z $=$ 2 $*$ P2. This can be satisfied by making CL large. The poles P2 and P3 can also be increased by decreasing the size of M3, M4, and M7 transistors. Next, the reduction of noise especially the flicker noise which dominates at the low frequencies depends on the sizing of the transistors. A practical technique to reduce the flicker noise is

Table 1: Comparison with other amplifiers.

Topology	Technology	V_{dd}	Current (μA)	Gain (dB)	Bandwidth (Hz)	V_{rms} (μ)	C_L (pF)
[8]	CMOS 0.5 μ	±1.8	8	70.4	116.9 m–1.5 K	2.5	15
[9]	CMOS 0.35 μ	±1.5	2	46	13–8.9 K	5.7	—
[6]	CMOS 1.5 μ	±2.5	16	40	130 m–7.5 K	3.1	17
This work	CMOS 0.18 μ	1.8	10	54.57	2.52–8.07 K	2.83	1

Table 2: Comparison and performance evaluation.

Parameter	[10]	[11]	[12]	This work
Technology	0.18 μ	0.18 μ	0.18 μ	0.18 μ
Bits	10	12	10	10
Supply (V)	1	1	1	1.8
Power (W)	6.7 μ	3.8 μ	42 μ	450 n
Sampling rate (KS/s)	100	100	500	100
SNDR (dB)	61.2	58	58.4	59.28
SFDR (dB)	84.8	64.2	75	78.74
ENOB	9.87	9.4	9.4	9.55
FOM (fJ/conv.-step)	71	56	124	6

to use PMOS transistor as input stage with large gate areas. So flicker noise can be avoided by adjusting the (W/L) ratio of M1 and M2 transistors. The band pass amplifier architecture is shown in Figure 3.

Such an amplifier features band pass characteristics. The depicted topology consists of a low noise amplifier (A1) following an inverting miller integrator in its feedback path. The miller integrator uses a second amplifier (A2), a capacitor (C_f), and a high value resistor (Req). In this scheme the DC rejection is achieved by an active integrator located in the feedback loop. The high pass cutoff frequency is set by the small capacitor C_f and MOS bipolar equivalent resistor (Ma, Mb). So A2 OTA occupies the miller integrator configuration. The integrator's time constant τ is set by a small capacitor (C_f) and the MOS bipolar devices acting as a high equivalent pseudoresistor in a configuration of a diode connected PMOS. The mid band gain of the bioamplifier is the same as the DC gain of main OTA (A1) and its −3 dB low pass cutoff is set by OTA (A1)'s dominant pole. Common mode rejection is provided through V_{ref} which senses the common mode voltage from terminal. −3 dB high pass cutoff frequency can be defined as

$$f_{hp} = \left(\frac{A_{v1}}{2\pi\tau}\right), \quad (1)$$

where $\tau = \text{Req} * C_f$.

The gain bandwidth and the input referred noise output are given in Figures 4 and 5.

The mid band gain achieved in this case is 54.57 dB for the input voltage of 1.8 V. The circuit is consuming 10 μA current here. The bandwidth is between 2.52 Hz and 8.07 KHz which is providing the opportunity of wide range of operation for the designed bioamplifier. The calculated input referred noise is 2.83 μV_{rms} which is lower than some other previously designed bioamplifiers. A comparison with the previously published results is shown in the performance evaluation table given in Table 1.

3. ADC Architecture

Figure 6 shows the designed SAR ADC block that is based on architecture from [16] where the building blocks are the comparator, T/H circuit, DAC, and a 10-bit successive approximation register (SAR) controller. For achieving better linearity binary-weighted capacitor array is used rather than a C-$2C$ capacitor array [17] in the designed SAR ADC.

In this charge redistribution based architecture, the capacitor network serves as both a T/H circuit and a reference DAC capacitor array. Therefore, this architecture does not require a high power consuming gigantic size Track and Hold circuit. Since this ADC is fully differential, the operation of the two input sides is complementary. After fetching the input signal, first, the ADC samples those signals on the top plates of the capacitor array via the Track and Hold circuits: $V_{in}+ = V_{ip}$ and $V_{in}- = V_{in}$, and at the same time the bottom plates of the capacitor array are connected to V_{ref}, the reference voltage of the designed ADC. The comparator then directly performs the first comparison without switching any capacitor as soon as ADC turns off the Track and Hold switches. Now, the largest capacitor (C_1) on the higher voltage potential side is switched to ground according to the comparator output. At the same moment of time the other one capacitor (on the lower side) remains unchanged and the digital output D1 is generated. The ADC repeats the procedure until the LSB is decided. For each bit cycle, there is only one capacitor switch, which reduces the power dissipation by the DAC network and switch buffer. The flow chart of the proposed successive approximation procedure is shown in Figure 7. Figure 8 shows an example of how V_{in} and V_{ip} vary at every comparison.

To extract 10 bits, 10 time slots are required for comparison and 9 for DAC switching. After each switching procedure, the common mode voltage of the DAC gradually decreases towards GND or 0 V as shown in the timing diagram in Figure 8.

3.1. Track and Hold Circuit. Figure 9 is the Track and Hold circuit using a bootstrapped switch originally presented in [18]. When the CLK is low ("off" phase or "Hold" phase) [19], MN7 and MN8 discharge the gate of MN4 to ground. At the same time, V_{dd} is applied across the capacitor C by MP1 and MN6 transistor. The capacitor will act as the battery across the gate and source of MN4 during "on" phase. MP2 and MN3 isolate the bootstrapped switch from the capacitor C while it

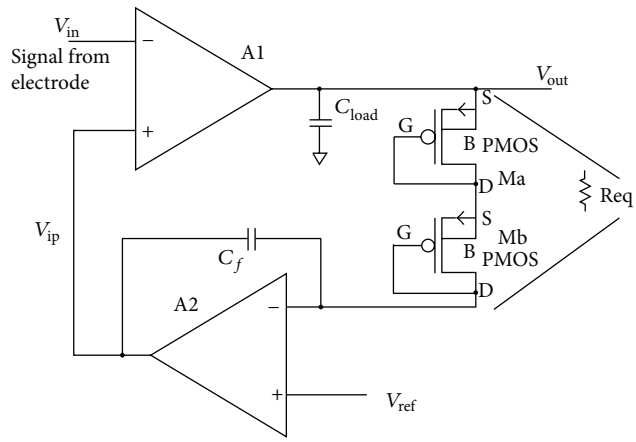

Figure 3: Loaded inductive link.

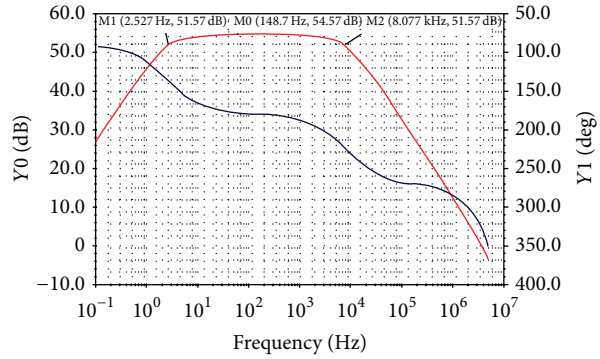

Figure 4: Gain bandwidth and phase diagram.

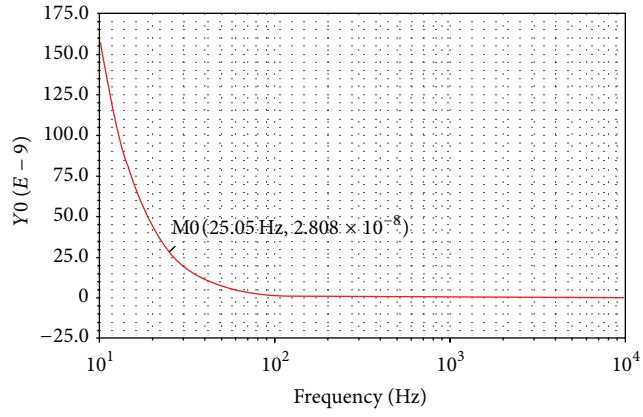

Figure 5: Input noise diagram.

is charging in "off" phase. When CLK is high ("on" phase or "Track" phase), MN5 pulls down the gate of MP2, allowing charge from battery capacitor C to flow on the gate of MN4. This turns both MN3 and MN4 on and give Track of the input voltage at V_{in}. Capacitor C must be sufficiently large (160 pF in this case) to supply charge to the gate of the switching device in addition to all parasitic capacitance in the charging path. The bulk of MP1 and MP2 are connected to the highest potential voltage, top plate of the bootstrapped capacitor C rather than V_{dd}.

To avoid the body effect (which can cause distortion at high frequency input signal) of the tracking switch MN4, bulk switching technique [20] is adopted. Transistors MN1 and MN2 are added to mitigate the body effect problem. During Track or "on" phase the bulk of MN4 is connected to input V_{in} via MN1 cancelling the body effect. In the Hold phase or

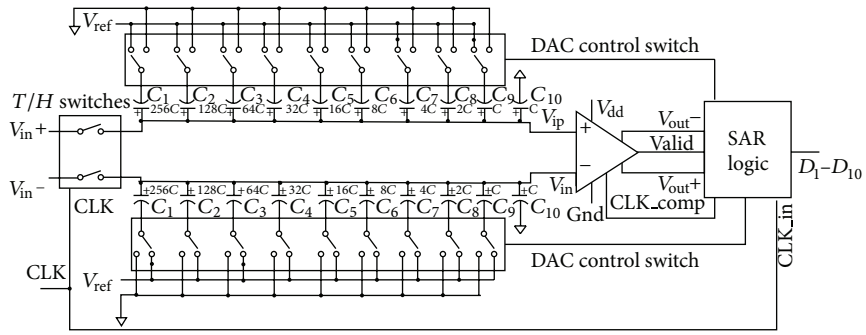

FIGURE 6: Proposed fully differential SAR ADC architecture.

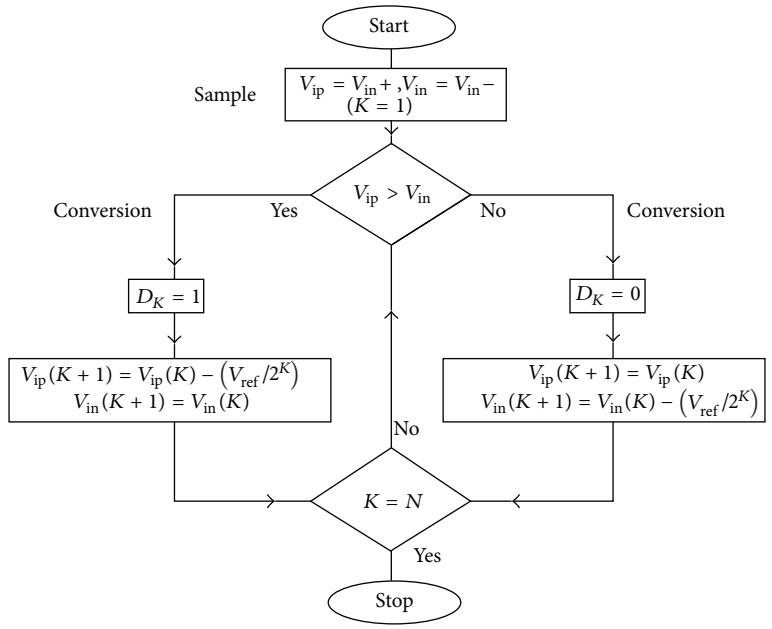

FIGURE 7: Logic flow of proposed SAR ADC.

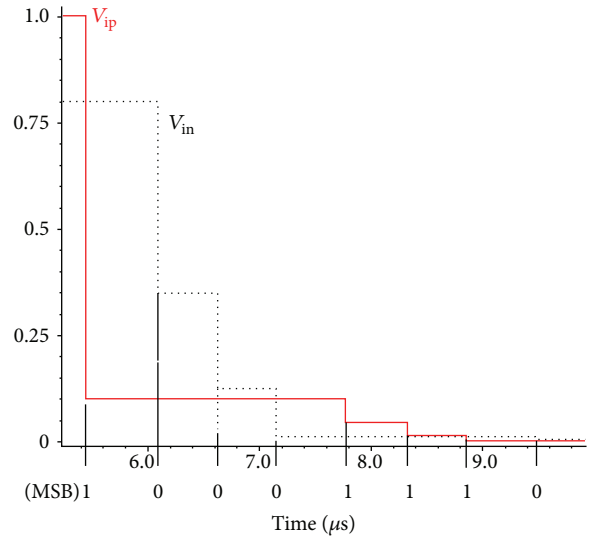

FIGURE 8: Timing diagram with monotonic switching procedure.

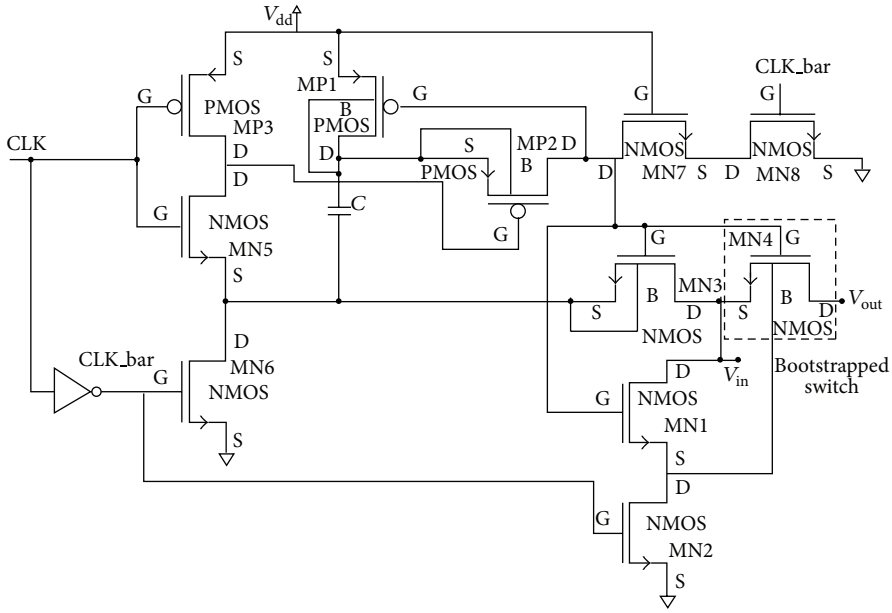

Figure 9: Track and Hold circuit.

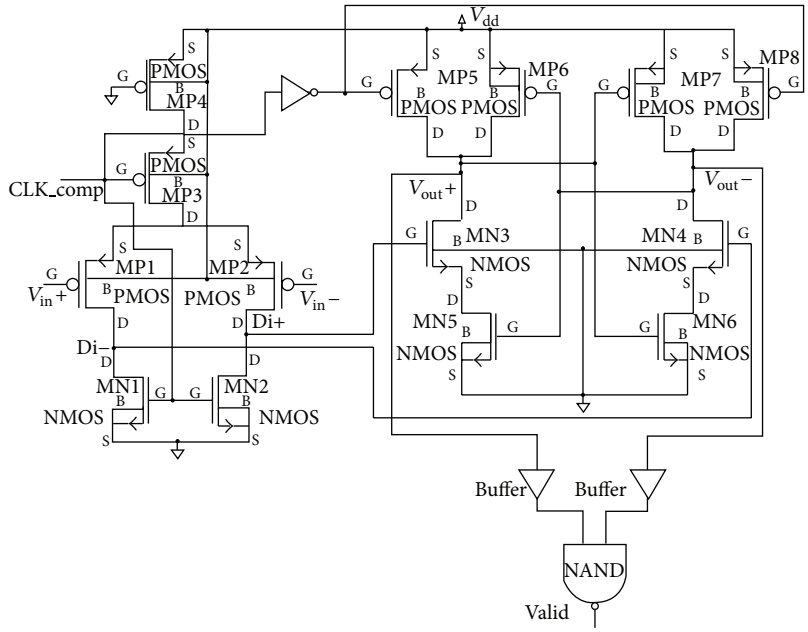

Figure 10: Dynamic comparator with Valid signal generation.

"off" phase the bulk is connected to GND via MN2 to prevent negative source-bulk voltage.

3.2. Dynamic Comparator. Figure 10 is showing the proposed dynamic comparator [21] circuit. It is a two-stage comparator: first stage is the input gain stage and 2nd stage is the output latch. This architecture made this comparator operate in a lower and stable offset. It also operates in a wide range of common mode voltages and at a lower supply voltage.

In precharge phase (CLK_comp = 1), Di+ and Di− are grounded by MN1, MN2 transistors and the V_{out} are precharged by MP5, MP8 transistors. In comparison phase (CLK_comp = 0), MP3 is on, so Di+ and Di− nodes voltage start to charge from ground to V_{dd} with a different time rate proportional to each input voltage. So MP1 and MP2 generate a differential voltage at Di+ and Di− nodes. This differential voltage is now passed to output latch through MN3 and MN4 transistors.

So the cross coupled inverter in output latch regenerates the V_{out} voltages according to the difference present at the input gain stage. Figure 12 is showing the output generated by the dynamic comparator.

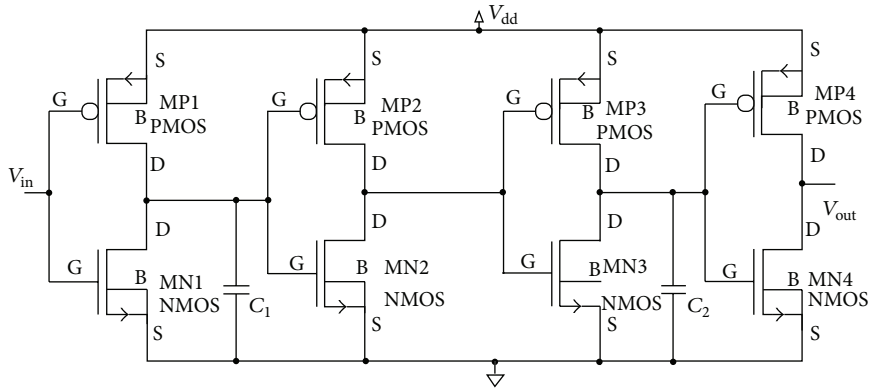

Figure 11: Delay buffer.

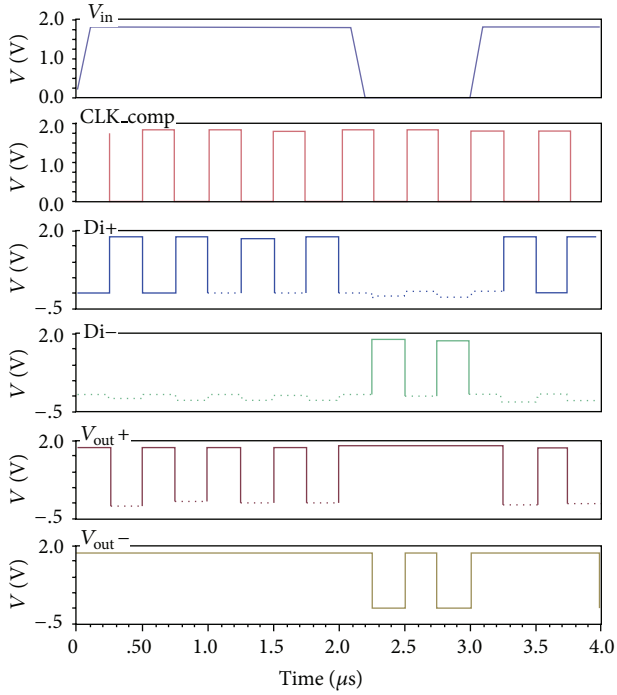

Figure 12: Dynamic comparator output.

The dynamic offset of the proposed comparator is minimized by adding MP4 transistor at the top of the gain stage. As MP4 is in the saturation region, the change of its drain to source voltage has a slight influence on the drain current. Hence MP4 keeps the effective voltage of the input pair near a constant value when common mode voltage changes. The dynamic offset thus has a minor influence on the conversion linearity. Again the MP1 and MP2 have large size to minimize the offset.

CLK_comp signal generation is dependent on a signal "Valid" extracted from the dynamic comparator using a two-input NAND gate. Figure 11 is showing a delay buffer of approximately 250 ns in between the NAND and the comparator output. In comparison phase (CLK_comp = 0), one of the comparator output V_{out} is going low which makes the NAND output high. This high signal passes through the SAR logic and brings CLK_comp signal to the precharge phase (CLK_comp = 1) and this process continues; thus an asynchronous clock signal (CLK_comp) is generated. But if the Valid signal is generated concurrently with the V_{out}, the CLK_comp will not continue in the comparison phase for a proper period of time; consequently the comparison will not be done appropriately. Figure 13 is showing the generation of Valid signal.

3.3. Asynchronous SAR Control Logic. Figure 14 shows the implemented SAR logic [16] and Figure 15 is showing the asynchronous static DFF circuit. The proposed circuit can generate necessary clock inside it, so no high frequency clock generator is required. SAR logic is asynchronous; by using the "Valid" indication from the comparator, a timing state machine is controlled.

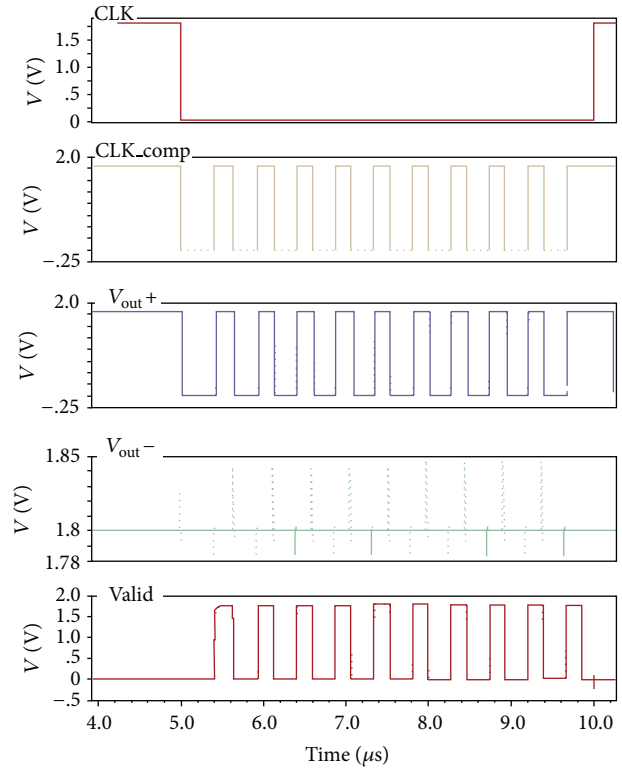

Figure 13: Valid signal generation.

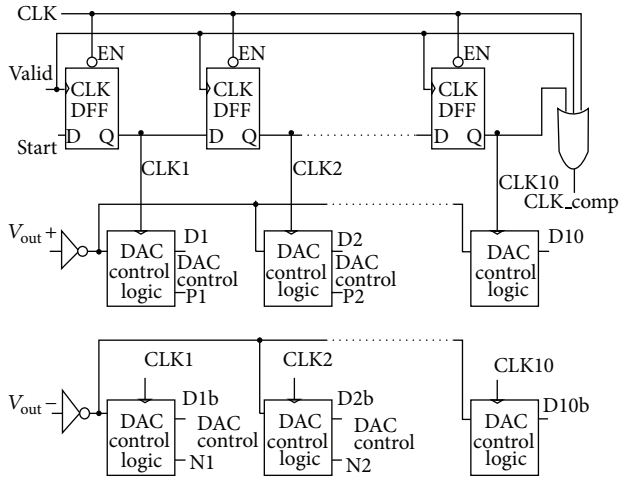

Figure 14: SAR logic controller with DAC control.

Figure 16 shows the timing diagram of asynchronous control logic. CLK1 to CLK10 sample the digital output codes of the comparator and serve as control signals for the capacitor arrays to perform the monotonic switching procedure via the DAC control logic. Figures 17 and 18 show a schematic and a timing diagram of the DAC control logic, respectively.

$V_{out}+$, $V_{out}-$ are precharged to VDD in precharge phase. When comparator works in comparison phase, one of the two outputs will go low. A logical NAND operation detects this high-to-low transition and generates an active-high Valid indication that will be used for the asynchronous SAR controller. The CLK1 to CLK10 also serve as control signals for the DAC capacitor arrays to perform monotonic switching procedure via 10 DAC control logic units.

As shown in Figures 14 and 15, the first 9 DAC control logic parts include a DFF, an AND gate, and a delay buffer to make sure that CLK triggers AND gate when the output of

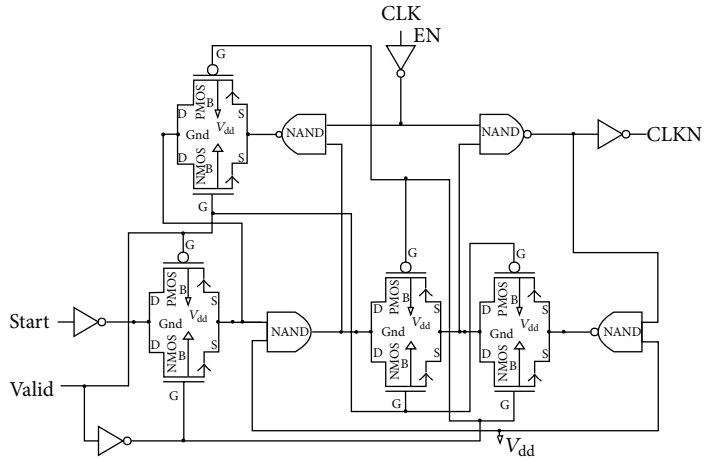

Figure 15: Positive edge triggered asynchronous static DFF.

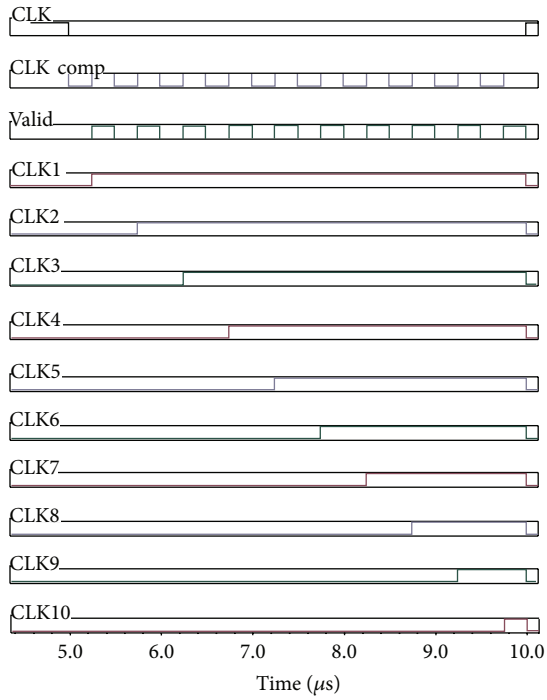

Figure 16: Timing diagram.

DFF generated; and the last DAC control part is only a DFF that will generate last bit, D10. Figure 18 shows example of the simulated waveforms of DAC control logic. At the rising edge of CLK1 and CLK2, DFF samples the comparator output $V_{\text{out}}+$. As $V_{\text{out}}+$ is low, the DAC control signals DAC CON P1 and DAC CON P2 are high to switch the relevant capacitor switches. Again at rising edge of CLK 3 comparator output $V_{\text{out}}-$ is high, which results in DAC CON N3 being high to control the corresponding capacitor switch.

3.4. Charge Redistribution DAC. Figure 19 shows the architecture of charge redistributing DAC. DAC control logic generates control signals DAC Control P $\langle 1:9 \rangle$ and DAC Control N $\langle 1:9 \rangle$ controlling the DAC capacitor arrays. The inverters can be used as switches to generate V_{ref} (= 1.8 V) and GND (= 0 V) for bottom plate of the DAC capacitors as shown in Figure 19. The ADC uses two T/H circuits to sample pseudodifferentially the input signal on top plate of the capacitors and uses inverters to switch between V_{ref} and GND. The small unit capacitance value is 1 pF.

4. Measurement

The ADC is designed in a standard 0.18 μm CMOS process and in cadence ADEL spectra simulator. Figure 20 shows the digital code output for an input of 1.8 V. Figure 21 is showing the die micrograph. The static performance is characterized through differential nonlinearity (DNL) and integral

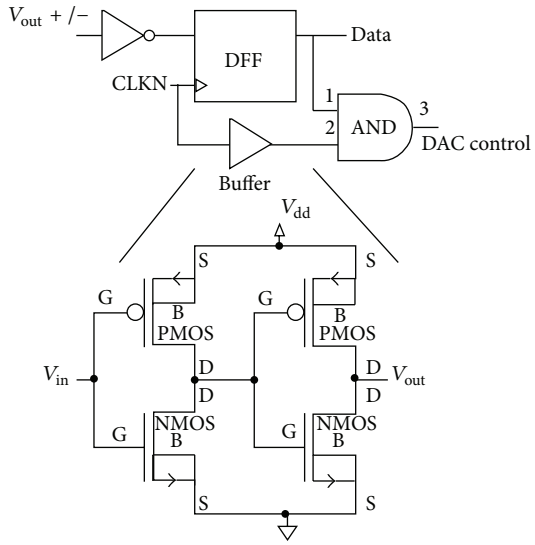

Figure 17: DAC control logic.

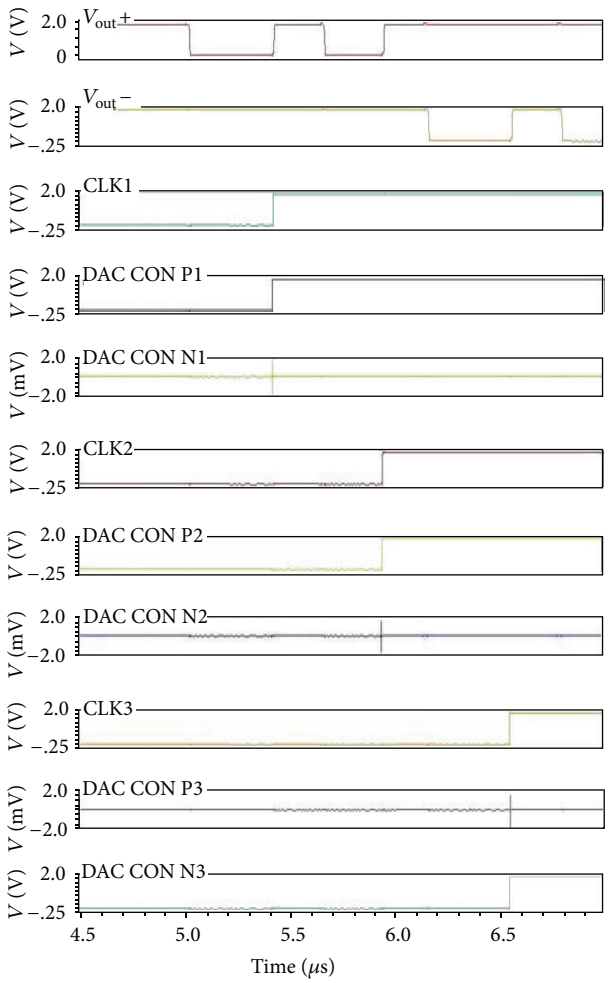

Figure 18: DAC control logic output.

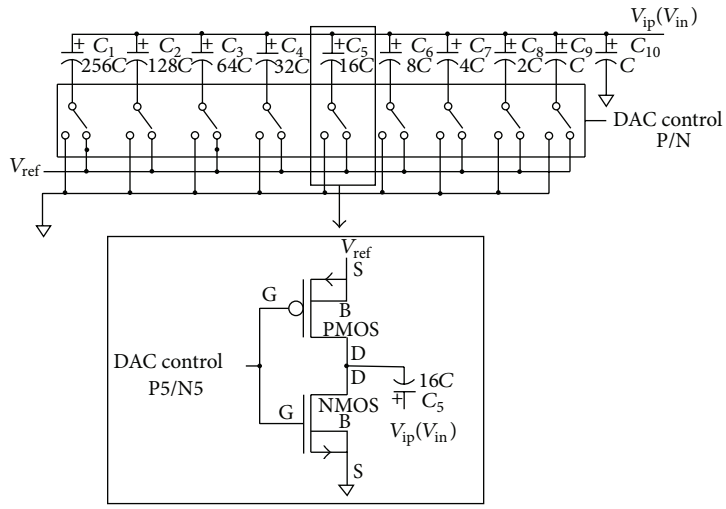

FIGURE 19: Charge redistribution DAC with inverter based switches.

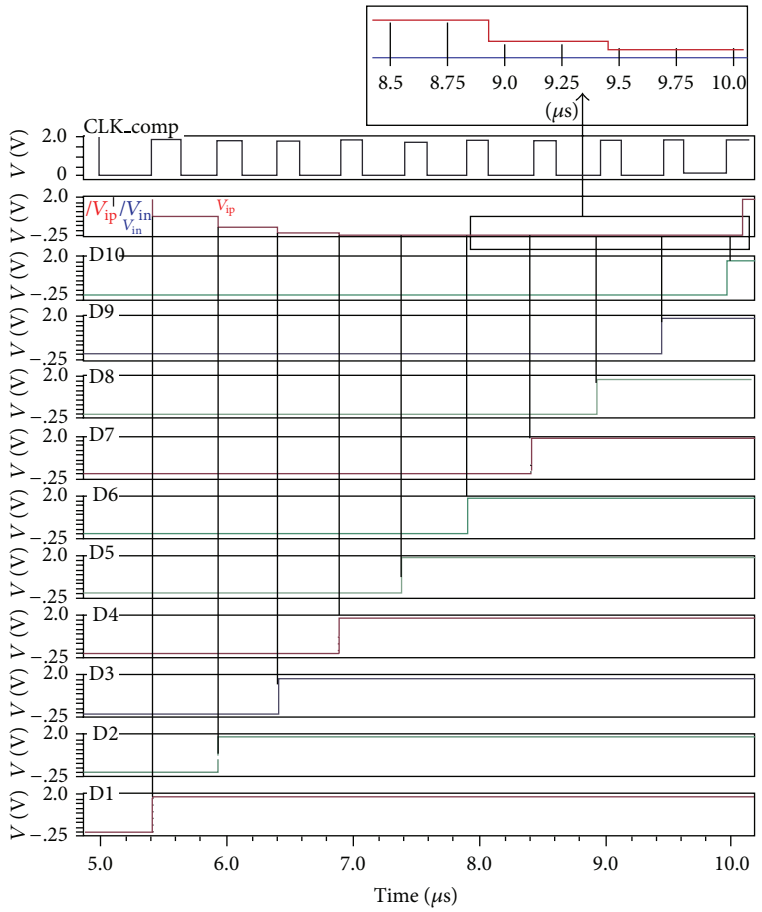

FIGURE 20: Digital code output for an input of 1.8 V.

nonlinearity (INL) measurement. The measured DNL and INL are +0.455/−0.43 LSB and +0.62/−0.58 LSB, respectively, and are shown in Figures 22 and 23. The measured FFT spectrum at input frequency 4.68 KHz and sample frequency of 100 KHz is shown in Figure 24. The measured SNDR is 59.28 dB which equals ENOB of 9.55 bits and the SFDR is 78.74 dB as shown in Figure 24. The total power dissipation of the ADC is 450 nW at 100 KS/s sampling rate and supply voltage of 1.8 V. T/H circuit and the DAC capacitor arrays are consuming 50 nA (approximately); dynamic comparator

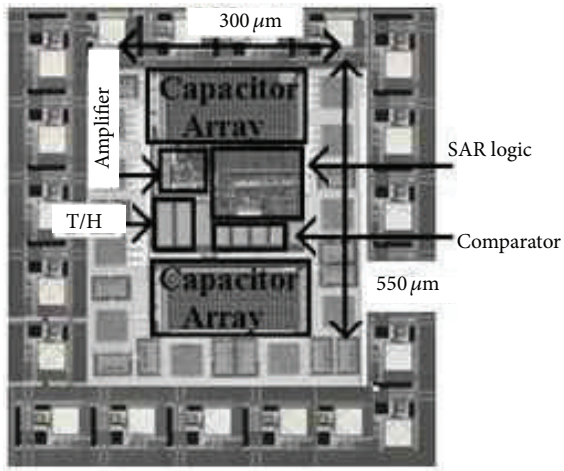

Figure 21: Die micrograph.

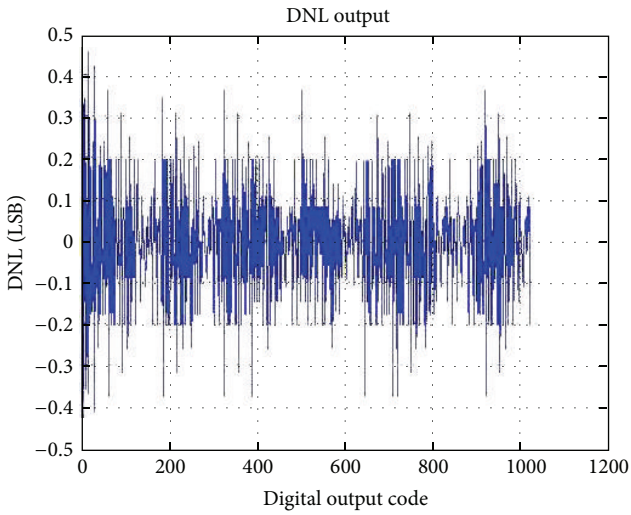

Figure 22: DNL plot.

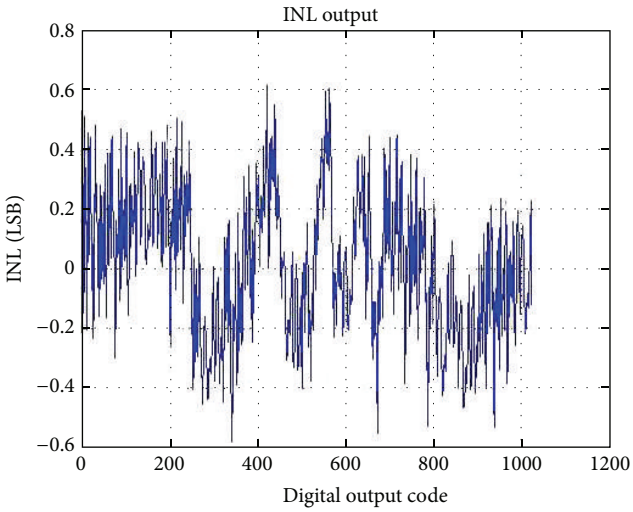

Figure 23: INL plot.

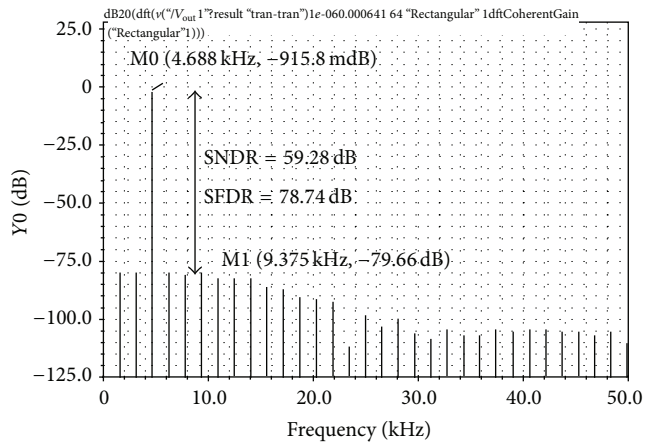

Figure 24: Measured FFT of input frequency 4.68 KHz.

is dissipating 100 nA and overall SAR logic circuit consuming 100 nA current. The typical figure of merit (FOM) definition of the ADCs is defined as

$$\text{FOM} = \frac{\text{Power}}{\left(2^{\text{ENOB}} * fs\right)}. \quad (2)$$

The FOM of this work corresponds to 6 fJ/conversion-step.

In 0.18 μm CMOS process the die micrograph occupies an active area of 300 μm × 550 μm. The experimental result provides a 51.2 dB gain for a loss of 14.2 μA of current in the front-end amplifier. The measured power loss including SAR ADC and the front-end amplifier is 21 μwatt. The ADC provides a practical 9.17 ENOB for 56.96 dB SNDR (see Table 2).

5. Conclusion

This paper proposed a low power and high bandwidth front-end amplifier as part of an implantable device for accumulating data from the tissue electrolyte and microelectrode interface. The proposed ADC reduces the power consumption as well as the total capacitance. The ADC delivers 9.55 ENOB with a power consumption of 450 nW at a sampling rate of 100 KS/s. It utilizes an ultralow power design strategy, imposing maximum simplicity in ADC architecture, low capacitive DAC switching scheme. So proposed low power design in this paper suited well the biomedical applications.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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