

Research Article

Electronically Tunable Quadrature Sinusoidal Oscillator with Equal Output Amplitudes during Frequency Tuning Process

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A new configuration of voltage-mode quadrature sinusoidal oscillator is proposed. The proposed oscillator employs two voltage differencing current conveyors (VDCCs), two resistors, and two grounded capacitors. In this design, the use of multiple/dual output terminal active building block is not required. The tuning of frequency of oscillation (FO) can be done electronically by adjusting the bias current of active device without affecting condition of oscillation (CO). The electronic tuning can be done by controlling the bias current using a digital circuit. The amplitude of two sinusoidal outputs is equal when the frequency of oscillation is tuned. This makes the sinusoidal output voltages meet good total harmonic distortions (THD). Moreover, the proposed circuit can provide the sinusoidal output current with high impedance which is connected to external load or to another circuit without the use of buffer device. To confirm that the oscillator can generate the quadrature sinusoidal output signal, the experimental results using VDCC constructed from commercially available ICs are also included. The experimental results agree well with theoretical anticipation.

1. Introduction

Quadrature sinusoidal oscillators are very important circuits in numerous applications such as communication, sound system, instrumentation, control system. Especially in modulation system, the quadrature oscillator is used to generate the carrier signal for quadrature amplitude modulation (QAM) and single-sideband modulation (SSB) [1, 2]. Most of sinusoidal oscillator designs required the following features: low THD of the quadrature sinusoidal output, independent control of frequency of oscillation (FO) and condition of oscillation (CO) [3], using minimum number of active and passive element [4], electronic controllability [5] and so on. However, the amplitude of quadrature sinusoidal output should be considered too. To avoid the use of external amplifier, the expected amplitude of quadrature output should be equal for all frequency or during tuning FO.

The design of electronic circuit in analog signal processing has been emphasized in the use of active building block [6–8]. Particularly, the electronically tunable active building

blocks have attracted significant research attention since analog circuits using electronically tunable active building block give more fine-tuning than adjusting the value of passive device. The voltage differencing current conveyor (VDCC) [9, 10] is a recently reported versatile active building block used in the realization of analog signal processing circuits. VDCC is also attractive due to its capability of electronic controllability. The analog circuits using VDCC as active element have been found in the literature, for examples, universal filter [11–14], first-order all-pass filter [15], ladder filter [16], passive element simulator [10, 17–21], and square and triangular wave generator [22]. The VDCC-based sinusoidal oscillators have been proposed in [19, 23–26]. In [19], the Colpitts oscillator using VDCC-based capacitance multiplier was proposed. In this oscillator, the FO and CO can be independently tuned. It can provide quadrature output waveform but the amplitude of quadrature output voltage is not equal during tuning the frequency. Also it requires dual output terminal VDCC (W_n and W_p terminal). The simple current-mode oscillator using single

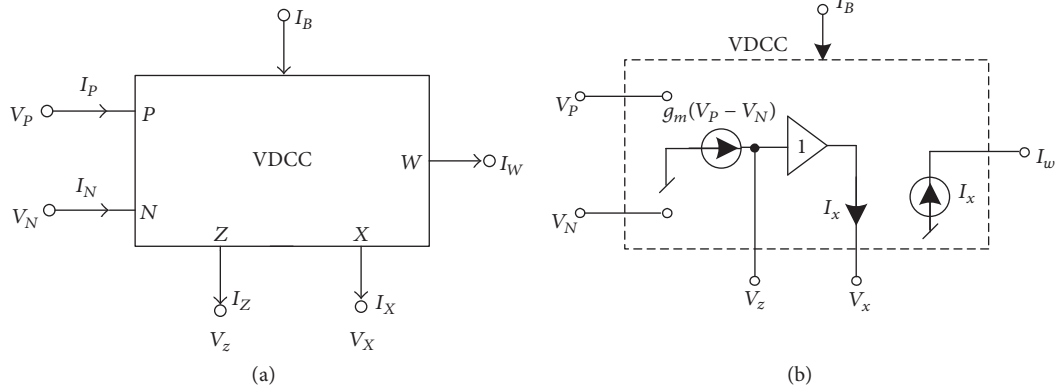


FIGURE 1: VDCC: (a) circuit symbol of VDCC; (b) equivalent circuit.

VDCC and grounded passive elements was presented in [23]. The FO and CO can be orthogonally controlled. The current-mode quadrature sinusoidal waveform is obtained. However, the FO cannot be electronically tuned without affecting CO. Also the amplitude of quadrature output waveform is not equal during tuning the frequency. The simple voltage-mode quadrature oscillator using single VDCC, two grounded resistors, and two grounded capacitors was implemented in [24]. The FO and CO can be orthogonally controlled. The FO can be electronically tuned without affecting the CO. However, the amplitude of quadrature output waveform is not equal during tuning the frequency. In [25], the quadrature oscillator using two VDCC, two grounded resistors, and two grounded capacitors was presented. The FO and CO can be independently/electronically controlled. However, the amplitude of quadrature output waveform is not equal during tuning the frequency. In [26], the quadrature oscillator using single controlled gain VDCC (CG-VDCC) and two grounded capacitors was presented. The FO and CO can be independently/electronically controlled. However, the amplitude of quadrature output waveform is not equal during tuning the frequency. Also the internal construction of CG-VDCC using the commercially available ICs is quite complicated.

The idea behind this work is to present the quadrature sinusoidal oscillator emphasized on the use of VDCC as active element. The amplitude of quadrature output waveform is equal during tuning of frequency. Also, the frequency of oscillation can be electronically tuned without affecting the condition of oscillation.

2. Proposed Circuit and Operation

2.1. Voltage Differencing Current Conveyor (VDCC). In this design, the active building block (ABB) called voltage differencing current conveyor (VDCC) is used as main active device. The international construction of CMOS VDCC was proposed by Kaçar et al. [10] in 2014. It is five-port device, namely, P , N , Z , X , and W port. The high impedance voltage input ports are P and N . The high impedance current output ports are Z and W port. The low impedance voltage output port is X port. In the original version of VDCC the output

current at W port provides the output current both positive and negative direction called W_n and W_p ports. However, in this purpose, only single W port is required. This can reduce the current tracking error at W port and can reduce the number of transistor in VDCC. The electrical symbol and equivalent circuit of VDCC are shown in Figure 1. The ideal electrical properties of VDCC are shown in

$$\begin{bmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_{WP} \\ I_{WN} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix}, \quad (1)$$

where g_m is the transconductance gain. For CMOS VDCC, g_m is controlled by DC bias current I_B as follows:

$$g_m = \sqrt{I_B \mu_n C_{ox} \left(\frac{W}{L} \right)}, \quad (2)$$

where I_B is bias current, μ_n is mobility of the carrier for MOS transistors, C_{ox} is gate-oxide capacitance per unit area, W is effective channel width, and L is effective channel length, respectively. The internal construction of CMOS VDCC is shown in Figure 2 [10]. The VDCC can be constructed from commercially available ICs as shown in Figure 3. It consists of LM13700 [27] and AD844 [28]. This construction contains only single w terminal. g_m for this construction is given as

$$g_m = \frac{I_B}{2V_T}, \quad (3)$$

where V_T is the thermal voltage.

2.2. Proposed Oscillator. The proposed oscillator consists of two VDCCs, two resistors, and two grounded capacitors. The quadrature output voltages V_{o1} and V_{o2} are the voltage dropped at Z port of VDCC1 and VDCC2, respectively.

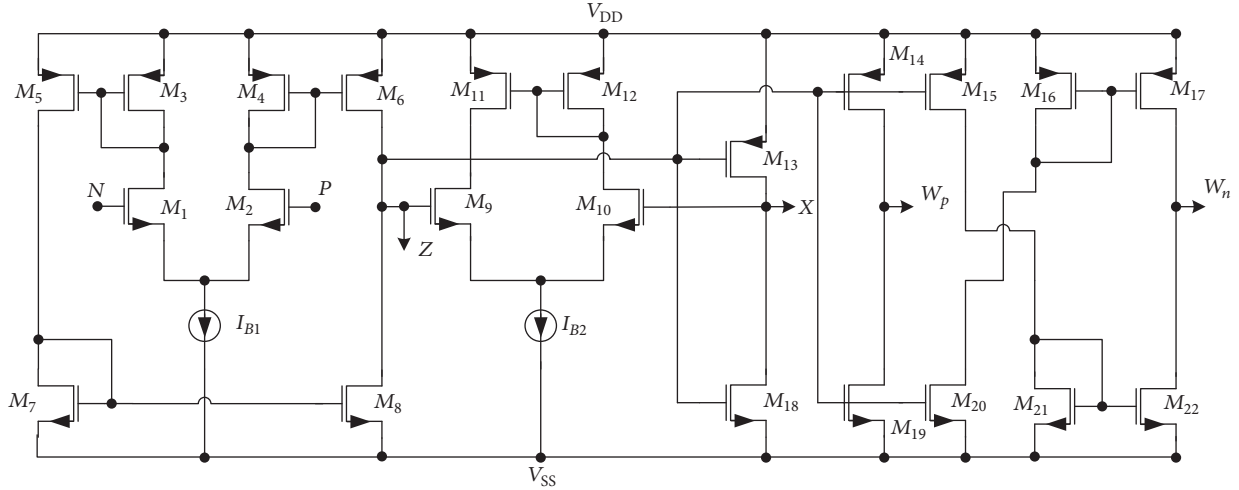
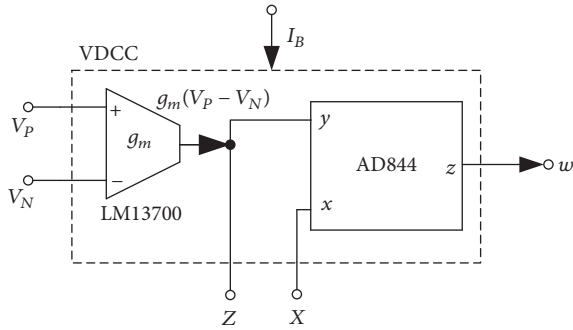


FIGURE 2: Internal construction of CMOS VDCC [10].


 FIGURE 3: VDCC (without dual W terminal) constructed from commercially available ICs.

However, the output voltages are taken from the non-low-impedance output nodes, so the voltage buffers are needed for cascading. The output current I_O with high impedance flows from W port of VDCC2. Taking into consideration the ideal port characteristics involved in VDCC as referred above (2) and the relevant notations appearing in Figure 4, the characteristic equation is as follows:

$$s^2 + s \left(1 - \frac{R_2}{R_1} \right) \frac{g_{m1}}{C_1} + \frac{R_2 g_{m1} g_{m2}}{R_1 C_1 C_2} = 0. \quad (4)$$

From (4), the frequency of oscillation is given as

$$\omega_0 = \sqrt{\frac{R_2 g_{m1} g_{m2}}{R_1 C_1 C_2}}. \quad (5)$$

Subsequently, the condition of oscillation is given as

$$R_2 \geq R_1. \quad (6)$$

It is evident from (5) and (6) that the frequency of oscillation can be controlled by g_{m1} and g_{m2} without affecting the condition of oscillation. Moreover, the frequency of oscillation

can be electronically tuned via g_{m1} and g_{m2} . If $R_2 \cong R_1$, the frequency of oscillation is rewritten as

$$\omega_0 = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}}. \quad (7)$$

From the circuit in Figure 4, the voltage ratio of V_{o1} and V_{o2} is as follows:

$$\frac{V_{o2}}{V_{o1}} = \frac{g_{m2}}{s C_2}. \quad (8)$$

It is found from (8) that the output voltages V_{o2} and V_{o1} are 90-degree phase difference which is called quadrature signal. The phase of output voltage V_{o1} leads the phase of output voltage V_{o2} to 90 degrees. At frequency of oscillation (ω_0), the magnitude of output voltage ratio in (8) becomes

$$\left| \frac{V_{o2}}{V_{o1}} \right| = \frac{g_{m2}}{\omega_0 C_2}. \quad (9)$$

Substituting (7) into (9), the magnitude of output voltage ratio in (9) becomes

$$\left| \frac{V_{o2}}{V_{o1}} \right| = \sqrt{\frac{g_{m2} C_1}{g_{m1} C_2}}. \quad (10)$$

If $C_1 = C_2$ and $g_{m1} = g_{m2}$, the magnitude of output voltage ratio is equal to unity. Therefore, the tune of frequency of oscillation with electronic method can simultaneously change g_{m1} and g_{m2} to keep the amplitude of output voltages V_{o1} and V_{o2} equal. This makes the sinusoidal output voltages meet low total harmonic distortions (THD). Moreover, if VDCC is constructed from commercially available ICs as illustrated in Figure 3 where its g_m is linearly tuned by bias current, the frequency of oscillation can be linearly controlled.

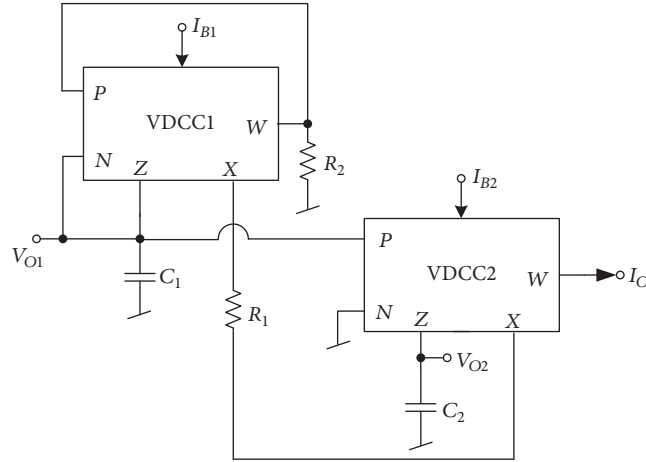


FIGURE 4: Proposed quadrature oscillator.

3. Analysis of Frequency Stability

The analysis of frequency stability of the proposed circuit is done by using the definition of the frequency stability factor (S_F) given in [29, 30]

$$S_F = \left. \frac{d\phi(u)}{du} \right|_{u=1}, \quad (11)$$

where $u = \omega/\omega_0$ is normalized frequency and $\phi(u)$ is the phase expression of the open loop transfer function of circuit in Figure 4 and its transfer function is expressed as follows:

$$T(s) = \frac{s(R_2 g_{m1}/R_1 C_1)}{s^2 + s(g_{m1}/C_1) + R_2 g_{m1} g_{m2}/R_1 C_1 C_2}. \quad (12)$$

With the above definition, the frequency stability factor of the proposed oscillator is given as

$$S_F = 2\sqrt{n}, \quad (13)$$

where $C_1 = C_2 = C$, $R_1 = R_2 = R$, $g_{m1} = 1/R$, and $g_{m2} = n/R$.

4. Effect of Nonideal Current/Voltage Gains and Parasitic Elements

Practically, the influence of nonideal current/voltage gain and parasitic element in VDCC will affect the performances of the proposed oscillator. Considering these gains, the electrical properties of VDCC are given as $I_z = g_m(V_P - V_N)$, $V_x = \beta V_z$, and $I_x = \alpha I_z$, where β and α represent the voltage and current gain error, respectively. At high impedance ports V_P , V_N , Z , and W , a parallel parasitic combination of a resistance and a capacitance appears and they are denoted

as R_P , C_P , R_N , C_N , R_Z , C_Z , R_W , and C_W , respectively. At low impedance port x , a series parasitic resistance appears and it is denoted as R_x . These parasitic impedances affect the performance of the proposed oscillator. Taking them into account, the characteristic equation of the circuit in Figure 4 is obtained as

$$Y_1 Y_2 + Y_2 g_{m1} \left(1 - \frac{\alpha_1 \beta_1}{R_1^* [1/R_2 + Y_3]} \right) + \frac{\alpha_1 \beta_2 g_{m1} g_{m2}}{R_1^* (1/R_2 + Y_3)} = 0, \quad (14)$$

where $Y_1 = s(C_1 + C_{N1} + C_{Z1} + C_{P2}) + G_{N1} + G_{Z1} + G_{P2}$, $Y_2 = s(C_2 + C_{Z2}) + G_{Z2}$, $Y_3 = s(C_{P1} + C_{W1}) + G_{P1} + G_{W1}$, and $R_1^* = R_1 + R_{x1} + R_{x2}$. If the operational frequency $f_{op} \ll 1/[(C_{P1} + C_{W1})(R_{P1} \parallel R_{W1})]$, the characteristic equation in (13) becomes

$$s^2 C_1^* C_2^* + s \left[C_1^* G_{z2} + C_2^* G_1^* + C_2^* g_{m1} \left(1 - \frac{\alpha_1 \beta_1 R_2}{R_1^*} \right) \right] + G_1^* G_{z2} + G_{z2} \left(1 - \frac{\alpha_1 \beta_1 R_2}{R_1^*} \right) + \frac{\alpha_1 \beta_2 R_2 g_{m1} g_{m2}}{R_1^*} = 0, \quad (15)$$

where $C_1^* = C_1 + C_{N1} + C_{Z1} + C_{P2}$, $G_2^* = G_{N1} + G_{Z1} + G_{P2}$, and $C_2^* = C_2 + C_{z2}$. From (14), the frequency of oscillation is obtained as

$$\omega_0^* = \sqrt{\frac{1}{(C_1 + C_{N1} + C_{Z1} + C_{P2})(C_2 + C_{z2})} \left[\left(\frac{1}{R_{N1}} + \frac{1}{R_{Z1}} + \frac{1}{R_{P2}} \right) \frac{1}{R_{z2}} + \frac{1}{R_{z2}} \left(1 - \frac{\alpha_1 \beta_1 R_2}{R_1 + R_{x1} + R_{x2}} \right) + \frac{\alpha_1 \beta_2 R_2 g_{m1} g_{m2}}{R_1 + R_{x1} + R_{x2}} \right]}. \quad (16)$$

Subsequently, the condition of oscillation is given as

$$\left[\frac{1}{g_{m1}R_{z2}} \left(\frac{C_1 + C_{N1} + C_{Z1} + C_{P2}}{C_2 + C_{z2}} \right) + \frac{1}{g_{m1}} \left(\frac{1}{R_{N1}} + \frac{1}{R_{Z1}} + \frac{1}{R_{P2}} \right) + 1 \right] \leq \frac{\alpha_1 \beta_1 R_2}{R_1 + R_{x1} + R_{x2}} \quad (17)$$

$$\left| \frac{V_{o2}}{V_{o1}} \right|^* = \frac{g_{m2}}{\sqrt{[\omega_0^* (C_2 + C_{z2})]^2 + [G_{z2}]^2}} \quad (18)$$

$$= \frac{g_{m2}}{\sqrt{((C_2 + C_{z2}) / (C_1 + C_{N1} + C_{Z1} + C_{P2})) [(1/R_{N1} + 1/R_{Z1} + 1/R_{P2})(1/R_{z2}) + (1/R_{z2})(1 - \alpha_1 \beta_1 R_2 / (R_1 + R_{x1} + R_{x2})) + \alpha_1 \beta_2 R_2 g_{m1} g_{m2} / (R_1 + R_{x1} + R_{x2})] + [1/R_{z2}]^2}} \quad (19)$$

It is found in (19) that although $C_1 = C_2$, $R_1 = R_2$, and $g_{m1} = g_{m2}$, the magnitude of output voltage ratio is not equal to unity. According to (19), the phase response of V_{o2} to V_{o1} becomes

$$\theta_{V_{o2}/V_{o1}}^* = -\tan^{-1} \frac{\omega_0^* (C_2 + C_{z2})}{G_{z2}} \quad (20)$$

5. Experimental Results

In order to verify the performances of the proposed oscillator in Figure 4, the experiment was performed by using VDCC constructed from commercially available ICs, LM13700 from Texas Instruments Incorporated and AD844 from Analog Devices, Inc. as illustrated in Figure 3. The power supply voltages of experiment were ± 5 V. The oscillator was designed to obtain the frequency of oscillation, $f_0 = 50$ kHz. From (7), an experimental setup was made by taking $C_1 = C_2 = 10$ nF, $R_1 = 7.23$ k Ω , $R_2 = 7.52$ k Ω , and $I_{B1} = I_{B2} = 163$ μ A. With the above component values, the experimented frequency of oscillation becomes $f_0 = 47$ kHz. The deviation of theoretical and experimental frequency of oscillation is about 6%. The deviation of theoretical and experimental value stems from the parasitic resistances and capacitances as shown in (16). However, $f_0 = 50$ kHz was obtained when I_{B1} and I_{B2} were set as 180 μ A. The measured sinusoidal quadrature waveforms V_{o1} , V_{o2} and their frequency spectrums are illustrated in Figure 5. The output current waveform and its spectrum which is measured from the voltage dropped on load resistor 10 k Ω are depicted in Figure 6. To obtain the frequency of oscillation $f_0 = 100$ kHz, the bias currents I_{B1} and I_{B2} were set to 370 μ A. Figure 7 represents the output waveforms V_{o1} and V_{o2} and their frequency spectrums. The output current waveform and its spectrum at $f_0 = 100$ kHz is depicted in Figure 8. Tuning of experimental and theoretical FO is shown in Figure 9, where I_{B1} and I_{B2} are equal and were adjusted from 100 μ A to 500 μ A. The range of FO controlled from 27 kHz–131 kHz was obtained. Figure 10 shows simulated dependence of output amplitudes V_{O1} and V_{O2} on FO. It can be clearly seen that the ratio of amplitudes V_{O1} and V_{O2} is quite constant on the tuning of FO if I_{B1} and I_{B2} are

From the circuit in Figure 4, the nonideal voltage ratio of V_{o1} and V_{o2} is as follows:

Substituting (16) into (18), the magnitude of output voltage ratio in (18) becomes

simultaneously tuned as predicted in (10). As stated above, VDCC consists of operational transconductance amplifier (OTA) where it is well known that the BJT OTA gives the linear range if input voltage is lower than $2V_T$ ($\cong 52$ mV). With the result in Figure 10, it is found that the amplitude of output voltages which dropped on input voltage of OTA is close to linear range of OTA. This implies that sinusoidal output waveforms provide good THD. However, at high value of bias current, the deviation of amplitude ratio of V_{o1} and V_{o2} obviously appears. This phenomenon results from the fact that the increment of bias current will decrease the value of parasitic resistance. Therefore, the amplitude of V_{o1} and V_{o2} is slightly different as analyzed in (19). The measured phase difference between the two outputs, V_{o1} and V_{o2} , is illustrated in Figure 11.

6. Comparison with Recent Quadrature Oscillators

A comparison between the proposed quadrature oscillator and recent quadrature oscillator published in scientific journals is shown in Table 1. The terms that will be taken into account are as follows: the used active building block (ABB), number of active and passive element, the way to tune FO and CO, amplitude of the quadrature output waveforms during tuning process, the used ABB without multiple or extra terminals, additional current output with high impedance, the connection of capacitors, and the way to test the circuit.

7. Conclusion

In this contribution, the quadrature sinusoidal oscillator using voltage differencing current conveyor as active element is presented. The proposed circuit comprises two VDCCs, two resistors, and two grounded capacitors. The proposed oscillator provides quadrature voltage output and a high impedance current output. The frequency of oscillation can be electronically tuned without affecting the condition of oscillation. During tuning of the frequency of oscillation, the amplitude of the quadrature output voltages V_{o1} and V_{o2}

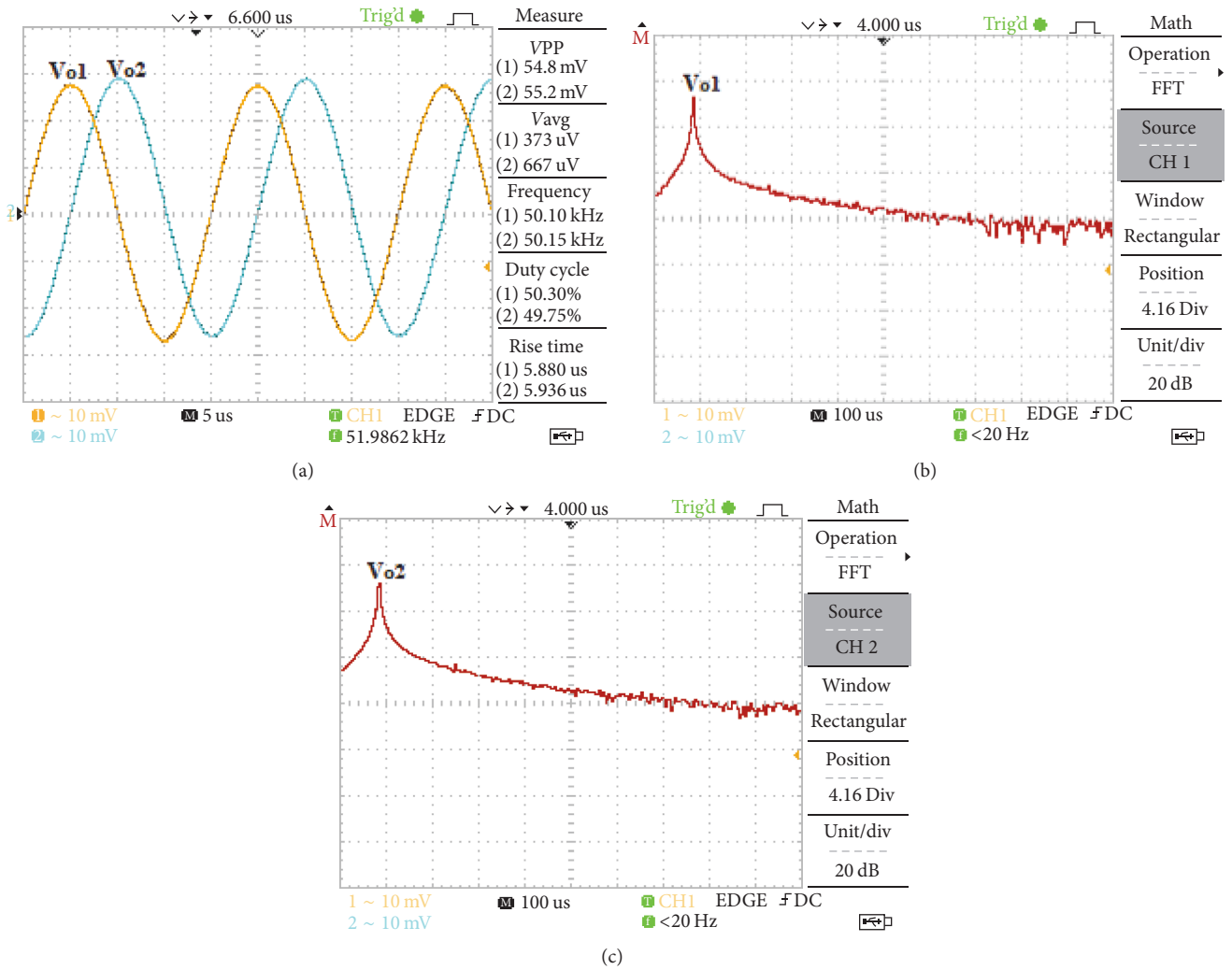


FIGURE 5: Measurement of output voltages and their spectrums at $f_0 = 50$ kHz.

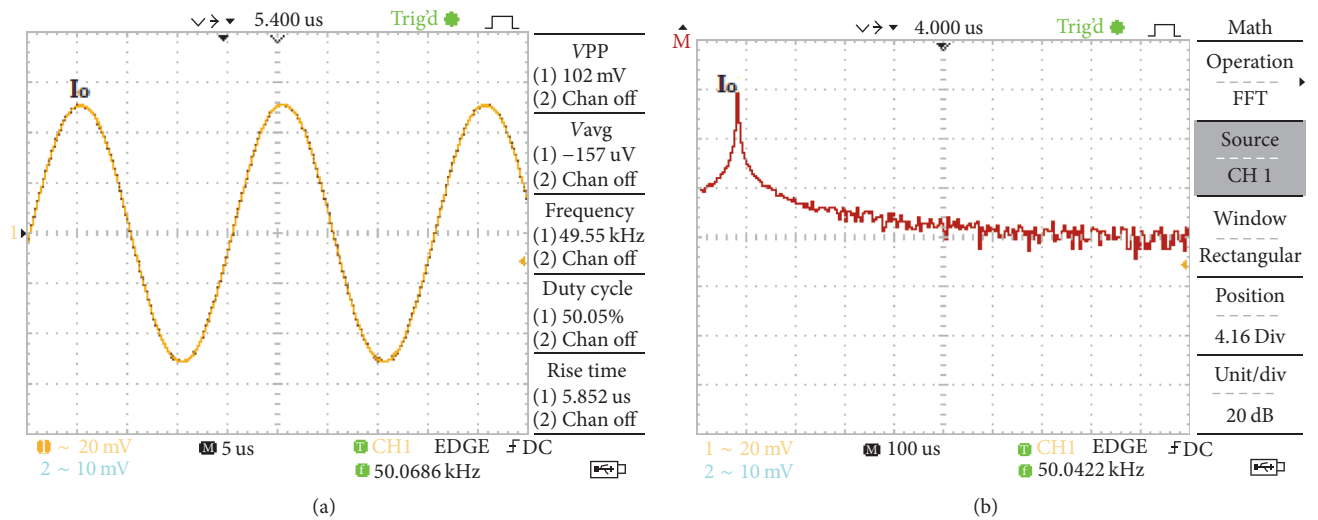


FIGURE 6: Measurement of output current and its spectrum at $f_0 = 50$ kHz.

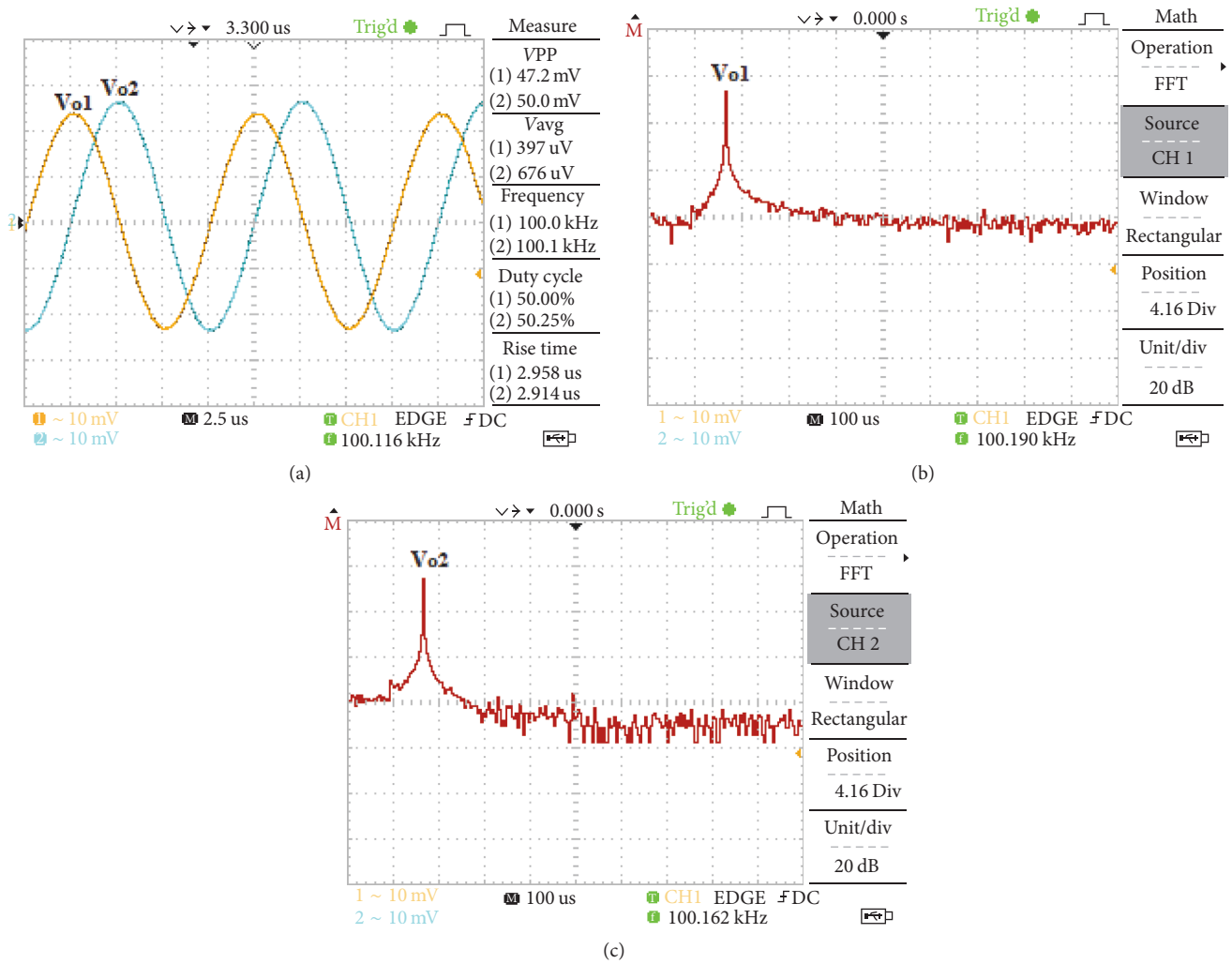


FIGURE 7: Measurement of output voltages and their spectrums at $f_0 = 100$ kHz.

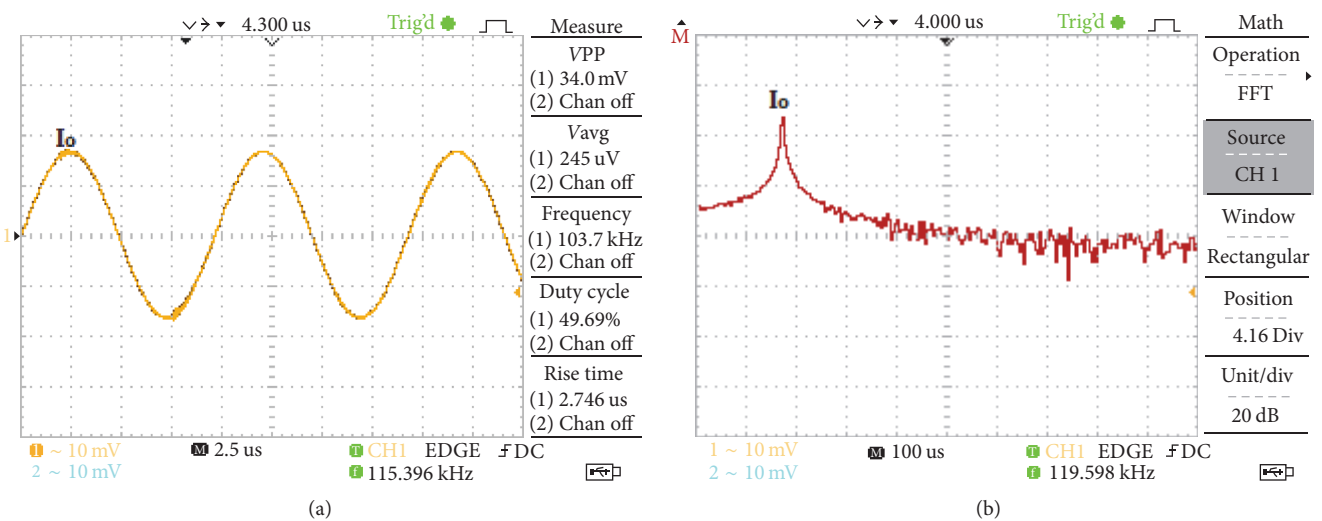


FIGURE 8: Measurement of output current and its spectrum at $f_0 = 100$ kHz.

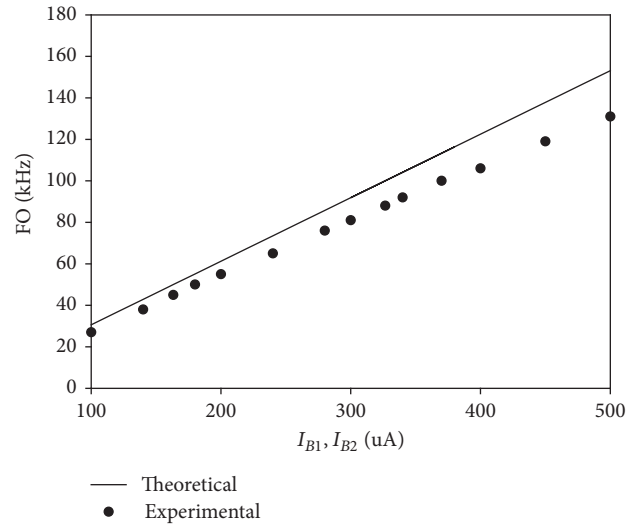


FIGURE 9: Tuning of experimental and theoretical FO by adjusting bias current.

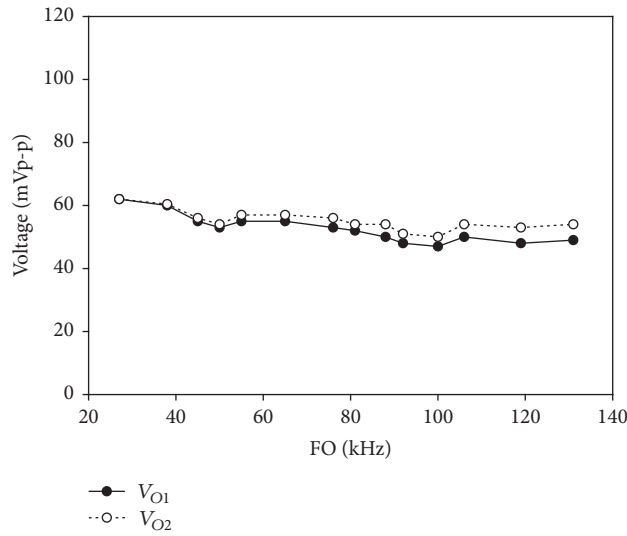


FIGURE 10: Dependence of amplitudes of V_{O1} and V_{O2} on FO.

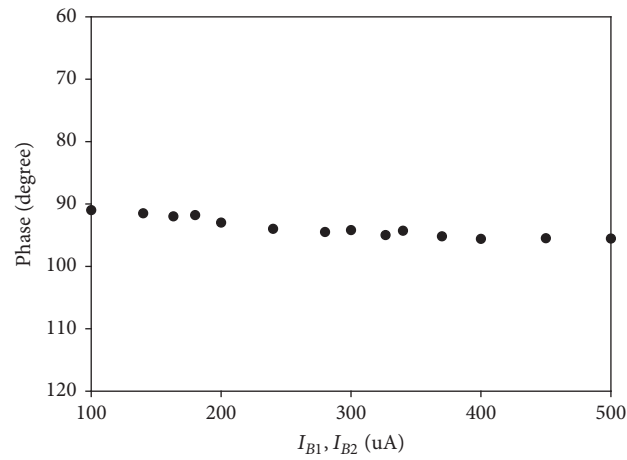


FIGURE 11: The measured phase difference of V_{O1} and V_{O2} .

TABLE 1: Comparison results of this work and recent works.

| Ref | ABB | Number of ABB | Number of R + C | Electronic tune of FO without affecting CO | Equal amplitudes during frequency tuning | No need of multiple output ABB | Providing additional sinusoidal current output with high impedance | Grounded C only | Experimental results |
|-----------|-----------|---------------|-----------------|--|--|--------------------------------|--|-----------------|----------------------|
| [23] | VDCC | 1 | 2 + 2 | No | No | No | Yes | Yes | No |
| [24] | VDCC | 1 | 2 + 2 | Yes | No | No | No | Yes | Yes |
| [25] | VDCC | 2 | 2 + 2 | Yes | No | No | Yes | Yes | No |
| [26] | CG-VDCC | 1 | 0 + 2 | Yes | Yes | No | No | Yes | No |
| [31] | CCCCTA | 1 | 2 + 2 | Yes | No | No | Yes | Yes | No |
| [32] | CCCCTA | 2 | 2 + 2 | Yes | No | No | Yes | Yes | No |
| [33] | CCII & BF | 3 | 4 + 2 | No | No | Yes | No | Yes | Yes |
| [34] | CCII | 3 | 2 + 2 | Yes | No | Yes | No | Yes | No |
| [35] | CDTA | 2 | 0 + 3 | Yes | No | No | Yes | Yes | No |
| [36] | CFOA | 2 | 2 + 2 | No | No | Yes | No | Yes | Yes |
| [37] | CFOA | 2 | 3 + 2 | No | No | Yes | No | Yes | Yes |
| [38] | DD-DXCCII | 1 | 3 + 2 | No | No | No | No | Yes | No |
| [39] | MDVCC | 1 | 2 + 2 | No | No | Yes | No | Yes | No |
| [40] | DVCCTA | 1 | 3 + 2 | Yes | No | No | Yes | Yes | No |
| [41] | FBVDBA | 1 | 1 + 2 | No | No | No | No | Yes | Yes |
| [42] | OTRA | 2 | 3 + 3 | No | No | Yes | No | No | Yes |
| [43] | MVDVTA | 1 | 1 + 2 | No | No | No | No | Yes | No |
| This work | VDCC | 2 | 2 + 2 | Yes | Yes | Yes | Yes | Yes | Yes |

is almost constant with slight differences due to the effect of the parasitic resistances and capacitances of the VDCC. The experimental results using VDCC constructed from commercially available ICs confirm the performance of the theoretical analysis.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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