Hindawi Publishing Corporation
International Journal of Antennas and Propagation
Volume 2013, Article ID 921859, 8 pages
http://dx.doi.org/10.1155/2013/921859

Research Article

Design of an Ultra-Wideband Transition from Double-Sided Parallel Stripline to Coplanar Waveguide

Young-Gon Kim and Kang Wook Kim

School of Electrical Engineering and Computer Science, Kyungpook National University, Sankyuk-dong, Buk-gu, Daegu 702-701, Republic of Korea

Correspondence should be addressed to Kang Wook Kim; kang_kim@ee.knu.ac.kr

Received 26 October 2012; Accepted 20 December 2012

Academic Editor: Tat Yeo

A design method of an ultra-wideband transition from double-sided parallel stripline (DSPSL) to coplanar waveguide (CPW) is proposed based on analytical expressions of characteristic impedance. The conformal mapping is used to obtain the characteristic impedance for each section of the transition within 3.7% accuracy as compared with the EM simulation results. An efficient and clear guideline for the design of the transition is proposed. The implemented transition performs less than 0.6 dB insertion loss per transition for frequencies from 40 MHz to 12 GHz and less than 1.2 dB insertion loss to 27 GHz, which well exceeds the previous results in the literature.

1. Introduction

Balanced transmission lines such as coplanar stripline (CPS), slot line, and double-sided parallel stripline (DSPSL) have frequently been used for applications such as antenna feeds, double balanced mixers, power dividers, and so on [1–5]. Since the DSPSL has broadside coupling between parallel lines on top and bottom planes, DSPSL has an advantage over other balanced lines for easy realization of low characteristic impedances within fabrication limitation. This important feature is very useful to obtain suitable characteristic impedances for various applications.

On the other hand, coplanar waveguide (CPW) consists of three conductors on the top surface of a dielectric substrate, where the center conductor is a signal strip separated from two ground planes on each side by a narrow gap. As one of the unbalanced lines, CPWs have frequently been used as transmission lines in a variety of microwave circuits [6–8]. Since the ground of the CPW can be obtained from the top side of the substrate close to the signal line, a short termination of the CPW can be obtained with much less spurious inductance than that of the microstrip line which uses vias. With the CPW, active devices can be easily mounted on top side of the substrate, and therefore CPW is widely used in implementing MMICs or MICs [7].

In the previous literature, designs for various DSPSL-to-CPW transitions have been reported in [9–11]. In [9], the transition showed performance with less than 1.8 dB insertion loss from 1.1 to 6.45 GHz. In [10], the transition utilized vertical coupling and showed performance with less than 1.4 dB insertion loss from 1.3 to 9 GHz. A vertical transition proposed in [11] operated from 0.5 GHz to 14 GHz with less than 1 dB insertion loss. However, most of the previous transitions had narrow bandwidth and suffered from design complexities due to lack of impedance analysis of the transitional structures.

In this paper, an efficient and clear guideline for the design of DSPSL-to-CPW transition based on analytical expressions of characteristic impedance is presented. The conformal mapping method is applied to obtain the analytical expressions, and details of the analysis process are described. The proposed transition is also designed and implemented to exhibit ultra-wideband performance from 40 MHz to 27 GHz.

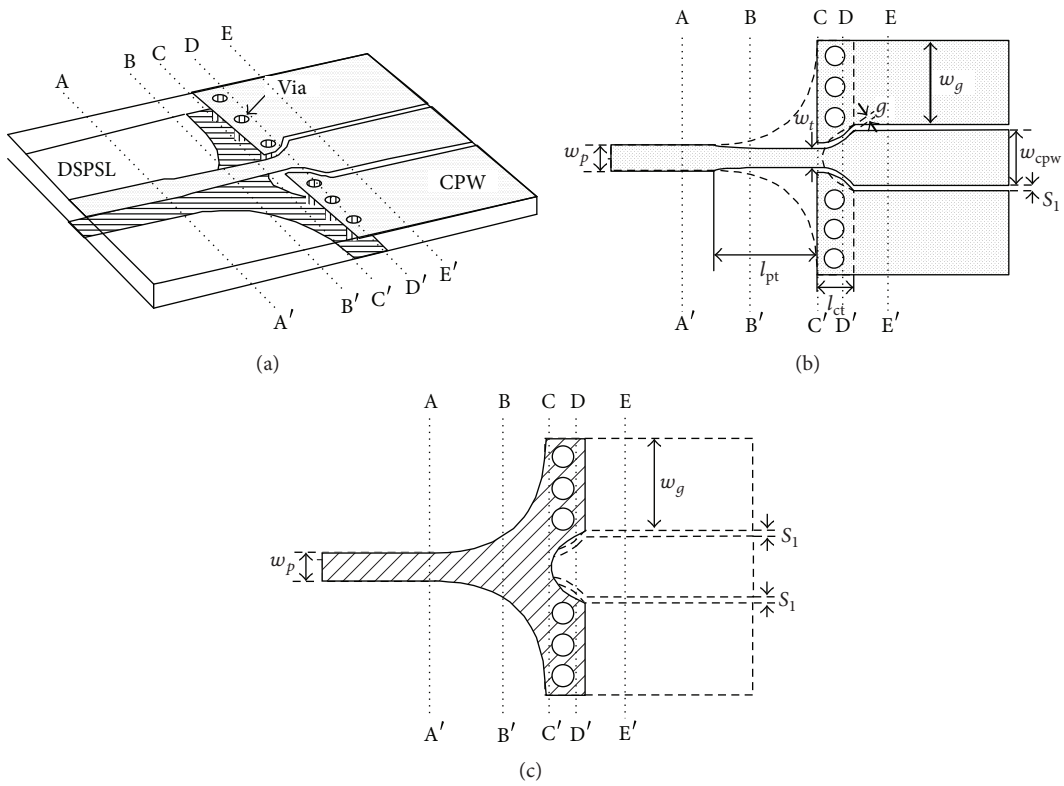

Figure 1: Proposed configuration of the DSPSL-to-CPW transition: (a) perspective view, (b) top view, and (c) bottom view.

2. Configuration of the Proposed Transition

The proposed structure of the DSPSL-to-CPW transition is illustrated in Figure 1. RT/Duroid 4003 with 8 mil thickness (dielectric constant of 3.38) is used as substrate for the transition. The proposed transition consists of two transitions: a DSPSL-to-conductor backed CPW (CBCPW) transition (A-A′ to C-C′) and a CBCPW-to-CPW transition (C-C′ to E-E′). Firstly, in the DSPSL-to-CBCPW transition, the top conductor of the DSPSL is connected to the center conductor of the CBCPW. From the DSPSL to CBCPW, the width of the top signal conductor line is changed to adjust the impedance of transitional structure. The bottom line of the DSPSL is shaped to become the bottom ground plane of CBCPW. Secondly, in the CBCPW-to-CPW transition, the ground is connected to the wings of CPW using via holes, which provide ground continuity. The center conductor line and bottom ground are tapered to achieve impedance matching and smooth field distributions along the transition.

The electric field lines at each cross-section in Figure 1 along the transition are briefly illustrated in Figure 2. In a DSPSL, the electric field lines are mostly vertical as shown in the A-A′ plot. As the bottom ground becomes gradually wider, the electric field lines spilt over the bottom ground plane gradually disappear as the signal propagates along the sections from A-A′ to C-C′. Via holes are used to connect bottom ground to top ground plane of the CBCPW. The electric field lines of the CBCPW are illustrated in the C-C′ plot. Next, as the bottom ground aperture opens wider smoothly, the vertical electric field transforms into the horizontally oriented field as shown in D-D′. After the bottom ground aperture is opened wide enough, horizontal CPW electric field lines are formed as shown in E-E′.

Table 1: Summary of the transition dimensions (unit: mil).

w_p	w_t	w_{cpw}	w_g	g	s_1	l_{pt}	l_{ct}
24	17	75	140	5	5	100	35

The dimensions of the designed transition are summarized in Table 1.

3. Analysis of the Characteristic Impedance of the Transition

In this paper, analysis of characteristic impedance and effective dielectric constant of the proposed DSPSL-to-CPW transition is performed separately for two adjoining transitional structures: DSPSL-to-CBCPW transition (A-A′ to C-C′) and CBCPW-to-CPW transition (C-C′ to E-E′). Firstly, for the sections from A-A′ to C-C′, analytical expressions for characteristic impedances of the transitional structure can be obtained from [3, 12, 13]. The impedance of this transitional structure is obtained using the method of moving perfect electric wall (MPEW) as shown in Figure 3 [13]. By using the MPEW, the transitional structure is divided into two

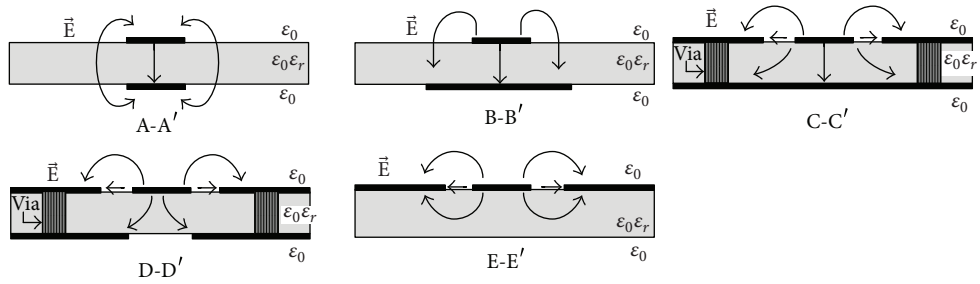

Figure 2: Electric field lines at each cross-section along the transition.

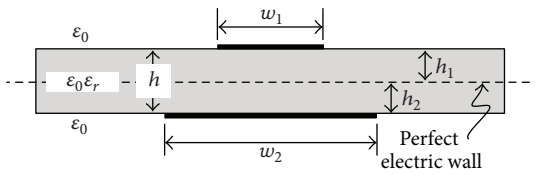

Figure 3: Transitional structure from A-A′ and C-C′.

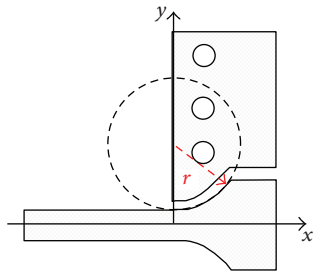

Figure 4: Top plane trace of the CBCPW-to-CPW transition (r = 39 mil).

conventional microstrip lines with infinite ground planes. The height of the divided substrate is obtained as

$$h_1 = \frac{h}{2} + \frac{h}{2}\frac{\left(w_2/w_1\right)^{w_2/h} - 1}{\left(w_2/w_1\right)^{w_2/h} + 1}. \quad (1)$$

Since $w_i > h_i$ (i = 1 and 2), the effective dielectric constant for each divided microstrip line can be obtained as

$$\varepsilon_{\text{eff}} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2\sqrt{1 + 12\left(h_i/w_i\right)}}, \quad i = 1 \text{ and } 2. \quad (2)$$

Also, the characteristic impedance for each divided microstrip line can be obtained as

$$Z_0 = 120\frac{\pi}{\sqrt{\varepsilon_{\text{eff}}}\left(\left(w_i/h_i\right) + 1.393 + 0.667\ln\left(\left(w_i/h_i\right) + 1.444\right)\right)}, \quad i = 1 \text{ and } 2. \quad (3)$$

Then, the total characteristic impedance of the transitional structure is obtained as the sum of the two divided microstrip lines. Initially, w_1 and w_2 of the 50 Ω DSPSL are 24 mils at A-A′, but the widths are varied along the transition. The conductor shape on the bottom plane is circularly tapered with the similar method suggested in [3]. The radius of the circular taper on the bottom plane is chosen as 100 mil (l_{pt}) in this design, and the conductor width on the top plane (w_1) is tapered to keep 50 Ω along the transition to obtain maximum bandwidth performance. In case of need, however, the DSPSL-to-CBCPW transition can also be designed to work as an impedance transformer.

Next, the CBCPW-to-CPW transition (sections from C-C′ to E-E′) is designed using the guideline in [7, 8]. Once the conductor trace of the transition on the top plane is determined by the taper in [14], the aperture gap on the bottom plane is adjusted to maintain the impedance at about 50 Ω. Figure 4 shows process of determining the top plane conductor trace. The diameter of the trace circle lies on the y-axis at the beginning of the transition, while the x-axis is at the center of the signal line of the CPW. The radius of the trace circle (r) is chosen as 39 mil in this design. However, the analytical method to obtain the characteristic impedance of the CPW transitional structure with a ground aperture on the bottom side of the substrate (D-D′ in Figure 2) has not yet been reported in the literature. Therefore, until now, EM simulations were solely used for the design of this transitional structure. In order to obtain the characteristic impedance and effective permittivity of the structure, the Schwarz-Christoffel conformal mapping method is applied.

The configuration of the CPW structure with a ground aperture on the bottom layer is shown in Figure 5(a). On the top side of the dielectric substrate (dielectric constant ε_r with thickness h), both sides of a center signal conductor (width w) are separated from two ground planes by gap width g. The following assumptions are used for this analysis.

(1) The ground planes are in infinite extent, and all conductors are perfectly conducting with zero thickness.

(2) The aperture is assumed to be symmetrical with respect to the center of the signal line.

(3) The RF signal along the structure propagates as a quasi-TEM mode.

(4) The dielectric boundaries, which can be considered as perfect magnetic walls, exist.

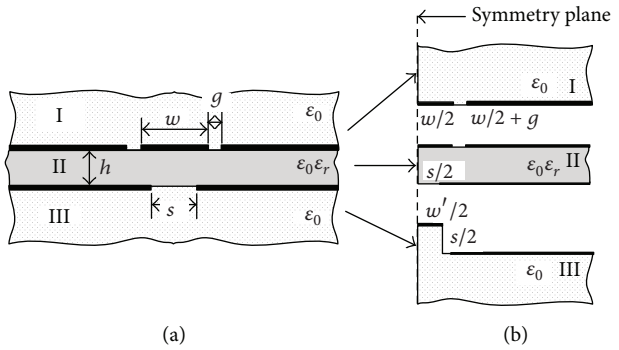

Figure 5: Configuration of the CPW transitional structure: (a) the whole structure and (b) divided structures for analysis.

In this analysis, the influence of the bottom ground aperture is carefully considered as the aperture width increases, since the field leakage from the aperture may not be negligible. For the analysis, the structure is divided into three regions as shown in Figure 5(b). For each region, the capacitance per unit length has been obtained using the mapping method. The total capacitance per unit length is the sum of capacitances for three regions.

An analytical expression for Region I of the CPW can be found in [6]. The capacitance is then calculated as

$$C_1 = 2\varepsilon_0 \frac{K(k_0)}{K\left(k_0^{'}\right)}, \tag{4}$$

where K is the complete elliptic integral of the first kind. The modulus k_0 and the complementary modulus $k_0^{'}$ are given by

$$k_0 = \frac{w}{w+2g}, \qquad k_0^{'} = \sqrt{1-k_0^{\,2}} \tag{5}$$

The accurate expression for the ratio $K(k)/K(k')$ has been reported in [15] as follows:

$$\frac{K(k)}{K\left(k^{'}\right)} = \frac{1}{\pi}\ln\left(2\frac{1+\sqrt{k}}{1-\sqrt{k}}\right), \quad 0.5 \le k^2 \le 1, \tag{6a}$$

$$\frac{K(k)}{K\left(k^{'}\right)} = \frac{\pi}{\ln\left(2\left(\left(1+\sqrt{k^{'}}\right)/\left(1-\sqrt{k^{'}}\right)\right)\right)}, \quad 0 \le k^2 \le 0.5, \tag{6b}$$

with $k^{'} = \sqrt{1-k^2}$.

Since Region II is also symmetric, only the right half region is considered in obtaining the capacitance as shown in Figure 6(a). The region is first converted into the t-plane as shown in Figure 6(b) using the following relation:

$$t = \cosh^2\left(\frac{\pi z}{2h}\right). \tag{7}$$

The corresponding points after transformation from z-plane are obtained by

$$t_a = \cosh^2\left(\frac{\pi w}{4h}\right),$$
$$t_b = \cosh^2\left(\frac{\pi(w/2+g)}{2h}\right), \tag{8}$$
$$t_e = \sinh^2\left(\frac{\pi s}{4h}\right).$$

The points on the t-plane transform through

$$w = \int_0^t \frac{dt}{\sqrt{(t+t_e)(t-1)(t-t_a)(t-t_b)}}. \tag{9}$$

By following integrals in [12], the capacitance per unit length, C_2, is then obtained as

$$C_2 = 2\varepsilon_0\varepsilon_r \frac{K(k_1)}{K\left(k_1^{'}\right)}, \tag{10}$$

where the moduli k_1 and $k_1^{'}$ are given by

$$k_1 = \sqrt{\frac{(t_a-1)(t_b+t_e)}{(t_b-1)(t_a+t_e)}}, \qquad k_1^{'} = \sqrt{1-k_1^{\,2}}. \tag{11}$$

The shape of Region III is carefully chosen to account for the effect of leakage field through the ground aperture on the bottom layer. The amount of leakage field flowing out of the ground aperture on the bottom layer will depend on the aperture width. In order to calculate the amount of capacitance caused by this leakage, the structure for Region III is modeled as Figure 7(a). The signal line width influencing leakage field is changed according to the aperture width (s) and substrate height (h). Points A and H are determined by line of flux departing from Points C and F, respectively [16]. The signal line width influencing leakage field is determined by the following relations:

$$\frac{w^{'}}{2} = \begin{cases} \dfrac{s}{2} - \dfrac{h}{\pi}, & \text{if } \dfrac{w}{2} > \dfrac{s}{2} - \dfrac{h}{\pi}, \\ \dfrac{w}{2}, & \text{elsewhere.} \end{cases} \tag{12}$$

Figure 7(a) illustrates the electric field lines that contribute to the capacitance in Region III, and the equivalent capacitance model (similar method presented in [17]) is shown in Figure 7(b). As shown in Figure 7, the total capacitance influencing Region III is divided into two parts of capacitances C_f and C_{f_cpw} for easy calculation. The capacitance C_f is the parallel plate capacitance between AH and BG as shown in Figure 7(a), and the capacitance is given by

$$C_f = \varepsilon_0 \frac{w^{'}}{h}. \tag{13}$$

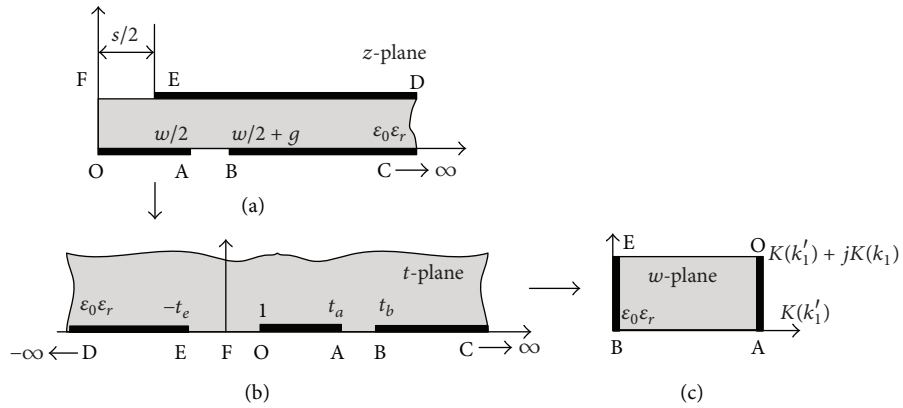

Figure 6: Conformal mapping transformation for Region II.

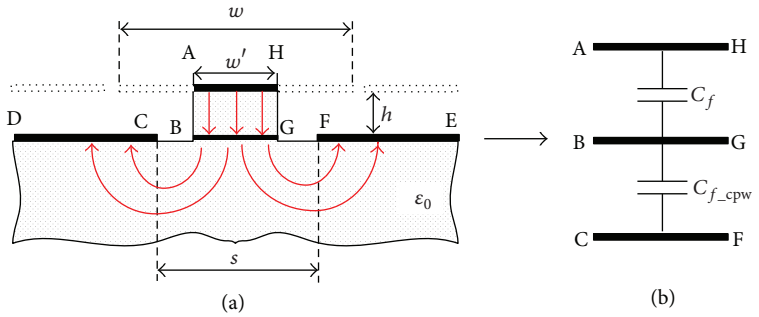

Figure 7: Model of Region III with consideration of leakage field: (a) field distributions and (b) equivalent circuit model.

Capacitance C_{f_cpw} is obtained with the same process applied to Region I. The capacitance is calculated as

$$C_{f\_cpw} = 2\varepsilon_0 \frac{K(k_2)}{K(k_2')}, \tag{14}$$

where k_2 and k_2' are the moduli

$$k_2 = \frac{w'}{s}, \qquad k_2' = \sqrt{1 - k_2^2}. \tag{15}$$

From (11) and (12), the final expression for the capacitance of Region III is obtained as

$$C_3 = \frac{C_f C_{f\_cpw}}{C_f + C_{f\_cpw}}. \tag{16}$$

The characteristic impedance and effective permittivity of the DSPSL-to-CPW transitional structure (C-C′ to D-D′) can be obtained as the sum of capacitance contributions of the three regions. The total capacitance is obtained as the sum of (4), (10), and (16). The characteristic impedance is then

$$Z_0 = \frac{1}{\sqrt{\varepsilon_{\text{eff}}}} \times \frac{60\pi}{\left[K(k_0)/K(k_0') + K(k_1)/K(k_1') + C_3/2\right]}. \tag{17}$$

The effective dielectric constant can be obtained as the ratio of the total capacitance to the calculated capacitance with air filling instead of the dielectric substrate

$$\varepsilon_{\text{eff}} = \frac{K(k_0)/K(k_0') + \varepsilon_r K(k_1)/K(k_1') + C_3/2}{K(k_0)/K(k_0') + K(k_1)/K(k_1') + C_3/2}. \tag{18}$$

Figures 8(a) and 8(b) compare the characteristic impedances obtained by the proposed analytical method with the commercial EM simulator (CST Microwave Studio) results. Figure 8(a) shows characteristic impedance variations with the signal width (w) for various dielectric constants. The impedance values via EM simulation are obtained at 8 GHz, but their deviations are within 0.3% up to 100 GHz. Also, the characteristic impedances are obtained with variation of the aperture width (s) for various dielectric constants in Figure 8(b). For both cases, the differences between the analytical expressions and EM simulation results are within 3.8% (average 1.8%).

With the proposed design process, the shape of the CBCPW-to-CPW transition can be easily obtained using the analytical expression of characteristic impedance, (17). Figure 9 shows computed characteristic impedances for various signal widths (w) as a function of the bottom aperture width (s). The shape of the bottom aperture can be determined by following the 50 Ω line as shown Figure 8: that is, from

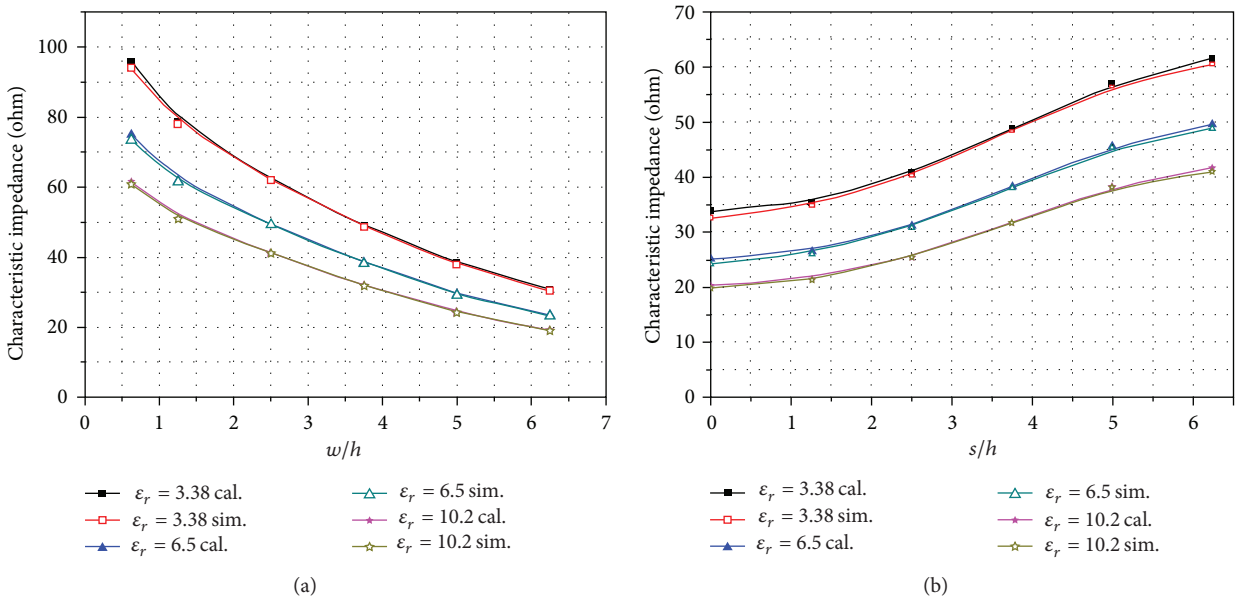

Figure 8: Characteristic impedance of the CBCPW-to-CPW transition (C-C′ to D-D′) as a function of w/h and s/h (cal.: calculated. Sim.: simulated). In case of (a), s = 30 mil, g = 5 mil, and h = 8 mil. In case of (b), w = 30 mil, g = 5 mil, and h = 8 mil.

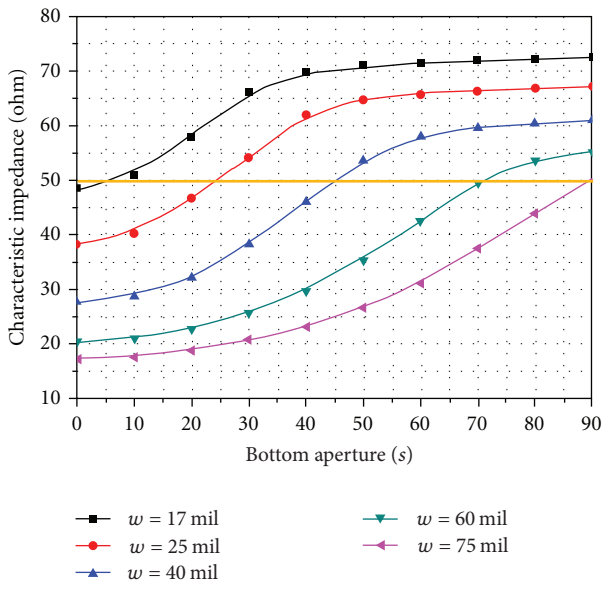

Figure 9: Characteristic impedances of the CBCPW-to-CPW transition (C-C′ to D-D′). The substrate is RT/Duroid 4003 with 8 mil thickness (dielectric constant: 3.38).

CBCPW (w = 17 mil, s = 0 mil) to CPW (w = 75 mil, s = 85 mil).

4. Simulation and Measurement

In order to demonstrate the performance of the proposed transition, a back-to-back configuration of the DSPSL-to-CPW transition was fabricated as shown in Figure 10. A microstrip- (MS-) to-DSPSL transition [3] was added at each side of the back-to-back DSPSL-to-CPW transition for ease of measurement as shown in Figures 10(a) and 10(b). With simulation, the MS-to-DSPSL transition has less than 0.15 dB insertion loss up to 15 GHz and 0.3 dB up to 30 GHz. The performance of the proposed transition was measured using the Anritsu network analyzer 37397C with the transition mounted in a universal test fixture as shown in Figure 10(c). The measurement setup is briefly illustrated in Figure 10(d).

The measured and simulated results of the return loss and insertion loss of the transition are compared in Figure 11. Similarly to the fabricated transition, the simulation configuration includes the additional MS-to-DSPSL transition at both sides of the back-to-back DSPSL-to-CPW transition. The discrepancies between the simulated and measured results are considered to be caused by fabrication inaccuracy, high loss tangent (loss tangent = 0.0027) of the substrate and interconnection mismatch of the test fixture. From the measurement, it is observed that the fabricated transition performs less than 0.6 dB insertion loss per transition for frequencies from 40 MHz to 12 GHz, as well as less than 1.2 dB insertion loss to 27 GHz. If the estimated losses due to additional MS-to-DSPSL transitions and universal test fixture are to be accounted from the measured values, the insertion loss for the single DSPSL-to-CPW transition is estimated less than 0.9 dB up to 27 GHz.

Table 2 compares the performance of the proposed transition with the previously published results. Overall performance of the proposed transition well exceeds performances of the previous transitions in terms of operating bandwidth and insertion loss. Due to the clear design guidelines including impedance analysis along the whole sections of the transitional structure, the proposed transition design was implemented with good performance.

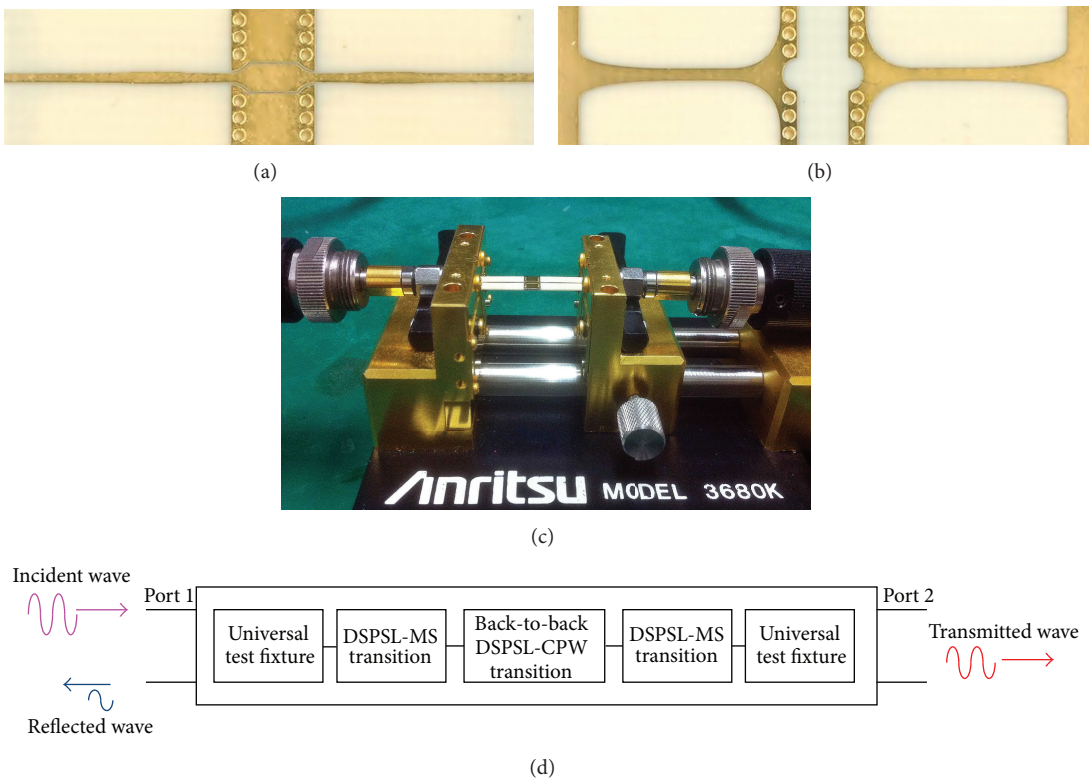

Figure 10: Picture of the fabricated ultra-wideband DSPSL-to-CPW transition in a back-to-back configuration including DSPSL-to-microstrip transitions for ease of measurement: (a) top view, (b) bottom view, (c) measurement using universal test fixture, and (d) measurement setup.

Table 2: Performance summary of DSPSL-to-CPW transitions.

	Bandwidth (GHz)	Insertion loss	Return loss	Dielectric constant of the substrate
[9]	1.1 ~ 6.45	<1.8 dB	>10 dB	9.6
[10]	1.3 ~ 9	<1.4 dB	>10 dB	6.15
[11]	0.5 ~ 14	<1 dB (Some resonant points exist)	>10 dB (Some resonant points exist)	3.38
This work	0.04 ~ 27	<1.2 dB	>10 dB	3.38

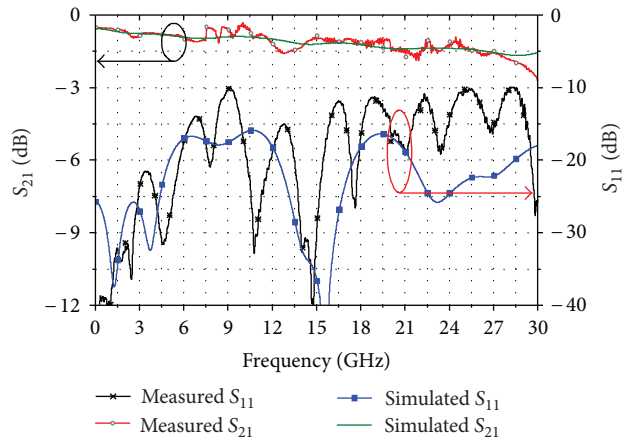

Figure 11: Simulated and measured insertion loss and return loss of the transition.

5. Conclusion

A design method of a novel ultra-wideband DSPSL-to-CPW transition based on analytical expressions of characteristic impedance is presented. In addition to reported analytical expressions of characteristic impedance for some sections of the transitional structure, conformal mapping is used to accurately obtain new analytical expressions of characteristic impedances for the CBCPW-to-CPW transitional structure. Therefore, in this paper, an efficient and clear guideline for the transition design is established. The implemented transition using the proposed design process has demonstrated to possess ultra-wideband performance excelling the previous reported results due to good impedance matching, smooth field transformation, and ground continuity. The transition design approach proposed in this paper is expected to find multitude of applications to circuits requiring balanced lines and CPW structures.

Acknowledgments

This research was supported by the National R&D Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2012034753).

References

[1] Q. Xue, "Double side parallel strip line and its applications," in *Proceedings of the IEEE MTT-S International Microwave Workshop Series on Art of Miniaturizing RF and Microwave Passive Components (IMWS '08)*, pp. 55–58, December 2008.

[2] K. C. Gupta, R. Garg, I. Bahl, and P. Bhartia, *Microstrip Lines and Slotlines*, Artech House, Norwood, Mass, USA, 1996.

[3] S. G. Kim and K. Chang, "Ultrawide-band transitions and new microwave components using double-sided parallel-strip lines," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 9, pp. 2148–2152, 2004.

[4] G. Q. Liu, L. S. Wu, and W. Y. Yin, "Miniaturised dual-band rat-race coupler based on double-sided parallel stripline," *Electronics Letters*, vol. 47, no. 14, pp. 800–802, 2011.

[5] D. S. Woo, Y. G. Kim, Y. K. Cho, and K. W. Kim, "Ultra-wideband Fermi antenna using microstrip-to-CPS balun," *IEICE Transactions on Communications*, vol. E93-B, no. 8, pp. 2219–2222, 2010.

[6] R. N. Simons, *Coplanar Waveguide Circuits, Components and Systems*, Wiley, New York, NY, USA, 2001.

[7] Y. G. Kim, W. Kim, and Y. K. Cho, "An ultra-wideband microstrip-to-CPW transition," in *Proceedings of the IEEE Microwave Theory and Techniques Society International Microwave Symposium Digest*, pp. 1079–1082, June 2008.

[8] Y. G. Kim, K. W. Kim, and Y. K. Cho, "A planar ultra-wideband balanced doubler," in *Proceedings of the IEEE Microwave Theory and Techniques Society International Microwave Symposium Digest*, pp. 1243–1246, 2008.

[9] J. X. Chen, J. L. Li, and Q. Xue, "Novel via-less double-sided parallel strip line to coplanar waveguide transition," *Microwave and Optical Technology Letters*, vol. 48, pp. 1717–1718, 2007.

[10] X. Y. Zhang, J. X. Chen, and Q. Xue, "Broadband transition between double-sided parallel-strip line and coplanar waveguide," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 2, pp. 103–105, 2007.

[11] D. H. Kwon and Y. Kim, "A wideband vertical transition between co-planar waveguide and parallel-strip transmission line," *IEEE Microwave and Wireless Components Letters*, vol. 15, no. 9, pp. 591–593, 2005.

[12] P. L. Carro and J. De Mingo, "Analysis and synthesis of double-sided parallel-strip transitions," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 2, pp. 372–380, 2010.

[13] J. Svacina, "New method for analysis of microstrip with finite-width ground plane," *Microwave and Optical Technology Letters*, vol. 48, no. 2, pp. 396–399, 2006.

[14] A. Beyer and I. Wolff, "Finline taper design made easy," *IEEE Microwave Theory and Techniques Society International Microwave Symposium Digest*, vol. 22, no. 3, pp. 144–147, 1976.

[15] W. Hilberg, "From approximations to exact relations for characteristic impedance," *IEEE Transactions on Microwave Theory and Techniques*, vol. 17, no. 5, pp. 259–265, 1969.

[16] N. Pesonen, W. K. Kahn, R. A. Allen, M. W. Cresswell, and M. E. Zaghloul, "Application of conformal mapping approximation techniques: Parallel conductors of finite dimensions," *IEEE Transactions on Instrumentation and Measurement*, vol. 53, no. 3, pp. 812–821, 2004.

[17] A. Bandsal, B. C. Paul, and K. Roy, "An analytical fringe capacitance model for interconnects using conformal mapping," *IEEE Transactions on Microwave Theory and Techniques*, vol. 25, no. 12, pp. 2765–2774, 2006.