Research Article

Realization of New Electronically Controllable Grounded and Floating Simulated Inductance Circuits Using Voltage Differencing Differential Input Buffered Amplifiers

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A new active circuit is proposed for the realisation of lossless grounded and floating inductance employing Voltage Differencing Differential Input Buffered Amplifiers (VD-DIBAs). The proposed grounded simulated inductance circuit employs two VD-DIBAs and a single-grounded capacitor whereas the floating simulated inductance circuit employs three VD-DIBAs and a grounded capacitor. The circuit for grounded inductance does not require any realization conditions whereas in case of floating inductance, only equality of two transconductances is needed. Some sample results demonstrating the applications of the new simulated inductors using VD-DIBAs have been given to confirm the workability of the new circuits.

1. Introduction

Several synthetic grounded and floating inductance circuits using different active elements such as operational amplifiers (op-amps) [1–5], current conveyors (CCs) [6–13], current controlled conveyors (CCCIIs) [14, 15], current feedback operational amplifiers (CFOAs) [16], operational mirrored amplifiers (OMAs) [17], differential voltage current conveyors (DVCCIIs) [18], current differencing buffered amplifiers (CDBAs) [19–21], current differencing transconductance amplifiers (CDTAs) [22, 23], and operational transconductance amplifier (OTA) [24] are reported in the literature. Recently, various active building blocks have been introduced in [25], VD-DIBA is one of them. Although some applications of VD-DIBAs have been reported in the literature such as in the realization of all pass section [26], to the best knowledge and belief of the authors, no grounded/ floating inductance simulation circuits using VD-DIBAs have yet been reported in the open literature so far. The purpose of this paper is, therefore, to propose new VD-DIBA-based lossless grounded and floating inductance simulation circuits.

2. The Proposed New Configurations

The schematic symbol and equivalent model of the VD-DIBA are shown in Figures 1(a) and 1(b) [26]. The model includes two controlled sources: the current source controlled by differential voltage $(V_+ \text{-} V_-)$, with the transconductance g_m, and the voltage source controlled by differential voltage $(V_z \text{-} V_v)$, with the unity voltage gain. The VD-DIBA can be described by the following set of equations:

$$\begin{pmatrix} I_{v+} \\ I_{v-} \\ I_z \\ I_v \\ V_w \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 \end{pmatrix} \begin{pmatrix} V_{v+} \\ V_{v-} \\ V_z \\ V_v \\ I_w \end{pmatrix}. \quad (1)$$

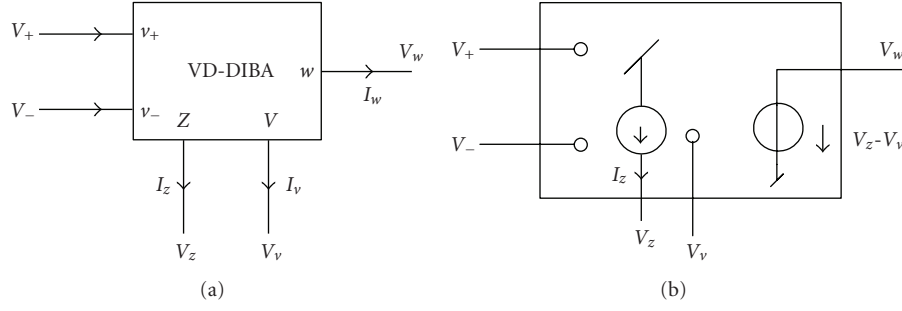The proposed configurations are shown in Figures 2 and 3, respectively.

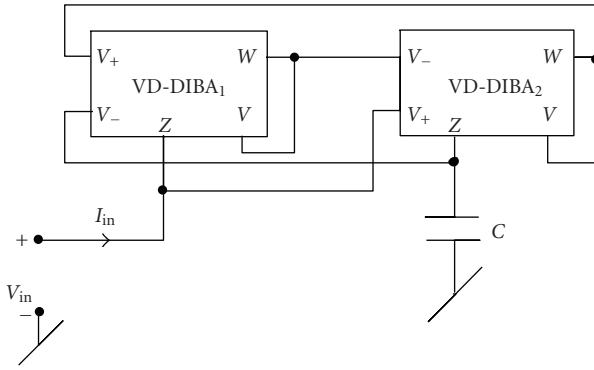Figure 1: (a) Schematic symbol and (b) equivalent model of VD-DIBA [26].

Figure 2: Proposed grounded inductance simulation configuration.

A routine analysis of the circuit shown in Figure 2 results in the following expression for the input impedance

$$Z_{in}(s) = s\left(\frac{4C}{g_{m_1}g_{m_2}}\right). \tag{2}$$

The circuit, thus, simulates a grounded inductance with resulting value given by

$$L_{eq} = \frac{4C}{g_{m_1}g_{m_2}}. \tag{3}$$

On the other hand, an analysis of the circuit shown in Figure 3 yields

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{g_{m_1}g_{m_2}}{4sC}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \quad \text{with } g_{m_1} = g_{m_3} \tag{4}$$

which proves that the circuit simulates a floating lossless inductance with resulting inductance value given by

$$L_{eq} = \frac{4C}{g_{m_1}g_{m_2}}. \tag{5}$$

Note that ensuring $g_{m_1} = g_{m_3}$ requires only the equality of the two DC bias currents of the VD-DIBAs which can be easily implemented in practice

3. Nonideal Analysis and Sensitivity Performance

Let R_z and C_z denote the parasitic resistance and parasitic capacitance of the Z terminal. Taking into account the nonidealities of the VD-DIBA, namely, $V_w = (\beta^+ V_z - \beta^- V_v)$, where $\beta^+ = 1 - \varepsilon_1$ ($\varepsilon_1 \ll 1$) and $\beta^- = 1 - \varepsilon_2$ ($\varepsilon_2 \ll 1$) are voltage tracking errors of the VD-DIBA.

For the circuit shown in Figure 2, the input impedance will become

$$Z_{in}(s) = \frac{4\{s(C + C_z) + 1/R_z\}}{4\{s^2C_z^2 + 1/R_z^2 + 2sC_z/R_z + s^2CC_z + sC/R_z\} + g_{m_1}g_{m_2}(2 - \beta_1^+)(2 - \beta_2^+)}. \tag{6}$$

The non-ideal equivalent circuit of the grounded inductor is shown in Figure 4

$$L = \frac{4(C + C_z)}{\left(4/R_z^2 + (2 - \beta_1^+)(2 - \beta_2^+)g_{m_1}g_{m_2}\right)},$$
$$C' = C_z,$$
$$R' = \frac{(C + C_z)R_z}{(C + 2C_z)},$$
$$D = C_z(C + C_z)R_z,$$

$$C'' = (C + 2C_z),$$
$$R'' = \frac{4R_z}{\left(4 + R_z^2(2 - \beta_1^+)(2 - \beta_2^+)g_{m_1}g_{m_2}\right)}. \tag{7}$$

The sensitivities of L with respect to active and passive elements are

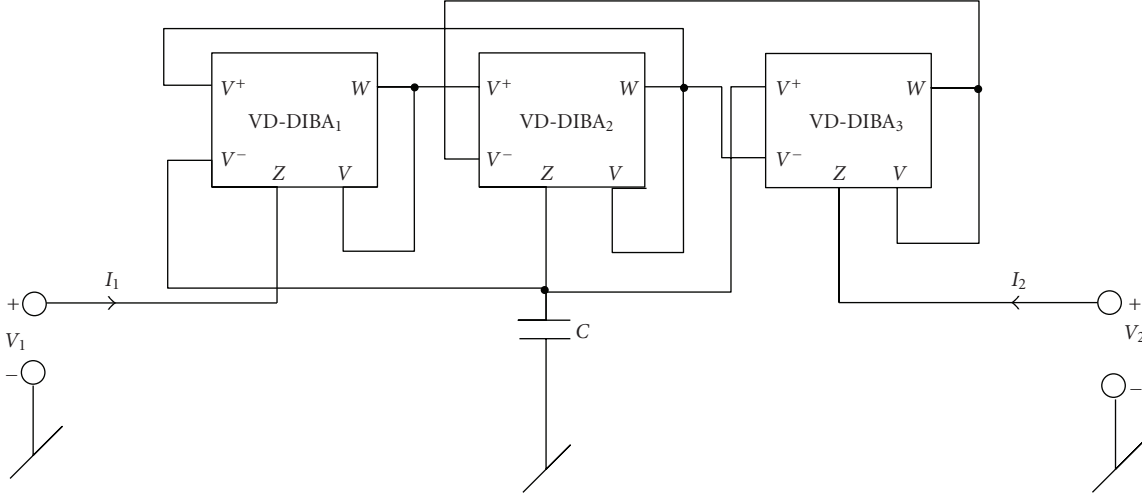$$S_C^L = \frac{C}{(C + C_z)}, \quad S_{C_z}^L = \frac{C_z}{(C + C_z)},$$

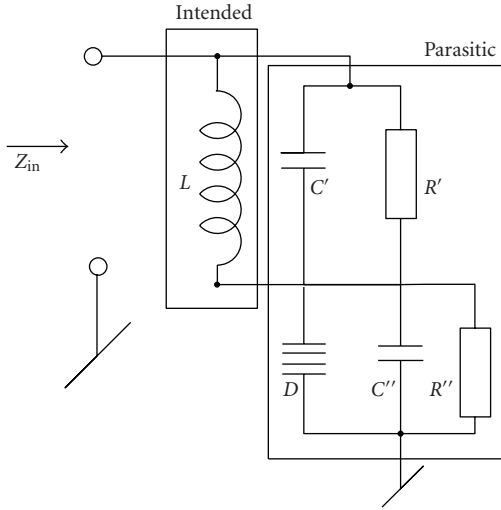FIGURE 3: Proposed floating inductance simulation configuration.

FIGURE 4: Non-ideal equivalent circuit of grounded inductor of Figure 2.
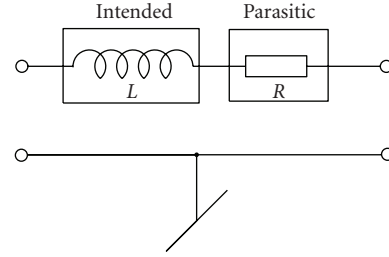

FIGURE 5: Non-ideal equivalent circuit of floating inductor of Figure 3.

For the circuit shown in Figure 3 the input-output currents and voltages relationship is given by:

$$
\begin{bmatrix} I_1 \\ I_2 \end{bmatrix}
= X \begin{bmatrix} \dfrac{sC_zR_z+1}{XR_z}+1 & -1 \\ -1 & \dfrac{sC_zR_z+1}{XR_z}+1 \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \tag{9}
$$

with $\beta_1 = \beta_3$,

$$X = g_{m_1}g_{m_2}R_z\beta_1^+(2-\beta_2^+)/4(s(C+C_z)R_z+1).$$

The non-ideal equivalent circuit of floating inductor is shown in Figure 5:

$$
S_{R_z}^L = \frac{2}{\left(4+(2-\beta_1^+)(2-\beta_2^+)R_z^2 g_{m_1}g_{m_2}\right)},
$$

$$
S_{\beta_1^+}^L = \frac{\beta_1^+(2-\beta_2^+)g_{m_1}g_{m_2}}{\left(4/R_z^2+(2-\beta_1^+)(2-\beta_2^+)g_{m_1}g_{m_2}\right)},
$$

$$
S_{\beta_2^+}^L = \frac{\beta_2^+(2-\beta_2^+)g_{m_1}g_{m_2}}{\left(4/R_z^2+(2-\beta_1^+)(2-\beta_2^+)g_{m_1}g_{m_2}\right)},
$$

$$
S_{g_{m_1},g_{m_2}}^L = -\frac{(2-\beta_1^+)(2-\beta_2^+)g_{m_1}g_{m_2}}{\left(\dfrac{4}{R_z^2}+(2-\beta_1^+)(2-\beta_2^+)g_{m_1}g_{m_2}\right)}. \tag{8}
$$

$$
L = \frac{4(C+C_z)}{\beta_1^+(2-\beta_2^+)g_{m_1}g_{m_2}},
$$

$$
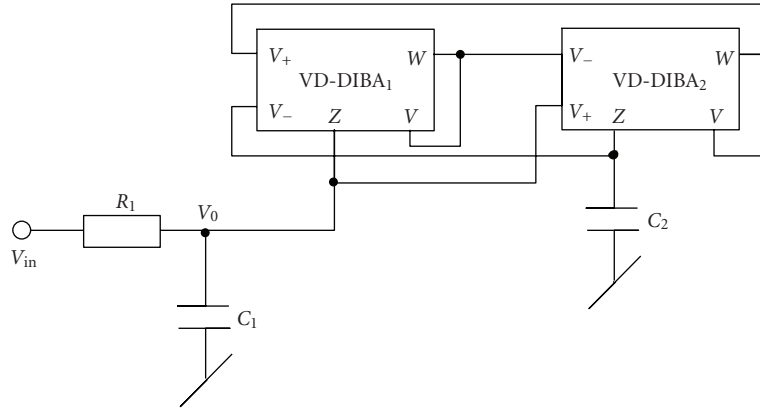R = \frac{4}{\beta_1^+(2-\beta_2^+)g_{m_1}g_{m_2}R_z}. \tag{10}
$$

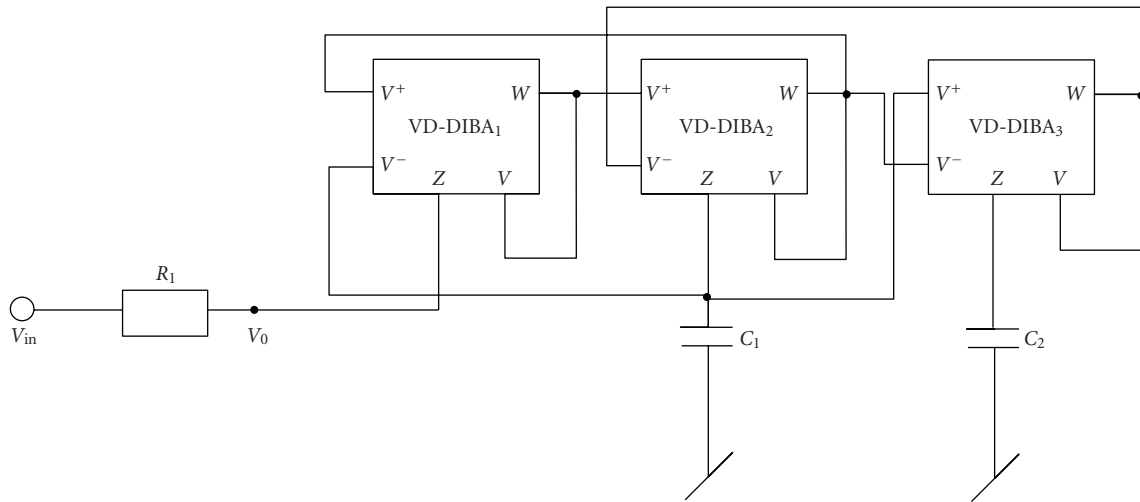FIGURE 6: BPF realized by the new grounded simulated inductor.

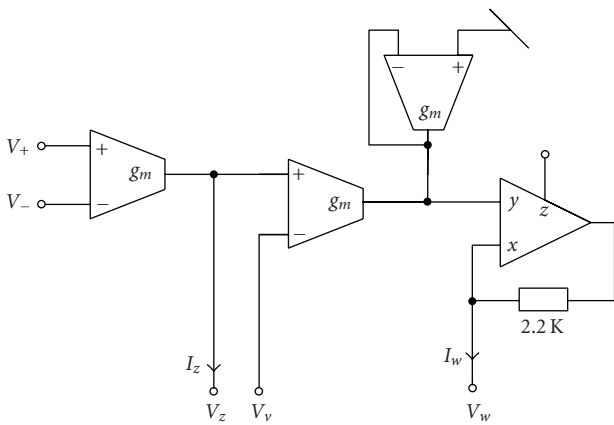FIGURE 7: BRF realized by the new floating simulated inductor.

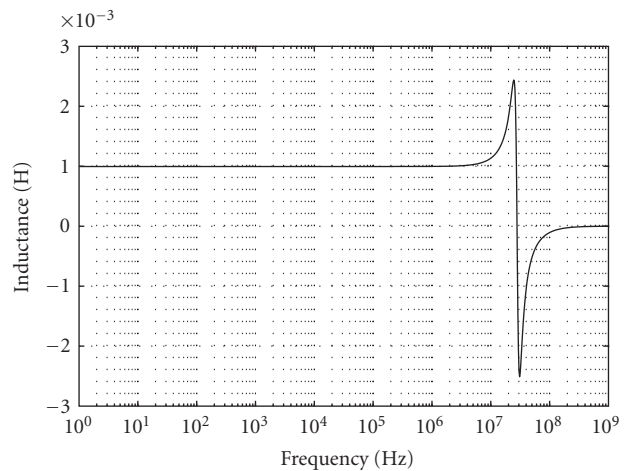FIGURE 8: A possible implementation of VD-DIBA.

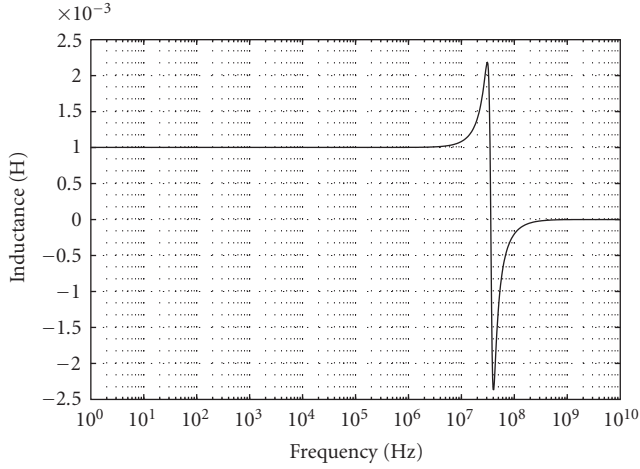FIGURE 9: Frequency response of simulated grounded inductor.

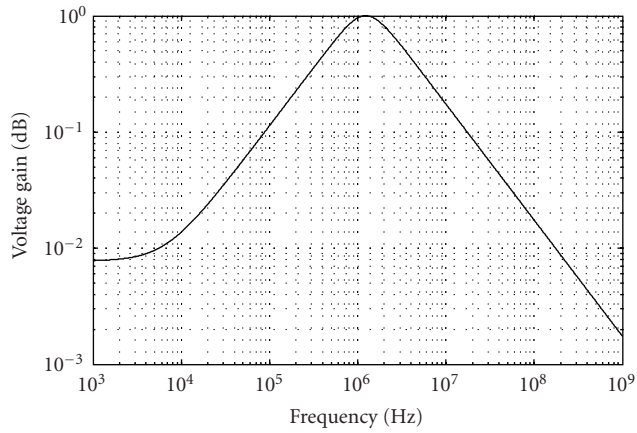FIGURE 10: Frequency response of simulated floating inductor.

FIGURE 11: Frequency response of BPF using simulated grounded inductor.
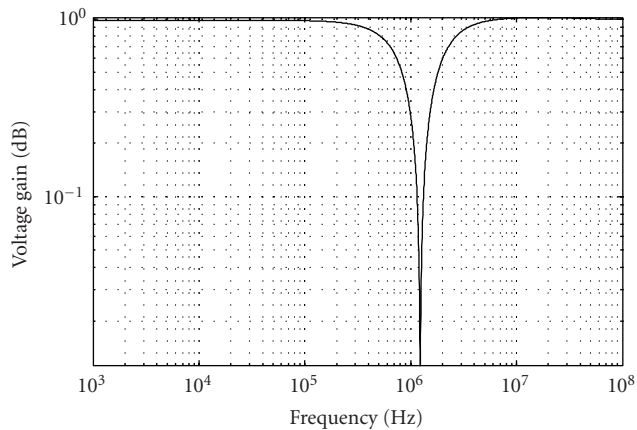
FIGURE 12: Frequency response of BRF using simulated floating inductor.
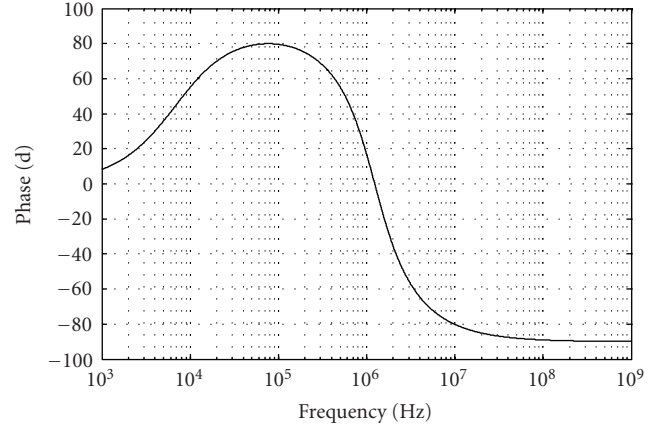
FIGURE 13: Phase response of BPF using simulated grounded inductor.
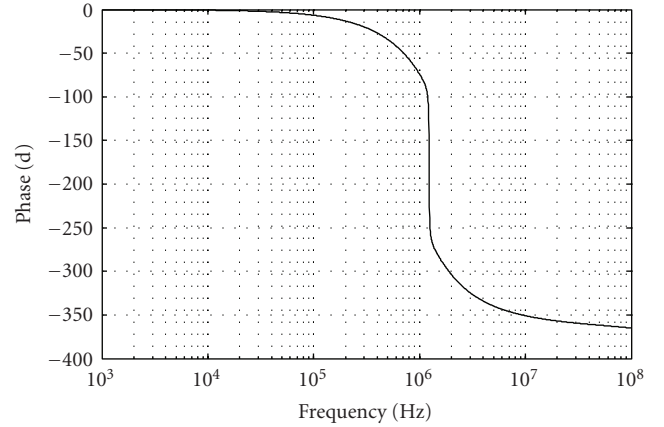
FIGURE 14: Phase response of BRF using simulated floating inductor.

The sensitivities of L with respect to active and passive elements are

$$
\begin{aligned}
S_C^L &= \frac{C}{(C + C_z)}, \\
S_{C_z}^L &= \frac{C_z}{(C + C_z)}, \\
S_{\beta_1^+}^L &= -1, S_{g_{m_1} g_{m_2}}^L \\
&= -1, S_{\beta_2^+}^L = \frac{\beta_2^+}{(2 - \beta_2^+)}.
\end{aligned}
\tag{11}
$$

Assuming $g_{m_1} = g_{m_2} = 258.091$ uA/V, $C_z = 0$, $R_z = \infty$, $C = 16.65$ pF, and $\beta_1^+ = \beta_2^+ = 1$. These sensitivities are found to be $(1, 0, 0, 1, 1, -1)$ and $(1, 0, -1, -1, 1)$ for (8) and (11), respectively. Thus, all the passive and active sensitivities of both the proposed circuits are low.

FIGURE 15: Step response of Figure 6.

FIGURE 16: Simulated spectrum of the output signal Vo in Figure 6.

4. Verification of the Workability of the New Proposed Grounded/Floating Inductance Configurations

The workability of the proposed simulated inductors has been verified by realizing a band pass filter (BPF) and band reject filter (BRF), respectively.

Figure 6 shows the schematics for the realization of a BPF, using the new simulated grounded inductor.

The transfer function realized by this configuration is given by

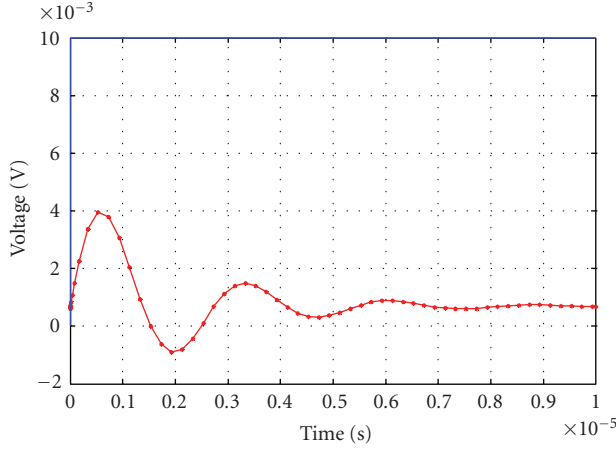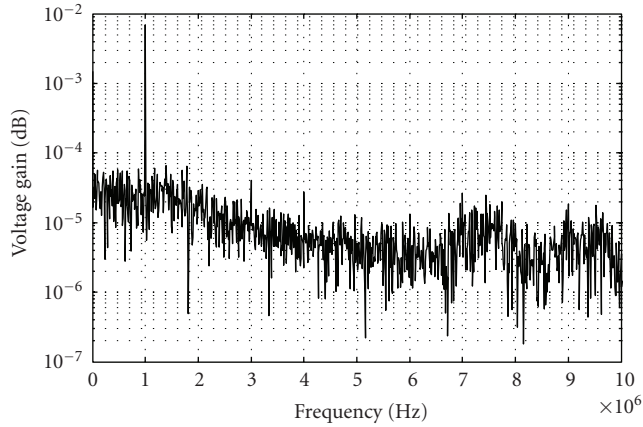$$\frac{V_0}{V_{\text{in}}} = \frac{s(1/R_1 C_1)}{s^2 + s(1/R_1 C_1) + (g_{m_1} g_{m_2}/4 C_1 C_2)}. \tag{12}$$

Figure 7 shows the schematics for the realization of a BRF, using the proposed floating inductor circuit.

The transfer function realized by this configuration is given by

$$\frac{V_0}{V_{\text{in}}} = \frac{\left(s^2 + g_{m_1} g_{m_2}/4 C_1\right)}{s^2 + s\left(R_1 g_{m_1} g_{m_2}/4 C_1\right) + g_{m_1} g_{m_2}/4 C_1 C_2}. \tag{13}$$
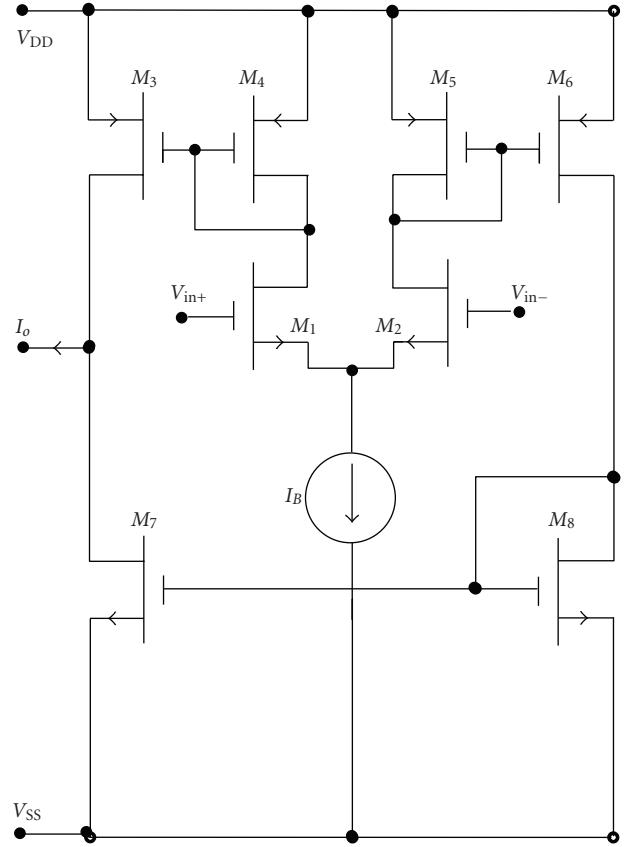

FIGURE 17: CMOS implementation of OTA.

The performance of the new simulated inductors was evaluated by PSPICE simulations. Since VD-DIBA is not a commercially available IC, a possible implementation of VD-DIBA using commercially available devices is shown in Figure 8. A CMOS-based OTA as shown in Figure 17 and CFOA SPICE macromodel of AD844 to realise VD-DIBAs as per the schematic of Figure 8 were used to determine the frequency response of the grounded and floating simulated inductors. The following values were used for grounded inductor $C = 16.65\,\text{pF}$, $g_{m_1} = g_{m_2} = 258.091\,\text{uA/V}$, for floating inductor $C = 16.65\,\text{pF}$, $g_{m_1} = g_{m_3} = 258.091\,\text{uA/V}$. From the frequency response of the simulated grounded inductor (Figure 9) it has been observed that the inductance value remains constant up to 1 MHz. From the frequency response of the simulated floating inductor (Figure 10) it has been observed that the inductance value remains constant up to 1 MHz.

To verify the theoretical analysis, the application circuits shown in Figures 6 and 7 have been simulated using CMOS-based OTA as shown in Figure 17 and CFOA SPICE macromodel of AD844 to realise VD-DIBAs as per the schematic of Figure 8. The component values used were for Figure 6, $C_1 = 16.65\,\text{pF}$, $C_2 = 16.65\,\text{pF}$, $R_1 = 5.479\,\text{k}\Omega$, and for Figure 7, $C_1 = 16.65\,\text{pF}$, $C_2 = 16.65\,\text{pF}$ and $R_1 = 10.959\,\text{k}\Omega$, the VD-DIBA was biased with ± 1 volts D.C. power supplies with $I_{B1} = I_{B2} = I_{B3} = 32\,\mu\text{A}$. I_{B1}, I_{B2}, and I_{B3} are the biasing currents for transconductances.

Table 1

Parameters	VD-DIBA	OTA (CA 3080)	CMOS OTA (Figure 17)
Input voltage linear range	-120 mV to 120 mV	-25 mV to 25 mV	-109 mV to 109 mV
-3 dB Bandwidth	121 MHz	2 MHz	119 MHz
Power consumption	62.5 mW	30 mW	0.194 mW

Figures 11 and 12 show the simulated filter responses of the BP and BR filters, respectively. Figures 13 and 14 show the phase responses of BP and BR filters, respectively. Figure 15 shows the step response of the filter of Figure 6 which confirms the stability of the implemented filter. Figure 16 shows the simulated spectrum of the output signal Vo in Figure 6, where the total harmonic distortion (THD) is found to be 2.98%. The comparison of performance characteristics of VD-DIBA with OTA (CA3080) and CMOS OTA (as shown in Figure 17) has been given in Table 1. These results, thus, confirm the validity of the application of the proposed grounded/floating simulated inductance circuits.

5. Concluding Remarks

Among various modern active building blocks, VD-DIBA is emerging as quite flexible and versatile building block for analog circuit design. However, the use of VD-DIBA in the realization of grounded/ floating inductor had not been known earlier. This paper has filled this void by introducing new VD-DIBA- based grounded and floating inductor configurations. This paper, thus, has added a new application circuits to the existing repertoire of VD-DIBA-based application circuits. The workability of new propositions has been confirmed by SPICE simulations.

Acknowledgments

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