

Research Article

Compact Shorted Stacked-Patch Antenna Integrated with Chip-Package Based on LTCC Technology

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A low profile chip-package stacked-patch antenna is proposed by using low temperature cofired ceramic (LTCC) technology. The proposed antenna employs a stacked-patch to achieve two operating frequency bands and enhance the bandwidth. The height of the antenna is decreased to 4.09 mm (about $\lambda/25$ at 2.45 GHz) due to the shorted pin. The package is mounted on a $44 \times 44 \text{ mm}^2$ ground plane to miniaturize the volume of the system. The design parameters of the antenna and the effect of the antenna on chip-package cavity are carefully analyzed. The designed antenna operates at a center frequency of 2.45 GHz and its impedance bandwidth ($S_{11} < -10 \text{ dB}$) is 200 MHz, resulting from two neighboring resonant frequencies at 2.41 and 2.51 GHz, respectively. The average gain across the frequency band is about 5.28 dBi.

1. Introduction

Recent developments in microelectronic technology have created a probability for system-on-package (SOP) antennas [1–8] in a more compact size. As a result, low temperature cofired ceramic (LTCC) package technology [9, 10] is becoming more and more popular for the production of highly integrated, specifically complicated multilayer modules and antennas, both in the military and commercial sectors. At the same time, this technology is applicable to complex structures and an arbitrary number of layers for its flexibility. However, due to the high relative dielectric constant of LTCC materials, the size of antenna is decreased. Consequently, it also reduces the impedance bandwidth. The contradiction between the size reduction and bandwidth enhancement of the antenna for a practical wireless communication system is more difficult to deal with; therefore, this problem is more challengeable.

In order to reduce the antenna size while maintaining and even improving its bandwidth, some techniques have been proposed and reported by researchers for designing compact broadband antennas over the past several years, for example,

slotting ground plane or embedding narrow slits at the patch's nonradiation edges [11, 12], stacked shorted patches [13–15], and aperture-coupled stacked patch [16]. When slots are embedded in the ground plane or the aperture-coupled feed method is applied for exciting stacked-patch antennas for broadband operation, the backward radiation is increased compared with the traditional patch antenna. This increase in the back-radiation is contributed by the embedded slots in the ground plane and the decreased ground-plane size in wavelength. The backscattered component is detrimental to the chip in the package cavity; that is to say, the back-radiation strengthens electromagnetic coupling between the antenna system and the system on chip. In addition, stacked patch antennas can be used for LP or CP and dual-polarization. However, the total height is still high and not compact enough.

In this paper, a RF system-level package integration of a low temperature cofired ceramic (LTCC) antenna is investigated for a highly integrated 2.45 GHz wireless transceiver module. The paper is organized as follows. Section 2 describes the geometry and the principle of the antenna design and presents the simulation results. In Section 3, the parametric

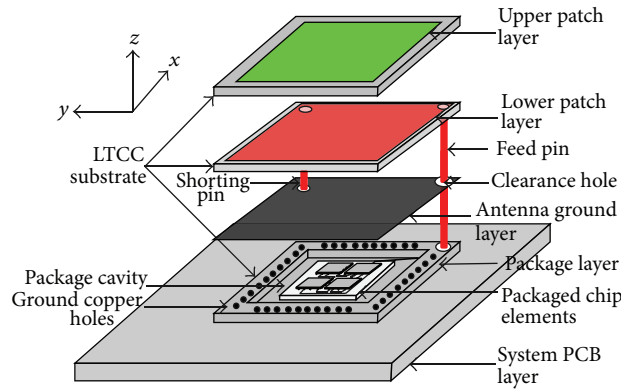


FIGURE 1: Expanded view of the proposed antenna integrated in package.

study of some key structural parameters and the effect of chip-package cavity are analyzed. Some design guidance and discussion are given. The paper is concluded in Section 4.

2. Antenna Structure and Operation Mechanism

As mentioned above, the RF system-level package integration on antenna is designed. The geometry of the considered LTCC multilayer antenna in this paper is depicted in Figure 1, where the shorted stacked-patch antenna is embedded on the top of a RF front-end module in LTCC multilayer package. For the sake of simplicity, we consider a probe-fed square patch antenna on a square grounded substrate with thickness $h_1 = 0.79$ mm. In order to miniaturize the antenna, the shorting technique (where the shorting position will be discussed in Section 3) is applied to the design scheme in this paper. A wide impedance bandwidth is achieved with the stacked patches. The upper and the lower layers are square patches, but it should be worth noting that the center of the lower patch is offset 2 mm from the coordinate center. The antenna ground plane is under the lower patch. Both the patches and the ground plane are made of copper. The package whose dimension is $10 \times 12 \times 0.96$ mm³ is between the antenna ground plane and the system PCB board. Just for fabrication convenience, all the LTCC substrates use the same material, with the relative dielectric constant $\epsilon_r = 7.8$ and a dielectric loss tangent $\delta = 0.0015$. In the procedure of fabrication, the manufacturing margin of the LTCC materials is 0.096 mm. The antenna ground plane and the system PCB board are directly connected with the metallic vias. The number of the vias and their radii will be discussed in Section 3. In order to reduce the size of patches and the height of the antenna, the probe is placed at the corner of the lower patch. The position of the shorting pin depends on the location of the feed. Good linear polarized radiation over a wide operating bandwidth can be achieved.

The dimensions of radiating patches are initially estimated by using simple microstrip patch antenna formulation [17]. The upper patch and the lower patch will interact with each other, which must be adjusted in width for

the proper impedance matching. The position of the shorting pin must be also modified appropriately for a wide impedance bandwidth and the desired polarization state. To meet the design requirement of the RF system-level package integrated antenna, the antenna thickness should be less than 5 mm without the superstrate thickness, while the antenna ground plane's size is assumed to be 44×44 mm². The sizes of the upper patch and the lower patch are determined to be 18×18 mm² and 20.5×20.5 mm², respectively. Due to the different sizes of the two patches and the mutual coupling between each other, these two patches resonate at different frequencies. The structure parameters influences on the performance of the antenna will be carefully considered and discussed in Section 3.

The detailed configuration of the proposed antenna integrated package topology as well as the design parameters of each layer is shown in Figure 2. It is shown that the total height of the antenna is 4.09 mm illustrated in Figure 2. The feed is connected into the lower patch though a clearance hole whose radius is larger than the feed pin's radius. Instead of microstrip line feed, the coaxial feed could be used to excite the lower patch and produce two operating modes. This is the reason why the impedance bandwidth is enhanced. For the comparison, the single layer patch antenna is designed. The substrate thickness of the single layer patch antenna is 12 mm and the size of the patch is 17.1×17.1 mm². The center frequency of the two antennas is at about 2.45 GHz and the simulated S_{11} is shown in Figure 3(a). Comparing the stacked-patch antenna and the single layer patch antenna shown in Figure 3(a), we can see that the height of the single patch antenna is much larger than that of the stacked patch antenna with the same impedance bandwidth. The results show that where the two neighboring resonant frequencies of the designed antenna are 2.41 GHz and 2.51 GHz, the contribution is from the lower and upper patches and the mutual coupling between them. The -10 dB absolute impedance bandwidth of S_{11} is 200 MHz from 2.35 GHz to 2.55 GHz. It is also known that the impedance matching characteristic at the low resonant frequency is better than that at the high one because the current distributing on lower patch is changed due to the shorting pin. For the present proposed structure, the antenna achieves two resonant frequencies. In this case,

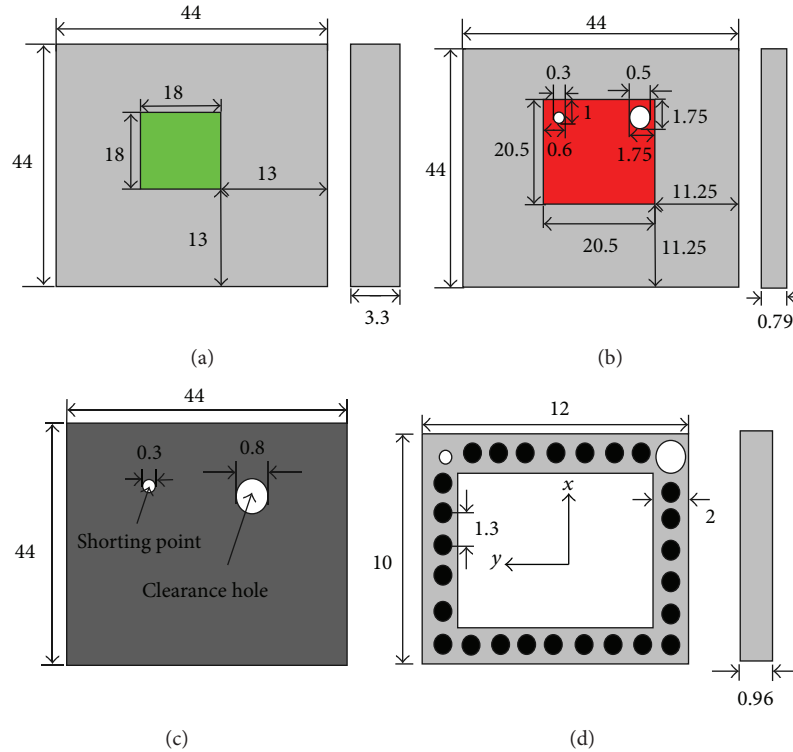


FIGURE 2: Design parameters of each layer, (a) upper patch layer, (b) lower patch layer, (c) antenna ground layer, and (d) package layer with complete grounded vias. The unit is in mm.

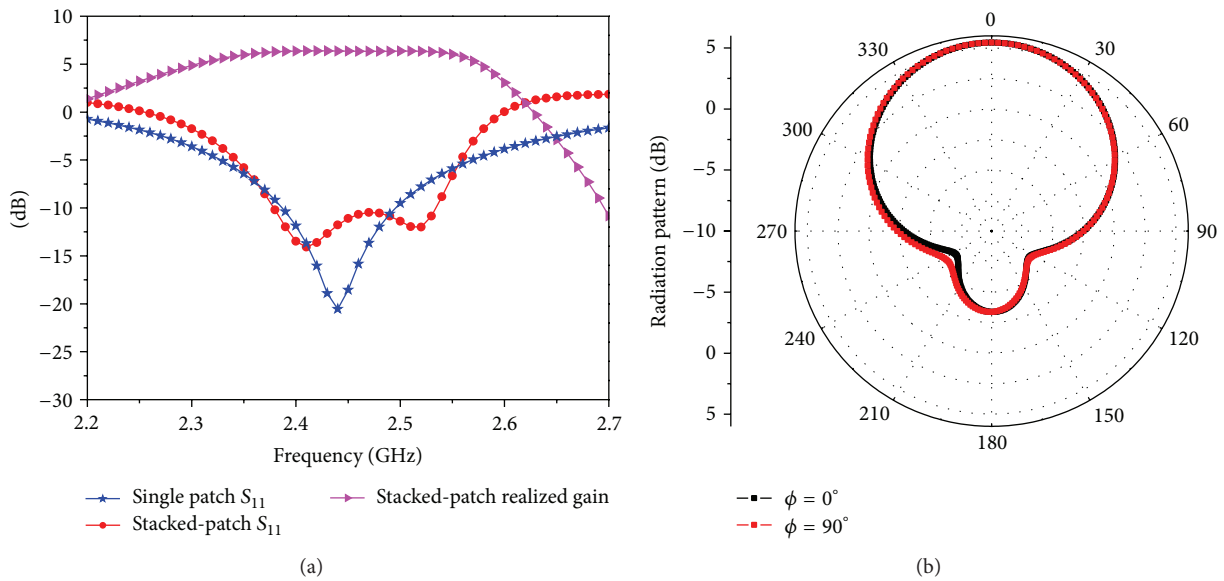


FIGURE 3: Simulated results of the proposed antenna. (a) S_{11} characteristics including single patch and stacked-patch antennas, stacked-patch antenna's realized gain in the broadside direction, and (b) radiation patterns at 2.45 GHz of stacked-patch antenna in $\phi = 0^\circ$ and $\phi = 90^\circ$ planes.

the impedance bandwidth is about 8.16% referenced to the center frequency at 2.45 GHz. Figure 3(a) shows that the gains across the whole frequency band are very flat. The maximum absolute gain at the boresight direction of the proposed antenna across the operating frequency band is

5.48 dB and the average gain is 5.28 dB within the operating frequency band. The broadside radiation patterns for the designed antenna are observed in Figure 3(b). The broadside patterns are symmetrical because of the modeling structure. The beamwidth within the required gain is greater than 100° .

3. Antenna and Package Parameters Analysis

Most 2.4 GHz commercial wireless communication systems currently deployed require more than 200 MHz of bandwidth. As described above, the stacked patch antenna topology on the packaged-chips is designed to achieve the desired impedance bandwidth owing to a relatively small volume. Considering the mutual coupling between the two patches, the proper sizes of the patches should be selected. The bandwidth and impedance matching of the antenna are influenced by various structure parameters. That is to say, the performance of the stacked patch antenna is mainly determined by the characteristics of the configuration of the patches including dimensions and heights and the positions of the feeding-pin and the shorting-pin. The ground plane is on the top of the package cavity layer while the printed circuit and some chips can be integrated into the package cavity. With the mutual coupling accounting for between the antenna and the system on chip, the ground plane and the system PCB board are connected with the copper vias. The number and positions of the grounded vias have an influence on the modules in the cavity, especially on the electromagnetic (EM) fields' mutual coupling. In this section, the effects of these parameters on the antenna performance and the package cavity are studied in detail. To better understand the effects of parameters on the performance of the proposed antenna and of the EM mutual coupling between the ground plane and chips in package cavity, only one parameter will be varied at one time, while the others are kept unchanged unless especially indicated.

3.1. Antenna Parameters Analysis. To study structure parameters effects on the antenna performance, parametric study is carried out on the parameters mentioned above, using the full-wave simulator Ansys HFSS [18].

Firstly, the effects of the dimensions of the two patches on the antenna performance are discussed. Figure 4(a) shows the comparison of S_{11} in different dimensions of the lower patches. It can be seen that the fundamental mode disappears and the impedance bandwidth is decreased as the size of the lower patch increases. For increasing the upper patch L_1 shown in Figure 4(b), it is seen that the fundamental resonant frequency is quickly shifted down, at the same time, the high mode vanishes. Thus, we can see from Figures 4(a) and 4(b) that the upper patch should be also increased when the lower patch increases for a good impedance matching in the frequency band of interest.

The thickness of the LTCC substrate under the lower patch of the antenna, h_1 , is then considered. Generally speaking, the thicker the substrate is, the wider the impedance bandwidth is. It is well understood that the inductance of the feeding-pin becomes larger and the impedance matching becomes better as the height of the feeding-pin increases. With such a large length, the effect of the inductive reactance of the probe pin in the LTCC substrate on the impedance matching is large and makes the antenna match well in the operating frequency band of interest. Figure 4(c) gives the effect of substrate thickness under the lower patch on S_{11} of the proposed antenna. What Figure 4(c) shows is just as

described above. In addition, the interaction between the driven and parasitic patches has a profound impact on the bandwidth of the antenna.

Secondly, the dependency of S_{11} on the separation of the lower and upper patches, h_2 , is shown in Figure 4(d). The separation of the lower and upper patches, h_2 , has a heavy influence on the antenna performance. The smaller or larger separation strengthens or weakens the coupling of the two patches, which results in a relatively narrow impedance bandwidth. Thus, a proper height should be selected to obtain a wide bandwidth. Simultaneously, the thinner substrate is also necessary to miniaturize the antenna's size. Figure 4(d) shows the effect of varying the height of the parasitic patch across the bandwidth of the antenna. The EM coupling between the driven and parasitic patches strengthens as the thickness h_2 increases. In order to enhance the gain and bandwidth of the antenna, a thin superstrate, which has a thin thickness of h_3 , is introduced to cover the upper patch. One of its advantages is that the abrasion of the antenna can be avoided by the superstrate. Another advantage is that the size of the antenna is miniaturized due to reducing the effect of the discontinuity of the antenna structure. The simulated S_{11} responses with different thickness of the superstrate layer are calculated and the results are illustrated in Figure 4(e). The characteristics of S_{11} with different thickness of the superstrate are similar to that reported S_{11} results which are obtained with different substrate thicknesses between the lower and upper patches.

3.2. Package Parameters Analysis. In the description above, the parametric studies of the proposed antenna have been performed. When the antenna is integrated into the chip-package, the effects of the grounded holes on the chips in the package cavity have to be also considered. The antenna performance is simulated in HFSS software and the simulated responses of the proposed antenna including S_{11} , the realized gains, and radiation patterns are shown in Figure 5 in the two cases: with and without the package layer. S_{11} of the two cases are compared in Figure 5(a). The impedance matching characteristic at the high resonant frequency is better than the low one because the current distributing on ground plane is changed due to the grounded holes when the package is embedded into the integrated-antenna. Figure 5(b) shows that the realized gain across the frequency band of interest is nearly unchanged. In other words, the gain versus the frequency of interest is very stable with the two cases. The broadside radiation patterns are observed in Figure 5(c). The broadside patterns are also symmetrical because of the symmetrical modeling structure. The beamwidth is stable for the two cases. It can be seen that the change of S_{11} is sensitive to the two cases, but the other parameters of the antenna do not. Thus, S_{11} will be paid more attention to during being analyzed in the following.

The effects of the number of the grounded vias on antenna and chips are sketched in Figure 6(a), where the complete wall means that there are metallic vias in four walls of the package cavity, but the partial wall means that there is lack of some vias around (close to) the feeding-pin. The results

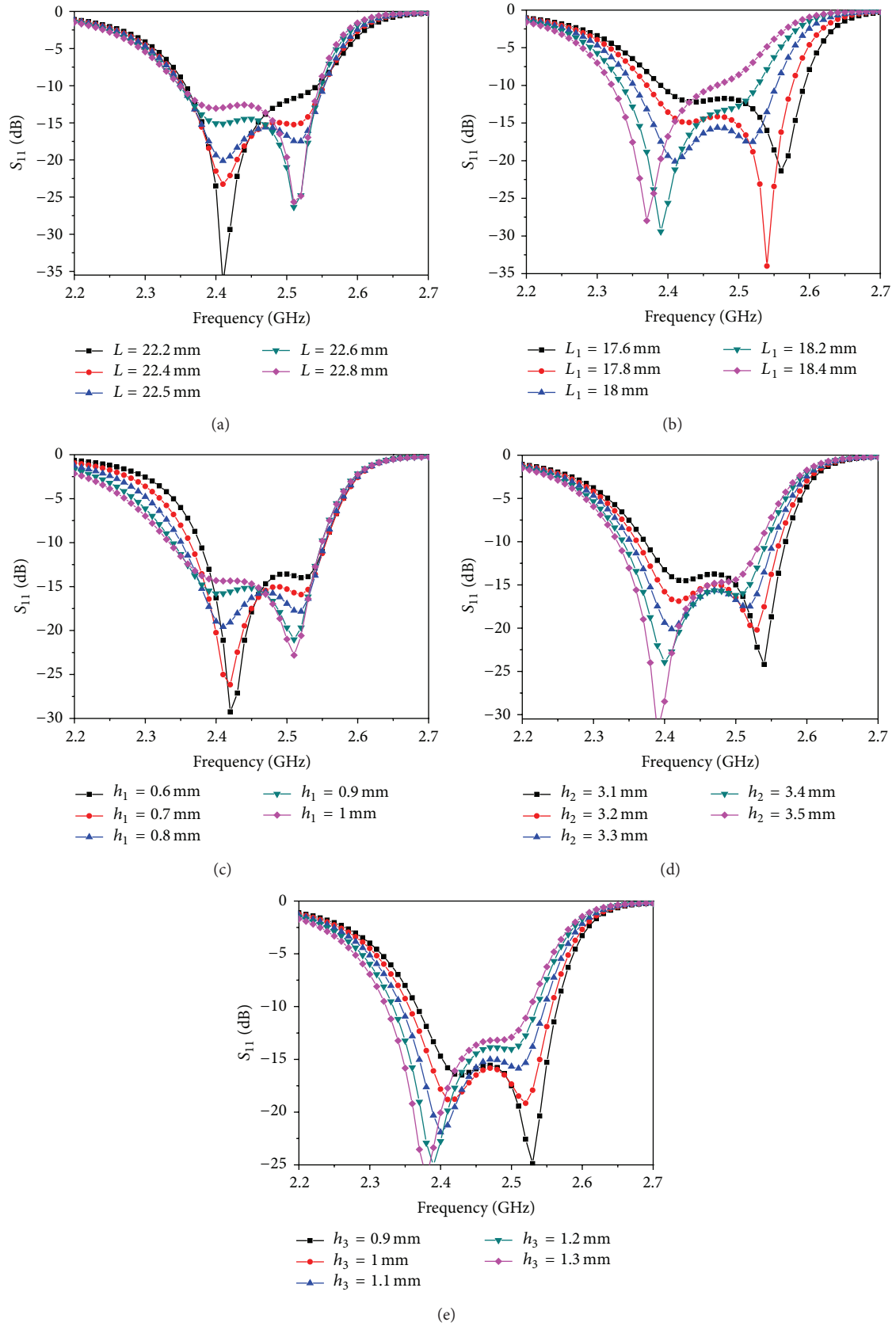


FIGURE 4: S_{11} characteristics, (a) lower patch L variation, (b) upper patch L_1 variation, (c) thicknesses of the LTCC substrate under the lower patch of the antenna variation, (d) separations of the lower and upper patches variation, and (e) thicknesses of the superstrate variation.

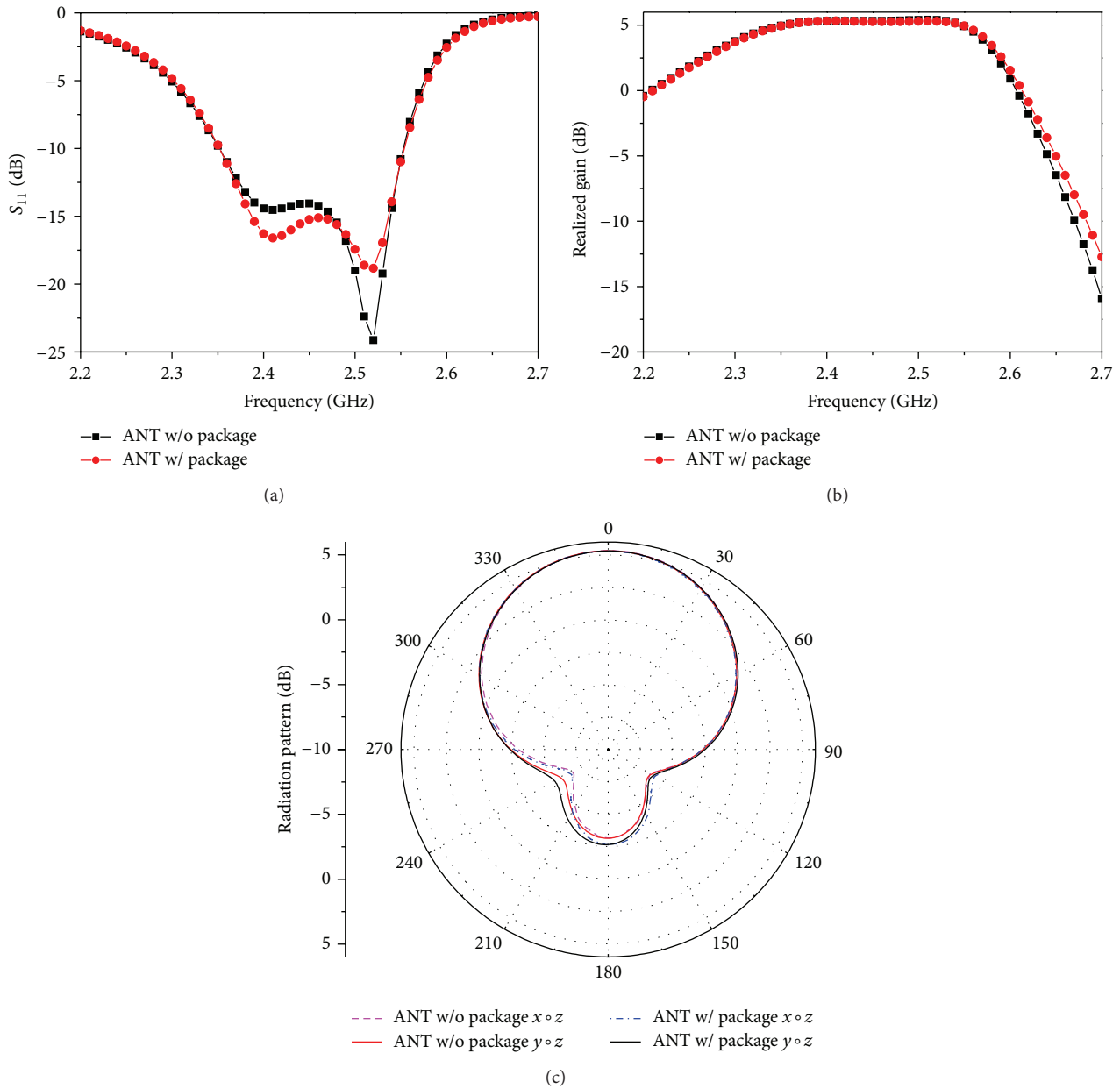


FIGURE 5: The calculated characteristics of the proposed system-on-chip antenna with and without the package: (a) S_{11} , (b) realized gain, and (c) radiation patterns.

show that the more the grounded vias are, the better the antenna at the high frequency matches and the worse the resonant characteristic at the low frequency band does. As a result, the required bandwidth is decreased slightly. The main reason is that the current distribution on the lower patch is changed due to the introduction of the grounded vias. The distributed electric field (E -field) on the chips is a major parameter that provides a detailed statement about the mutual coupling between the antenna and the chips in the package cavity. The E -field distribution in the package cavity is illustrated in Figures 6(b) and 6(c) for two cases. Notice that the relative positions of the package cavities to the antenna are identical. It should also be mentioned that the number of

the complete vias is 59 and the partial via is 45. When the case of partial wall is compared with the case of complete wall, the results show that the leaked E -field from feeding-pin of the antenna and the ground plane is larger for the former. It is worth noting that the maximum and minimum values of E -field shown in Figures 6, 7, 8, and 9 are normalized to 2.5 and 0.01 voltage per meter.

The number of the grounded vias (which is discussed in the following part) controls the strength of coupling between the antenna and the package cavity and, to a lesser extent, the amount of reactive loading that can detune the electromagnetic leakage. This is mainly because the chip circuit is shielded by metallic wall consisting of these grounded vias.

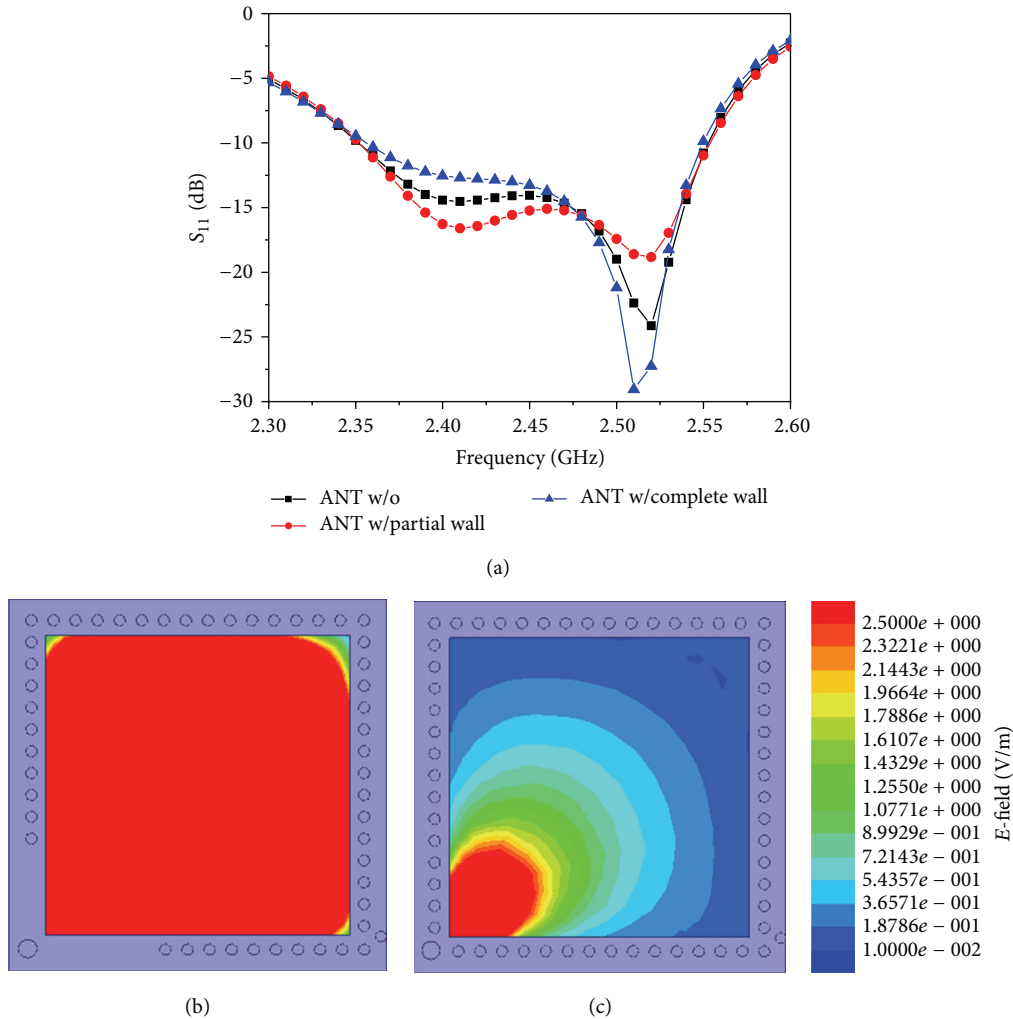


FIGURE 6: Effect of the number of vias on the packaged-chip and the proposed integrated antenna, (a) S_{11} in three cases, (b) E -field distribution in the cavity with partial wall, and (c) E -field distribution in the cavity with complete wall.

The primary effect of a change in the number of the grounded vias is shifting the characteristic of the impedance matching seen by S_{11} . A typical example is shown in Figure 7(a). We can conclude that, in terms of EM mutual coupling, the larger the number is, the less the EM leakage is before the antenna performance has not been heavily affected. At the same time, the position and number of grounded via holes distributed between the antenna ground layer and the system PCB board are also a key factor that affects the antenna performance. Next paragraph will be presented.

The antenna ground layer is connected directly with the system ground plane through the addition of grounded vias distributed on all four side-walls (where the number of the vias will be discussed in following part). The loci of the package cavity and the chips have a crucial effect on the mutual coupling between the chips and the antenna. The position of the cavity and the number and the radii of the grounded vias must be carefully selected, because it is directly related to the antenna performance and the coupling E -field level in the package cavity. We take four typical cases of

the positions of the package cavity into account operating at the center frequency. Note that the graphs shown in Figures 6, 7, 8, and 9 of the electric field distributed in the package cavity are plotted in xy -plane. For comparison's convenience, the maximum and minimum values of the all E -field are selected to be 2.5 and 0.01 voltage per meter, respectively. What is shown in Figure 7 will be described in the following part. The feed points are shown in figures to better understand the location of the package cavity, relative to the antenna. The first one shown in Figure 7(a) is that the package cavity is beneath the patch and the feed is at the corner of the package cavity. The others are offset from case one. The detailed offset parameters are shown in Figure 7. It should be noted that the position of the antenna is unchanged when the position of the package is different. It is shown that the former two cases, shown in Figures 7(a) and 7(b), have a uniform and weak electric field intensity distributed in the package cavity compared with the offset model relative to the case shown in Figure 7(b). The latter two cases, plotted in Figures 7(c) and 7(d), illustrate a relative nonuniform and strong electric

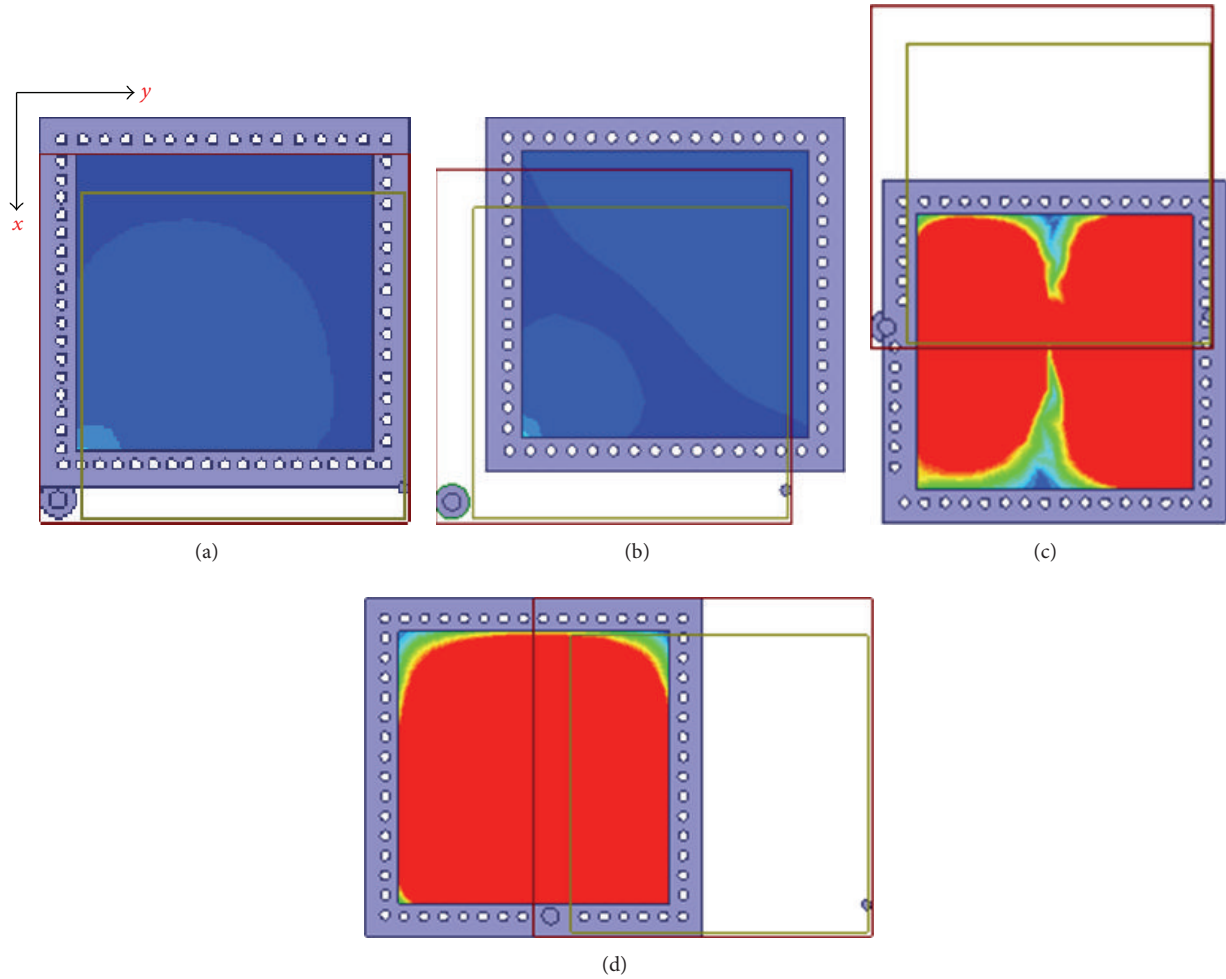


FIGURE 7: Electric field intensity distribution in the package cavity, (a) model of the package near the feed, (b) model of the package offset 2 mm from the feed along x -axis and y -axis, respectively, (c) model of the package offset 5 mm from the feed along x -axis, and (d) model of the package offset 7 mm from the feed along y -axis.

field distribution; moreover, the electric field near the feed is strengthened. So an effective way to weaken the coupling E -field is increasing distance from the feed to the package edge. Furthermore, if the antenna has a relative larger size, the package, to some degree, should be away from the feed as far as possible. Finally, the position of the package is selected to the first case shown in Figure 7(a).

In the previous section, we can see from the two cases of the complete and partial cavity walls that the number of the vias has an impact on the performance of the antenna and the chips due to the effect of the EM coupling. That is to say, a proper number of vias are necessary. Therefore, the number of vias will be discussed in the following. For convenience of discussion, we take account of four specific examples in the following discussion. The number of vias is assumed as 16, 36, 56, and 76, respectively. It is obviously seen from Figure 8 that the distributed E -field in the cavity becomes weak as the number of vias increases. It is also noted that the smaller the E -field intensity on the chips is, the farther the distance of the cavity is away from the feeding pin.

As described above, the position of the package cavity and the number of vias have an effect on the EM mutual coupling. In addition, the size of the via is also a major factor which affects the mutual coupling between the antenna and the chips in the package cavity. The influence is described in the following part. There are three cases that are taken into consideration. The size of the radius is discussed in three cases: 0.2 mm, 0.4 mm, and 0.6 mm, maintaining that the number of the grounded vias is 56.

The strongest coupling E -field is observed when the radius is equal to 0.2 mm; however, the inducing electric field is the weakest with the radius of 0.6 mm. It can be seen from Figure 9 that the smaller the radius is, the stronger the electric field intensity distribution in the package cavity is. It is well understood that the electric strength becomes large as the radius of the vias decreases. When the radius of the grounded vias is large enough, the package cavity can be effectively shielded by the metallic vias distributed on the four sides.

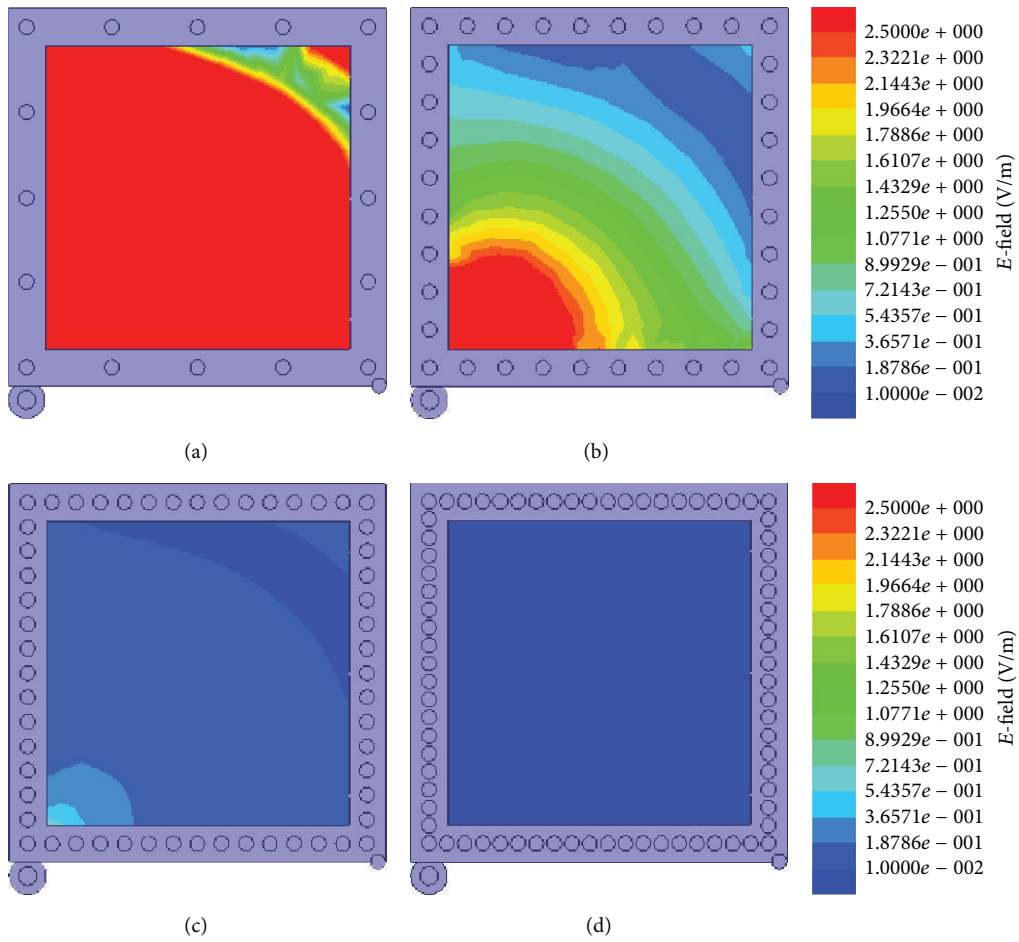


FIGURE 8: Electric field intensity distribution in the package cavity versus different number of the grounded vias, (a) 16, (b) 36, (c) 56, and (d) 76.

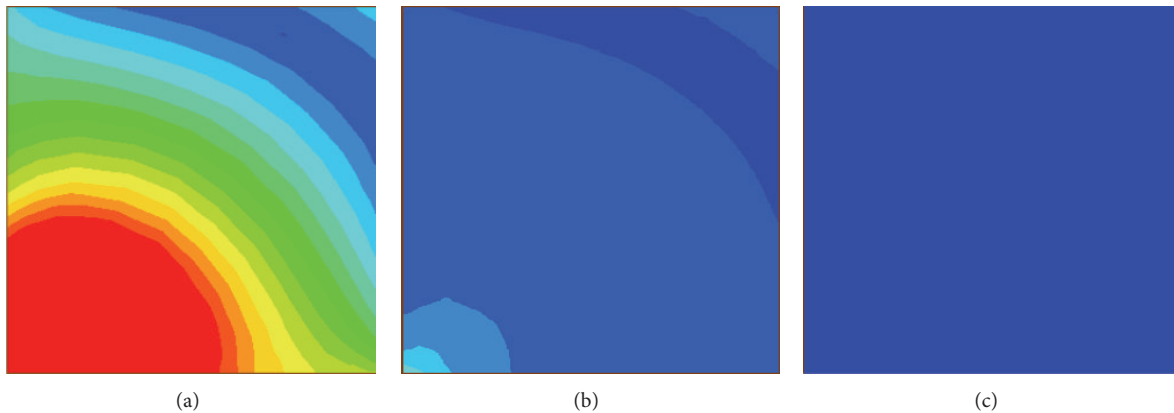


FIGURE 9: Electric field intensity distribution in the package cavity versus different radii of the grounded vias with the number of vias of 56, (a) 0.2 mm, (b) 0.4 mm, and (c) 0.6 mm.

To research the effect of vias on the performance of antenna, the current distributions on the stacked-patch and the ground of the antenna are plotted in Figure 10 including four cases. It can be seen that the current distributions on the stacked-patch are nearly unchanged for the former of two cases with and without vias shown in Figures 10(a) and

10(b). That is to say, the effects of vias on the performance of the antenna are very small. At the same time, it can be seen that the strength of the current distribution on the ground without vias is much stronger than that of the case with vias for the latter of two cases shown in Figures 10(c) and 10(d).

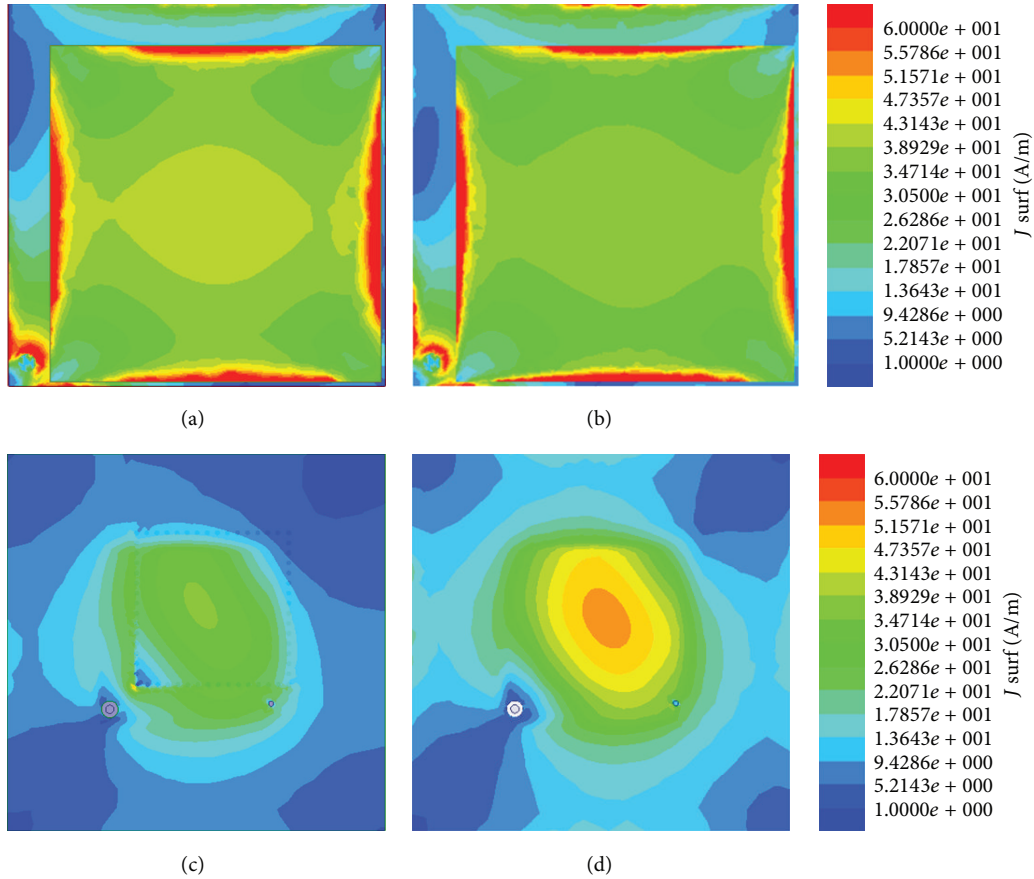


FIGURE 10: Current distribution characteristics, (a) current distribution on the stacked-patch with vias, (b) current distribution on the stacked-patch without vias, (c) current distribution on the ground with vias, and (d) current distribution on the ground without vias.

4. Conclusion

In this paper, a compact and low-profile shorted stacked-patch antenna integrated into the chip package using low temperature cofired ceramic (LTCC) package technology is designed for applications of system-on-package antennas. Broadband linear polarization radiation is achieved and the two modes together give a fractional impedance bandwidth of 8.16% with respect to the center frequency at about 2.45 GHz. The total height of the proposed chip-on-package antenna is 4.09 mm and the average absolute gain is 5.28 dBi across the operating frequency band. Good broadside radiation characteristics for this compact design can be obtained. The EM mutual coupling between the antenna and the package cavity is carefully considered through this paper. The analyses of the number of the grounded vias and their radii have been conducted to identify the EM mutual coupling level of the effects of the parameters on the chips for design guidance. Finally, the number of the grounded vias is determined to be 56 and the radii of the metallic via are selected to be 0.5 mm. These analyses provide a guidance for selecting appropriate position of the package cavity and the number of vias. The mutual coupling between the antenna and the chips is very weak in this design. It shows that the chips in the package cavity can be effectively shielded by

the metallic grounded vias. The proposed antenna structure can also be used to design the other operating frequency band antennas (e.g., Wimax).

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

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