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Research Article

The Application of Approximate Entropy Theory in Defects Detecting of IGBT Module

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Defect is one of the key factors in reducing the reliability of the insulated gate bipolar transistor (IGBT) module, so developing the diagnostic method for defects inside the IGBT module is an important measure to avoid catastrophic failure and improves the reliability of power electronic converters. For this reason, a novel diagnostic method based on the approximate entropy (ApEn) theory is presented in this paper, which can provide statistical diagnosis and allow the operator to replace defective IGBT modules timely. The proposed method is achieved by analyzing the cross ApEn of the gate voltages before and after the occurring of defects. Due to the local damage caused by aging, the intrinsic parasitic parameters of packaging materials or silicon chips inside the IGBT module such as parasitic inductances and capacitances may change over time, which will make remarkable variation in the gate voltage. That is to say the gate voltage is close coupled with the defects. Therefore, the variation is quantified and used as a precursor parameter to evaluate the health status of the IGBT module. Experimental results validate the correctness of the proposed method.

1. Introduction

The survey carried out in [1] shows that the reliability of power electronic converters deserves increasing interest from industry in recent years, but the satisfaction level with reliability monitoring is low at 50%. This suggests more research effort is needed. One of the major challenges is the health management of power electronic devices due to their significant impacts on the degradation of power electronic converters. At present, the IGBTs are the most used power electronic devices in many industrial applications as well as some safe-critical fields such as traction and renewable energy [2, 3], where stringent reliability is required. Though the reliability of IGBTs has been substantial developed recently, the failure rate of IGBTs dropped from 1,000 FITs in 1995 to 20 FITs in 2000, and to only a few FITs currently where 1 FIT is equal 1×10^{-9} failures per device-hour [4], the IGBTs used in those safe-critical fields mentioned above may undergo severe electrical and thermal stress. Such as wind power generation, the IGBTs are subject to large-junction temperature swings during normal operation due to the inherent intermittent nature of the wind speed and low-converter-modulation frequencies [5]. Therefore, monitoring reliability degradation of IGBTs becomes an important issue and still remains as an open topic for research [6].

Reliability is the ability of a product or system to perform as intended for a specified time, in its life-cycle environment [7]. Traditional reliability prediction methods rely on the collection of failure data of the components, but are not applicable for IGBTs because of vast time consumption. More and more researches on detecting reliability degradation of IGBTs are reported in recent years [4, 5, 8–14]. Most of those researches are based on the external indication of aging or impending failure and physics of failure. However, since many of the physical wear-out mechanisms give little external indication [15] or it is very difficult to sense the junction temperature during operation [5], those methods are still under development [6]. Relevant researches indicate that the reliability degradation of IGBTs depends on the fatigue accumulated over time, there are some localized defects induced inside the IGBT module before catastrophic failure, such as the bond wire liftoff and the solder layer cracking [16]. Besides significantly reducing the reliability of

IGBTs, these localized defects may also affect some intrinsic parasitic elements of the IGBT module and consequently change the gate voltage. This provides a practical way to monitor those defects inside the IGBT module by identifying the variation of the gate voltage. Unlike post-fault detections [17–19], monitoring defects inside the IGBT module allows operators to find out an unhealthy IGBT module in a prefault condition and replace it timely to avoid burnout and subsequently collateral damage to the rest of the converter.

The gate circuit consists of intrinsic junction capacitances and associated parasitic inductances and resistances of packaging materials, so it is firmly coupled with those intrinsic parasitic elements inside the IGBT module and sensitive to the occurring of defects. But, sensing the gate voltage during converter operation may be affected by many uncertain factors such as noises, which would lead the conclusion to be ambiguous. To circumvent this limit, a diagnostic method based on the approximate entropy theory is proposed in this paper, which can provide statistical diagnosis [20]. Such statistical diagnosis can be well understood and accepted.

The rest of this paper is organized as follows. Firstly, the failure mechanisms of IGBTs and the influences of defects over the performance of the gate circuit are discussed, a linearization of the gate circuit over a particular time period of the turn-on process of the IGBT module is adopted to eliminate disturbance caused by the nonlinear gate to collector capacitor C_{GC}, then the approximate entropy theory is overviewed and the calculation of the cross ApEn is also carried out. Finally, a diagnostic method based on the variation of the cross ApEn of the gate voltages before and after the occurring of defects is proposed to find out the possible abnormality, and a confirmatory experiment is also carried out by adopting a special unencapsulated IGBT module to verify the correctness of the diagnostic method proposed in this paper.

2. Failure Mechanisms and Defects of IGBTs

2.1. Failure Mechanisms of IGBTs. Modern IGBTs are characterized by numerous advantages such as low on-state resistance, good switching speed and excellent safe-operating area. They are widely used in low-to-medium-power and high-frequency applications, and nowadays even replaced the gate turn-off (GTO) thyristors in high power range. There are a variety of configurations of IGBTs from discrete IGBTs to IGBT modules. Among those configurations, the IGBT modules are very popular in high-power applications. Though upcoming semiconductor materials, such as silicon carbide has attracted more and more attention, most commercial available high-power IGBT modules are still fabricated using silicon as the base material. Being limited by the material properties of silicon, the power density of the IGBT chip is restricted, thus many IGBT chips are connected in parallel inside the IGBT module, together with diode chips antiparallel placed serving as freewheeling diodes (FWD) at present, in order to enhance the current conducting capability as shown in Figure 1. In this case, there are two

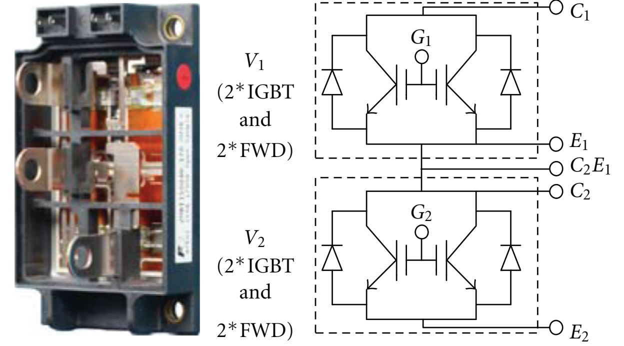
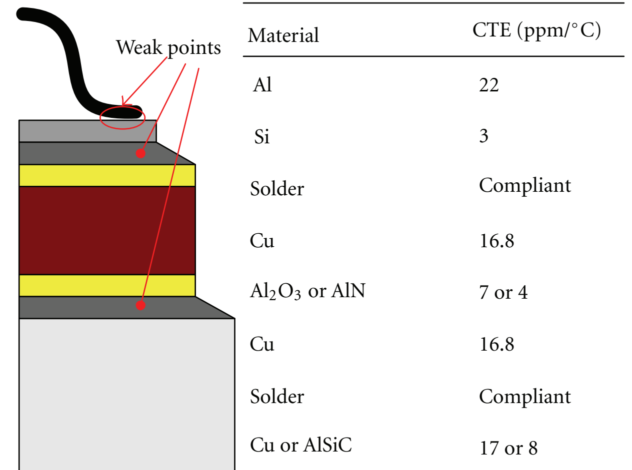


Figure 1: A typical half bridge module and its equivalent circuit.



Material	CTE (ppm/°C)
Al	22
Si	3
Solder	Compliant
Cu	16.8
Al_2O_3 or AlN	7 or 4
Cu	16.8
Solder	Compliant
Cu or AlSiC	17 or 8

Figure 2: Cross section of an IGBT Module and related CTEs of its component materials.

IGBT switches in the IGBT module. Each switch consists of two parallel IGBT chips and two antiparallel FWD chips.

The IGBT module is complex multilayered structure with different materials in intimate contact with each other, which provide mechanical stability, electrical insulation, and thermal conduction. Thermal interactions between these materials play an important role in the long-term reliability of the IGBT module [16, 21]. The schematic cross-section of the IGBT module and related coefficients of thermal expansion (CTE) of its component materials are represented in Figure 2. From top to bottom are bond wire, silicon chip, direct bonded copper ceramic substrate (DBC), and baseplate. From Figure 2, it can be seen that there are two weak points within the IGBT module due to the CTE mismatch, one is the interface between bond wire and silicon chip, the other is solder layer. Thermal stress caused by large junction temperature swings (up to 80°C) occurred in some fields has a severe effect on the reliability of IGBTs [4, 5]. Bond-wire fatigue and solder fatigue have been identified as the main failure mechanisms [9, 22].

2.2. Defects and Their Influences. There are two main defects observed inside the IGBT module: the liftoff of bond wire

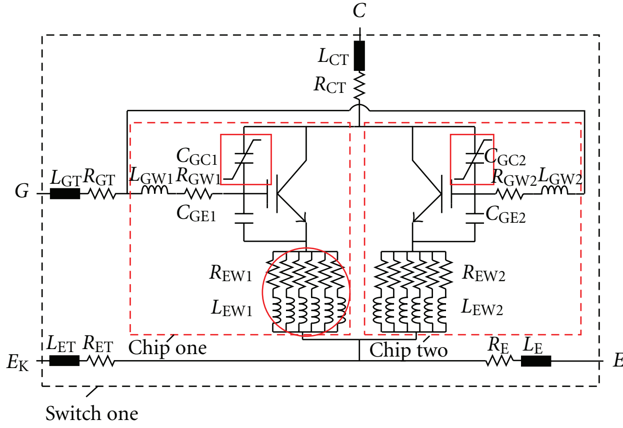


Figure 3: Parasitic elements of one switch inside an IGBT module.

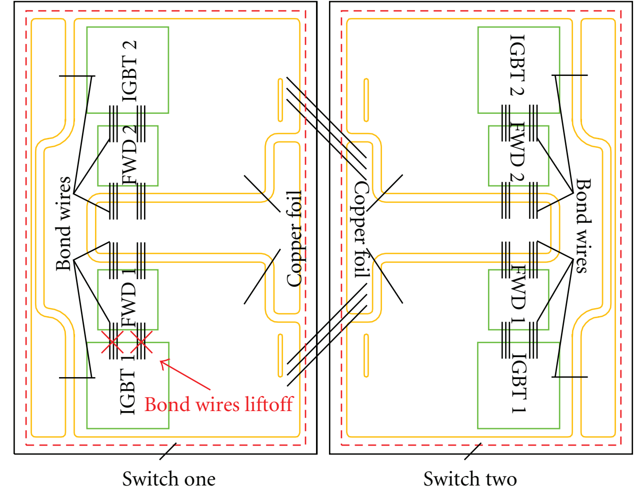


Figure 4: Bond wires liftoff inside an IGBT module.

and the crack of solder layer as a results of aging. These defects would affect some intrinsic parasitic elements of the IGBT module like parasitic inductance and resistance of the emitter bond wires or junction capacitances, as shown in Figure 3 [23, 24], where L_{GT} and R_{GT} are the parasitic inductance and resistance of the gate lead respectively, L_{GW} and R_{GW} are the parasitic inductance and resistance of the gate bond wire respectively, C_{GE} is the gate-emitter capacitance, C_{GC} is the gate-collector capacitance, L_{EW} and R_{EW} are the parasitic inductance and resistance of the emitter bond wires respectively, L_{ET} and R_{ET} are the parasitic inductance and resistance of the auxiliary emitter lead respectively, L_E and R_E are the parasitic inductance and resistance of the emitter lead respectively, L_{CT} and R_{CT} are the parasitic inductance and resistance of the collector lead respectively, and the numbers in those symbols indicate different chips in the switch. Note that the collector-emitter capacitance C_{CE} is not included in Figure 3 because it has little effect on the switching characteristics of the IGBT module [25].

The liftoff of bond wire can change not only the parasitic inductance and resistance of emitter bond wires, but also the layout of the IGBT module. For example, if six bond wires connecting the emitter of chip one are liftoff as shown in Figure 4, this chip will be to failure, then the layout of the IGBT module is altered that two paralleled chips become one. Consequently, the equivalent total gate-emitter parasitic capacitance is also changed. Cracks at silicon-substrate or substrate-baseplate solder layers can reduce the effective area for heat conduction and increase the thermal resistance from junction to case, which will lead to higher junction temperature [6] and ionize more hot carriers to change the junction capacitance. In addition, the gate electrostatic discharge and the collector over-voltage can also ionize hot carriers and affect the junction capacitance, but they should be accidental factors. On the whole, defects would affect some intrinsic parasitic elements involved in gate circuit.

2.3. Linearization. From Figure 3, it can be seen that the gate voltage V_{GE} is electrically coupled with the collector-emitter voltage V_{CE} by the Miller capacitance C_{GC} including C_{GC1} and C_{GC2}. This Miller capacitance consists of the series combination of the gate-drain-overlap oxide capacitance C_{OXD} and the gate-drain-overlap depletion capacitance C_{GDJ}, is a typical nonlinear intrinsic parasitic element due to the voltage dependence of the capacitance C_{GDJ} [26].

$$C_{GC} = \begin{cases} C_{OXD} & V_{CE} < V_{GE} - V_{GE(th)} \\ \dfrac{C_{OXD}C_{GDJ}}{C_{OXD} + C_{GDJ}} & V_{CE} \geq V_{GE} - V_{GE(th)} \end{cases}, \qquad (1)$$

$$C_{GDJ} = \frac{A_{GD}\varepsilon_{Si}}{\sqrt{2\varepsilon_{Si}(V_{CE} - V_{GE(th)})/q/N_B}},$$

where A_{GD} is the gate-drain overlap area, ε_{Si} is the dielectric constant of silicon, $V_{GE(th)}$ is the gate threshold voltage, and N_B is the base doping concentration. The significant change in C_{GC} can be as large as a factor of 10 to 100 [25]. Since V_{CE} differs in different applications, the direct use of the gate voltage would lead the diagnostic results to be ambiguous. So a linearization of the gate circuit over a particular time period of the turn-on process of the IGBT module is employed. As shown in Figure 5, during the beginning stage of the turn-on process, that is, the time interval from t_0 to t_1, the collector-emitter voltage V_{CE} remains at the high DC voltage as long as the free-wheeling diode is conducting, C_{GC} remains at a small constant value because of the high and unchanged V_{CE} and almost equals to C_{GDJ} which is far less than C_{GE}. So the beginning from t_0 to t_1, is the most relevant stage, where the nonlinear influence caused by C_{GDJ}, and V_{CE} is eliminated and the whole intrinsic parasitic elements involved in the gate circuit can be seen as linear elements because rest-associated intrinsic parasitic inductances and resistances like L_{EW1} and R_{EW1} are linear elements and not affected by V_{CE}.

Then the gate voltage can be seen as a step response of a second-order linear system as shown in Figure 6, where V_1 and V_2 are negative and positive supply voltage of the gate circuit, respectively, S_1 is the control signal, R represents the total external resistance, L represents the total external inductance, R_G represents the total intrinsic parasitic

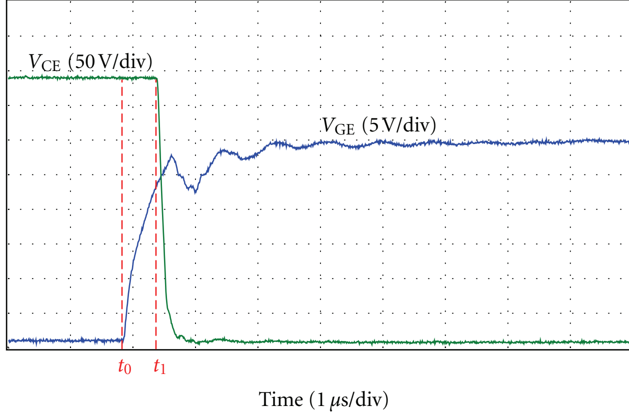


Figure 5: Turn-on waveforms of the IGBT module.

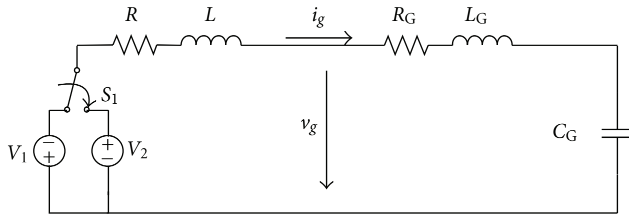


Figure 6: A simplified gate-drive circuit of an IGBT.

resistance involved in the gate circuit, L_G represents the total intrinsic parasitic inductance involved in the gate circuit, C_G represents the total intrinsic parasitic capacitance involved in the gate circuit. In most cases, the external components of the gate circuit are fixed. Therefore, the variation of the gate voltage is mainly contributed by the change of intrinsic elements. The purpose of this paper is to extract precursor information from variation of the gate voltage at the beginning stage of the turn-on process.

3. Approximate Entropy Theory and Defects Diagnosis

From analysis mentioned above, it is clear that the variation of the gate voltage at the beginning stage of the turn-on process is closely coupled with defects inside the IGBT module. So this variation can be used as precursor parameter to develop a diagnostic methodology for IGBT defects. However, sensing the gate voltage during converter operation may be affected by many uncertain factors such as noises, which may have impact on the diagnostic results. To overcome this limit, a diagnostic method based on the approximate entropy theory is proposed in this paper.

3.1. Theory of ApEn. The ApEn is developed from statistics, and is used to quantify the amount of system complexity and the unpredictability of variations over time-series data, which has the advantages of lower computational demand, small data samples, less noise effects [20]. The definition and algorithm for the ApEn of the gate voltage are introduced in the following.

(1) Given a time series of the gate voltage data $U = \{u_i, i \in N\}$ from measurements equally spaced in time. The value N presents the length of the time series.

(2) Fix $m < N$, an integer, and r, a positive real number. The value m presents the length of compared run of data, and r presents a tolerance level. Typically choose $m = 2$, and $r = 0.1\sim0.2SD(U)$, $SD(U)$ is the standard deviation of U.

(3) Form a sequence of vectors $X = [u(i), u(i+1), \ldots, u(i+m-1)]$, in R^m, real m-dimensional space.

(4) Define for each i, $i = 1\sim N-m+1$,

$$C_i^m(r) = \frac{(\text{number of } x(j) \text{ such that } d[x(i), x(j)] \le r)}{(N-m+1)}, \tag{2}$$

where, $d[x(i), x(j)] = \max_{k=1,2,\ldots,m}(|u(i+k-1) - u(j+k-1|)$.

(5) Define $\Phi^m(r) = (N-m+1)^{-1}\sum_{i=1}^{N-m+1}\log(C_i^m(r))$.

(6) Form $X \in R^{m+1}$, and repeat (4) ∼ (5), get $\Phi^{m+1}(r)$.

(7) Define approximate entropy as

$$\text{ApEn}(m, r, N) = \Phi^{m+1}(r) - \Phi^m(r). \tag{3}$$

3.2. Cross ApEn of Gate Voltage Developed from the Theory of ApEn. In order to distinguish the gate-voltage data sampled at different stages of the life cycle, the algorithm for the cross ApEn is also provided as follow.

(1) Given one time series of the gate-voltage data $U = \{u_i, i \in N\}$ from measurements equally spaced in time as references, and another one $V = \{v_i, i \in N\}$ of real-time samples. The value N presents the length of the time series.

(2) Fix $m < N$, an integer, and r, a positive real number. The value m presents the length of compared run of data, and r presents a tolerance level. Typically choose $m = 2$, and $r = 0.1\sim0.2COV(U, V)$, $COV(U, V)$ is the covariance of U and V.

(3) Form a sequence of vectors $X = [u(i), u(i+1), \ldots, u(i+m-1)]$, in R^m, real m-dimensional space.

(4) Form a sequence of vectors $Y = [v(i), v(i+1), \ldots, v(i+m-1)]$, in R^m, real m-dimensional space.

(5) Define for each i, $i = 1 \sim N-m+1$,

$$C_i^m(r) = \frac{(\text{number of } y(j) \text{ such that } d[x(i), y(j)] \le r)}{(N-m+1)}, \tag{4}$$

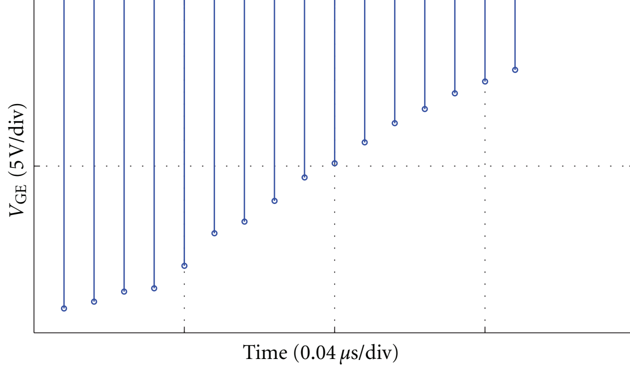


Figure 7: One data acquisition of the gate voltage.

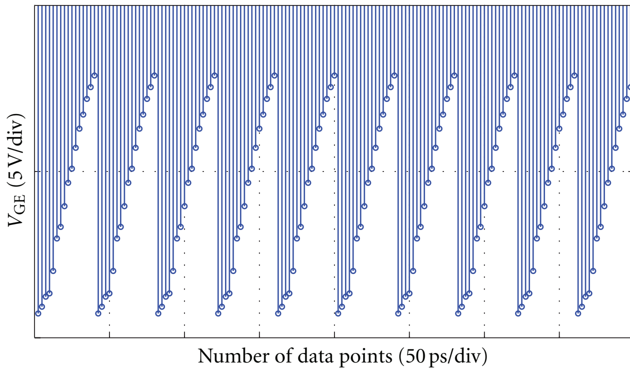


Figure 8: One sample of the gate voltage.

where, $d[x(i), y(j)] = \max_{k=1,2,\ldots m}(|u(i+k-1) - v(j+k-1|)$.

(6) Define $\Phi^m(r) = (N-m+1)^{-1}\sum_{i=1}^{N-m+1}\log(C_i^m(r))$.

(7) Form $X \in R^{m+1}$, and repeat (4) $\sim$ (5), get $\Phi^{m+1}(r)$.

(8) Define cross ApEn as

$$\text{CApEn}(m, r, N) = \Phi^{m+1}(r) - \Phi^m(r). \quad (5)$$

3.3. Sample of Gate Voltage. The time interval from t_0 to t_1 shown in Figure 5 is very short. Generally, this time interval is less than 1 μs. But, the highest sampling rate of an analog-to-digital converter at a reasonable price is about 125 M. This implies one data acquisition is not enough to carry out the algorithm for the ApEn and the cross ApEn as shown in Figure 7.

To circumvent this limit, a number of successive cycles of the gate voltage are measured and reassembled to one sample as shown in Figure 8, in this case 10 cycles.

4. Valiadation and Discussion

4.1. Validation. In order to examine the diagnostic method provided in this paper, a test rig is built in lab as shown in Figure 9. An especially uncovered 2MBI150U4H-170 IGBT module provided by FUJI as shown in Figure 1 is included, together with a power source (Agilent 6813B), a control board, a gate driver, and a oscilloscope (TDS5104B). The inductive load has 10 Ω resistance in series with 300 μH inductance, and the switching frequency of the device under test (DUT) is 10 kHz, and the sampling rate of TDS5104B is set to 125 MS/s, at approximately the same rate of an analog-to-digital converter AD9600ABCPZ-125 from ADI. Two levels of bond-wire liftoff defect are simulated, the first one is three bond wires are liftoff inside the DUT, and the other one is chip failure, namely, six bond wires which are connected to the emitter of chip one inside the DUT are all liftoff as shown in Figure 4. The experiment results are shown in the following. Here, the gate voltage data at the health state is used as reference.

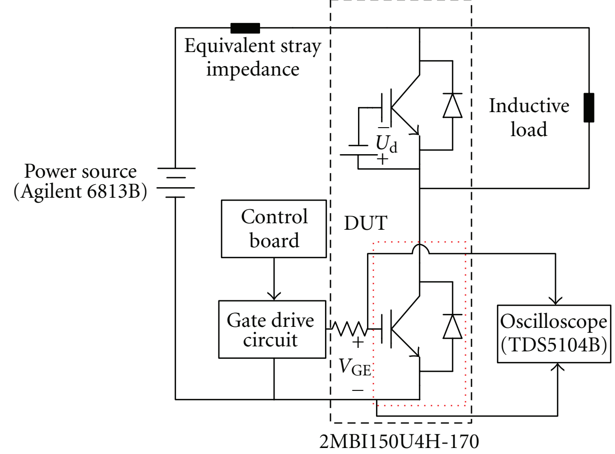


Figure 9: A test rig built for verification.

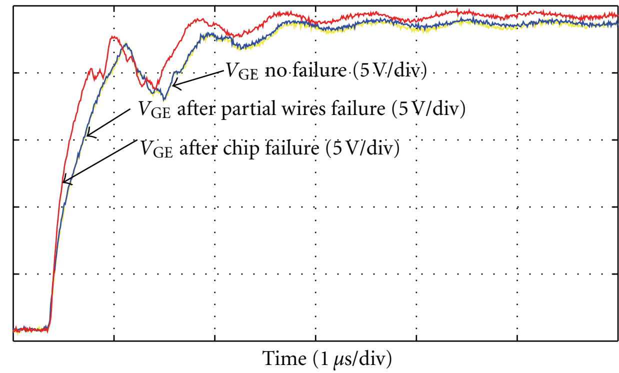


Figure 10: Turn-on waveforms of the gate voltage according to different states.

From the experiment results detailed in Figures 10 and 11, it is clear that partial bond wires failure contributes little to the variations of the gate voltage. This is because the values of parasitic inductances and resistances of bond wires are very small, so they do not play an important role in deciding the gate voltage as shown in Figure 10. But, after the chip failure, the significant changes can be found as shown in Figures 10 and 11, and the corresponding inference results by ApEn model also suggests that the cross ApEn of the gate voltage has a remarkable change from 0.189 to 0.457,

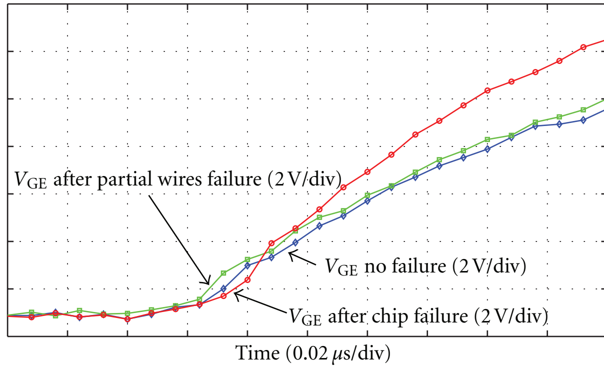


Figure 11: Detailed waveforms of the gate voltage according to different states.

Table 1: Predicted results.

Defect level	ApEn	CApEn
No failure	0.163	0.167
Wire failure	0.284	0.189
Chip failure	0.231	0.457

comparing to partial bond wire failure which just changes from 0.167 to 0.189 as shown in Table 1. Though the results show that the ApEn of the gate voltage also changes with defects, the trend is not obvious. Hence, the cross ApEn of the gate voltage will be better for defects diagnosis. Due to the fact that enormous number of chips in an IGBT module in high-power case, a single or two chips failure would not lead to an catastrophic failure to the entire module, in other words, the IGBT module is still operable, and the post-fault detection methods may do not work here. Therefore, the method proposed in this paper can be considered as prefault detection, which gives the operators a chance to replace the defective modules and avoid a sudden breakdown, and the maintenance can also be scheduled.

5. Conclusion

This paper proposed an ApEn-based method to monitor defects in an IGBT module using gate voltage at beginning state. This method can be seen as prefault detection, and is able to accurately detect chip defect in an IGBT module, that may cause the rest chips over current and the whole module damaged. The method may give enough time for the operators to replace the defective IGBT modules. Experimental results are provided to verify the effectiveness of the method. And it is hopeful to improve the operational reliability of power converter. The future work should consider online acquisition of the gate voltage, and so forth.

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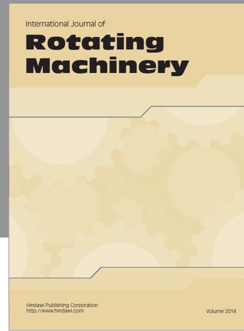
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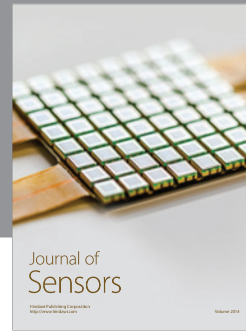
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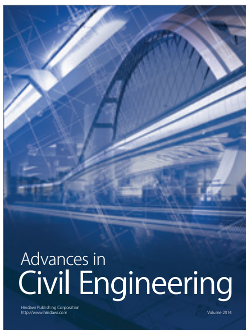
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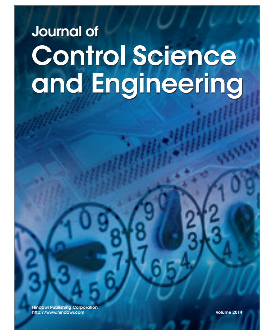
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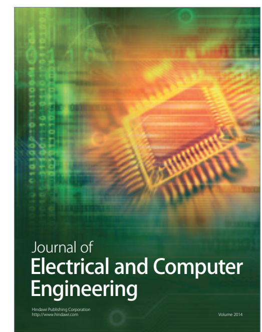
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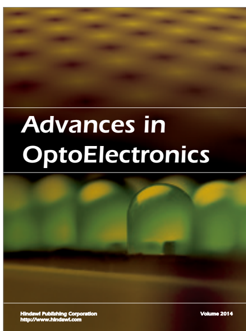
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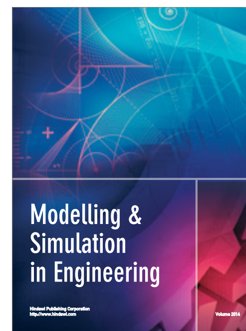
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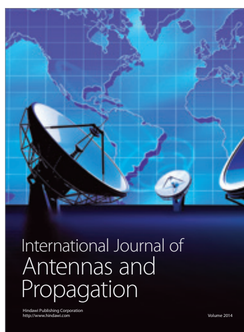
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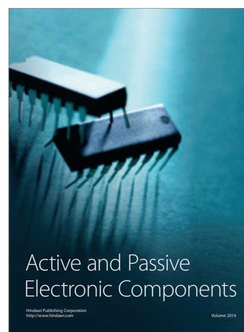
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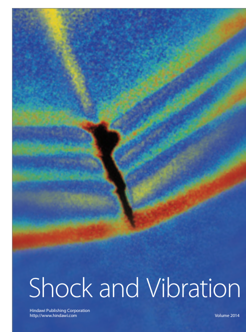
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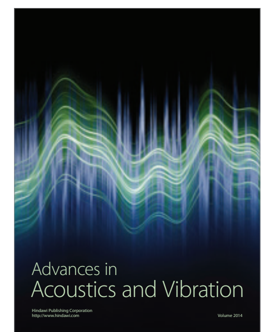
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