A SIMPLIFIED SPICE MODEL FOR IGBT

A. HADDI*, A. MAOUAD, O. ELMAZRIA, A. HOFFMANN and J. P. CHARLES

Centre Lorrain d'Optique et d'Electronique des Solides, Supélec, 2 rue Edouard Belin, 57078 Metz Cedex 3, France

A simplified IGBT (Insulated Gate Bipolar Transistor) SPICE macromodel, based on its equivalent circuit, is proposed. This macromodel is provided to simulate various mechanisms governing the behavior of the IGBT, and it takes into account specific phenomena limiting its SOA (Safe Operating Area), such as forward and reverse biased SOA, as well as latch-up. The validity of this model is confirmed by comparison between simulation and experimental results as well as the data sheets. This comparison is tested for two IGBT devices showing two different powers and switching speeds, and a good agreement is recorded for both IGBT devices.

Keywords: Insulated gate bipolar transistor; simulation; spice

I. INTRODUCTION

The Insulated Gate Bipolar Transistor (IGBT) was added to the family of power devices to overcome the high on-state loss of power MOSFETs. The IGBT is an hybrid device that combines the advantages of a MOSFET (high switching speed and low power drive requirement) and of a bipolar junction transistor (BJT) (low conduction losses) [1].

The combined top perspective and cross-sectional views, not to scale, of one from the thousands of cells the IGBT comprises are shown in Figure 1. Its structure is similar to that of a Vertical Double diffused MOSFET (VDMOSFET) with the exception that a p-type,

---

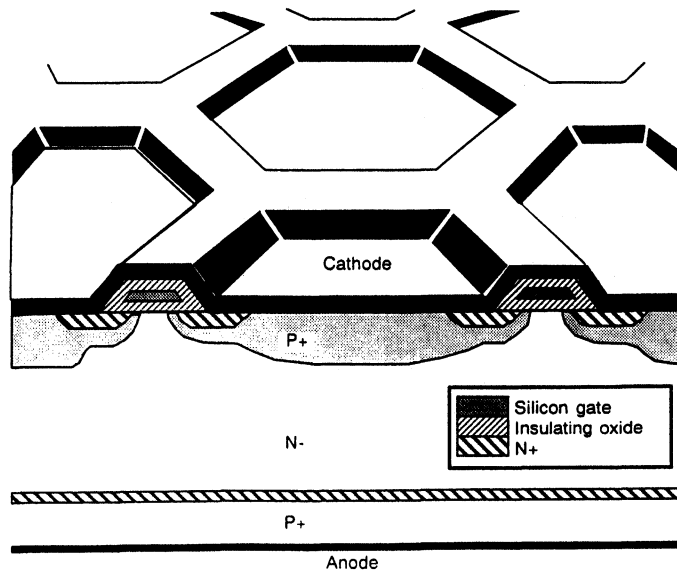*Corresponding author. Fax: (+33/0) 3 87 75 96 01.

FIGURE 1   Top view and cross section, not to scale, of one from the thousand cells of an n-channel IGBT.

heavily doped substrate, replaces the n-type drain contact of the conventional VDMOSFET.

Analytical models exist already [2]. Their implementation sets many problems due to the complexity of the equations used for calculating the current and charges of the IGBT. Some authors [3] proposed simplified equations, but the simulation results show inaccurate results near limit or non standard operating conditions. Another solution is to translate the physical equations into electrical circuits with original solutions to replace the derivative functions and other operators [4 – 7], but this solution requires a specific SPICE version like IG-SPICE (Interactive Graphics SPICE).

In this work we present another approach which consists in defining the IGBT as a simple macromodel based on its equivalent circuit. The validity of this model is confirmed by comparison between simulation and experimental results as well as the manufacturer's data. Two IGBT devices from International Rectifier, IRGBC20S and IRGBC40F, showing different powers and switching speeds, are modelled and tested.

II. CIRCUIT MODEL

The complete macromodel of IGBT that we suggest is given in Figure 2. The core of this macromodel is the IGBT equivalent circuit marked with bold typeface, *i.e.*, a p−n−p bipolar transistor driven by a n-channel MOSFET in a pseudo-Darlington configuration [8]. This core has been completed with some components to help simulate various mechanisms governing the behavior of the IGBT, such as forward and reverse biased SOA, latch-up, switching parameters, *etc.*

II.1. DC Model of IGBT

The transfer characteristics of an IGBT and a power MOSFET are similar apart from a shift due to the built-in potential of the base-emitter junction of the p−n−p bipolar transistor. Indeed, the IGBT current is equal to the MOSFET one multiplied by the current gain of the p−n−p bipolar transistor. Therefore, several static parameters of the IGBT depend on the SPICE parameters of the MOSFET.

In our study, the SPICE models used for the BJT and the MOSFET are the Gummel Poon and the Shishman Hodges models respectively.
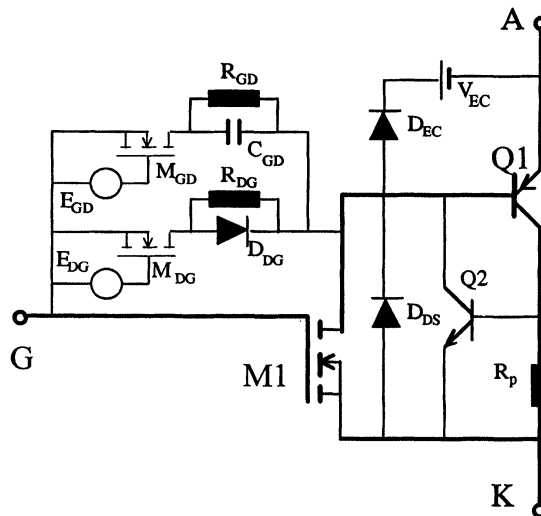

FIGURE 2 Macromodel, based on the equivalent circuit of the IGBT, used for modelization.

The SPICE parameters which provide for adjustment of saturation current, conductivity, and static saturation voltage of the IGBT are: K_p (Transconductance coefficient), W and L (channel width and length respectively), GAMMA (bulk threshold parameter), PHI (surface potential), and LAMBDA (channel-length modulation) for the MOSFET element, and the current gain for the BJT.

II.2. Dynamic Model of IGBT

After calibration of the static parameters, one can proceed with the dynamic model. Two branches, with components names indicated GD and DG in the sub-circuit, between the gate and drain of the MOSFET, are used to simulate the dynamic parameters [9]. Typical dynamic parameters, used to characterize the IGBT, are the switching characteristics times: rise time (t_r), fall time (t_f), turn-on delay time (t_{don}), turn-off delay time (t_{doff}), turn-on time (t_{on}), and turn-off time (t_{off}), with:

$$t_{on} = t_r + t_{don} \quad \text{and} \quad t_{off} = t_f + t_{doff}.$$

Fall Time Calibration

The biggest limitation to the turn-off speed of an IGBT is the lifetime of the minority carriers in the n^- epi. layer, *i.e.*, the base of the $p-n-p$ bipolar transistor. The charges stored in the base produce a characteristic "tail" in the current waveform of an IGBT at turn-off. When the MOSFET's channel turns off, electron current decreases and the IGBT current drops rapidly to the level of the hole recombination current at the inception of the tail. Since the base current of the $p-n-p$ bipolar transistor corresponds to the MOSFET drain current, the current gain of the $p-n-p$ transistor is then, given by [1]:

$$\beta(Q1) = \frac{I_c}{I_{MOS}}.$$

This current gain, *BF* parameter in SPICE, allows to adjust the abrupt fall amplitude and implicitly the fall time value, this can be also adjusted directly by the ideal forward transit time of the parasitic $n-p-n$ transistor (parameter *TF* in SPICE).

Turn-off Delay Time Calibration

Because of the particular structure of the IGBT where the gate metalization covers a big part of the MOSFET's drain (n^- layer), the gate-drain capacitance C_{GD} is the main cause of the turn-off delay time [10]. In addition, C_{GD} is the capacitance of a MOS structure, its value is function of the gate voltage. This capacitance is the equivalent capacitance of the oxide capacitance C_{ox} and of the depletion drain capacitance C_{GDd}. The equivalent sub-circuit used here is a fixed capacitance C_{GDmax} representing C_{ox} and a diode D_{DG} used because the diode transit capacitance has the same behavior as C_{GDd}. Two MOSFET transistors, M_{GD} and M_{DG}, controlled respectively by gate-drain voltage E_{GD} and E_{DG} can switch alternatively to C_{GDmax} or C_{GDd}. The SPICE parameters of M_{GD} and M_{DG} are chosen to be that of an ideal MOSFETs in order not to disturb the sub-circuit working. Therefore, the turn-off delay time, t_{doff}, can be adjusted by the value of C_{GDmax} and the SPICE parameters of the diode D_{DG}.

Turn-on Delay Time Calibration

The turn-on delay time fitting can be obtained by adjusting the SPICE parameters of the MOSFET. These parameters are the capacitances C_{GBO} (gate-bulk overlap capacitance per channel length) and C_{GSO} (gate-source overlap capacitance per channel width). The turn-on delay time t_{don} increases as these capacitance values increase.

Rise Time Calibration

Parameters of the sub-circuit allowing to adjust the rise time are, mainly, K_p (transconductance coefficient) and IS (bulk p–n saturation current). Since K_p is used to regulate the static characteristics, we use especially IS to regulate t_r.

II.3. Parameters Limiting the SOA

Safe Operating Area (SOA) is very important in power electronics. Its determination allows one to know the limits of the normal device operating condition. In the IGBT case, the most interesting

parameters, limiting the SOA, are the forward and reverse biased SOA voltages and latch-up current.

Forward Biased SOA

The breakdown voltage is not forecasted by the bipolar transistor model included in standard SPICE library. This is why an appropriate breakdown voltage value is chosen for the D_{DS} diode to model this behavior. This additional diode is connected between the MOSFET's drain and source. When the anode bias voltage is positive (*i.e.*, $V_{AK} \geq 0$) and the MOSFET's n-channel turns off (when $V_{GK} \leq 0$), the p−n−p bipolar transistor is not conducting. The anode voltage is, therefore, given as:

$$V_{AK} = V_{EB}(Q1) + V_{D_{DS}}, \text{ where } V_{EB}(Q1) \approx 0.7\,\text{V}.$$

By using the SPICE parameter BV (reverse Breakdown Voltage of the diode D_{DS}), the equation can be rewritten as:

$$BV = V_{BV} - 0.7\,(\text{V}).$$

V_{BV} is the forward biased SOA voltage value of the IGBT. So this value is fixed by adjusting the BV parameter.

Reverse Biased SOA

This phenomenon is represented by the D_{EC} and D_{DS} diodes conduction states for some negative values of anode bias voltage V_{AK}, $V_{AK} = V_{EB} + V_{BC} - V_{EC}$. In operating conditions such as: $V_{EB} \leq -0.7\,\text{V}$ and $V_{BC} \leq -0.7\,\text{V}$, the negative current is the current flowing from the cathode through both diodes and the supply voltage V_{EC} to the anode of the IGBT when: $V_{AK} \leq -1.4 - V_{EC}\,(\text{V})$. The reverse biased SOA voltage of the IGBT is, therefore, adjusted by the supply voltage V_{EC} value. This value will be determinated as function of the IGBT's reverse biased SOA voltage measured or given in the data sheets.

Static Latch-up Modelling

When an IGBT goes into latch-up, the parasitic n−p−n transistor of the device starts to conduct. This behavior can be modelled by

introducing a n−p−n bipolar transistor between the MOSFET's drain and source, which is controlled by the series resistance R_p of the p-well. Latch-up occurs when the voltage drop over this resistor is large enough to turn on the parasitic n−p−n transistor, *i.e.*, when:

$$R_p \times I_c(Q1) > V_{EB}(Q2).$$

Where V_{EB} is the built-in potential of the n−p−n transistor Base-Emitter junction.

The value of the resistor R_p can be expressed using the IGBT's current I_{AKlup} (measured or given in the data sheets) causing the latch-up and the current gain of the bipolar transistor $\beta(Q1)$:

$$R_p = \frac{V_{EB}(Q2)}{I_c(Q1)} = \frac{V_{EB}(Q2)}{I_{Aklup}} \times \frac{\beta(Q1) + 1}{\beta(Q1)}.$$

Although this latch-up model is simple, it allows for modelling the static latch-up in circuit simulation.

III. RESULTS

We have adjusted our model to simulate two IGBT devices from International Rectifier (IR): IRGBC20S and IRGBC40F with various powers and switching speeds. The first one is a standard type 600 V − 20 A, and the second one is a fast type 600 V − 40 A.

The SPICE parameters of the models corresponding to the two IGBT devices are determined so as to fit the data sheet static and dynamic electrical characteristics.

Figures 3 and 4 show the I−V characteristics, simulated (a) and given in the manufacturer's data book (b), for an IRGBC20S and an IRGBC40F samples respectively. A good agreement is recorded for both IGBT devices.

Concerning the switching parameters, only the switching time values are given in the data sheets. These values are compared in Table I with those obtained by our model.

The data sheets correspond generally to typical value or to average values obtained from several samples. To verify the accuracy of our
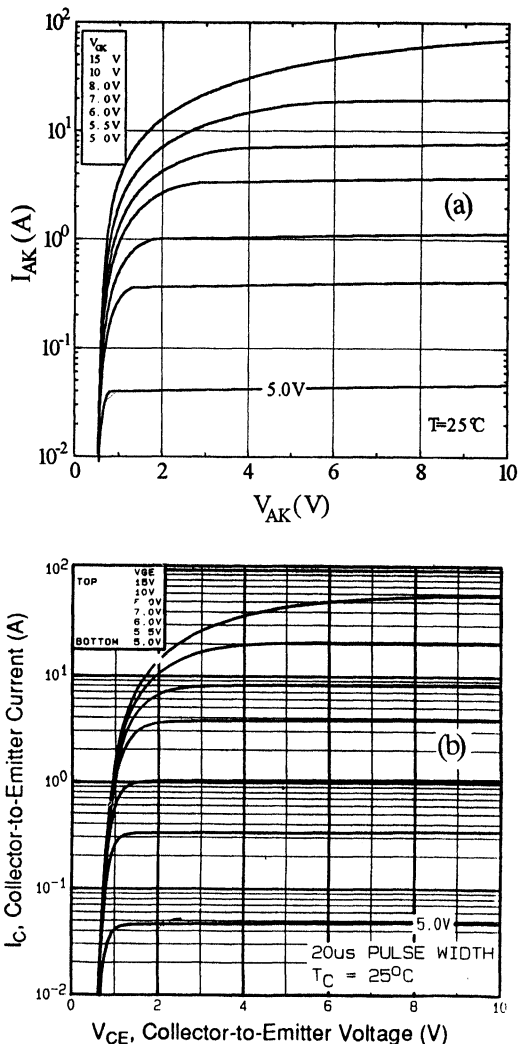
FIGURE 3   I – V characteristics obtained by simulation (a) and given in the data sheets (b) for an IRGBC20S.

model, we have compared its results with experimental ones performed on a given IGBT sample. The results of this comparison are shown in Figures 5 and 6, for static and dynamic characteristics, respectively. The simulation fits very well the experimental characteristics.
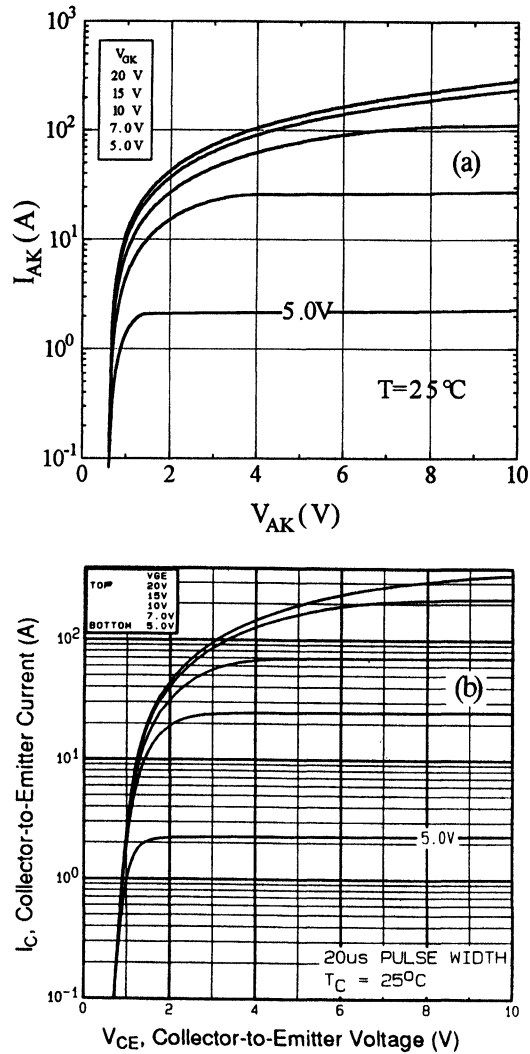
FIGURE 4   I–V characteristics obtained by simulation (a) and given in the data sheets (b) for an IRGBC40F.

The forward biased SOA voltage value measured for an IRGBC20S sample is ≈ 815 V, therefore, the BV parameter value is fixed in the SPICE program as 815.7 V. Figure 7 shows the I–V characteristics

TABLE I   Comparison of the switching times simulated and given in the data sheets for two IGBT devices: IRGBC20S and IRGBC40F

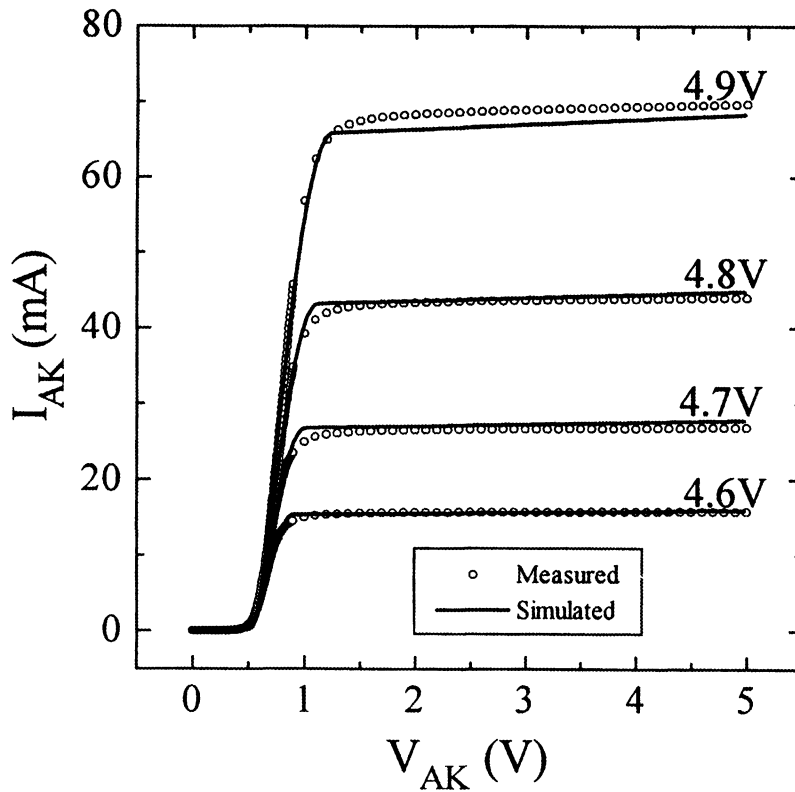|	IRGBC20S		IRGBC40F	
	Data sheets	Model	Data sheets	Model
Fall time t_f (ns)	1600	1425	420	414
Turn-off delay time t_{doff} (ns)	1200	1147	410	408
Turn-on delay time t_{don} (ns)	24	23	26	26
Rise time t_r (ns)	23	26	37	32

FIGURE 5   I−V characteristics obtained by simulation and by measurements for an IRGBC20S sample.
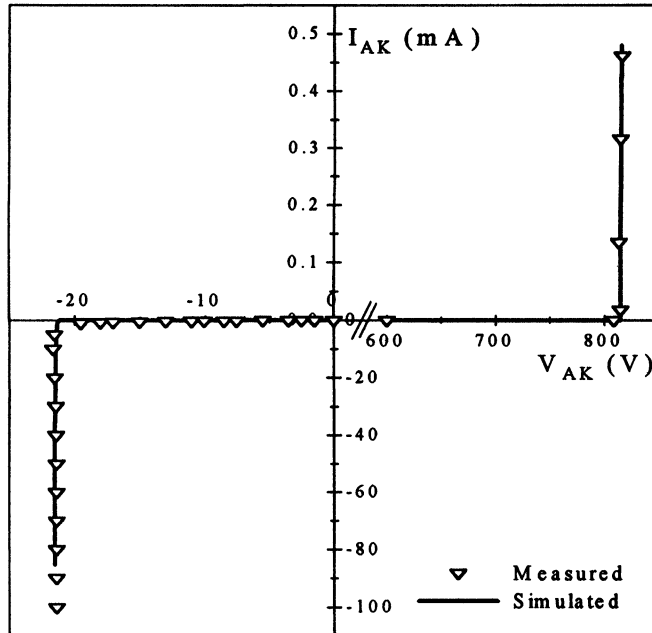
FIGURE 6   Simulated (a) and experimental (b) anode current and anode voltage waveforms for turn-off of the IRGBC20S.

simulated and measured showing the forward biased SOA of an IGBT.

For the same sample, the IGBT reverse biased SOA voltage value measured is $\approx 22\,$V, with a fixed supply voltage value V_{EC} as 20.6 V. The anode current *versus* anode–cathode voltage characteristics simulated and measured are shown in Figure 7. This is to demonstrate the ability of our model to simulate the reverse biased SOA of an IGBT.

Latch-up occurs when the voltage drop over the R_p resistor is larger than the built-in potential of the Base-Emitter junction of the parasitic n–p–n transistor. To illustrate the ability of our circuit model to simulate latch-up phenomena, arbitrarily values I_{AKlup} of the anode current have chosen as $I_{AKlup} = 19\,$A and 35 A for IRGBC20S and IRGBC40F respectively. The value of the R_p resistor is then adjusted so as to obtain a current latch-up value greater than or equal to I_{AKlup}. Figure 8 shows the simulated I–V characteristics for the two devices
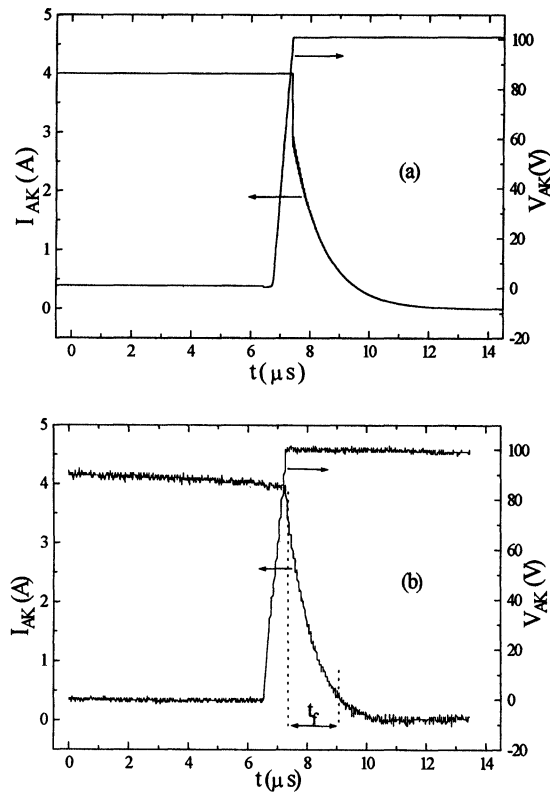
FIGURE 7   I–V characteristics simulated and measured showing the forward and reverse biased SOA of the IRGBC20S and IRGBC40F.

and the beginning of the latch-up. The R_p value is not used in Figures 3 and 4 simulations, these IR devices being latch-proof.

IV. CONCLUSION

In this paper, a simplified IGBT SPICE model has been described. This model is built from consideration of static and dynamic operating conditions. Although this model is simple, it is capable to simulate the operation of the IGBT and its different behaviors. This model presents two main advantages:

– an easier adaptation to any IGBT type, such as vertical or lateral, high or low power range. The model fitting is done by adjustment
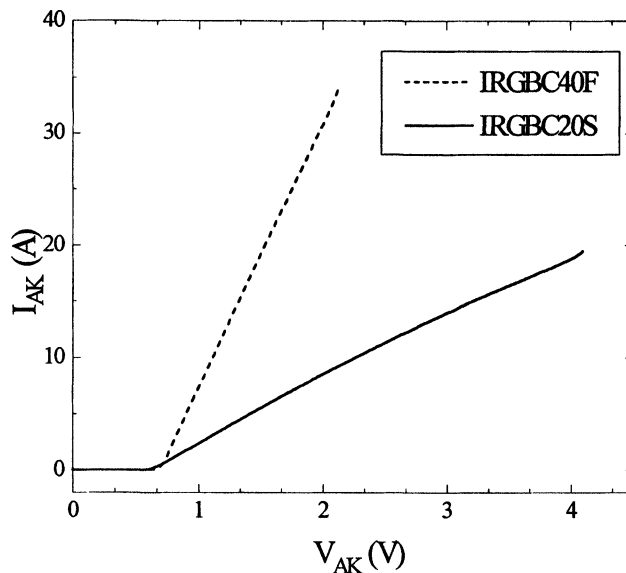
FIGURE 8   Simulated I–V characteristics showing the start of latch-up for the two IGBT devices for arbitrarily chosen current latch-up values.

of the macromodel component parameters, and their effects on the IGBT characteristics are identified and indexed to make the fitting easier.

— the possibility of implementation into all SPICE versions, because neither the access to the simulator code nor addition of equation are necessary.

The simulation results are confirmed by comparison with the experimental results and with manufacturer's data. The results are in perfect agreement.

References

[1] Baliga, B. J. (1984). "The Insulated Gate Transistor, a New Three-Terminal-MOS-Controlled Bipolar Power Device", *IEEE Trans. on Electron Devices*, **ED-31**, 1790–1828.
[2] Hefner, A. R. (1988). "An Analogycal Model for the Steady-state and Transistent of the Power IGBT", *Solid-State Electronic*, **31**(10), 1513.
[3] Silvaco International, SmartSpice/UTMOST III Modeling, User Manual, Santa Clara (1995).

[4] Mitter, C. S., Hefner, A. R., Chen, D. Y. and Lee, F. C. (1993). "Insulated Gate Bipolar Transistor (IGBT) Modeling using IG-SPICE", *IEEE Trans. on Industry Applications*, **30**(1), 24–33.

[5] Petrie, A. F. and Hymowitz, C. (1995). "A SPICE Model for IGBTs", *IEEE Applied Power Electronics Conference*, pp. 147–152.

[6] Shen, Z. and Chow, T. P. (1993). "Modeling and Characterisation of the Insulated Gate Bipolar Transistor (IGBT) for SPICE Simulation", *IEEE International Symposium on Power Semiconductor Devices and ICs*, pp. 165–170.

[7] Protiwa, F. F., Apeldoorn, O. and Groos, N. (1993). "New IGBT Model for PSPICE", *European Power Electronics Conference*, pp. 226–231.

[8] Elmazria, O., "Caractérisation et simulation de l'IGBT dans le but d'optimiser ses performances au Moyen de l'irradiation par électrons", *Doctorate Thesis*, Metz University, France, Nov. 1996, 120 pages.

[9] Charlot, J. J. and Pesic, I. (1994). "SPICE and User developed Modeling. Application: Implementation of an IGBT model in SmartSpice", Private Communication, Silvaco.

[10] Chung-Min Liu. and James B. Kuo. (1995). "Turn-off Transient Analysis of a Double Diffused Metal-Oxide-Semiconductor Device Considering Quasi Saturation", *J. Appl. Phys.*, **34**, Part 1, No. 2B, 869–873.