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Research Article

A Statistic-Based Calibration Method for TIADC System

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Time-interleaved technique is widely used to increase the sampling rate of analog-to-digital converter (ADC). However, the channel mismatches degrade the performance of time-interleaved ADC (TIADC). Therefore, a statistic-based calibration method for TIADC is proposed in this paper. The average value of sampling points is utilized to calculate offset error, and the summation of sampling points is used to calculate gain error. After offset and gain error are obtained, they are calibrated by offset and gain adjustment elements in ADC. Timing skew is calibrated by an iterative method. The product of sampling points of two adjacent subchannels is used as a metric for calibration. The proposed method is employed to calibrate mismatches in a four-channel 5 GS/s TIADC system. Simulation results show that the proposed method can estimate mismatches accurately in a wide frequency range. It is also proved that an accurate estimation can be obtained even if the signal noise ratio (SNR) of input signal is 20 dB. Furthermore, the results obtained from a real four-channel 5 GS/s TIADC system demonstrate the effectiveness of the proposed method. We can see that the spectra spurs due to mismatches have been effectively eliminated after calibration.

1. Introduction

In the past decades, modern electronic systems have been revolutionized with fast developing of digital signal processing techniques which offer unprecedented performance and adaptivity. However, the application of DSP is hindered by difficulty in capturing ultrafast signal in high speed electronic systems. The capturing of ultrafast electrical signals is a difficult problem that requires high speed analog-to-digital converters (ADCs). Because of the limitation of fabrication technology, maximum achievable sampling rate of single ADC is limited. Thus, time-interleaved technique proposed by Black and Hodges [1] that results in a time-interleaved ADC (TIADC) is widely used to increase sampling rate.

Ideally, TIADC is formed by M identical parallel ADCs (sub-ADC or channel). Each ADC should have the same gain and offset and should be operating at the equally displaced sampling time instants. However, due to fabrication dispersion, mismatch errors in TIADC system are inevitable. Channel mismatches, such as gain mismatch, offset mismatch, and timing skew mismatch, will result in distortion of sampled waveform and degrade the performance of TIADC. This has been proved in some contributing works [2–5].

A lot of methods have been proposed to calibrate the mismatches in TIADC [6–20]. Blind calibration techniques have been researched in [7–11]. The attractive advantage of blind calibration is that it does not require a dedicated calibration period. However, blind methods typically require a very high computational cost. In [12], a FFT-based gain and offset error calibration method is proposed, but as we know, many multipliers and other resources are needed in FFT (fast Fourier transform). An adaptive calibration method is proposed in [13], where a reference signal is introduced to identify mismatch parameters. In [14], a synthesis calibration method is proposed. This method can calibrate three mismatches simultaneously, but the calibration process is too complex, and it takes a long time for calibration. Some digital compensation methods for timing skew calibration, such as fractional delay filters [15], multichannel filters [16], Lagrange polynomial interpolation [17], and perfect reconstruction [18], are presented, but timing skew must be estimated before these methods are employed to compensate timing skew.

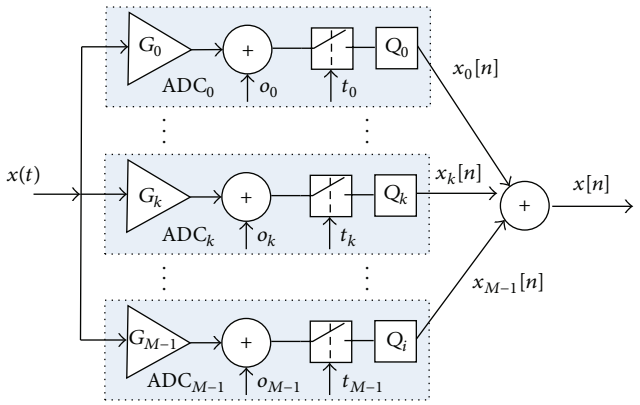

Figure 1: Mismatch model of TIADC system.

A code-density based timing skew detection method is proposed in [19], where an auxiliary circuit is added to detect timing skews. A timing skew calibration method based on zero-crossing is proposed in [20], where a zero-crossing detector is added for calibration.

A very easy calibration method is proposed in this paper. Compared with the previous methods, it has the following contributions. Firstly, this method can obtain gain and offset error accurately by simple addition operation. Secondly, the identification of timing skew is not required. This avoids the complicated measurement or estimation of timing skew. Finally, no auxiliary hardware circuits and filters are added for calibration. Thus, the implementation cost is reduced.

This paper is organized as follows. Section 2 gives the model and impact of TIADC mismatch. The calibration method is derived and explained in Section 3. In Section 4, the implementation of proposed calibration method is given. Section 5 shows the simulation results, and experiments results obtained from real four-channel 5 GS/s TIADC system are presented to validate the proposed method. Section 6 is dedicated to the conclusion of our work.

2. Model and Impact of TIADC Mismatch

In this section, to propose the calibration method, the mismatch model of TIADC is depicted first. Then, the output of sub-ADC is derived. Finally, the output spectrum of TIADC is also calculated to demonstrate the impact of TIADC mismatches.

As shown in Figure 1, a TIADC system consists of M parallel ADCs. Each ADC operates with a sampling frequency of f_s/M and samples the input in turn, so the TIADC system has a sampling frequency of f_s. For a nonideal TIADC, mismatches are inevitable, each ADC has different gain and offset, and the sampling time intervals between adjacent ADC are not equal. Therefore, in Figure 1, gain, offset, and sampling instant of ADC$_k$ are denoted by G_k, O_k, and t_k, respectively.

As we know, for an ideal TIADC, the sampling instant of ADC$_k$ is

$$t_k = (nM + k)\, T_s, \tag{1}$$

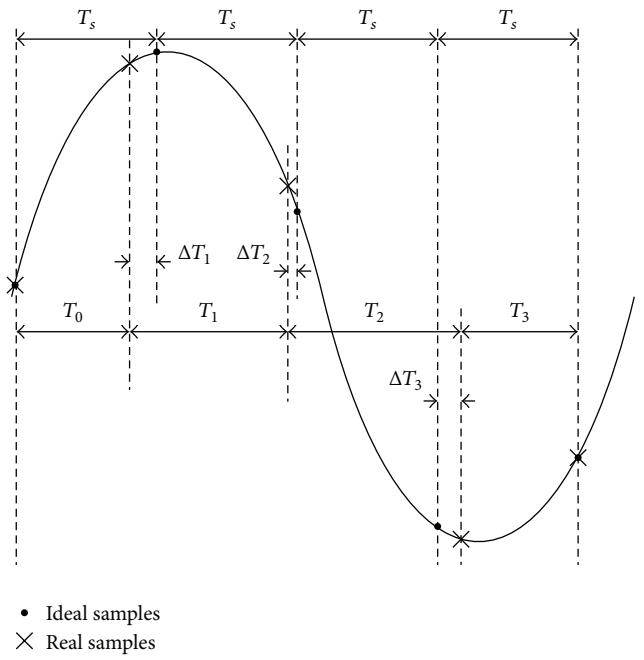

Figure 2: Timing skew in a four-channel TIADC.

where T_s refers to the sample period of TIADC system. Considering the relative timing skew Δt_k in ADC$_k$, sampling instant of ADC$_k$ can be denoted as

$$t_k = \left(nM + k + \Delta t_k\right) T_s. \tag{2}$$

Thus, for a sinusoidal $x(t)$, the output of TIADC will be

$$\begin{aligned} x_k[n] &= G_k \sin\left(2\pi f_{\text{in}} \left(nM + k + \Delta t_k\right) T_s + \phi\right) + O_k \\ &= G_k \sin\left(\omega_0 \left(nM + k + \Delta t_k\right) + \phi\right) + O_k, \end{aligned} \tag{3}$$

where f_{in} refers to input signal frequency and ω_0 refers to the normalized angular frequency. In the following part of this paper, we assume that $x(t)$ is a sinusoidal signal, and $x_k[n]$ shown in (3) will be utilized.

Figure 2 shows the timing skew in a four-channel TIADC. As shown in Figure 2, ΔT_k refers to the absolute timing skew of channel k and T_k refers to the sampling time interval between channel k and channel $k + 1$. These notations will be used in the following description.

According to the principle of TIADC, the sampling impulse of TIADC can be represented as

$$P(t) = \sum_{n=-\infty}^{\infty} \delta\left(t - kT_s - nMT_s\right). \tag{4}$$

Thus, considering mismatches in TIADC, the output signal of TIADC is

$$\begin{aligned} \widehat{x}(t) = &\sum_{k=0}^{M-1} \left(\Delta g_k x\left(t - \Delta T_k\right) + \Delta o_k\right) \\ &\times \sum_{n=-\infty}^{\infty} \delta\left(t - kT_s - nMT_s\right), \end{aligned} \tag{5}$$

where Δg_k and Δo_k refer to gain error and offset error, respectively. The Fourier transform of (4) is

$$P(j\Omega) = \frac{2\pi}{MT_s}\sum_{n=-\infty}^{\infty}\delta\left(\Omega - n\frac{2\pi}{MT_s}\right)e^{-jnk(2\pi/M)}, \quad (6)$$

and the Fourier transform of $x_k(t) = \Delta g_k x(t - \Delta T_k) + \Delta o_k$ gives

$$\widehat{X}_k(j\Omega) = \Delta g_k X(j\Omega)\, e^{j\Omega\Delta T_k} + \Delta o_k 2\pi\delta(\Omega); \quad (7)$$

thus, the Fourier transform of (5) can be calculated as

$$\begin{aligned}\widehat{X}(j\Omega) &= \sum_{k=0}^{M-1}\frac{1}{2\pi}\widehat{X}_k(j\Omega) * P(j\Omega)\\ &= \frac{1}{MT_s}\sum_{k=0}^{M-1}\sum_{n=-\infty}^{\infty}\left[\Delta g_k X\left(j\left(\Omega - n\frac{\Omega_s}{M}\right)\right)e^{j(\Omega - n(\Omega_s/M))\Delta T_k}\right.\\ &\qquad \left. + \Delta o_k 2\pi\delta\left(\Omega - n\frac{\Omega_s}{M}\right)\right]e^{-jnk(2\pi/M)},\end{aligned} \quad (8)$$

where $\Omega_s = 2\pi/T_s$. From (8), we can see that if offset error is not zero, spectrum spurs will appear at $n\Omega_s/M$. For a sinusoidal $x(t)$ whose angular frequency is Ω_0, spectrum spurs due to gain and timing skew will appear at $n\Omega_s/M \pm \Omega_0$. What is more, amplitudes of spectrum spurs due to gain error are only relative to the value of gain error, while the amplitudes of spurious peaks introduced by timing skew are determined by both the value of timing skew and the input frequency.

3. Statistic-Based Calibration Method for TIADC

In this section, offset, gain, and timing mismatch calibration methods are introduced separately.

3.1. Offset Mismatch Calibration. Assuming that infinite sampled points of $x_k[n]$ are obtained, it is easy to see from (3) that the average value of these points is

$$E[x_k[n]] = O_k. \quad (9)$$

Considering N sampling points are obtained, the average value of these points can be written as

$$E_N[x_k[n]] = \frac{1}{N}\sum_{n=0}^{N-1}\left(G_k \sin(\omega_0(nM + k + \Delta t_k) + \phi) + O_k\right). \quad (10)$$

When N is large enough, $E_N[x_k[n]]$ approaches $E[x_k[n]]$; thus,

$$E_N[x_k[n]] = O_k. \quad (11)$$

From (11), we can know that the offset of each ADC can be obtained by calculating the average value of sampling points. In general, one chooses channel 0 as a reference and then matches all other channels to this reference channel. Therefore, offset mismatch can be calculated as

$$\begin{aligned}\Delta o_k &= E_N[x_k[n]] - E_N[x_0[n]]\\ &= \frac{1}{N}\sum_{n=0}^{N-1}x_k[n] - \frac{1}{N}\sum_{n=0}^{N-1}x_0[n].\end{aligned} \quad (12)$$

3.2. Gain Mismatch Calibration. For convenience, a simple sinusoidal signal $A \times \sin(t)$ is used in the following derivations. Supposing that the analog signal $A \times \sin(t)$ is sampled with a sampling period T_s, the sampling points will be $A \times \sin(nT_s)$ ($n = 0, 1, 2, \ldots$). Let us assume that N_h sampling points are obtained in a half cycle of the sinusoidal signal; thus,

$$N_h = \frac{\pi}{T_s}. \quad (13)$$

The summation of these N_h sampling points can be written as

$$\sum_{n=0}^{N_h-1}A \times \sin[nT_s] = A \times \frac{N_h}{\pi}\sum_{n=0}^{N_h-1}\sin[nT_s] \times \frac{\pi}{N_h}. \quad (14)$$

When N_h is very large, π/N_h approaches zero. For this case, according to the definition of integral, the summation can be changed to integral. Therefore, we have

$$\sum_{n=0}^{N_h-1}\sin[nT_s] \times \frac{\pi}{N_h} = \int_0^{\pi}\sin(x)\,dx = 2. \quad (15)$$

Finally, from (13)–(15), we can get

$$\sum_{n=0}^{N_h-1}A \times \sin[nT_s] = \frac{2A}{T_s}. \quad (16)$$

Furthermore, for N_t sampling points which include one cycle of the sinusoidal signal, it can be obtained that

$$S_t = \sum_{n=0}^{N_t-1}\left|A \times \sin[nT_s]\right| = 2 \times \sum_{n=0}^{N_h-1}A \times \sin[nT_s] = \frac{4A}{T_s}, \quad (17)$$

where $|\cdot|$ represents the absolute value. It is clear that the initial phase of the sinusoidal signal does not affect S_t. Therefore, from (3) and (17), it gives that

$$S_k = \sum_{n=0}^{N-1}\left|x_k[n] - O_k\right| = \frac{4G_k}{M\omega_0} \times \frac{N}{N_t}, \quad (18)$$

where O_k is calculated as (11). From (18), it can be seen that the gain is relative to S_k. Without loss of generality, we choose channel 0 as a reference; thus, the gain error can be calculated as

$$\Delta g_k = \frac{S_k}{S_0} = \frac{\sum_{n=0}^{N-1}\left|x_k[n] - O_k\right|}{\sum_{n=0}^{N-1}\left|x_0[n] - O_0\right|}. \quad (19)$$

It is noted that the premise of (15) is that N_h is large enough. Considering that the frequency of input signal is f_{in} and the TIADC system has a sampling frequency of f_s and M channels, for one subchannel we can obtain that

$$N_h = \frac{f_s}{2Mf_{\text{in}}}. \tag{20}$$

Thus, to make N_h large enough, the sampling rate should be much larger than signal frequency. However, if N/N_h is large enough, the sampling points will cover many cycles of the signal. Assuming

$$f_{\text{in}} \neq \frac{f_s}{Mn} \quad n = 1, 2, 3, \ldots, \tag{21}$$

the sampling points obtained in different cycles will be different. Then, as random equivalent sampling, we can use the sampling points obtained from different cycles to reconstruct one cycle of the input signal. Therefore, as long as N/N_h is large enough and (21) is satisfied, the gain error can be estimated accurately by (19).

3.3. Timing Mismatch Calibration. After offset and gain mismatches are calibrated, we can assume that $O_k = 0$ for any k, and the gain of each channel is G. Under this assumption, the product of two adjacent channels can be written as

$$\begin{aligned} C_{k,k+1}(n) &= x_k[n] \cdot x_{k+1}[n] \\ &= G\sin\left(\omega_0\left(nM + k + \Delta t_k\right) + \phi\right) \\ &\quad \cdot G\sin\left(\omega_0\left(nM + k + 1 + \Delta t_{k+1}\right) + \phi\right). \end{aligned} \tag{22}$$

By using the product-to-sum formula, (22) is changed to

$$\begin{aligned} C_{k,k+1}(n) &= \frac{1}{2}G^2\cos\left(\omega_0\left(1 + \Delta t_{k+1} - \Delta t_k\right)\right) \\ &\quad - \frac{1}{2}G^2\cos\left(\omega_0\left(2nM + 2k + 1 + \Delta t_k + \Delta t_{k+1}\right) + 2\phi\right). \end{aligned} \tag{23}$$

When sampling point number approaches infinity, the average value of the second part of (23) will be zero. Therefore, the average value of $C_{k,k+1}(n)$ is

$$E\left[C_{k,k+1}(n)\right] = \frac{1}{2}G^2\cos\left(\omega_0\left(1 + \Delta t_{k+1} - \Delta t_k\right)\right). \tag{24}$$

If there is no timing skew in all channels, for any k ($0 \leq k \leq M-1$), $E[C_{k,k+1}(n)]$ will be $(1/2)G^2\cos\omega_0$. According to the Nyquist criterion, the range of ω_0 is $[0, \pi]$. In this range, cosine is a monotone decreasing function. Thus, if $E[C_{k,k+1}(n)]$ is larger than $(1/2)G^2\cos\omega_0$, it implies that the sampling interval between channel k and channel $k+1$ is smaller than standard value T_s. Conversely, it means that the sampling interval is larger than T_s. Therefore, $E[C_{k,k+1}(n)]$ can be used as a metric to calibrate timing skew.

Assuming that N sampling points are used to calculate $E[C_{k,k+1}(n)]$, the estimated value of $E[C_{k,k+1}(n)]$ is

$$E_N\left[C_{k,k+1}(n)\right] = \frac{1}{2}G^2\cos\left(\omega_0\left(1 + \Delta t_{k+1} - \Delta t_k\right)\right) + R_{k,k+1}, \tag{25}$$

where

$$R_{k,k+1} = \frac{G^2}{2N}\sum_{n=0}^{N-1}\cos\left(\omega_0\left(2nM + 2k + 1 + \Delta t_k + \Delta t_{k+1}\right) + 2\phi\right). \tag{26}$$

In order to get an accurate estimation value of $E[C_{k,k+1}(n)]$, suitable N and ω_0 are needed to make $R_{k,k+1}$ approach zero. Firstly, N must be large enough. Secondly, when the angular frequency of $\cos(\omega_0(2nM + 2k + 1 + \Delta t_k + \Delta t_{k+1}) + 2\phi)$ is $2n\pi$ ($n = 1, 2, 3, \ldots$), $R_{k,k+1}$ will not approach zero. Thus,

$$\omega_0 \neq \frac{n\pi}{M} \quad (n = 1, 2, 3, \ldots). \tag{27}$$

As mentioned above, $E_N[C_{k,k+1}(n)]$ is utilized to calibrate timing skew. When there is no timing skew, the reference value of $E_N[C_{k,k+1}(n)]$ is $(1/2)G^2\cos\omega_0$. However, it is not easy to get G accurately, so we cannot calibrate timing skew simply by adjusting Δt_k and Δt_{k+1} to make $E[C_{k,k+1}(n)]$ approach $(1/2)G^2\cos\omega_0$. An iterative method is proposed here.

First, $E_N[C_{k,k+1}(n)]$ for each k are calculated as

$$E_N\left[C_{k,k+1}(n)\right] = \frac{1}{N}\sum_{k=0}^{N-1}x_k[n]\,x_{k+1}[n]. \tag{28}$$

Then, Δt_k is adjusted to make $E_N[C_{k,k+1}(n)]$ ($k = 1, 2, \ldots, M-2$) be equal to $E_N[C_{0,1}(n)]$. Δt_k is adjusted as

$$\Delta t_k^{(m+1)} = \Delta t_k^{(m)} + d \times \Delta u, \tag{29}$$

where $\Delta t_k^{(i)}$ represents the residual timing skew of channel k after i times iteration, Δu refers to the adjustment step, and d refers to the adjustment direction. If $E_N[C_{k,k+1}(n)]$ is larger than $E_N[C_{0,1}(n)]$, d is +1; otherwise, d is −1. Δu is decided by the adjustment method of timing skew. There are two methods to adjust Δt_k. One method is adjusting the sampling clock of channel k directly. This method needs digital control delay element (DCDE) in ADC or clock generation circuit. The other method is making use of fraction delay filters [15]. After this step, all T_k except T_{M-1} are equal. What is more, when $E_N[C_{k,k+1}(n)]$ is equal to $E_N[C_{0,1}(n)]$, it is obtained from (24) that

$$\Delta t_{k+1} - \Delta t_k = \Delta t_1 - \Delta t_0. \tag{30}$$

By substituting $\Delta t_0 = 0$ into (30) and after some recursive derivations, we can get

$$\Delta t_k = k \times \Delta t_1. \tag{31}$$

Furthermore, Δt_k is adjusted to make T_{M-1} be equal to other T_k. It is clear that Δt_{M-1} should be adjusted. However,

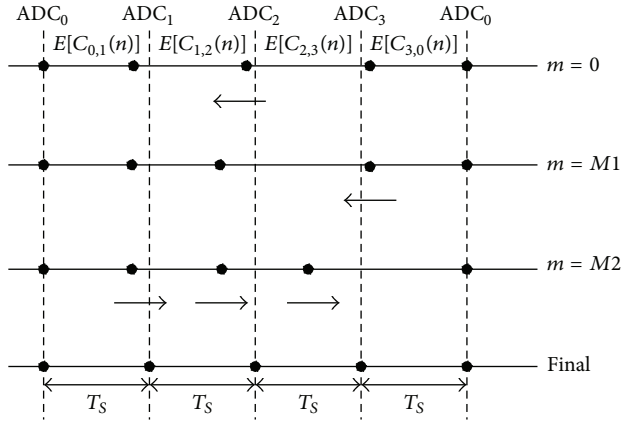

Figure 3: Illustration of calibration process in a four-channel TIADC.

once Δt_{M-1} is modified, not only T_{M-1} but also T_{M-2} is changed. Therefore, considering the residual timing skew shown in (31), to keep all T_k except T_{M-1} equal in this calibration step, each Δt_k is adjusted as

$$\Delta t_k^{(m+1)} = \Delta t_k^{(m)} + k \times d \times \Delta u. \tag{32}$$

If $E_N[C_{M-1,0}(n)]$ is larger than other $E_N[C_{k,k+1}(n)]$, it means that T_{M-1} is smaller than other T_k; thus, Δt_{M-1} should be decreased to increase T_{M-1} and d is −1. Conversely, T_{M-1} should be decreased, and Δt_{M-1} should be increased and d is +1. When all $E_N[C_{k,k+1}(n)]$ $(k = 0, 1, \ldots, M-1)$ have the same value, the calibration is finished.

The calibration process of four-channel TIADC can be shown as in Figure 3. At the beginning of calibration, it is assumed that the timing skews are [0, −0.02, −0.01, 0.01]. Because $E[C_{1,2}(n)]$ is smaller than $E[C_{0,1}(n)]$, Δt_2 is decreased. After $M1$ iterations, $E[C_{0,1}(n)]$ and $E[C_{1,2}(n)]$ are equal, and the timing skews are [0, −0.01, −0.02, 0.01]. Then, Δt_3 is also decreased since $E[C_{2,3}(n)]$ is smaller than $E[C_{0,1}(n)]$. After $M2$ iterations, $E[C_{2,3}(n)]$ and $E[C_{0,1}(n)]$ are equal, and the timing skews are [0, −0.01, −0.02, −0.03]. Finally, $E[C_{0,1}(n)]$ and $E[C_{3,0}(n)]$ are compared. Because $E[C_{0,1}(n)]$ is larger than $E[C_{3,0}(n)]$, Δt_1 is increased by Δu. To keep $E[C_{1,2}(n)]$ and $E[C_{2,3}(n)]$ be equal to $E[C_{0,1}(n)]$, Δt_2 and Δt_3 are increased by $2 \times \Delta u$ and $3 \times \Delta u$, respectively. When $E[C_{0,1}(n)]$ and $E[C_{3,0}(n)]$ are equal, the iteration is stopped and the calibration finishes.

4. Implementation

The proposed calibration method is implemented in a 5 GS/s TIADC-based data acquisition system (DAS), whose diagram is shown in Figure 4. The whole system is composed of front end circuits of ADC, clock generation circuits which include crystal and phase locked loop (PLL), ADC, field programmable gate array (FPGA), and digital signal processor (DSP). FPGA is employed for sampled data receiving and storage. In FPGA, the sampled data from ADC are received by input double data rate (IDDR) elements firstly. Then, the sampled data are stored in FIFO (fist in fist out) which is built by memory in FPGA. At last, the sampled data are transmitted to DSP. Because the calculation speed of FPGA is faster than DSP, the addition and multiplication operation needed for calibration are also implemented in FPGA. DSP48E elements in Xilinx FPGA are utilized to implement addition and multiplication operation. The whole system is controlled by DSP.

The part number of 5 GS/s ADC is EV8AQ160, which consists of four 1.25 GS/s ADC cores. The simplified block diagram of this ADC is also shown in Figure 4. It can be seen that there are offset, gain, and phase adjustment elements in ADC. These adjustment elements are controlled by digital control word (DCW), which is sent from FPGA by serial peripheral interface (SPI). The adjustment steps of offset, gain, and phase are 0.2 LSB, 0.14%, and 110 fs, respectively.

The calibration process is conducted as follows.

First, the average value of sampled data of each channel is calculated, and offset error is obtained by (12). After the offset error is obtained, it is corrected by sending DCW to offset adjustment element. The DCW is calculated as

$$\mathrm{DCW}_{\mathrm{offset}}^{N} = \mathrm{DCW}_{\mathrm{offset}}^{O} - \frac{\Delta o_k}{0.2}, \tag{33}$$

where the superscripts N and O refer to new DCW and original DCW, respectively.

Secondly, (19) is utilized to obtain gain error. Gain error is corrected by gain adjustment element, whose DCW is calculated as

$$\mathrm{DCW}_{\mathrm{gain}}^{N} = \mathrm{DCW}_{\mathrm{gain}}^{O} + \frac{1 - \Delta g_k}{0.14\%}. \tag{34}$$

Finally, timing skew is calibrated. Phase adjustment element is used to adjust timing skew in the process of iteration. The calibration of timing skew has been discussed in Section 3. Timing skew is adjusted by phase adjustment element, and the adjustment step is 110 fs. When all $E[C_{k,k+1}(n)]$ are equal, the calibration is finished.

5. Experimental Results

5.1. Simulation. A four-channel 5 GS/s TIADC system is simulated to present the performance of proposed method in the following part of this section. Zero-mean Gaussian white noise is added to each channel. The offset, gain, and timing skew errors are set as $\Delta o_{0,1,2,3} = [0, 0.5, 1.6, -2.2]$, $\Delta g_{0,1,2,3} = [1, 1.06, 1.13, 0.91]$, and $\Delta t_{0,1,2,3} = [0, 0.02, 0.03, -0.03]$, respectively. The number of sampling points used for calibration mismatches is selected to be 20000.

First, two experiments are carried out to demonstrate the estimation accuracy of offset and gain error. One experiment is to evaluate the impact of noise on the estimation accuracy of the proposed method. The signal frequency is set to 600 MHz. As shown in Figures 5 and 6, the proposed method can estimate offset and gain error accurately in a wide SNR range from 20 dB to 60 dB. The other experiment aims at evaluating the impact of signal frequency on the estimation accuracy of the proposed method. The SNR is set to 45 dB. From Figures 7 and 8, it is shown that the proposed method has high

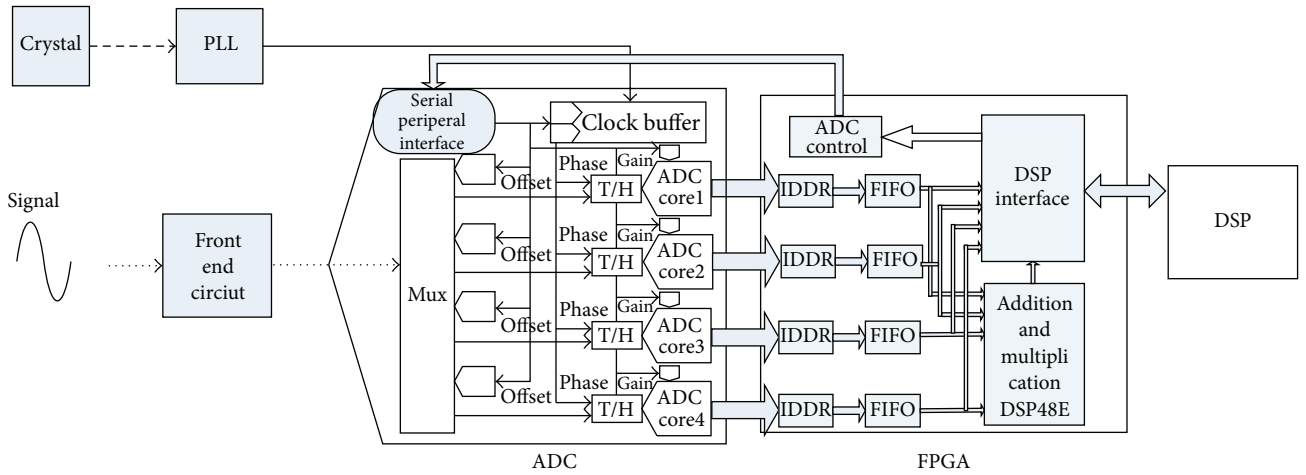

Figure 4: Diagram of 5 GS/s TIADC-based data acquisition system.

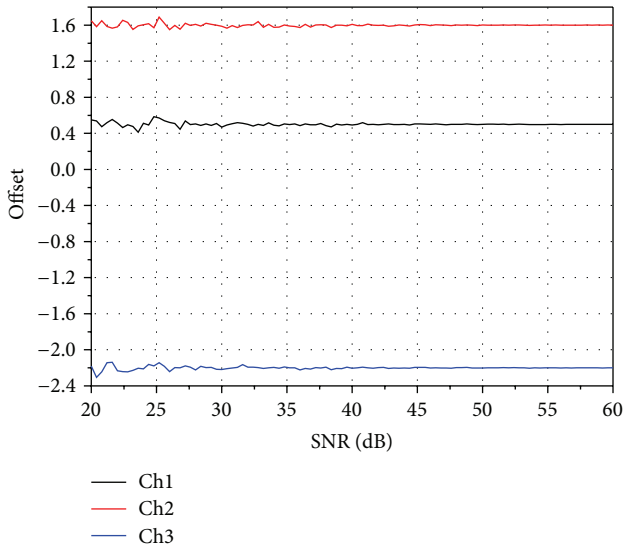

Figure 5: Estimated offset error versus SNR.

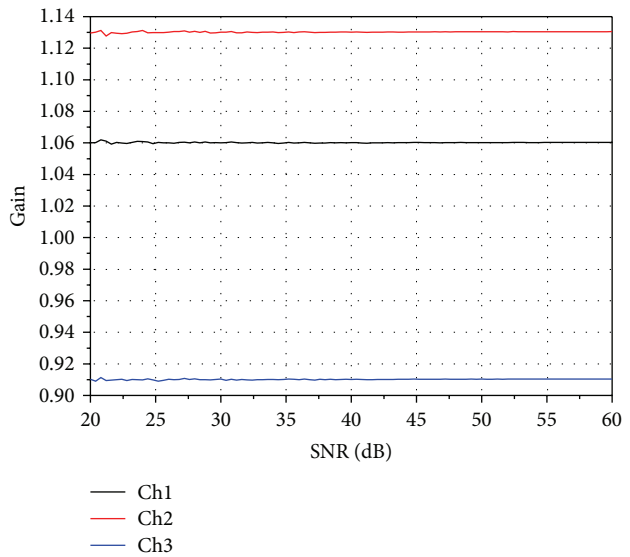

Figure 6: Estimated gain error versus SNR.

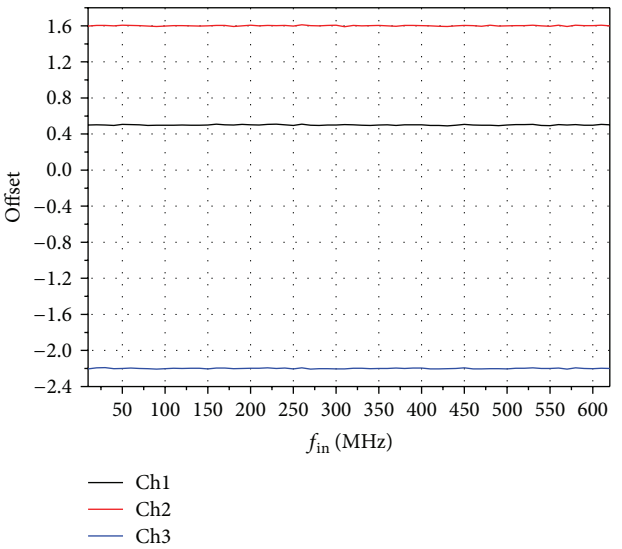

Figure 7: Estimated offset error versus signal frequency.

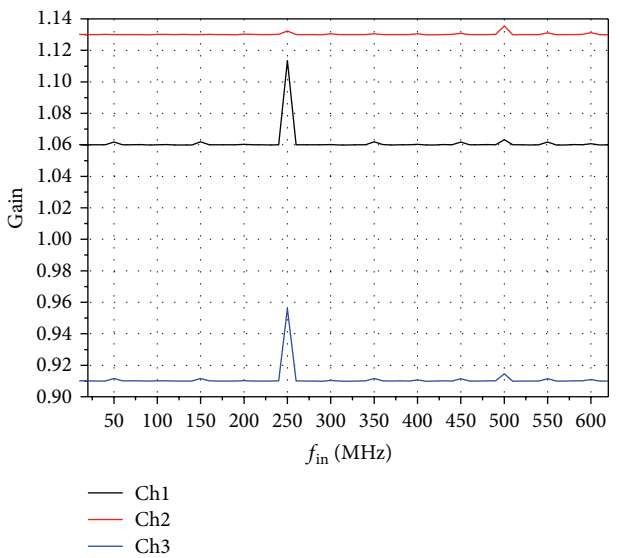

Figure 8: Estimated gain error versus signal frequency.

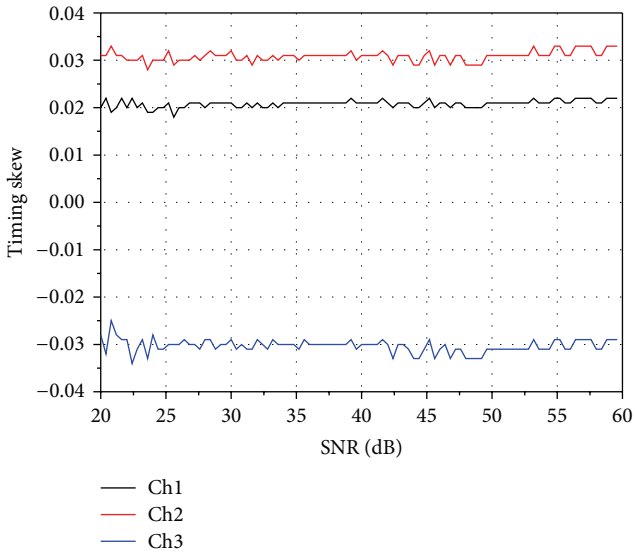

Figure 9: Estimated timing skew versus SNR.

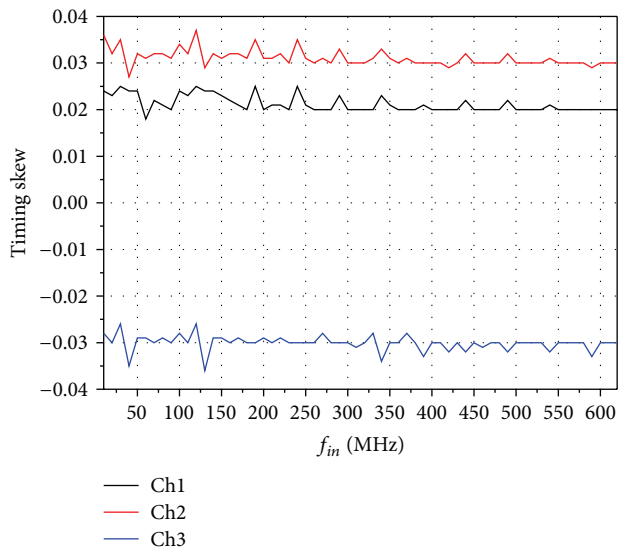

Figure 10: Estimated timing skew versus signal frequency.

estimate accuracy in a wide frequency range from 10 MHz to 620 MHz except for some special frequencies shown in (21). It should be noted that Figures 5 to 10 are obtained by some discrete points. In Figures 5, 6, and 9, the step of SNR is 0.4 dB. The step of frequency in Figures 7, 8, and 10 is 10 MHz.

Secondly, the performance of timing skew calibration is demonstrated. Although timing skew is calibrated directly without estimation, after the calibration is finished, the estimated timing skew $\Delta\widehat{t}_k$ can be calculated as

$$\Delta\widehat{t}_k = \Delta t_k^{(P)} + \Delta t_k^{(0)}, \tag{35}$$

where P refers to the iteration times when calibration is finished. We calibrate timing skew after offset and gain errors are corrected by the proposed method. As offset and gain error, the impacts of SNR and signal frequency on calibration

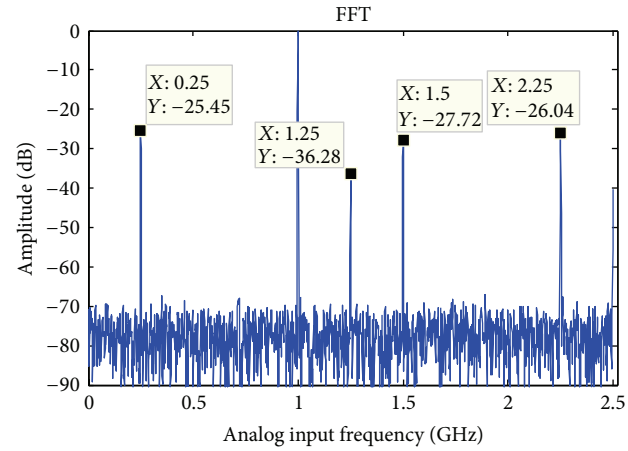

Figure 11: The spectrum of TIADC output without calibration.

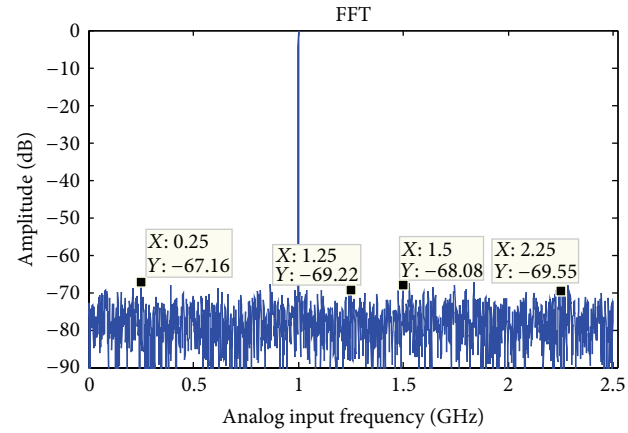

Figure 12: The spectrum of TIADC output with calibration.

performance are researched, respectively. The estimated timing skews versus SNR and signal frequency are shown in Figures 9 and 10, respectively. From Figure 9, where the signal frequency is set to 600 MHz, it can be seen that $\Delta\widehat{t}_k$ is very close to real timing skew Δt_k in a wide SNR range from 20 dB to 60 dB. Thus, it is concluded that the proposed method can calibrate timing skew accurately in a wide SNR range. Similarly, it is seen from Figure 10 that timing skew can be calibrated with different signal frequency. It should be noted that the proposed method does not work well at some frequencies as shown in (27). Because Figure 10 is obtained by discrete points with a step of 10 MHz, these frequencies are not shown.

Finally, the spectra before and after calibration are shown in Figures 11 and 12. It is shown that after calibration, the spectrum spurs due to mismatches are degraded greatly. This proves the good performance of the proposed method.

5.2. Testing Result of 5 GS/s TIADC System. In this part, the experiment results got from a real 5 GS/s TIADC system, whose diagram is shown in Figure 4, are shown to demonstrate the effectiveness of the proposed calibration method. Figure 13 shows the experiment board of 5 GS/s TIADC. The

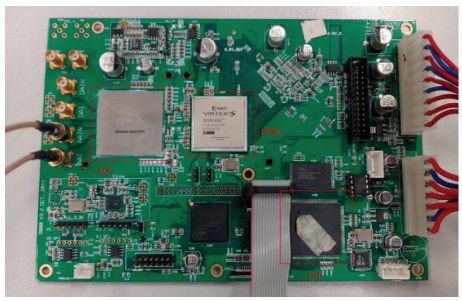

Figure 13: Experiment board of 5 GS/s TIADC.

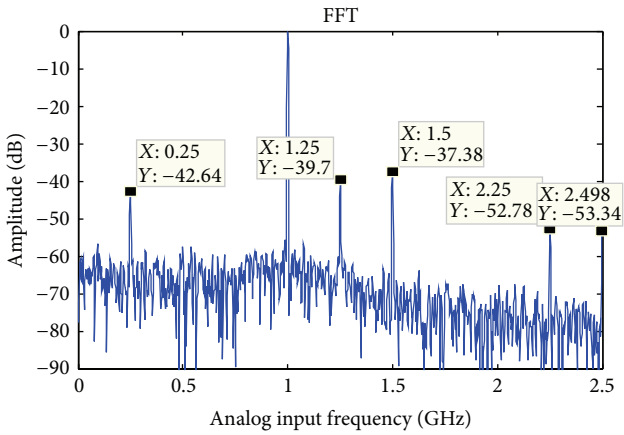

Figure 14: The spectrum of real 5 GS/s TIADC output before calibration.

proposed method is implemented in this system. The main chips which include ADC, FPGA, and DSP are marked in Figure 13. The signal is input by a pair of SMA (Sub-Miniature-A) connectors and then sampled by ADC. The main function of FPGA is sampled data storage. All sampled data are stored in FIFO built by Block RAM (random access memory) of FPGA. In addition, as mentioned in Section 4, the proposed calibration method is also implemented in FPGA. The main function of DSP is system control. ADC and IDDR modules shown in Figure 4 are all controlled by DSP. Moreover, when the FIFO in FPGA is full, the sampled data are transmitted to DSP for analysis.

Since the real mismatches in the system are unknown, the spectra before and after calibration are utilized to prove the effectiveness of the proposed method. From the comparison of Figures 14 and 15, we can clearly see that the spectrum spurs due to the mismatches have been effectively eliminated. These experimental results prove that the proposed method works very well in real system.

6. Conclusion

The mismatches in TIADC degrade the performance of the system. In particular, in high speed TIADC system, small mismatches will introduce big spectrum spurs. A new calibration method is proposed for a four-channel 5 GS/s TIADC in this paper. It can calibrate mismatches accurately with different SNR and signal frequency. This method can be easily realized in a real system with low cost. It especially suits high speed digital storage oscilloscope and other systems where TIADC-based high speed data acquisition is used.

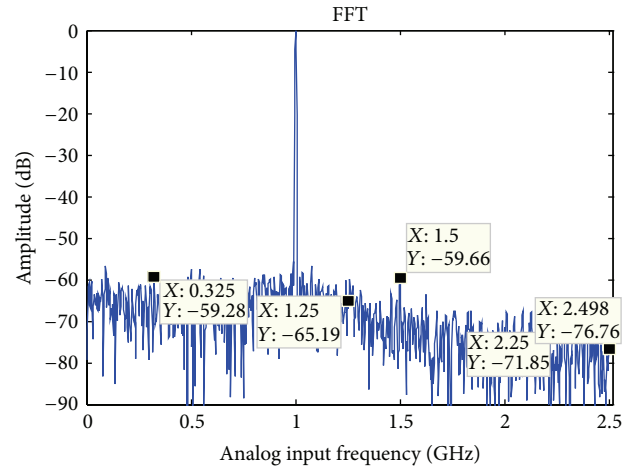

Figure 15: The spectrum of real 5 GS/s TIADC output after calibration.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

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