Hindawi Publishing Corporation
Journal of Nanomaterials
Volume 2013, Article ID 702094, 7 pages
http://dx.doi.org/10.1155/2013/702094

*Research Article*

# Multifunctional Logic Gate by Means of Nanodot Array with Different Arrangements

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Received 8 November 2012; Revised 11 February 2013; Accepted 12 February 2013

Academic Editor: Sung Oh Cho



Multifunctional logic gate devices consisting of a nanodot array are studied from the viewpoint of single electronics. In a nanodot array, the dots come in a random variety of sizes, which sometimes has a negative effect on the performance of electrical device applications. Here, this feature is used in a positive sense to achieve higher functionality in the form of flexible logic gates with low power consumption in which the variability of logic functions is guaranteed. Nanodot arrays with two input gates and one control gate in a variety of arrangements are considered, in which the two-input logic functions (such as NAND, NOR, or exclusive-OR (XOR) gates) are selected by changing the voltage applied to the control gate. To ensure the flexibility of the device, it is important to guarantee the performance with any one of the six important logic functions: NAND, AND, NOR, OR, XOR, and XNOR. We ran a selection simulation using a nanodot array consisting of six nanodots with different dot arrangements to clarify the relation between the variability of the logic functions and the dot arrangements.

## 1. Introduction

Single-electron devices (SEDs) are an attractive alternative for future large-scale integrated (LSI) circuits because of their small size and very low power consumption [1–6]. However, the dot sizes of room-temperature-operating SEDs are too small to control them accurately. To overcome this problem, we proposed the use of nanodot-array-type SEDs consisting of many nanodots connected via tunnel junctions [7]. The dot-size fluctuation is positively used to achieve a flexible logic gate in which the logic function of the device can be selected by setting the voltage applied to control gates. Our final objective is to achieve a reconfigurable logic device with very low power consumption.

Miniaturization is a problem that also affects metal-oxide-semiconductor (MOS) field-effect transistors (FETs) because it is difficult to suppress the fluctuation of their sizes, when the size is less than 10 nm [8, 9]. Although small MOSFETs in LSI circuits are capable of providing high-performance features such as high current drivability, the size fluctuation results in electrical characteristics that are fairly unpredictable. Even in CMOS LSIs, we have to introduce some tolerant operations. Another problem with highly integrated CMOS LSIs is their huge power dissipation [10]. SEDs enjoy a great advantage in this regard, even though their current drivability is quite low compared with the MOSFETs. However, nanodot arrays circumvent this disadvantage because the dots are directly connected to one another and do not have any wires to charge.

The simplest SED is a single-electron transistor (SET) that has only one dot. Its most unique characteristic is conductance oscillation as a function of the gate voltage, in which the oscillation period is determined by the capacitance between the dot and the gate. When many dots with different sizes are connected in one array, complicated characteristics seem to occur because many dots having a different oscillatory conductance with different periods and phases are connected in parallel and in series. Here, the fluctuation of the dot size can be used positively. Another important feature of SEDs is their multiple-gate capability, since the operation principle of SEDs enables them to inherently have many input gates [11]. When the nanodots and the gates are small and are arranged as shown in Figure 1, each gate couples with many nanodots capacitively. If we use one of the gates as a control gate,

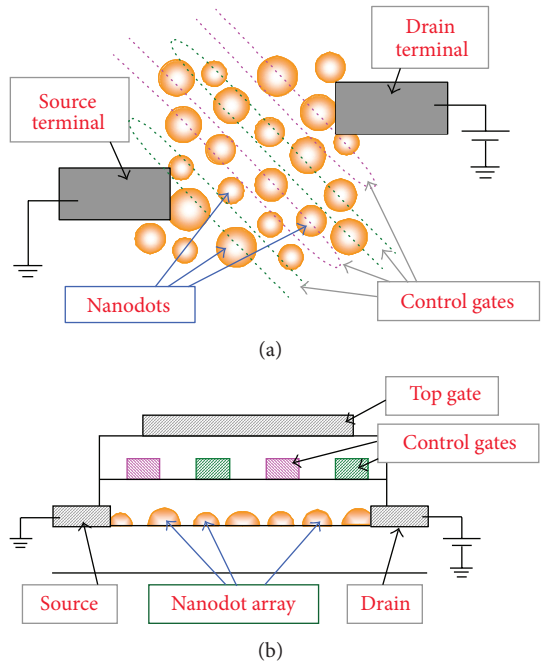


Figure 1: (a) Schematic top view of a nanodot-array flexible-logic-gate device with many input gates and (b) cross section of the nanodot-array device.

the conductance oscillation of each dot shifts in accordance with each capacitance between the gate and each dot. This means that the total conductance of the array can be changed so as to select the function of the device by the voltages applied to the control gates. It thus works as a multifunctional device in which the functions can be selected by the control-gate voltage.

The biggest problem of this concept is that several sets of suitable control-gate voltage have to be found out corresponding to the expected logic functions because we cannot predict the actual characteristics of nanodot arrays. However, if the nanodots are fabricated with a size close to the designed size, current oscillations in which the periods and phases are slightly distributed are achieved as a function of the input- and control-gate voltages. Since the oscillation period and phase change in accordance with the input- and control-gate voltages, a control-gate voltage can be identified so as to produce a required logic function. After the specific control-gate voltage is identified, it should be stored into nonvolatile memory. Then, another control gate voltage for another logic function should be identified and stored. Once several series of control-gate voltages corresponding to various logic functions are identified and stored, the device can be used as a multifunctional device with functions selected by using the stored control-gate voltages.

The simplest logic gate is a two-input logic gate such as NAND, NOR, or exclusive-OR (XOR) gates. When a flexible two-input logic gate is considered, the logic function should be flexibly changed by the voltage applied to the control gates. Three gates are needed at least to realize such devices: two for input and one for control. The most important point is for the device to achieve as many logic functions as possible by changing the control-gate voltage. The variability of the function is thought to be strongly affected by the arrangement of nanodots because current transport paths play an important role in deciding the electrical characteristics of the device. In this paper, we assume the most simple nanodot arrays considering the fabrication of the array by the use of the established method and the use of conventional silicon technologies named pattern-dependent oxidation (PADOX) [12, 13]. The PADOX method converts a lattice of Si nanowires to an Si nanodot array, where the nanodots are arranged in vertical and horizontal directions, which provide parallel and series paths of current flow [11, 12]. To design the nanodot array, it is important to know which current path is more crucial. In this paper, the effect of nanodot arrangement on the functionality of a flexible two-input logic gate is investigated.

## 2. Nanodot-Array Device Structure and Simulation

Nanodot arrays typically have a variety of different dot arrangements. The most important point of any flexible device is accuracy in achieving the target function. Fluctuations of dot size and position, which are inevitable in nanodot array devices, cause fluctuations in tunnel resistances and in tunnel capacitances between dots and in gate capacitances between dots and gates. It is impossible to predict what the electrical characteristics will be, which makes it difficult to guarantee the functionality of the device. However, we propose using these fluctuations in a positive way to achieve a highly flexible device.

Here, a two-input, two-terminal logic device, in which output current or resistance between source and drain terminals, is changed by changing the combination of voltages applied to the two-input gates is considered. The device acts as a conventional two-input logic gate (such as a NAND, NOR, or XOR gate). One control gate to select the logic function of the device is attached. When the voltage applied to the control gate is changed, the logic function can be changed, for example, from NAND to XOR, and then to NOR [7, 12].

The electrical characteristics of the nanodot-array devices are calculated with different dot arrangements. When six-dot arrays are assumed, four kinds of dot arrangement can be typically made, as shown in Figures 2(a)–2(d). Here, we use nanodot arrangements assuming the fabrication by the PADOX method [11, 12]. The two reserves, the source and drain terminal, were attached to the dot array. These four dot arrangements are named series, $2 \times 3$, $3 \times 2$, and parallel. Every dot in the array is connected via a tunnel capacitor to the neighboring dots and source or drain terminal. As an example, Figure 3(a) shows the equivalent circuit of a $2 \times 3$ dot array connected with tunnel capacitors. In addition, three gates that couple capacitively to all the dots are also attached as shown in Figure 3(b). Note that the structure in which every gate couples to all the dots is effective in terms of achieving the most important two-input logic functions (AND, OR, NAND, NOR, XOR, and XNOR). One reason for this is that these important logic functions are symmetric: the output is the same between the two input combinations

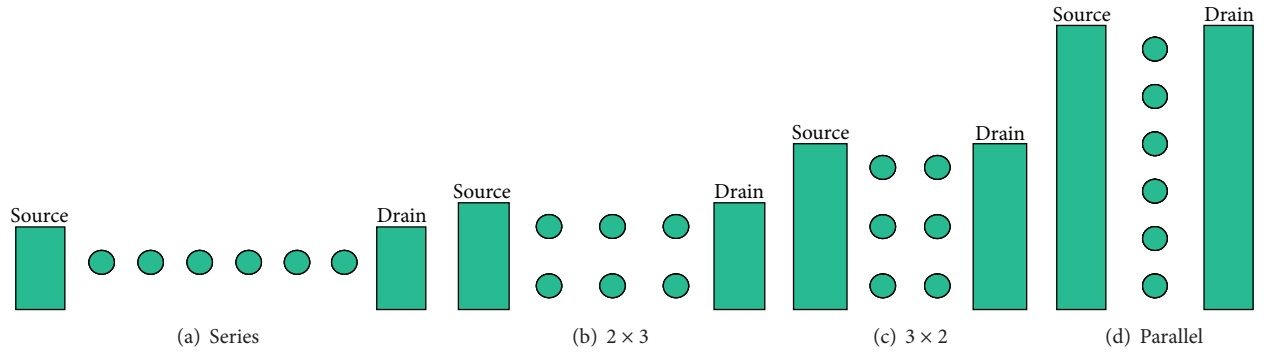


FIGURE 2: Four types of dot arrangement of an array consisting of six nanodots sandwiched by the source and drain electrode. (a) Series, (b) 2 × 3, (c) 3 × 2, and (d) parallel.

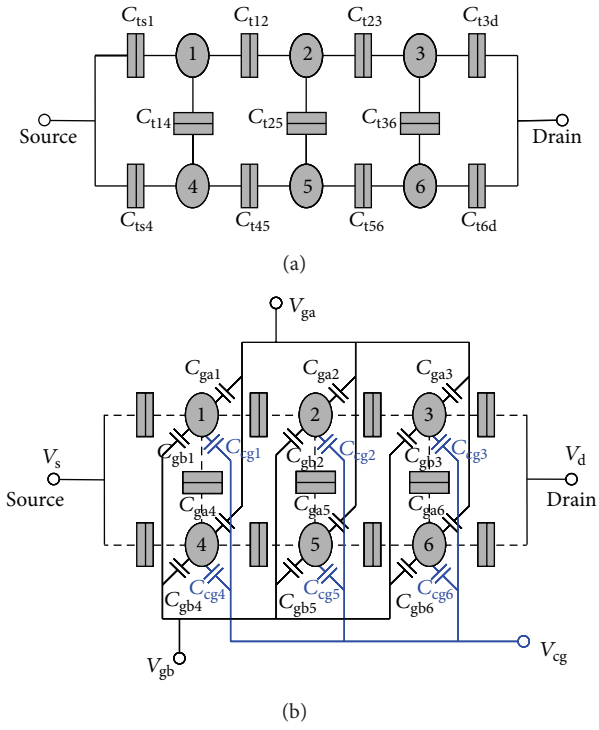


FIGURE 3: (a) The equivalent circuit of a 2 × 3 nanodot array and (b) an equivalent circuit with gate capacitors. The device has two input gates corresponding to the $V_{ga}$ and $V_{gb}$ terminals and one control gate corresponding to the $V_{cg}$ terminal.

of high-low and low-high [7]. Two of the three gates, $V_{ga}$ and $V_{gb}$, were used as input gates to create a two-input logic gate. The other gate, $V_{cg}$, was used as a control gate to change the logic function of the device.

Here, fluctuations in these values were introduced as shown in Table 1. The average tunnel capacitance between islands, or between a dot and source or drain terminal, was assumed to be 2 aF. The average capacitance between a control gate and each nanodot was also assumed to be 2 aF, and the average capacitance between an input gate and a nanodot was 1 aF, so the average total capacitance of the typical dots is about 10 aF. This enables the device to operate at around 10 K, which is the temperature used for simulation. An average tunnel resistance of 2 MΩ and no offset charges were assumed. An important issue to achieve such a multifunctional device by the use of nanodot arrays is to introduce a fluctuation in these capacitances and resistances caused by the fluctuation of nanodot sizes and positions. In the actually fabricated devices, we can control the island size within about 20% fluctuation [13, 14]. A distribution of all capacitances was introduced so as to ensure a standard deviation of 0.2. This corresponds to the distribution in which 68% of capacitances are included within ±20% of the average, which is thought to be attained in actual SEDs. Tunnel resistance distribution was also introduced as a log-normal distribution with a standard deviation of 0.2. This means that 68% of the tunnel resistances are included within the resistance from 126 kΩ to 31.6 MΩ. More than 200 examples were created for each dot arrangement with different capacitances and tunnel resistances in accordance with the variation shown above by generating random numbers and simulated the electrical characteristics by a Monte Carlo simulation [7]. It should be noted that the too much fluctuated capacitances and tunnel resistances sometimes provide specific nanodot arrays which do not work as logic gates using small arrays consisting of six nanodots, even though the slight fluctuations are needed for achieving multifunctional device operation.

TABLE 1: Distribution of tunnel resistances, tunnel capacitances, and gate capacitances.

| | Average | Distribution function | $\sigma$ |
|---|---|---|---|
| Tunnel resistance | 2 MΩ | Log normal | 0.2 |
| Tunnel capacitance | 2 aF | Gaussian | 0.2 |
| Input-gate capacitance | 1 aF | Gaussian | 0.2 |
| Control-gate capacitance | 2 aF | Gaussian | 0.2 |

The drain voltage $V_d$ was set so that the average current $I_d$ flowing between the source and drain terminal was constant at a high-temperature limit. To realize this condition, the $V_d$ for series, 2 × 3, 3 × 2, and parallel are set to 42 mV, 12 mV, 6 mV, and 2 mV, respectively. Although the average drain current $I_d$ at high temperature was 3 nA, the simulated

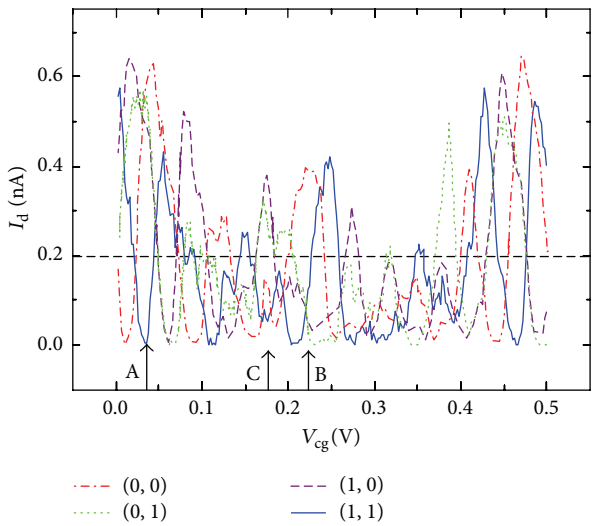


Figure 4: Simulated drain current $I_d$ as a function of control-gate voltage $V_{cg}$ of a "parallel" nanodot-array device. Parameters are a combination of input-gate voltages $V_{ga}$ and $V_{gb}$. "1" corresponds to a "high" input voltage (60 mV) and "0" corresponds to a "low" input voltage (0 V). The arrows at A, B, and C correspond to the positions of $V_{cg}$, where the logic functions of NAND, NOR, and XOR are, respectively, achieved when the current threshold is set to 0.2 nA.

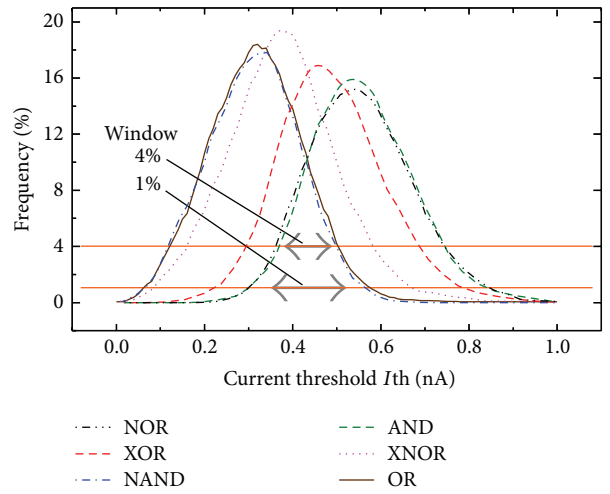


Figure 5: Occurrence frequencies of the six important logic functions (AND, OR, NAND, NOR, XOR, and XNOR) as a function of threshold current for a "parallel" nanodot-array device. We changed $V_{cg}$ from 0 to 5 V.

average $I_d$ at 10 K was about 0.5 nA due to the Coulomb blockade effect.

The two input-gate voltages, $V_{ga}$ and $V_{gb}$, were set to 60 mV for the "high" state and 0 V for the "low" state. The input-gate voltage of 60 mV corresponds to 75% of the voltage needed for a half-period shift of the Coulomb oscillation if a single-electron transistor consisting of a dot without capacitance fluctuation is assumed [7]. The control-gate voltage $V_{cg}$ ranged from 0 to 5 V.

## 3. Results and Discussion

Figure 4 shows a typical result of $I_d$-$V_{cg}$ characteristics simulated for a device with a "parallel" nanodot arrangement in which tunnel resistances, tunnel capacitances, and gate capacitances were distributed by the method described above. The parameters are the four combinations of input-gate voltages, $V_{ga}$ and $V_{gb}$. Here, "1" corresponds to the "high" input voltage (60 mV) and "0" corresponds to the "low" input voltage (0 V). The oscillation characteristics changed depending on the combination of the two input-gate voltages. This change was complicated due to the nonuniform capacitances and tunnel resistances. In other words, the control-gate voltage $V_{cg}$ is what switched the characteristics of the array. Here, the drain current $I_d$ is used as an output and introduces a current threshold to determine whether the current is "high" or "low." If the current threshold is set to 0.2 nA as shown by the broken line in Figure 4, and select a $V_{cg}$ of around 0.04 V as indicated by the as indicated by arrow A in Figure 4, the output function is a NAND gate because the output current is low only for the input combination ($V_{ga}$, $V_{gb}$) = (1, 1). In the same way, if $V_{cg}$ of around 0.22 V and 0.18 V are selected, as shown by arrows B and C in Figure 4, these functions are NOR and XOR gates, respectively. We can find every one of the important two-input logic functions—AND, OR, NAND, NOR, XOR, and XNOR—by changing $V_{cg}$.

It should be noted here that conventional CMOS circuits usually use voltage outputs. In addition, when the current threshold is used in the current output waveform characteristics shown in Figure 4, the on/off current ratio seems to be small. As shown in Figure 9 of [12], the current output can be converted to a voltage output with a relatively high on/off ratio by using a cascode MOSFET [15].

It is easily understood that the current threshold plays an important role in the occurrence frequency of each logic function: when the threshold is changed, the occurrence frequency is changed because OR and NAND frequently appear at the lower current threshold conditions while AND and NOR appear at the higher current threshold condition. Figure 5 summarizes the frequency of occurrence of each important logic function as a function of current threshold for a nanodot-array device of "parallel," where $V_{cg}$ was changed from 0 to 5 V. If the current threshold is set from about 0.30 nA to 0.55 nA, any one of the important logic functions appears with a frequency higher than 1%. We call this current threshold region the "window" for 1%. A wide window is convenient for achieving a flexible logic gate. In order to define the width of the window, we introduce a standard frequency, as shown in Figure 5. The two arrows correspond to the windows for 1% and 4% frequency, respectively. The current threshold window for 4% frequency means that a 4% occurrence of all six of the important functions is guaranteed when the current threshold is set anywhere in the window.

Since the nanodot array has fluctuation in capacitance and tunnel resistance, the window also fluctuates. Figures 6(a)–6(c) show examples of the relation between the occurrence frequency of each important logic function and

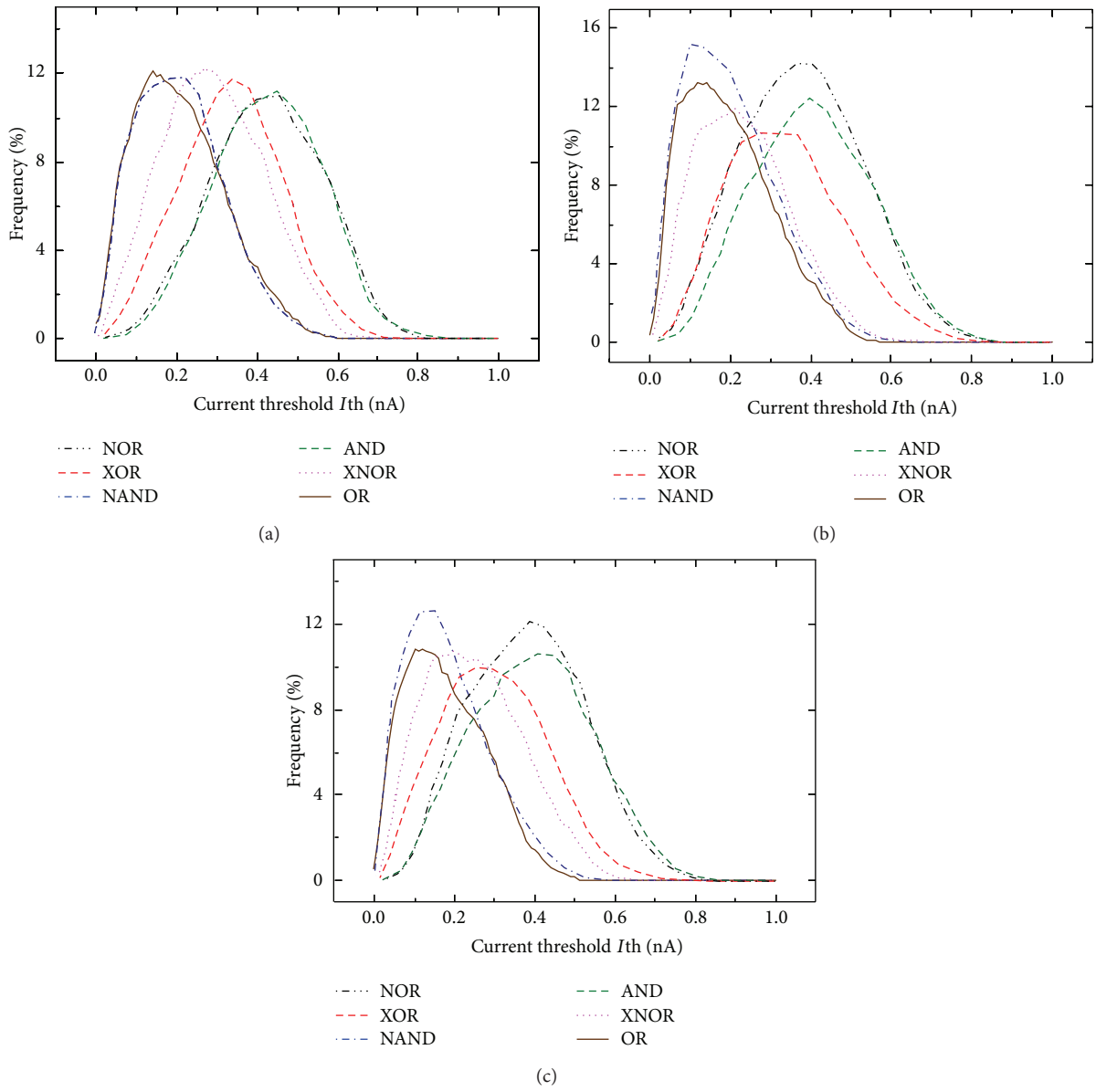


FIGURE 6: Occurrence frequency of the six important logic functions as a function of current threshold for three different "series" nanodot-array devices: (a), (b), and (c). We changed $V_{cg}$ from 0 to 5 V.

the current threshold calculated for three nanodot. arrays of "series" with different sets of capacitances and tunnel resistances. Although the frequency characteristics are all different, relatively wide windows are attained for all three arrays. We calculated more than 200 nanodot arrays with different sets of gate capacitances, tunnel capacitances, and tunnel resistances and confirmed that all arrangements have a window of 4%, as shown in Figure 6. We obtained the same results for the other dot arrangements (2 × 3, 3 × 2, and parallel) and confirmed that all arrays had at least a 4% window. An important point is that there were slight fluctuations in the position and width of the window, as shown in Figures 6(a)–6(c). When the array as a logic device is used, the current threshold has to be set at the initial setup of the logic device without measuring the $I_d$-$V_{cg}$ characteristics. A wider window and a stable center of the window of the current threshold are preferable for prospecting the occurrence probability of the logic functions. If the probability of occurrence of the six important logic functions is 1, we can always change to a different important logic function by changing $V_{cg}$.

We introduced a "normalized window width" that is normalized on the basis of the averaged value of the center of the window. Here, the center of the window of the current threshold is also normalized by the averaged value in order to compare the probability of the occurrence of six important logic functions in the four array arrangements. The electrical characteristics of more than 200 examples

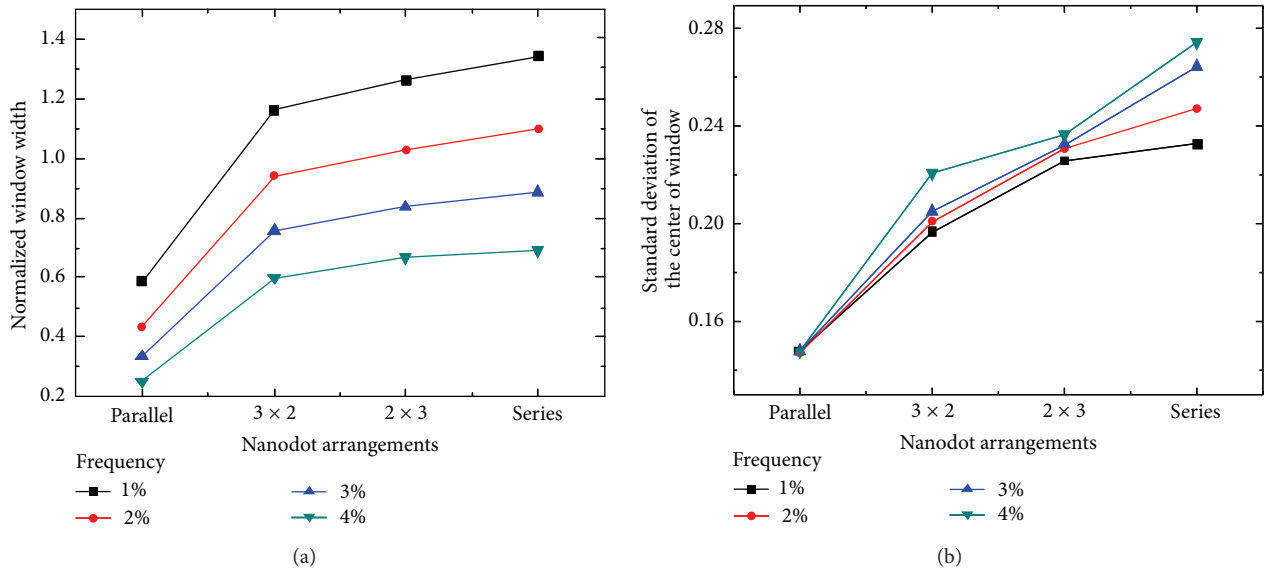


FIGURE 7: (a) Normalized window width and (b) standard deviation of the normalized center of the current threshold of the window for the four nanodot arrangements of arrays. The parameter is the minimum frequency of the six important logic functions.

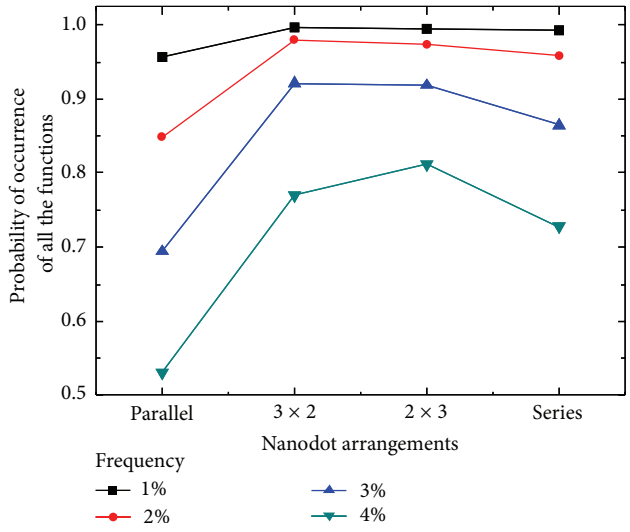


FIGURE 8: Occurrence probability of all the six important logic functions for the four nanodot arrangements of arrays when the current threshold is fixed at the most appropriate value for obtaining the highest probability. The parameter is the minimum frequency of the six important logic functions.

were calculated for each nanodot arrangement and the statistics of the normalized window width and the center of the window were evaluated. Figures 7(a) and 7(b) show the results of the averaged normalized window width and standard deviation of the normalized center of the current threshold of the window, respectively. The parameter is the minimum frequency of the six important logic functions, which guarantees the minimum frequency of the occurrence of the functions. Although the normalized window width becomes wider as the arrangement of the array changes from parallel to series, the standard deviation of the normalized center of the current threshold of the window also increases.

In order to determine the best arrangement of the dot array, the probability of the occurrence of all the six important logic functions was evaluated. Figure 8 shows the results when the current threshold was fixed at the most appropriate value for obtaining the highest probability to meet the minimum frequency. The best nanodot arrangement seems to be the 3 × 2 or 2 × 3 nanodot arrays. If a frequency of occurrence of 1% is permitted, the probability is almost 100%. This means that we can find any one of the six important logic functions with an appearance probability of at least 1% by changing the control-gate voltage from 0 V to 5 V. If a probability higher than 1% is claimed, some nanodot arrays do not work, which means that the appearance probability of all six logic functions is lower than the claimed value in some nanodot arrays. The nanodot array of series is not so bad if a relatively lower appearance probability of the six logic functions can be permitted. These results show that both parallel and series tunnel paths play an essential role for the operation as multifunctional logic gates, while the results suggest that the parallel paths are slightly important.

We also calculated the probability when the tunnel resistances have no fluctuation—namely, when they are constant at 2 MΩ—to investigate the origin of the results shown in Figure 8. As shown in Figure 9, all the nanodot-array arrangements recover the probability of the occurrence of the six logic functions. However, only the series with the frequency of 4% maintains a degraded state. If some dots in the series connections of nanodots have small capacitors, the charging energy becomes high, which inhibits the tunneling of electrons and makes the current lower. The large charging energy of the smallest dot makes the current level low in

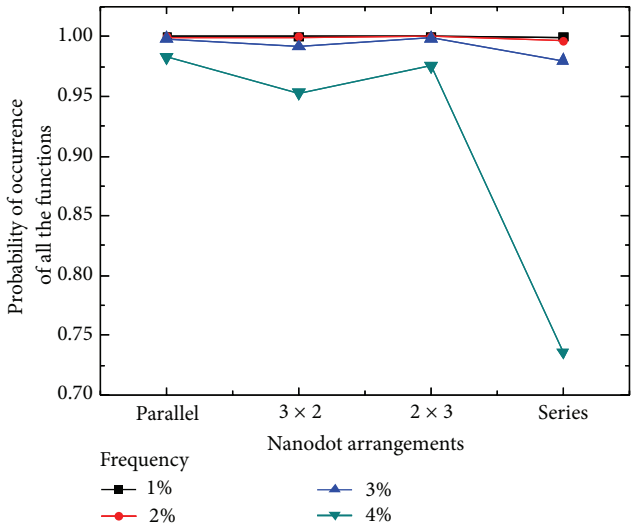


FIGURE 9: Occurrence probability of all the six important logic functions for the four nanodot arrangements of arrays without tunnel resistance fluctuation. The parameter is the minimum frequency of the six important logic functions.

the nanodot array of series, which limits the possibility of obtaining a wider current threshold window for high-occurrence probability. In the other arrays, since there are other parallel current paths, current levels are kept relatively high. When the fluctuation of tunnel resistance is introduced, and when both sides of the tunnel resistances of one of the dots in the parallel array is low, the current level increases, which also makes the current threshold window narrower. The tunnel resistance fluctuation degrades the appearance probability of the six logic functions. Consequently, it is important that the arrays have some parallel and some series connections in order to maintain current levels and to provide almost the same logic characteristics with a similar threshold current.

## 4. Conclusion

The Monte Carlo simulation was used to investigate flexible logic-gate devices consisting of a nanodot array assuming the fabrication by the use of the PADOX method in which lattice-like arrangement of nanodot arrays are attained easily. We changed the arrangement of the nanodots to clarify the importance of the parallel and series tunnel paths and then studied the variability of the logic functions of a device operating as a two-input logic gate. We introduced fluctuations in tunnel resistances, tunnel capacitances, and gate capacitances and then calculated the electrical characteristics of more than 200 sets for each nanodot arrangement as a function of the control voltage $V_{cg}$. We evaluated the appearance probability of the six important logic functions and clarified that both parallel and series tunnel paths play an essential role for the operation as multifunctional logic gates. The results also suggest that the parallel paths seem to be more critical than the series ones.

## Acknowledgments

The authors are grateful to A. Fujiwara, Y. Ono, H. Inokawa, K. Nishiguchi, T. Kaizawa, and T. Oya for their invaluable discussions. This work was partly supported by JSPS KAKENHI (2156081, 22240022, and 24360128).

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