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Research Article

Modelling, Design, and Performance Comparison of Triple Gate Cylindrical and Partially Cylindrical FinFETs for Low-Power Applications

Sanjeev Rai,[1] Jyotsna Sahu,[2] Wanjul Dattatray,[3] R. A. Mishra,[1] and Sudarshan Tiwari[4]

[1] *Department of Electronics and Communication Engineering, Motilal Nehru National Institute of Technology, Allahabad 211004, India*
[2] *RV VLSI Design Centre, CA 17, 36th Cross, Jayanagar Bangalore, Bangalore 560041, India*
[3] *Wipro VLSI, Electronic City, Bangalore 560100, India*
[4] *National Institute of Technology, Raipur 492010, India*

Correspondence should be addressed to Sanjeev Rai, sanjeev_rai96@yahoo.com

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The FinFETs recently have been the rallying point for the engineers as far as the development of the technology is concerned. The authors here have tried successfully to compare the performance of 30 nm conventional triple gate (Conv) FinFET structure with that of partially cylindrical (PC) FinFET. In PC-FinFET the fin is divided into two regions. Region I is partially cylindrical and has curvature of half of the fin width, and Region II is like a conventional FinFET (having flat region). The results show that there is considerable improvement in Ion, Ioff, and subsequent suppression of short channel effects, that is, subthreshold slope, DIBL, self heating effect, and so forth. The improvement has also been felt in series resistance in PC-FinFET as compared to C-FinFET. It is noteworthy also to mention that in PC-FinFET the corner of fin is rounded thus reducing the side wall area which further reduces the gate capacitance reducing the intrinsic delay. The DC and transient analysis of CMOS inverter using C-FinFET and PC-FinFET have been done which shows that PC-FinFET inverter has reduced propagation delay as compared to C-FinFET.

1. Introduction

In recent days the pace of scaling of MOSFETs has slowed down due to the number of reasons one being the short channel effects (SCEs) like drain-induced barrier lowering (DIBL), threshold voltage roll off, increase in subthreshold slope, increment in I_{off} off state current, and so forth. Therefore, in order to continue further scaling of the devices we require better suppression of (SCE) short channel effect and unconventional structures such as multigate devices [1]. These multigate FinFETs are very promising alternative to planner devices. In sub 50 nm gate length regime, the triple gate FinFET is one of the best alternatives to planner devices. In a trigate transistor, the gate surrounds the channel from all the three sides with three gates Top, Front, and Back gates as shown in Figure 2; the structure of the type mentioned has much better control over the channel. The width (Weff) of a trigate transistor is the (sum of all the three sides), that is, (twice the fin height) + the fin width (Weff $=$ 2 $\times$ Hfin + Wfin). The stronger control decreases the subthreshold leakage, threshold voltage roll off, and off state current which makes the scaling possible to meet the ITRS trends [2]. Further, the triple gate FinFET has reduced the doping concentration required in the channel to the extent of $10^{15}/\text{cm}^3$. However, variation in the height and width of the trigate is now an issue and needs to be tightly controlled. In FinFETs, It has been observed that with decreases in fin-width (SCE) short channel effects can be reduced but with reduced fin-width performance of the FinFET may degrade due to increase in parasitic drain/source resistance which leads to reduction of drive current and transconductance of the device [3–5]. Also, with smaller fin width, heat cannot flow through easily and device temperature increases. This is more severe in case of SOI

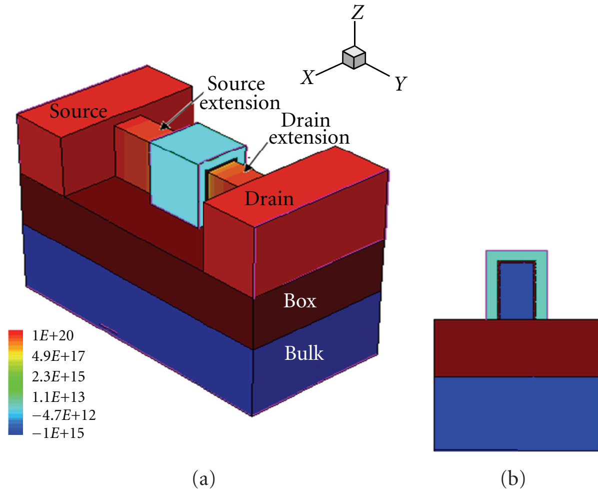

Figure 1: (a) Structure of C-FinFET, (b) cross-sectional view of C-FinFET.

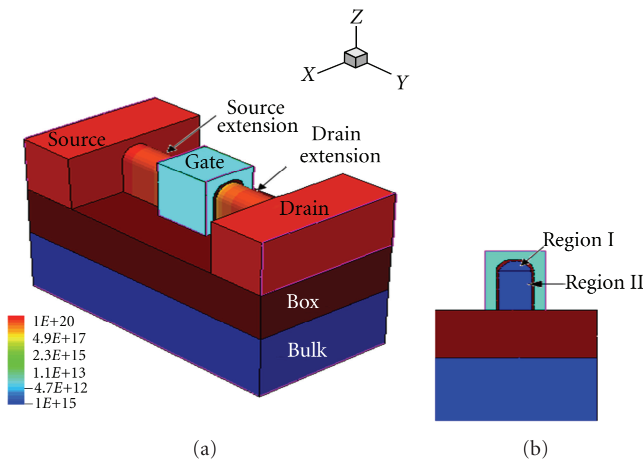

Figure 2: (a) Structure of PC-FinFET, (b) cross-sectional view of PC-FinFET.

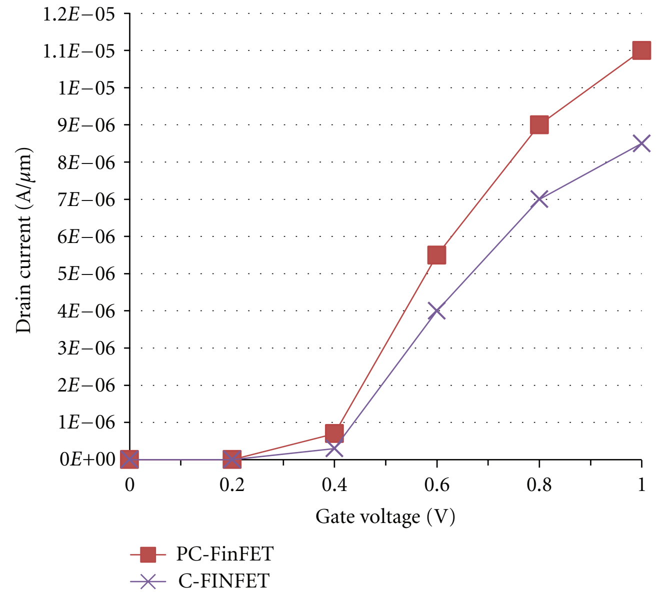

Figure 3: Transfer characteristics of C and PC FinFET.

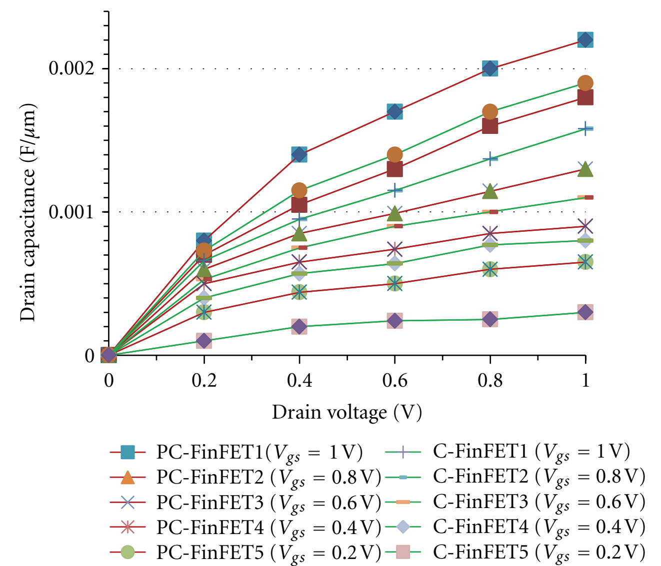

Figure 4: Output characteristics for C-FinFET and PC-FinFET.

technology, where buried insulating layer causes severe self-heating effects due to low thermal conductivity of oxide layer [6]. Figure 1 shows structure and the cross-sectional view of a triple gate FinFET. The charge sharing occurs in the corner region of the two adjacent gates due to the proximity of gates. This gives rise to premature inversion at the corners. The corners present in the triple gate FinFET result in the formation of independent channels with different threshold voltages. This premature inversion of corners in triple gate FinFET is known as "Corner Effect" [7]. This premature inversion at the corners of the triple gate FinFET degrades the subthreshold characteristics of the FinFET which results in higher off state leakage current (I_{off}). Thus, it is necessary to suppress the corner effects in order to avoid leakage currents. There are various techniques available to eliminate the corner effects such as reduction in oxide thickness, reduction in doping concentration in channel, and corner rounding which the authors have tried to present in the current paper.

This paper is arranged as follows; Section 2 analyses and describes the device used for the simulation. In section 3, comparisons have been made between conventional FinFET and PC-FinFET in terms of different parameters, while Section 4 shows the inverter simulation with both types of FinFET. Section 5 concludes the paper.

2. Device Structure and Simulation

Conventional triple gate FinFET (C-FinFET) and partially cylindrical triple gate FinFET (PC-FinFET) device simulations were performed using Sentaurus TCAD tools [8].

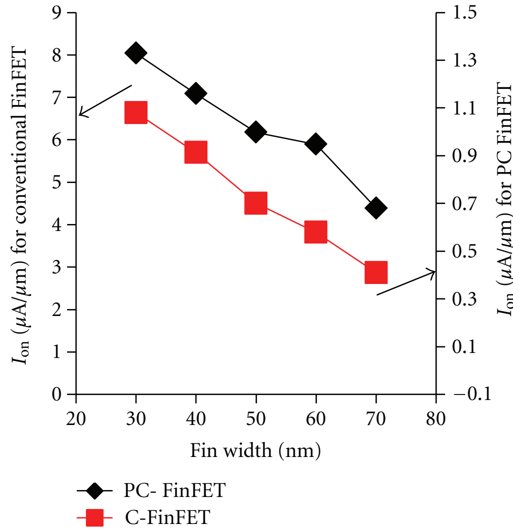

Figure 5: On current for C-FinFET (left y-axis) and PC-FinFET (right y-axis) for different values of Fin width.

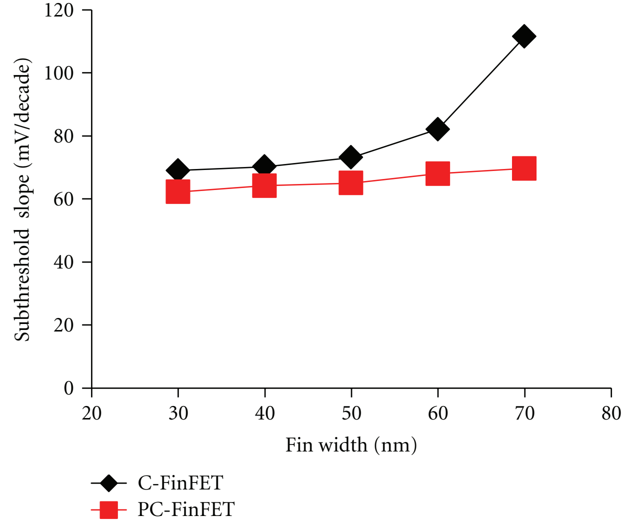

Figure 7: Subthreshold slope for C-FinFET and PC-FinFET for different values of fin width.

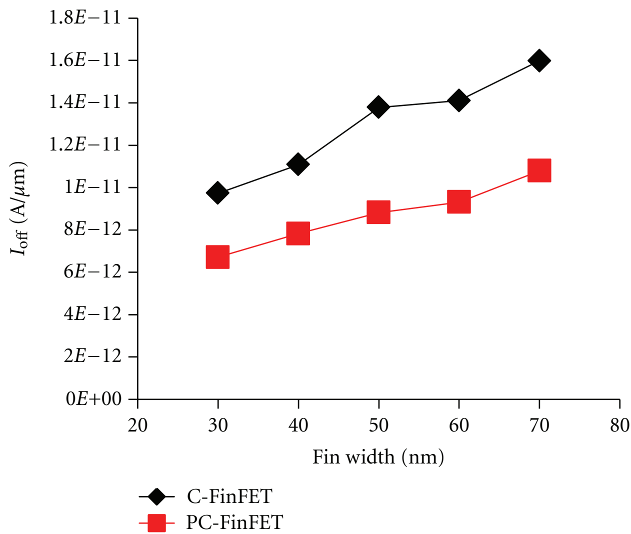

Figure 6: Off current for C-FinFET and PC-FinFET for different values of fin width.

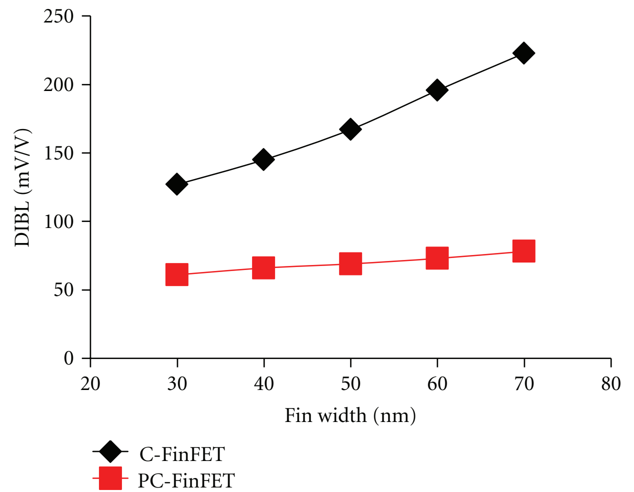

Figure 8: DIBL for C-FinFET and PC-FinFET for different values of fin width.

SOI structure is used in both types of devices. Gate length of the device is 30 nm and is varied up to 70 nm for different parameter analysis. The fin width is varied from 15 nm up to 70 nm. The EOT (effective oxide thickness) is taken as 1.2 nm, and the fin height is 30 nm. The device has uniform low doped channel region having doping concentration of 10^{15} cm^{-3}. The three gates are poly silicon gates. Source/drain region has the doping concentration of 10^{20} cm^{-3}, while source/drain extensions have an analytical Gaussian doping with peak concentration of 10^{20} cm^{-3}. The supply voltage used here is 1 V. For the analysis of different short channel effects fin width and gate lengths are varied. Figures 1 and 2 show structure and cross-section view of C-FinFET and PC-FinFET, respectively [6].

Table 1 depicted below shows the simulation result of conventional FinFET with that of PC-FinFET which has been compared for 30 nm fin height. The various parameters like I_{on}, I_{off}, Subthreshold slope, DIBL, and Maximum Temperature have been compared. The results have been verified on Sentaurus TCAD [8].

3. Comparison of Triple Gate C-FinFET with PC-FinFET

Partially cylindrical FinFET has advantage over conventional FinFET in the corner effects. Figure 3 shows the transfer characteristics of the PC-FinFET and C-FinFET for drain to source voltage of 0.05 V. It is evident from the drain characteristics of the devices in Figure 4. This is further clear

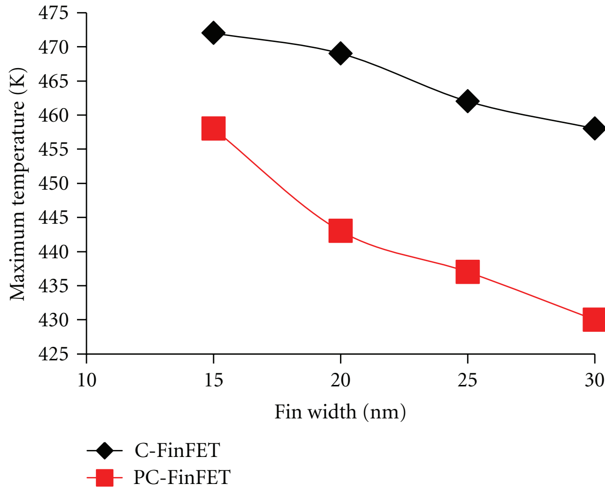

Figure 9: Maximum temperature for C-FinFET and PC-FinFET for different values of fin width.

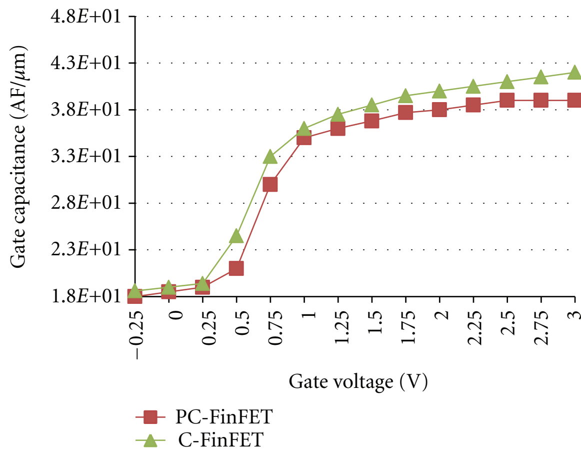

Figure 10: Gate capacitance for C-FinFET and PC-FinFET for different values of gate voltage.

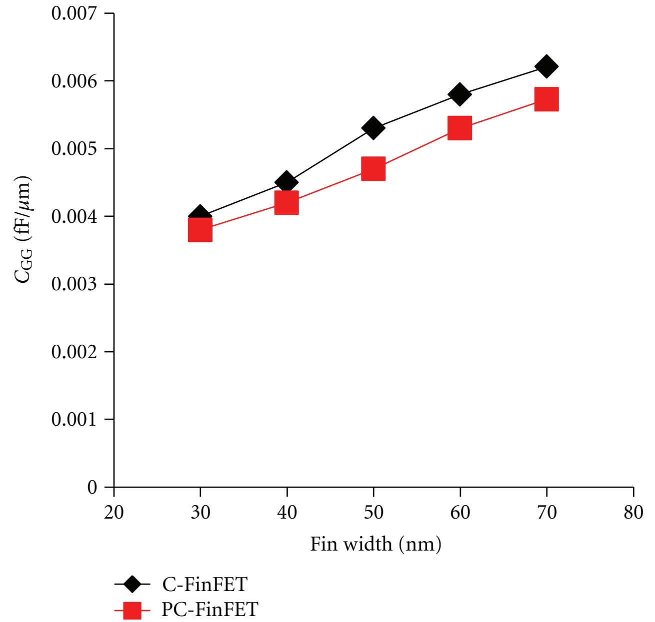

Figure 11: Total gate capacitance for C-FinFET and PC-FinFET for different values of fin width.

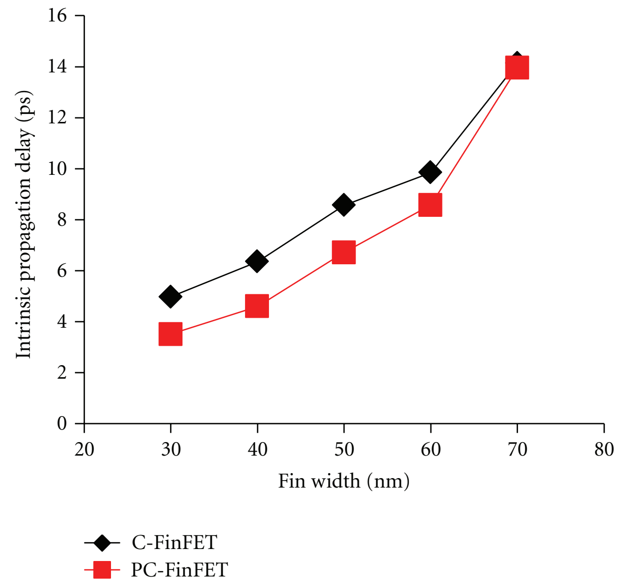

Figure 12: Intrinsic delay for C-FinFET and PC-FinFET for different values of fin width.

from Figure 5 that the on state current of the PC-FinFET has improved compared to the C-FinFET.

In PC-FinFET as the corners are rounded, the heat can flow easily, which reduces the self heating phenomenon thereby improving the mobility of the carriers [9]. This reduces the series resistance of the PC-FinFET, which results in increase of on state current. Figure 5 shows the variation in on state current of the C-FinFET and PC-FinFET with variation in the fin width of the respective devices. The variation in off state leakage current with variation of the fin width of the C-FinFET and PC-FinFET is shown in Figure 6. Thus, PC-FinFET results in higher I_{on}/I_{off} ratio by increasing the on state current and decreasing the off state current. The rounding of the corners also helps in reduction of the off state leakage current, as the premature inversion is avoided. The sub-threshold slope and drain-induced barrier are important parameters analyzed here.

The subthreshold slope of PC-FinFET is considerably lower than that of C-FinFET. The variation in subthreshold slope with the variation of fin width of C-FinFET and PC-FinFET is depicted in Figure 7. For the C-FinFET the subthreshold slope decreases with decreases in fin width, while for the PC-FinFET the subthreshold slope is moreover constant as the fin width is varied.

The drain-induced barrier lowering indicates the change in threshold voltage of the devices with change in drain voltage. DIBL of both devices with variation of fin width is plotted in Figure 8. The DIBL for PC-FinFET is less compared to the C-FinFET. The DIBL decreases for the C-FinFET with the decrease in the fin width of the device. In

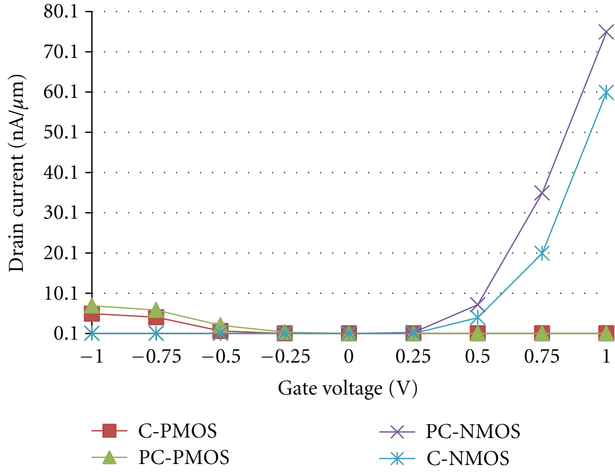

Figure 13: Transfer characteristics for nmos and pmos using C-FinFET and PC-FinFET.

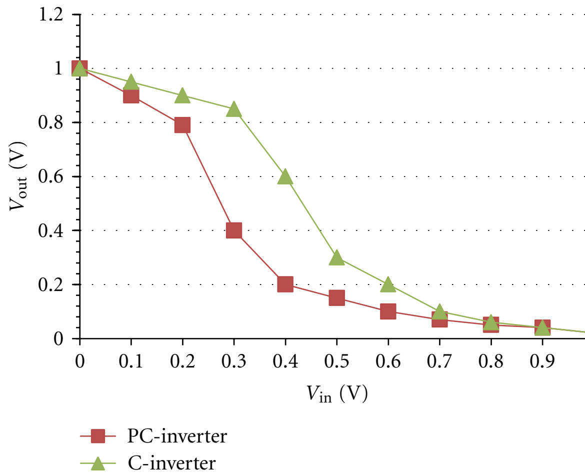

Figure 14: Transfer characteristics for cmos inverter using C-FinFET and PC-FinFET.

Table 1: Simulation result for 30 nm C-FinFET and PC-FinFET.

Parameter	C-FinFET (fin width 30 nm)	PC-FinFET (fin width 30 nm)
V_{th} (V)	0.40245	0.38826
I_{on} (A/μm)	8.30485×10^{-6}	1.08006×10^{-5}
I_{off} (A/μm)	9.73041×10^{-12}	6.71352×10^{-12}
Sub-threshold slope (mV/decade)	69.0125	62.247
DIBL (mV/V)	127.03	61.037
Maximum Temperature (K)	458	430

this paper SOI FinFET is used, which has various advantages over bulk FinFET due to presence of a buried oxide layer (BOX), but this insulating layer causes lower conductivity which improves device temperature; this results in self heating effect. Also with narrow fin transistor heat cannot

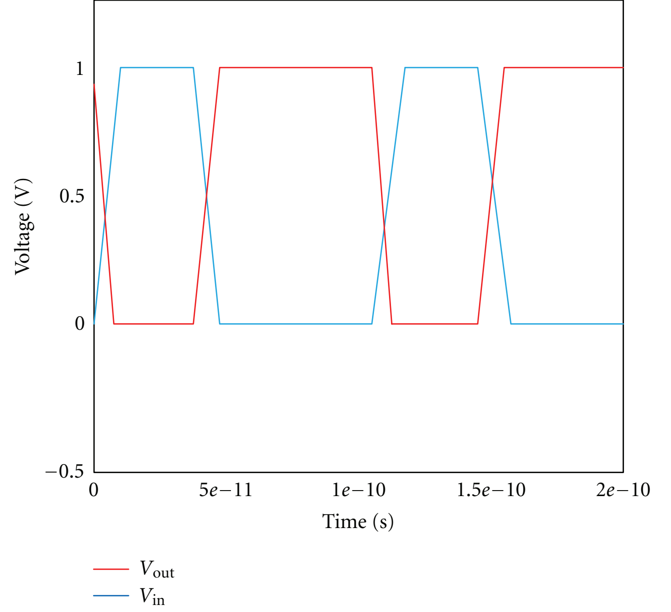

Figure 15: Transient characteristics for CMOS inverter using C-FinFET.

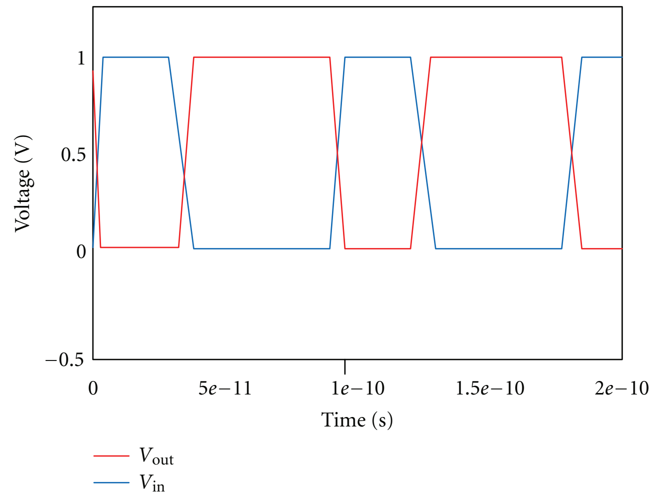

Figure 16: Transient characteristics for CMOS inverter using PC-FinFET.

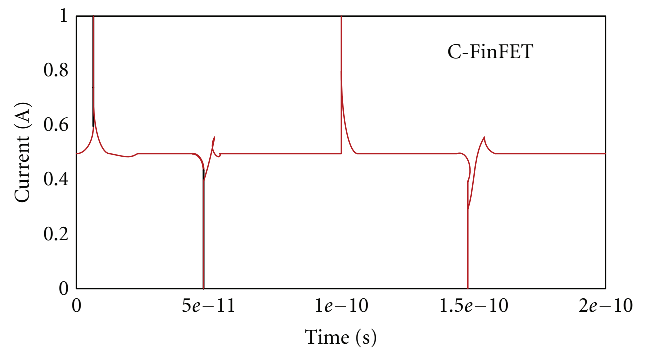

Figure 17: Output current for CMOS inverter using C-FinFET.

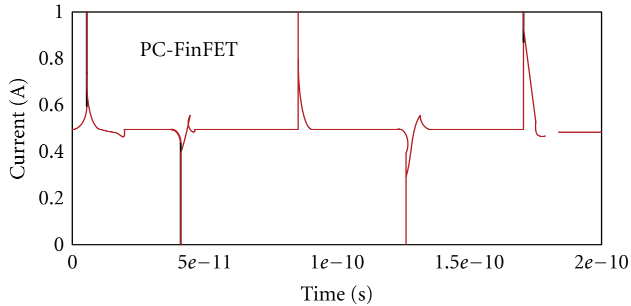

Figure 18: Output current for CMOS inverter using PC-FinFET.

Table 2: DC analysis of CMOS Inverter using C-FinFET and PC-FinFET.

Voltage level	C-FinFET	PC-FinFET
V_{OH} (V)	0.9584	0.9584
V_{OL} (V)	0.1235	0.1421
V_{IH} (V)	0.4969	0.3749
V_{IL} (V)	0.2936	0.1461

Table 3: Delay parameters for CMOS Inverter using C-FinFET and PC-FinFET.

Delay parameter	C-FinFET	PC-FinFET
tpHL (pS)	3.429	2.371
tpLH (pS)	2.087	1.170
Avg dealy (pS)	2.758	1.771

flow easily which improves device temperature as we scale down the fin width. As corners of the fin are rounded, the heat can flow easily as compared to conventional structure. From Figure 9 we can see that FinFET that is partially cylindrical has a lower device temperature as compared to conventional one.

The gate capacitance of the device is responsible for deciding the intrinsic delay of the device. As the corners are rounded in PC-FinFET, the side wall area under the gate region is reduced which reduces the gate capacitance of the PC-FinFET. Thus, PC-FinFET has lower gate capacitance compared with the C-FinFET. The relationship between the gate capacitance and the gate voltage is plotted in Figure 10 for both C-FinFET and PC-FinFET. The current drive capability and switching speed are the most important and basic parameters for measuring the device performance. The intrinsic gate delay is calculated as ($C_{GG} \cdot V_{DD}/I_{ON}$) where, C_{GG} is the total effective gate capacitance. C_{GG} includes gate-to-source capacitance C_{GS}, gate-to-drain capacitance C_{GD}, and gate-to-substrate capacitance C_{GB}, with C_{GS} being the dominating component. Total gate capacitance for both the devices for different values of gate voltage is shown in Figure 11. The Intrinsic delay of PC-FinFET is lesser than that of C-FinFET. This delay decreases with decrease in fin width of the device as shown in Figure 12. The technology over the years has advanced such that development of high-performance devices can be done with the help of FinFETs [10].

4. Comparison of C-FinFET and PC-FinFET, CMOS Inverter

In previous sections, it is observed that PC-FinFET has lower gate capacitance and offers several advantages over C-FinFET. In this section, CMOS inverter is built with C-FinFET and PC-FinFET to analyze the effectiveness of PC-FinFET over C-FinFET in circuit simulations. Figure 13 shows the transfer characteristics of the n-FinFET and p-FinFET for conventional and partially cylindrical types. The change in the threshold voltage of the CMOS inverters of both devices can be seen from Figure 14. The different input, output voltage levels required for noise margin calculation are tabulated in Table 2 for C-FinFET and PC-FinFET. There is small drop in the noise margin of the inverter if PC-FinFETs are used.

DC and transient analysis of the inverters using C-FinFETs and PC-FinFETs are done and are compared for the delay, noise margin parameters. The input output waveforms of the inverter using C-FinFETs and using PC-FinFETs are shown in Figures 15 and 16, respectively. Figure 17 shows output current for C-FinFET and Figure 18 shows output current for PC-FinFET. The rising edge delay, falling edge delay, and average delay of the respective inverters are tabulated in Table 3, which shows that inverter with PC-FinFETs has lesser delay compared to the inverter with C-FinFETs which we would expect in modern devices [11]. This is because PC-FinFET has less capacitance than C-FinFET. Thus, switching is faster in case of inverter design of PC-FinFET.

5. Conclusion

The C-FinFET suffers from corner effects due to the charge overlap in the corner areas which leads to the self heating. In PC-FinFET the corners of the C-FinFET are rounded. Rounding of corners allows free flow of heat which reduces the self heating effect. The reduced temperature increases the mobility of the carriers and in turn the on-state current of the device (I_{on}). The results have shown that PC-FinFET has better on state current, off state current, subthreshold slope, and drain-induced barrier lowering than the C-FinFET. The gate capacitance of the PC-FinFET is lesser than that of C-FinFET thus lowering the intrinsic delay in PC-FinFET. The CMOS inverter has been taken as an application circuit which shows that PC-FinFET offers lower delay than the C-FinFET due to the reduced capacitance of the devices. The authors suggest that larger circuits can be implemented by using PC-FinFET thus producing better delays. Also it is worth noting that FinFET devices with extension of source/drain with spacer technologies have also gained prominence over the years where lot of work can be done [12]. The various results shown above correspond to the device parameters mentioned in Section 2. The tools used for the purpose were from TCAD, synopsis, and few to mention were structure editor, s-device, Tecplot, and so forth.

Acknowledgments

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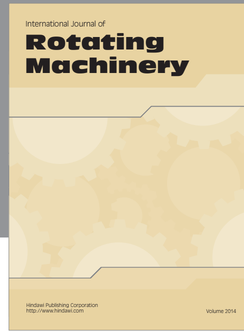
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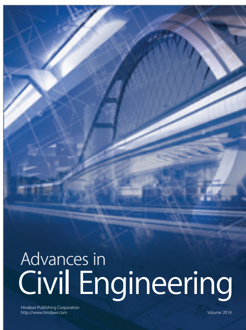
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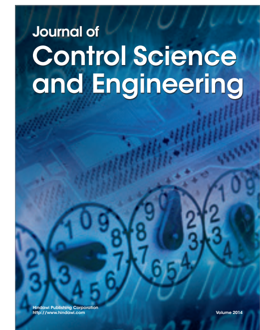
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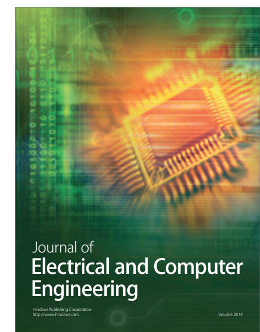
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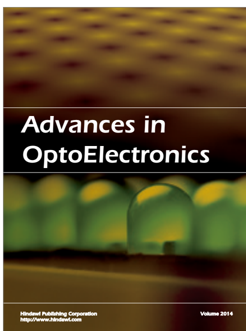
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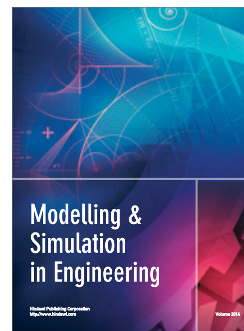
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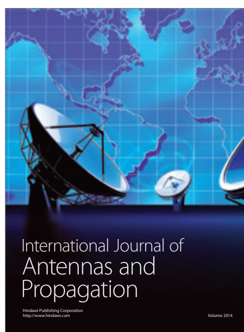
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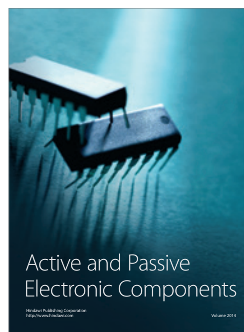
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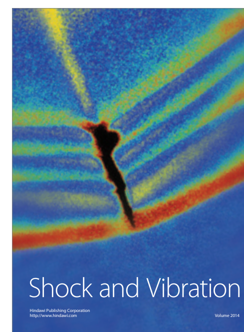
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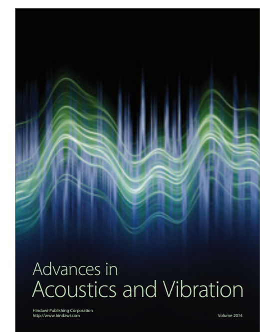
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