Hindawi Publishing Corporation
Active and Passive Electronic Components
Volume 2013, Article ID 217674, 9 pages
http://dx.doi.org/10.1155/2013/217674

Research Article

MCML D-Latch Using Triple-Tail Cells: Analysis and Design

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Received 25 June 2013; Accepted 17 September 2013

Academic Editor: Ching Liang Dai

A new low-voltage MOS current mode logic (MCML) topology for D-latch is proposed. The new topology employs a triple-tail cell to lower the supply voltage requirement in comparison to traditional MCML D-latch. The design of the proposed MCML D-latch is carried out through analytical modeling of its static parameters. The delay is expressed in terms of the bias current and the voltage swing so that it can be traded off with the power consumption. The proposed low-voltage MCML D-latch is analyzed for the two design cases, namely, high-speed and power-efficient, and the performance is compared with the traditional MCML D-latch for each design case. The theoretical propositions are validated through extensive SPICE simulations using TSMC 0.18 μm CMOS technology parameters.

1. Introduction

The advances in semiconductor technology have led to the integration of high performance digital and analog circuits on the same silicon substrate. The traditional CMOS logic style does not provide an analog friendly environment due to the large switching noise [1–3]. Many alternate logic styles have been suggested in [3–6] and the reference mentioned therein. MOS current mode logic (MCML) style is the most promising one due to the lower switching noise in comparison to traditional CMOS logic style [6–9]. Also, it exhibits better power delay than the traditional CMOS logic style at high frequencies [6–15]. Therefore, MCML style is appropriate for designing high performance digital circuits wherein a D-latch is widely used as a building block in different applications such as prescalars, frequency dividers, and sequential logic circuits [16–20].

The D-latch topology given in [16–20] is referred to as traditional D-latch and is based on the series-gating approach (i.e., stacked source-coupled transistor pairs) [9] which puts a limit on the minimum power supply. The power supply may, however, be lowered by reducing the number of stacked transistor pair levels with triple-tail cell concept [21–23]. In this paper, a new low-voltage MCML D-latch is proposed. The static parameters for the proposed D-latch are analytically modeled and applied to develop a design approach. From the knowledge of the transistor sizes, the delay is expressed in terms of the bias current and the voltage swing so that it can be traded off with the power consumption. The proposed low-voltage multiplexer is analyzed for high-speed and power-efficient design cases. A comparison in performance of the proposed D-latch with the traditional one is carried out for all the cases.

The paper first briefs the operation of the traditional MCML D-latch in Section 2. Thereafter, a new low-voltage MCML topology for the D-latch is proposed, and analytical formulations for different static parameters and delay are put forward in Section 3. The analysis of the proposed D-latch for the different design cases is presented, and its performance is compared with the traditional one in Section 4. Extensive SPICE simulations are carried out to validate the proposed theory. Section 5 concludes the paper.

2. Traditional MCML D-Latch

A traditional MCML D-latch with differential inputs D and CLK is shown in Figure 1 [24]. It consists of two levels of source-coupled transistor pairs to implement the logic function and a constant current source M_{TR1} to generate

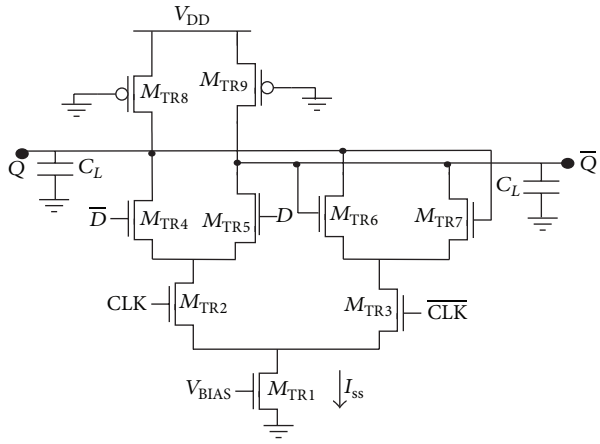

Figure 1: Traditional MCML D-latch.

bias current I_{SS}. The differential input CLK drives the lower level transistor pair M_{TR2}-M_{TR3} that alternatively activates the upper level transistor pairs M_{TR4}-M_{TR5} and M_{TR6}-M_{TR7}. When differential input CLK is high, M_{TR3} is OFF and the bias current I_{SS} flows through M_{TR2} and is steered either to M_{TR4} or M_{TR5} according to the differential input D to ensure that the D-latch operates in the transparent state. Conversely, when the differential input CLK is low, the bias current I_{SS} flows through M_{TR3} and is steered to one of the two transistors, that is, either M_{TR6} or M_{TR7} according to the previous output value such that the output does not respond to the changes in the input; thus, D-latch remains in the hold state. The bias current I_{SS} is converted to the differential output voltage ($V_Q - \overline{V_Q}$) through the PMOS transistors M_{TR8} and M_{TR9} [24]. The load capacitance C_L includes the effect of fanout and the interconnect capacitances.

The minimum supply voltage, $V_{DD\_MIN\_TR}$, for the traditional D-latch is defined as the lowest voltage at which all the transistors in the two levels and the current source operate in the saturation region [25] and is computed as

$$V_{DD\_MIN\_TR} = 3V_{BIAS} - 3V_{T\_TR1} + V_{T\_TR}, \tag{1}$$

where V_{T_TR} is the threshold voltage of the transistors $M_{TR4,5,6,7}$, V_{T_TR1} is the threshold voltage of M_{TR1}, and V_{BIAS} is the biasing voltage of M_{TR1}.

3. Proposed Low-Voltage MCML D-Latch

The proposed low-voltage D-latch with differential inputs D and CLK is shown in Figure 2. It consists of two triple-tail cells (M_{LV3}, M_{LV4}, M_{LV7}) and (M_{LV5}, M_{LV6}, M_{LV8}) biased by separate current sources of $I_{SS}/2$ value. The transistors M_{LV7} and M_{LV8} are driven by the differential CLK input and are connected between the supply terminal and the common source terminal of transistor pairs M_{LV3}-M_{LV4} and M_{LV5}-M_{LV6}, respectively. A high differential CLK voltage turns ON the transistor M_{LV8}, and deactivates the transistor pair M_{LV5}-M_{LV6}. At the same time, the transistor M_{LV7} turns OFF so that the transistor pair M_{LV3}-M_{LV4} generates the output according to the differential input D. Thus, the D-latch works in the transparent state. Similarly, the transistor pair M_{LV5}-M_{LV6} gets activated for low differential CLK voltage and preserves the previous output. Therefore the D-latch operates in the hold state for low value of the differential CLK input.

The minimum supply voltage, $V_{DD\_MIN\_LV}$, for the proposed D-latch is computed by the method outlined in [25] as

$$V_{DD\_MIN\_LV} = 2V_{BIAS} - 2V_{T\_LV1} + V_{T\_LV}, \tag{2}$$

where V_{T_LV} is the threshold voltage of transistor $M_{LV3,4,5,6}$, V_{T_LV1} is the threshold voltage of M_{LV1}, and V_{BIAS} is the biasing voltage of M_{LV1}.

3.1. Static Model. The static model is derived by modeling the load transistors M_{LV9}, M_{LV10} by an equivalent linear resistance, R_P [26]. Using the standard BSIM3v3 model, the linear resistance, R_P is computed as

$$R_P = \frac{R_{int}}{1 - \left(\left(R_{DSW}10^{-6}\right)/W_P\right)/R_{int}}, \tag{3}$$

where R_{DSW} is the empirical model parameter, W_P the channel width of the load transistor, and the parameter R_{int} is the intrinsic resistance of the PMOS transistor in the linear region and is given as

$$R_{int} = \left[\mu_{eff,p}C_{ox}\frac{W_P}{L_P}\left(V_{DD} - \left|V_{T,p}\right|\right)\right]^{-1}, \tag{4}$$

where C_{ox} is the oxide capacitance per unit area. The parameters $\mu_{eff,p}$, $V_{T,p}$, W_P, and L_P are the effective hole mobility, the threshold voltage, and the effective channel length of the load transistor, respectively.

It may be noted that if equal aspect ratio of all transistors in the triple-tail cells is considered, then the transistors M_{LV7} and M_{LV8} will not be able to completely switch OFF the transistor pair M_{LV3}-M_{LV4} and M_{LV5}-M_{LV6}. Hence, for proper operation, the aspect ratio of transistors M_{LV7}, M_{LV8} is made greater than the other transistors' aspect ratio by a factor N. As an example if the value of differential input D is chosen such that the transistors M_{LV3}, M_{LV5} are ON while the transistors M_{LV4}, M_{LV6} are OFF, then a high differential CLK voltage turns ON the transistor M_{LV8}. But since the transistors M_{LV5} and M_{LV8} have the same gate-source voltages, the currents flowing through M_{LV5} ($i_{D,5}$) and M_{LV8} ($i_{D,8}$) can be written as

$$i_{D,5} = \frac{I_{SS}}{2}\frac{1}{1+N}, \tag{5a}$$

$$i_{D,8} = \frac{I_{SS}}{2}\frac{N}{1+N}. \tag{5b}$$

The current through M_{LV5} can be minimized by increasing factor N. This input condition produces minimum output voltage V_{OL} as

$$\begin{aligned} V_{OL} &= V_Q - \overline{V_Q} \\ &= R_P\left[\left(i_{D,4} + i_{D,6}\right) - \left(i_{D,3} + i_{D,5}\right)\right] \\ &= -\frac{R_P I_{SS}}{2}\left(1 + \frac{1}{1+N}\right), \end{aligned} \tag{6}$$

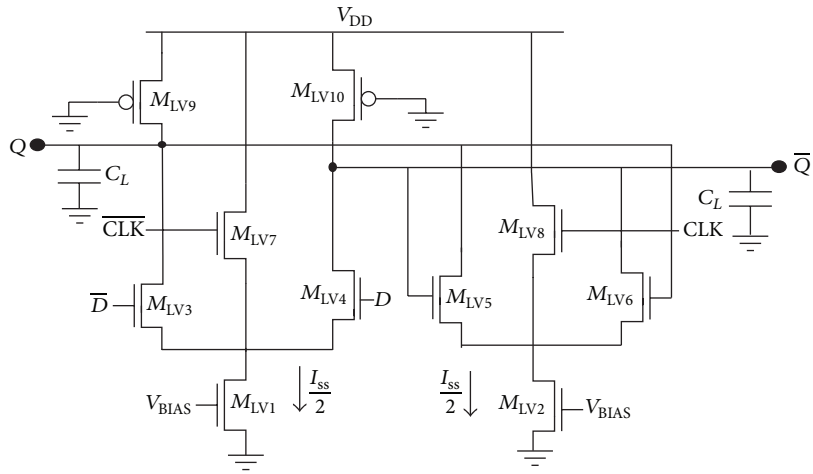

Figure 2: Proposed low-voltage D-latch.

Table 1: Differential output voltages of the proposed D-latch for various input combinations.

Differential inputs		Present state	Currents through the transistors						Next state differential output ($V_Q - \overline{V_Q}$)	
CLK	D	Q	M_{LV3}	M_{LV4}	M_{LV5}	M_{LV6}	M_{LV7}	M_{LV8}	Level	$R_P[(i_{D,4}+i_{D,6})-(i_{D,3}+i_{D,5})]$
L	L	L	I_3	0	I_1	0	I_2	0	V_{OL1}	$-R_P(I_{SS}/2)(1+1/(1+N))$
L	L	H	I_3	0	0	I_1	I_2	0	V_{OH2}	$R_P(I_{SS}/2)(N/(1+N))$
L	H	L	0	I_3	I_1	0	I_2	0	V_{OL2}	$-R_P(I_{SS}/2)(N/(1+N))$
L	H	H	0	I_3	0	I_1	I_2	0	V_{OH1}	$R_P(I_{SS}/2)(1+N/(1+N))$
H	L	L	I_1	0	I_3	0	0	I_2	V_{OL1}	$-R_P(I_{SS}/2)(1+N/(1+N))$
H	L	H	I_1	0	0	I_3	0	I_2	V_{OL2}	$-R_P(I_{SS}/2)(N/(1+N))$
H	H	L	0	I_1	I_3	0	0	I_2	V_{OH2}	$R_P(I_{SS}/2)(N/(1+N))$
H	H	H	0	I_1	0	I_3	0	I_2	V_{OH1}	$R_P(I_{SS}/2)(1+N/(1+N))$

L/H = low/high differential input voltage, $I_1 = I_{SS}/2$, $I_2 = (I_{SS}/2)(N/(1+N))$, and $I_3 = (I_{SS}/2)(1/(1+N))$.

where $i_{D,3}, i_{D,4}, i_{D,5}$, and $i_{D,6}$ are the currents through transistors M_{LV3}, M_{LV4}, M_{LV5}, and M_{LV6}, respectively. The differential output voltages for various input combinations are enlisted in Table 1. It can be observed from Table 1 that there are two values of maximum output voltage (V_{OH}) and minimum output voltage (V_{OL}) for different input and output combinations. Consequently, the voltage swing, V_{SWING1}, when the input and output are the same can be expressed as

$$V_{SWING1} = V_{OH1} - V_{OL1} = R_P I_{SS}\left(1 + \frac{1}{1+N}\right), \quad (7a)$$

where V_{OH1}, V_{OL1} are maximum output voltage and minimum output voltage, respectively, for the same input/output. The voltage swing, V_{SWING2}, when the input and output are different can be expressed as

$$V_{SWING2} = V_{OH2} - V_{OL2} = R_P I_{SS}\left(\frac{N}{1+N}\right), \quad (7b)$$

where V_{OH2}, V_{OL2} are maximum output voltage and minimum output voltage, respectively, for different input/output.

As $V_{SWING2} < V_{SWING1}$, V_{SWING2} has been considered as the worst case voltage swing:

$$V_{SWING} = R_P I_{SS}\left(\frac{N}{1+N}\right). \quad (8)$$

The small-signal voltage gain (A_v) and noise margin (NM) for the proposed D-latch are computed by the method outlined in [26] as

$$A_v = g_{m,n} R_P = \frac{1+N}{N}\frac{V_{SWING}}{2}\sqrt{2\mu_{eff,n} C_{OX}\frac{W_N}{L_N}\frac{1}{I_{SS}}} \quad (9)$$

$$NM = \frac{V_{SWING}}{2}\left[1 - \frac{\sqrt{2}}{A_v}\right], \quad (10)$$

where $\mu_{eff,n}$, $g_{m,n}$, W_N, and L_N are the effective electron mobility, the transconductance, the effective channel width, and length of transistors $M_{LV3,4,5,6}$, respectively.

3.2. Transistor Sizing. In this section, an approach to size the transistors of the proposed low-voltage D-latch on the basis of static model is developed.

For a specified value of NM, factor N, and A_v (≥1.4 for MCML [8]), the voltage swing of the proposed D-latch is calculated using (10) as

$$V_{SWING} = \frac{2NM}{1 - \left(\sqrt{2}/A_v\right)}. \quad (11)$$

It may be noted that V_{SWING} should be lower than the maximum value of $2V_T$ so as to ensure that transistors $M_{LV3,4,5,6}$ operate in saturation region. The voltage swing obtained from (11) requires sizing of the load transistor with equivalent resistance R_P $(= ((1+N)/N)(V_{SWING}/I_{SS}))$. To this end, the equivalent resistance, R_{P_MIN}, for the minimum sized PMOS transistor is first determined, and then the bias current I_{HIGH} for the required voltage swing is determined as

$$I_{HIGH} = \frac{V_{SWING}}{R_{P\_MIN}}. \tag{12}$$

If the bias current is higher than I_{HIGH}, then R_P should be less than R_{P_MIN}, and this is achieved by setting L_P to its minimum value, that is, L_{MIN} and W_P which is calculated by solving (3) and (4) as

$$\begin{aligned} W_P = {} & \frac{N}{1+N}\frac{I_{SS}}{V_{SWING}}(L_{MIN}) \\ & \times \left(\mu_{eff,p} C_{ox} \left(V_{DD} - \left| V_{T,p} \right| \right) \right. \\ & \quad \times \left\{ 1 - \frac{R_{DSW} 10^{-6}}{L_{MIN}} \right. \\ & \qquad \left. \left. \times \left[\mu_{eff,p} C_{ox} \left(V_{DD} - \left| V_{T,p} \right| \right) \right] \right\} \right)^{-1}. \end{aligned} \tag{13}$$

Similarly, if the bias current is lower than I_{HIGH}, then R_P should be greater than R_{P_MIN}, and this is achieved by setting W_P to its minimum value, that is, W_{MIN} and L_P which is calculated by solving (3) and (4) as

$$\begin{aligned} L_P = {} & W_{MIN} \mu_{eff,p} C_{ox} \left(V_{DD} - \left| V_{T,p} \right| \right) \\ & \times \left(\frac{1+N}{N} \frac{V_{SWING}}{I_{SS}} - \frac{R_{DSW} 10^{-6}}{W_{MIN}} \right). \end{aligned} \tag{14}$$

The small-signal voltage gain (A_v) (9) has been used to size transistors $M_{LV3,4,5,6}$. Assuming minimum channel length for the said transistors, the width is computed as

$$W_N = \frac{2}{\mu_{eff,n} C_{ox}} \left(\frac{N}{1+N} \right)^2 \left(\frac{A_v}{V_{SWING}} \right)^2 I_{SS} L_{MIN}. \tag{15}$$

Sometimes (15) results in a value of W_N smaller than the minimum channel width. This happens when the bias current is lower than the current of the minimum sized NMOS transistor, I_{LOW}, given as

$$I_{LOW} = \frac{1}{2} \left(\frac{1+N}{N} \right)^2 \frac{W_{MIN}}{L_{MIN}} \mu_{eff,n} C_{ox} \left(\frac{V_{SWING}}{A_v} \right)^2 \quad \text{from (9)}. \tag{16}$$

Therefore, in such cases, W_N is also set to W_{MIN}. For proper switching, the width of transistors $M_{LV7,8}$ is made N times the width of transistors $M_{LV3,4,5,6}$.

The accuracy of the static model for the proposed D-latch is validated through SPICE simulations by using TSMC 0.18 μm CMOS process parameters and with a power supply of 1.1 V. The proposed D-latch was designed and simulated for wide range of operating conditions: voltage swing of 300 mV and 400 mV, small-signal voltage gain of 2 and 4, $N = 5$, and the bias current ranging from 10 μA to 100 μA. The designs were simulated, and the error in simulated and theoretical values for voltage swing, small-signal voltage gain, and noise margin using (8), (9), and (10), respectively, are calculated and are plotted in Figure 3. It may be noted that maximum error in voltage swing, small-signal voltage gain, and noise margin are 10%, 8%, and 14%, respectively.

Table 2: Effect of process variation on static parameters of the proposed and the traditional D-latch.

Parameter	NMOS T / PMOS T	NMOS F / PMOS F	NMOS S / PMOS S	NMOS F / PMOS S	NMOS S / PMOS F
V_{SWING} (mV)					
Proposed	427	590	327	447	417
Traditional	416	508	300	509	457
A_v					
Proposed	4.3	5.34	3.9	4.14	4.9
Traditional	4.34	4.42	4	4.46	5
NM (mV)					
Proposed	143	216	104	147	148
Traditional	139	172	97	173	163

Different design corners are denoted by T: typical, F: fast, and S: slow.
Simulation condition: $A_v = 4$, $V_{SWING} = 0.4$ V, $C_L = 100$ fF, and $I_{SS} = 100\,\mu$A.

The impact of parameter variation on proposed low-voltage and traditional MCML D-latch performance is studied at different design corners. The findings for various operating conditions are given in Table 2. It is found that the voltage swing, small-signal voltage gain, and noise margin of the proposed low-voltage D-latch varies by a factor of 1.8, 1.4, and 2.1, respectively, between the best and the worst cases. For the traditional MCML D-latch, the voltage swing, small-signal voltage gain, and noise margin vary by a factor of 1.7, 1.2, and 1.7, respectively, between the best and the worst cases. Thus, the proposed low-voltage D-latch shows slightly higher variations than those of the traditional MCML D-latch for different design corners which can be attributed to the smaller aspect ratio of transistors in the proposed low-voltage D-latch [8].

3.3. Delay Model. In this section, a delay model of the proposed D-latch is formulated in terms of bias current and the voltage swing. For a low-to-high transition on CLK input that causes output to switch by activating (deactivating) the transistor pair M_{LV3}-M_{LV4} (M_{LV5}-M_{LV6}), the circuit reduces to a simple MCML inverter. The equivalent linear half circuit is shown in Figure 4 where C_{gdi}, C_{dbi} represent the gate-drain capacitance and the drain-bulk junction capacitance of the ith transistor. For NMOS transistors operating in saturation region, C_{gd} is equal to the overlap capacitance $C_{gdo}W_n$

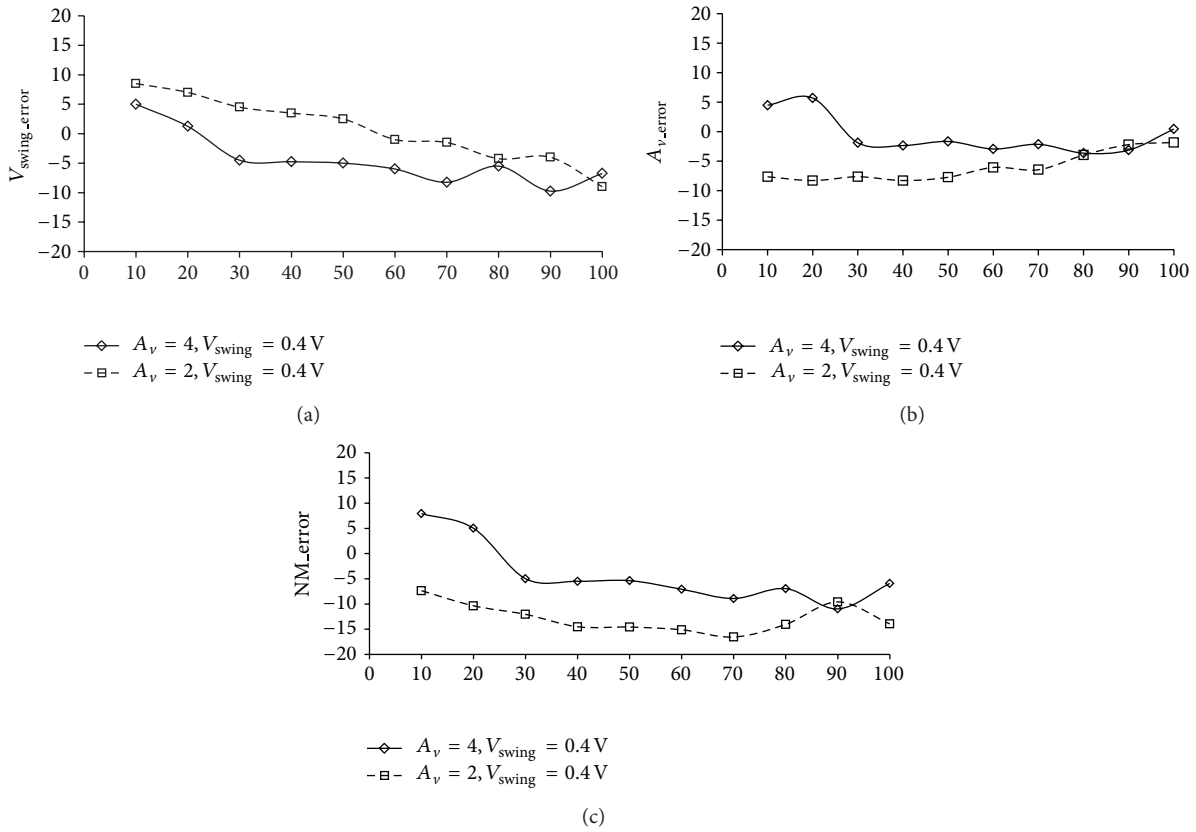

Figure 3: Errors in the static parameters (a) voltage swing, (b) small-signal voltage gain, and (c) noise margin.

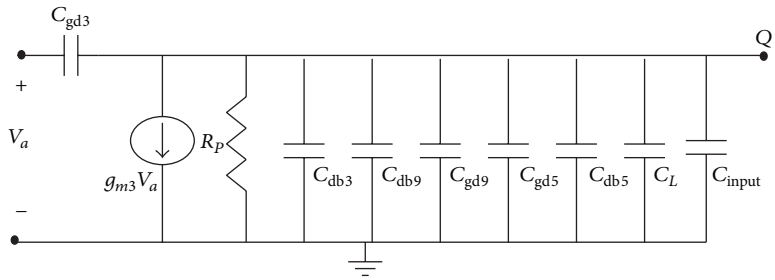

Figure 4: Linear half circuit (with low-to-high transition on CLK).

between the gate and the drain [26]. For the PMOS transistor operating in linear region, C_{gd} is evaluated as the sum of the overlap capacitance and the intrinsic contribution associated with its channel charge [26]. The junction capacitance C_{db} for the transistors is computed as explained in [27]. The input capacitance C_{input} represents the input capacitance of the source-coupled pair (M_{LV5}-M_{LV6}) [9].

The delay of the proposed D-latch can be expressed as

$$t_{PD} = 0.69\ R_P \left(C_{db3} + C_{gd3} + \ C_{gd9} + C_{db9} + C_{db5} + C_{gd5} + \ C_L + \ C_{input}\right) \quad (17)$$

with $C_{db3} = C_{db5}$, $C_{gd3} = C_{gd5}$ and, $R_P = ((1 + N)/N)(V_{SWING}/I_{SS})$; (17) can be rewritten as

$$t_{PD} = 0.69 \frac{1 + N}{N} \frac{V_{SWING}}{I_{SS}} \left(2C_{db3} + 2C_{gd3} + C_{gd9} + C_{db9} + C_L + C_{input}\right). \quad (18)$$

The capacitances may be expressed in terms of the bias current and the voltage swing as

$$C_{xy} = a_{xy} \frac{I_{SS}}{(V_{SWING})^2} + b_{xy} \frac{V_{SWING}}{I_{SS}} + c_{xy}, \quad (19)$$

Table 3: Coefficients of the capacitances for the proposed D-latch.

NMOS coefficients	
a_{db3}	$(2A_v^2 L_{MIN}/\mu_{eff,n}C_{ox})\,(N/(1+N))^2\,(K_{jn}C_{jn}L_{dn} + 2K_{jswn}C_{jswn})$
a_{gd3}	$2A_v^2 C_{gdo}(N/(1+N))^2\,(L_{MIN}/\mu_{eff,n}C_{ox})$
a_{input}	$(4A_v^2/3\mu_{eff,n})\,(N/(1+N))^2 {L_{MIN}}^2$
c_{db3}	$2K_{jswn}C_{jswn}L_{dn}$
$b_{db3}, b_{gd3}, c_{gd3}$	0
PMOS coefficients	
b_{gd9}	$(3/4)\,((1+N)/N)\,A_{bulk,max}\,\mu_{eff,p}C_{ox}^2 W_{MIN}^2\,(V_{DD} - \lvert V_{T,p}\rvert)$
c_{gd9}	$C_{gdo}W_{MIN} - (3/4)\;A_{bulk,max}\,\mu_{eff,p}C_{ox}^2 W_{MIN}\,(V_{DD} - \lvert V_{T,p}\rvert)\,R_{DSW}10^{-6}$
c_{db9}	$K_{jp}C_{jp}L_{dp}W_{MIN} + 2K_{jswp}C_{jswp}\,(L_{dp} + W_{MIN})$
$a_{gd9}, a_{db9}, b_{db9}$	0

The symbols have their usual meaning.

where C_{xy} is the capacitance between the terminals x and y and a_{xy}, b_{xy}, and c_{xy} are the associated coefficients. Using (14) and (15), various capacitances in (18) for I_{SS} ranging from I_{LOW} to I_{HIGH} may be expressed as

$$C_{gd3} = C_{gdo}W_3 = 2A_v^2 C_{gdo}\left(\frac{N}{1+N}\right)^2 \frac{L_{MIN}}{\mu_{eff,n}C_{OX}}\frac{I_{SS}}{(V_{SWING})^2}, \tag{20}$$

where C_{gdo} is the drain-gate overlap capacitance per unit transistor width. Consider the following:

$$\begin{aligned} C_{db3} &= W_3\left(K_{jn}C_{jn}L_{dn} + 2K_{jswn}C_{jswn}\right) + 2K_{jswn}C_{jswn}L_{dn} \\ &= 2A_v^2\frac{L_{MIN}}{\mu_{eff,n}C_{OX}}\left(\frac{N}{1+N}\right)^2\left(K_{jn}C_{jn}L_{dn} + 2K_{jswn}C_{jswn}\right) \\ &\quad\times\frac{I_{SS}}{(V_{SWING})^2} \\ &\quad+\; 2K_{jswn}C_{jswn}L_{dn}, \end{aligned} \tag{21}$$

where C_{jn}, C_{jswn} are the zero-bias junction capacitance per unit area and zero-bias sidewall capacitance per unit parameter, respectively. The coefficients K_{jn}, K_{jswn} are the voltage equivalence factor for the junction and the sidewall capacitances [27]. Parameter L_{dn} is extrapolated from design rules [9]. Consider the following:

$$\begin{aligned} C_{input} &= \frac{2}{3}C_{ox}L_{MIN}W_5 \\ &= \frac{4}{3\mu_{eff,n}}\left(\frac{N}{1+N}\right)^2\left(\frac{A_v}{V_{SWING}}\right)^2 I_{SS}{L_{MIN}}^2, \end{aligned} \tag{22}$$

$$C_{gd9} = C_{gdo}W_{MIN} + \frac{3}{4}A_{bulk,max}\;W_{MIN}L_P C_{ox} \tag{23a}$$

$$\begin{aligned} &= C_{gdo}W_{MIN} + \frac{3}{4}A_{bulk,max}W_{MIN}C_{ox} \\ &\quad\times\left\{\mu_{eff,p}C_{ox}W_{MIN}\left(V_{DD} - \lvert V_{T,p}\rvert\right)\right. \\ &\quad\left.\times\left[\frac{1+N}{N}\frac{V_{SWING}}{I_{SS}} - \frac{R_{DSW}10^{-6}}{W_{MIN}}\right]\right\}, \end{aligned} \tag{23b}$$

where $A_{bulk,max}$ is a parameter defined in BSIM3v3 model [24]. Consider the following:

$$\begin{aligned} C_{db9} &= W_{MIN}\left(K_{jp}C_{jp}L_{dp} + 2K_{jswp}C_{jswp}\right) \\ &\quad+ 2K_{jswp}C_{jswp}L_{dp}, \end{aligned} \tag{24}$$

where C_{jp}, C_{jswp} are the zero-bias junction capacitance per unit area and zero-bias sidewall capacitance per unit parameter respectively. The coefficients K_{jp}, K_{jswp} are the voltage equivalence factor for the junction and the sidewall capacitances of the PMOS transistor, respectively [27]. Parameter L_{dp} is extrapolated from design rules [9]. The coefficients a_{xy}, b_{xy}, and c_{xy} of all the capacitances in (18) are summarized in Table 3. Using (20)–(24), (18) can be written as

$$\begin{aligned} t_{PD} &= 0.69\frac{1+N}{N}V_{SWING} \\ &\quad\times\left(\frac{a}{{V_{SWING}}^2} + b\frac{V_{SWING}}{I_{SS}^2} + \frac{c + C_L}{I_{SS}}\right), \end{aligned} \tag{25}$$

where

$$a = 2a_{db3} + 2a_{gd3} + a_{input} \tag{26a}$$

$$b = b_{gd9} \tag{26b}$$

$$c = 2c_{db3} + c_{gd9} + c_{db9}. \tag{26c}$$

Table 4: Effect of process variation on the delay of the proposed and the traditional D-latch.

Parameter	NMOS T PMOS T	NMOS F PMOS F	NMOS S PMOS S	NMOS F PMOS S	NMOS S PMOS F
t_{PD} (ps)					
Proposed	467	380	580	410	430
Traditional	589	565	984	587	590

Simulation condition: $A_v = 4$, $V_{SWING} = 0.4$ V, $C_L = 100$ fF, and $I_{SS} = 100\,\mu$A.

The delay model can also be used for I_{SS} value outside the range $[I_{LOW}, I_{HIGH}]$. This is because for $I_{SS} > I_{HIGH}$, the capacitance coefficients of PMOS transistor in (25) differ as explained in Section 3.2. But since for high values of I_{SS}, the capacitive contribution of PMOS transistor is negligible, therefore (25) can predict the delay. Similarly, for $I_{SS} < I_{LOW}$, the capacitance coefficients of NMOS transistor in (25) differ. But since for low values of I_{SS}, the delay majorly depends on the capacitances of PMOS transistor, so expression (25) can estimate the delay of the proposed D-latch.

The accuracy of the delay model for the proposed D-latch is validated through SPICE simulations by using TSMC 0.18 μm CMOS process parameters and with a power supply of 1.1 V. The proposed D-latch was designed for wide range of operating conditions: voltage swing of 300 mV and 400 mV, small-signal voltage gain of 2 and 4, the bias current ranging from 10 μA to 100 μA, $N = 5$, and load capacitance of 0 fF, 10 fF, 100 fF, and 1 pF. It is found that there is a close agreement between the simulated and the predicted delay for all the operating conditions. The simulated and the predicted delay in particular for NM = 130 mV and $Av = 4$ and with different load capacitances are plotted in Figure 5.

The impact of parameter variation on proposed low-voltage and traditional MCML D-latches delay is studied at different design corners. The findings for various operating conditions are given in Table 4. It is found that the propagation delay of the proposed low-voltage D-latch varies by a factor of 1.8 between the best and the worst cases. For the traditional MCML D-latch, the delay varies by a factor of 1.7 between the best and the worst cases. Thus, the proposed low-voltage D-latch shows slightly higher variation than the traditional MCML D-latch in delay for different design corners which can be attributed to the smaller aspect ratio of transistors in the proposed low-voltage D-latch [8].

4. Design Cases

In the previous section, the proposed D-latch has been modeled, and different parameters are expressed as a function of bias current and voltage swing. In practice, the voltage swing is set on the basis of the specified noise margin while the bias current is chosen according to power-delay considerations. Therefore, the proposed low-voltage D-latch for high-speed and power-efficient design cases is discussed.

4.1. High-Speed Design. A high-speed design requires bias current that results in minimum delay. The delay (25) decreases with the increasing I_{SS} and tends to an asymptotic minimum value of 0.69 $((1 + N)/N)(a/V_{SWING})$ for $I_{SS} \to \infty$. A substantial improvement in delay with increasing bias current is achieved if condition

$$\frac{a}{V_{SWING}{}^2} \geq b\frac{V_{SWING}}{I_{SS}^2} + \frac{c + C_L}{I_{SS}} \tag{27}$$

is satisfied. However, high value of bias current results in large transistor sizes. Therefore, the bias current should be set to such a value after which the improvement in speed is not significant. If equality sign in (27) is considered, then the delay is close to its minimum value, and the use of high bias current is avoided. Therefore, this assumption leads to a bias current (I_{SS_HS}) and delay (t_{PD_MIN}) as

$$I_{SS\_HS} = \frac{c + C_L}{2a} V_{SWING}^2 \left(1 + \sqrt{1 + 4\,\frac{ab}{(c + C_L)^2}\frac{1}{V_{SWING}}}\right) \tag{28}$$

$$t_{PD\_MIN} = 2 \times 0.69\,\frac{1 + N}{N}\frac{a}{V_{SWING}}. \tag{29}$$

The proposed high-speed D-latch, designed with a power supply of 1.1 V, noise margin of 130 mV, small-signal gain of 4, $N = 5$, and load capacitance of 100 fF, gives I_{SS_HS} as 254 μA. A delay of 265 ps and 255 ps is obtained from (29) and simulations, respectively. On the contrary, a traditional high-speed D-latch designed using the method outlined in [24] and with power supply of 1.4 V for the same specifications results in a delay of 598 ps. This indicates that the proposed D-latch can achieve a much higher speed than the traditional one.

4.2. Power-Efficient Design. A power-efficient design requires a bias current that results in minimum power-delay product (PDP). The power is calculated as the product of V_{DD} and I_{SS}. So, the PDP of the proposed D-latch may be expressed as

$$\begin{aligned} \text{PDP} = {} & 0.69\,V_{DD}V_{SWING}\frac{1 + N}{N} \\ & \times \left(\frac{a}{V_{SWING}{}^2}I_{SS} + b\frac{V_{SWING}}{I_{SS}} + c + C_L\right). \end{aligned} \tag{30}$$

Therefore, the current I_{SS_PDP} for minimum PDP may be given as

$$I_{SS\_PDP} = \sqrt{\frac{b}{a}}(V_{SWING})^{3/2}. \tag{31}$$

Accordingly, the minimum PDP results in

$$\text{PDP} = 0.69\,V_{DD}V_{SWING}\frac{1 + N}{N}\left(\frac{2\sqrt{ab}}{\sqrt{V_{SWING}}} + c + C_L\right). \tag{32}$$

The proposed power-efficient D-latch, designed with a power supply of 1.1 V, noise margin of 130 mV, small signal gain of 4,

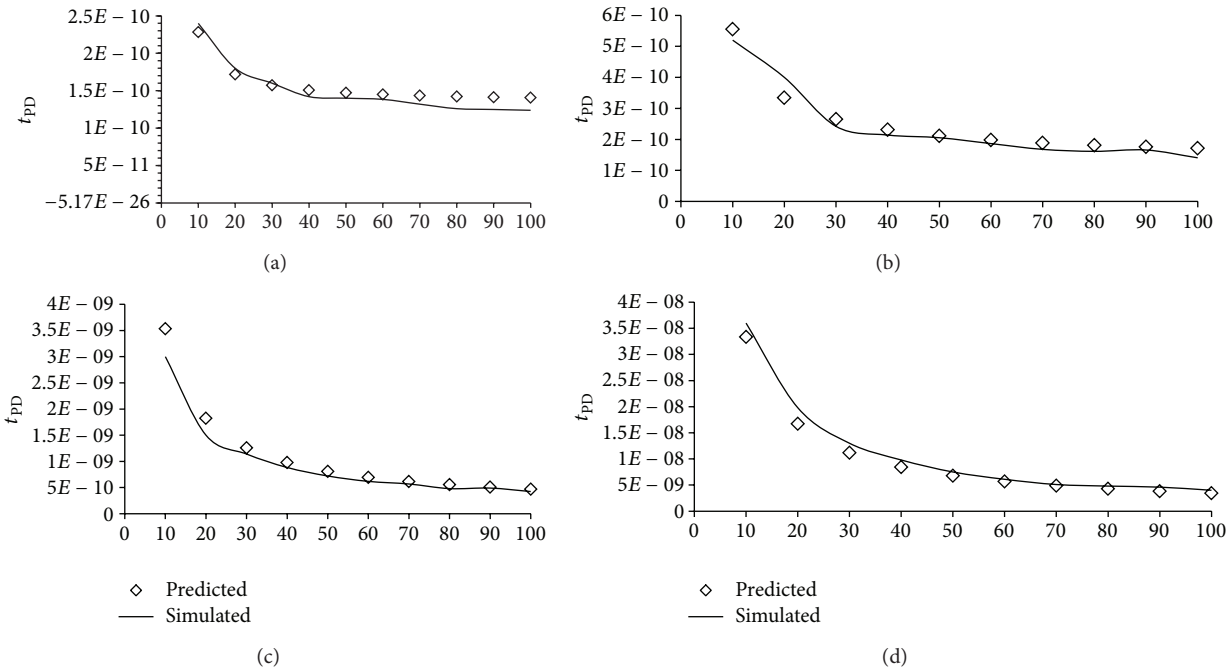

FIGURE 5: Simulated and predicted delay of proposed D-latch versus I_{SS} with NM = 130 mV, $A_v = 4$, and different load capacitances (a) $C_L = 0$ fF, (b) $C_L = 10$ fF, (c) $C_L = 100$ fF, and (d) $C_L = 1$ pF.

$N = 5$, and load capacitance of 100 fF, gives I_{SS_PDP} as 5.3 μA. A PDP value of 38.5 fJ has been obtained for the proposed D-latch. On the other hand, a traditional power-efficient D-latch designed using the method outlined in [24] and with power supply of 1.4 V for the same specifications results in a PDP value of 24 fJ. The result signifies that the proposed D-latch results in higher PDP values than the traditional one.

5. Conclusions

A new low-voltage MCML D-latch based on the triple-tail cell concept is proposed. Its static parameters are analytically modeled and are used to develop a design approach for the proposed low-voltage MCML D-latch. The delay is formulated as a function of the bias current and the voltage swing and is traded off with power consumption for high-speed and power-efficient design cases. It is found that the proposed low-voltage D-latch is better than those of the traditional MCML D-latch for the high-speed design case.

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