

## Research Article

# Novel Basic Block of Multilevel Inverter Using Reduced Number of On-State Switches and Cascaded Circuit Topology

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Received 22 November 2016; Revised 7 March 2017; Accepted 21 March 2017; Published 18 April 2017

Academic Editor: George E. Tsekouras

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In this paper a basic block of novel topology of multilevel inverter is proposed. The proposed approach significantly requires reduced number of dc voltage sources and power switches to attain maximum number of output voltage levels. By connecting basic blocks in series a cascaded multilevel topology is developed. Each block itself is also a multilevel inverter. Analysis of proposed topology is carried out in symmetric as well as asymmetric operating modes. The topology is investigated through computer simulation using MATLAB/Simulink and validated experimentally on prototype in the laboratory.

## 1. Introduction

Recently, multilevel inverter technology has become popular in industry for medium and high voltage applications. Hi-Tech industry demands quality electric power that multilevel inverter technology can supply. Multilevel inverter uses number of power semiconductor devices, dc sources (batteries/capacitors) to synthesize staircase output voltage waveform. By increasing number of levels the output voltage waveform approaches near to sine wave improving its quality. As compared to traditional two-level inverter it generates high quality output voltage using low switching frequency with low harmonic distortion. Other advantages of this technology are lower switching losses, have more efficiency, have low voltage stress on power switches, have low electromagnetic interference, and have low  $dv/dt$  stress on load. Due to these advantages they found wide applications in adjustable speed drives, HVDC, FACTS, wind farms, photovoltaic systems, electric vehicles, and so on [1–3].

The popular commercially available topologies of multilevel inverter are neutral point clamped (NPC) proposed by Nabae et al. [4], flying capacitor (FC) proposed by

Meynard and Foch [5], and cascaded H bridge (CHB) proposed by Peng and Lai [6]. NPC is also known as diode clamped (DC) multilevel inverter which is well-known as first generation of multilevel technology. It was basically a three-level inverter and known as state-of-the-art of multilevel technology. The FC topology is an alternative to NPC topology which uses capacitors in ladder form to clamp voltage instead of diodes. To generate higher levels both topologies, NPC and FC, require many components and also suffer due to capacitor voltage imbalance problem [7]. In CHB, H-bridges with separate dc sources of equal magnitude are connected in series. This characteristic makes the topology modular. Total output voltage is obtained by adding voltages generated by each H-bridge. Each H-bridge generates three voltage levels. This is an appropriate topology to generate large number of levels as it requires less number of components.

Recently, some new multilevel inverter topologies have been presented. It includes asymmetric and/or hybrid inverters [8]. In asymmetric topology unequal dc source magnitudes are used while hybrid inverters are designed by using different topologies, applying different modulation techniques or semiconductor technologies.

Nowadays, research is engaged to develop novel topologies with objectives to reduce number of components, dc sources, and complexity of the circuit [9–12]. Total harmonic distortion for output voltage waveform, power losses, and voltage stress on power switches are also optimization factors while designing novel topologies [13]. Some of the recently proposed multilevel inverter topologies with reduced power switch count are reviewed and analysed in [14].

**1.1. Related Work.** In order to increase the number of output voltage levels, various new cascaded topologies are presented. In [15], a new basic unit for a cascaded multilevel inverter is proposed. By the series connection of several basic units, a cascaded multilevel inverter can generate positive levels at the output. In order to generate all voltage levels an H-bridge is added to the proposed inverter. Four different algorithms are proposed to determine the magnitude of the dc voltage sources, to generate even and odd voltage levels at the output.

In [16], a novel 17-level inverter configuration is presented. This configuration is formed by cascading a three-level flying capacitor and three floating capacitor H-bridges. It uses single dc power supply. It can control capacitor voltage during inverter switching cycles.

A new type of cascaded modular multilevel inverters (CMMLIs) is presented in [17]. It can produce a considerable number of output voltage levels with a reasonable number of components. Two same basic units are connected in each series stage of the proposed CMMLI. To determine an appropriate value for the dc sources' magnitude four different algorithms are also presented in this paper.

A new module named Envelope Type (E-Type) module for cascaded multilevel inverter is proposed in [18]. It can generate 13 levels with reduced components. In [19], a new general multilevel inverter topology based on cascade connection of submultilevel units is presented. This topology uses reduced switching components, dc voltage sources, and blocked voltage by switches. The topology can be used in high voltage applications as it uses the switches with low voltage rating. In [20], single phase  $\pi$ -type five-level inverter using three-terminal switch-network is proposed. For multilevel power inversion this new structure is suitable with low dc-bus voltage. Using only four active power switches five-level operation can be attained.

A new cascaded seven-level inverter is developed in [21]. It uses single dc source and switched capacitor technique. The proposed topology substitutes all the separate dc voltage sources with capacitors, as compared with the conventional cascaded multilevel inverter. In [22], a new topology of six-level inverter is proposed. It consists of flying capacitor inverter units inside and two-level inverter units outside. It is suitable for medium-voltage high power applications. A new symmetric cascade multilevel inverters structure is presented in [23]. This structure requires minimum number of power electronic components, gate driver circuits, a power diode, and a dc voltage source. In [24], a new method for generating higher number of output voltage levels by stacking multilevel converters with lower voltage space vector structures is presented. Low voltage devices are used in

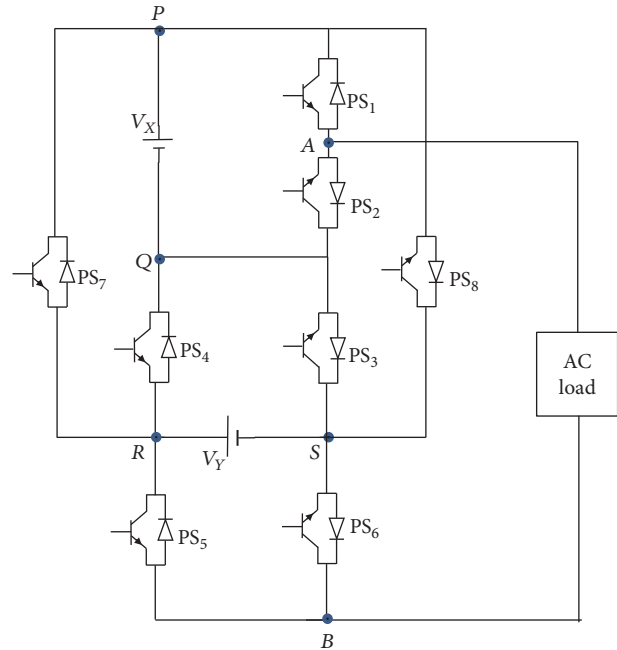


FIGURE 1: Basic block of proposed multilevel inverter topology.

stacked structure. It can be used in electric vehicles as direct battery drive is possible. A new fundamental switch-ladder multilevel inverter structure and cascade switch-ladder multilevel inverter topology are presented in [25]. To generate maximum number of levels with minimum number of switching elements, dc sources, and voltage on switches, the proposed cascade topology is optimized.

In this paper, a basic unit of new multilevel inverter topology is suggested. This single unit can generate different output voltage levels. Also in order to generate higher levels a cascaded topology with series connection of basic blocks is proposed. The detailed working of proposed topology is presented. Also, analysis is carried out in both symmetric and asymmetric operating modes. The proposed structure uses minimum number of on-state switches and dc sources as compared to topologies presented in literature.

The rest of the paper is organized as follows. Section 2 presents basic block of proposed topology. Detailed operation of proposed topology is described in this section. In Section 3 a generalized cascaded circuit topology and seven different combinations to select magnitude of dc voltage sources for this circuit are addressed. Section 4 contains calculation of standing voltage of switches. Section 5 presents the comparison among seven different combinations as well as with conventional topologies of CHB. Simulation and experimental results for laboratory prototype are given in Section 6. Finally conclusions are summarized in Section 7.

## 2. Proposed Topology

The basic block of proposed multilevel inverter topology is shown in Figure 1. It consists of eight power semiconductor switches ( $PS_1, PS_2, PS_3, PS_4, PS_5, PS_6, PS_7,$  and  $PS_8$ ) and two

TABLE 1: Switching sequence and output voltages of proposed topology.

Sw. mode	PS <sub>1</sub>	PS <sub>2</sub>	PS <sub>3</sub>	PS <sub>4</sub>	PS <sub>5</sub>	PS <sub>6</sub>	PS <sub>7</sub>	PS <sub>8</sub>	Output voltage
1	1	0	0	1	0	1	0	0	$V_X + V_Y$
2	1	0	1	0	0	1	0	0	$V_X$
2'	1	0	0	1	1	0	0	0	$V_X - V_Y$
3	1	0	1	0	1	0	0	0	$V_X - V_Y$
4	0	1	0	1	0	1	0	0	$V_Y$
4'	1	0	0	0	0	1	1	0	$V_Y$
5	0	1	1	0	0	1	0	0	0
5'	0	1	0	1	1	0	0	0	0
6	0	1	1	0	1	0	0	0	$-V_Y$
6'	1	0	0	0	1	0	0	1	$-V_Y$
7	0	1	0	0	0	1	1	0	$-V_X + V_Y$
8	0	1	0	0	1	0	1	0	$-V_X$
8'	0	1	0	0	0	1	0	1	$-V_X$
9	0	1	0	0	1	0	0	1	$-V_X - V_Y$

TABLE 2: Output voltage levels and magnitudes for symmetric and asymmetric mode of operation.

Sr. number	Output voltage	Symmetric mode		Asymmetric mode	
		$V_{AB}$ for $V_X = V_Y = E$	$V_{AB}$ for $V_X = 2E, V_Y = E$	$V_{AB}$ for $V_X = 3E, V_Y = E$	$V_{AB}$ for $V_X = 3E, V_Y = E$
1	$V_X + V_Y$	$2E$	$3E$	$4E$	$4E$
2	$V_X$	$E$	$2E$	$3E$	$3E$
3	$V_X - V_Y$	0	$E$	$2E$	$2E$
4	$V_Y$	$E$	$E$	$E$	$E$
5	0	0	0	0	0
6	$-V_Y$	$-E$	$-E$	$-E$	$-E$
7	$-V_X + V_Y$	0	$-E$	$-2E$	$-2E$
8	$-V_X$	$-E$	$-2E$	$-3E$	$-3E$
9	$-V_X - V_Y$	$-2E$	$-3E$	$-4E$	$-4E$

dc voltage sources ( $V_X$  and  $V_Y$ ). When voltage sources are of equal magnitude ( $V_X = V_Y = E$ ), the basic block operates in symmetric mode and generates five levels at output (two positive, two negative, and zero). However in order to generate more output levels unequal magnitudes of voltage sources can be selected and the basic block operates in asymmetric mode.

(i) Case I:  $V_X = 2 \times V_Y$ ; it can generate seven levels at output (three positive, three negative, and zero).

(ii) Case II:  $V_X = 3 \times V_Y$ ; it can generate nine levels at output (four positive, four negative, and zero).

Table 1 shows switching sequence and output voltages generated for both symmetric and asymmetric mode of operation.

**2.1. Operation of Basic Block of Proposed Topology.** The operation of proposed topology is explained using single phase basic block shown in Figure 1. It consists of two voltage sources  $V_X$  and  $V_Y$  and eight semiconductor switches. Each switch consists of a MOSFET/IGBT with antiparallel diode

and has two operating states. The sequence of operation of all possible states is shown in Figure 2. It is seen that only three switches are conducting in any switching mode. The load is supplied by different voltage levels. According to magnitude of voltage sources selected the same basic block generates five-level, seven-level, or nine-level output voltage as shown in Table 2.

### 3. Generalized Cascaded Circuit Topology

The generalized cascaded circuit can be formed by connecting  $n$  number of basic blocks in series. The number of output voltage levels increases by this series connection. Figure 3 shows generalized cascaded circuit. The sum of output voltages of all the blocks connected in series gives total output voltage of cascaded circuit.

$$V_L = V_{01} + V_{02} + \dots + V_{0n}$$

$$V_L = \sum_{k=1}^n V_{0k} \quad (1)$$

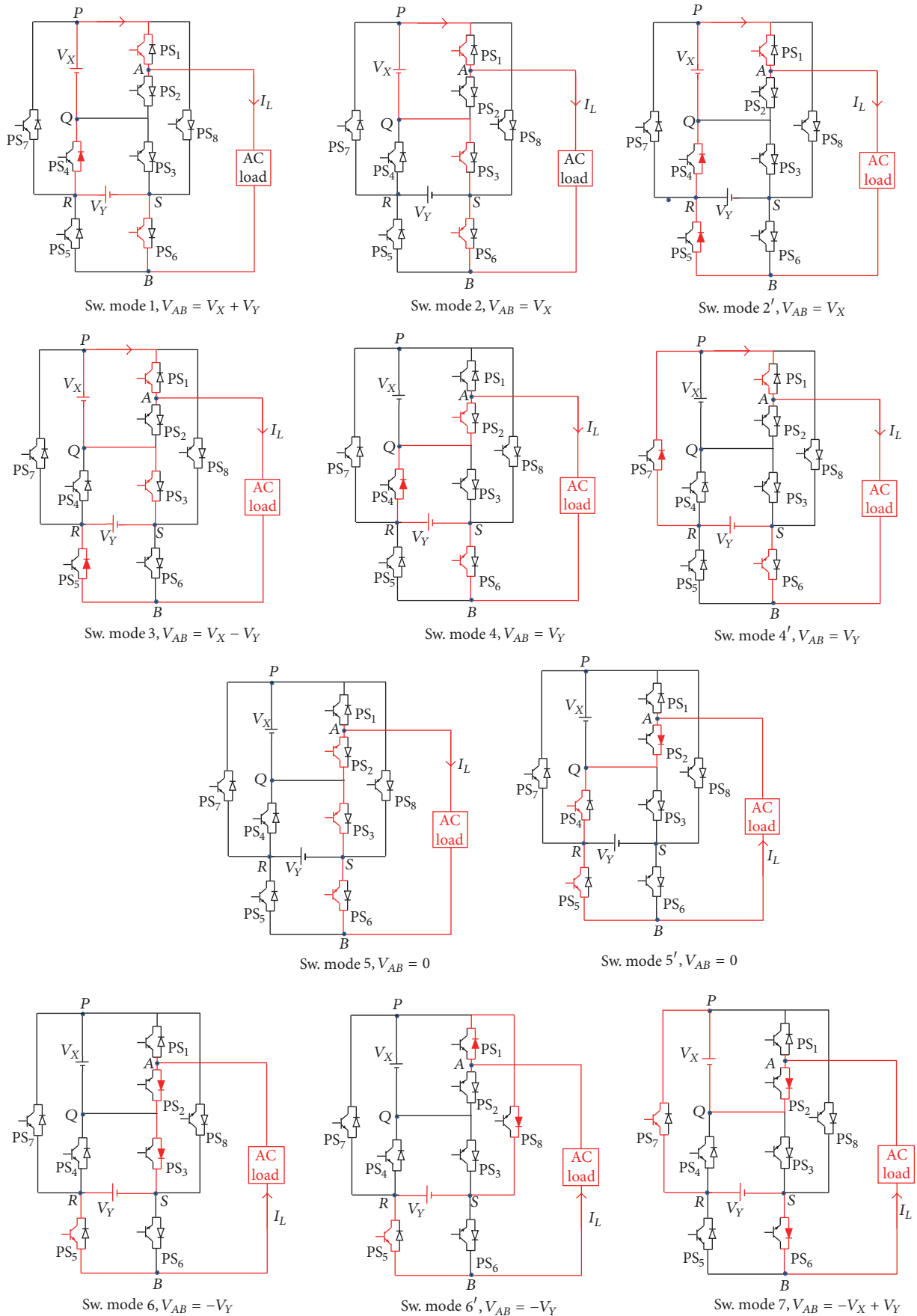


FIGURE 2: CONTINUED.

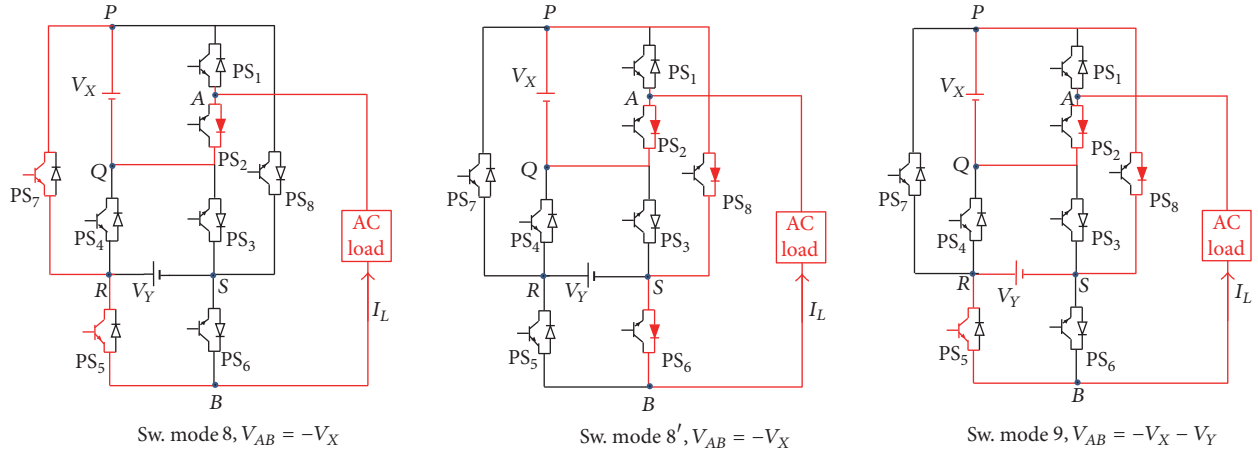


FIGURE 2: Sequence of operation of all possible states of proposed multilevel inverter topology.

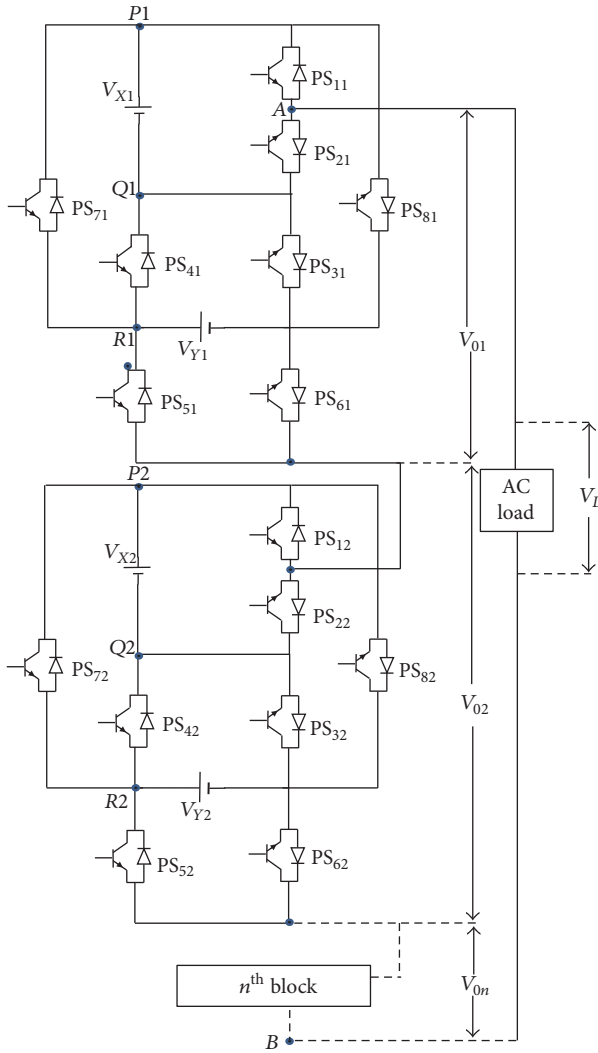


FIGURE 3: Cascaded circuit multilevel inverter topology.

Here  $k$  is number of units connected in series to form cascaded circuit.

The following expressions present number of power switches and number of dc sources required for cascaded circuit of proposed topology.

$$N_{PS} = 8 \times n$$

$$N_{dc} = 2 \times n.$$
(2)

Different combination of dc voltage source magnitudes can be selected for operation of this cascaded circuit. It can enrich performance of multilevel inverter and can also increase the number of levels. Seven different combinations to select magnitude of dc voltage sources are discussed here.

3.1. *First Combination (C1)*. This arrangement consists of series connection of  $n$  basic blocks with equal magnitude of dc voltage sources called symmetric blocks. The following equations can be written:

$$V_{X(k)} = V_{Y(k)} = E \quad \text{where } k = 1, 2, 3, \dots, n$$

$$V_m^k = 2E$$

$$V_m = 2nE.$$
(3)

$V_m^k$  is maximum output voltage of  $k$ th block and  $V_m$  is total maximum output voltage of cascaded circuit. The number of levels obtained in this combination is

$$N_l = 4n + 1.$$
(4)

Consider that two basic blocks are connected in this arrangement, and then according to above equations the following calculations can be written:

$$V_{X(1)} = V_{Y(1)} = V_{X(2)} = V_{Y(2)} = E$$

$$V_m^1 = V_m^2 = 2E;$$

$$V_m = 4E$$

$$N_l = 9.$$
(5)

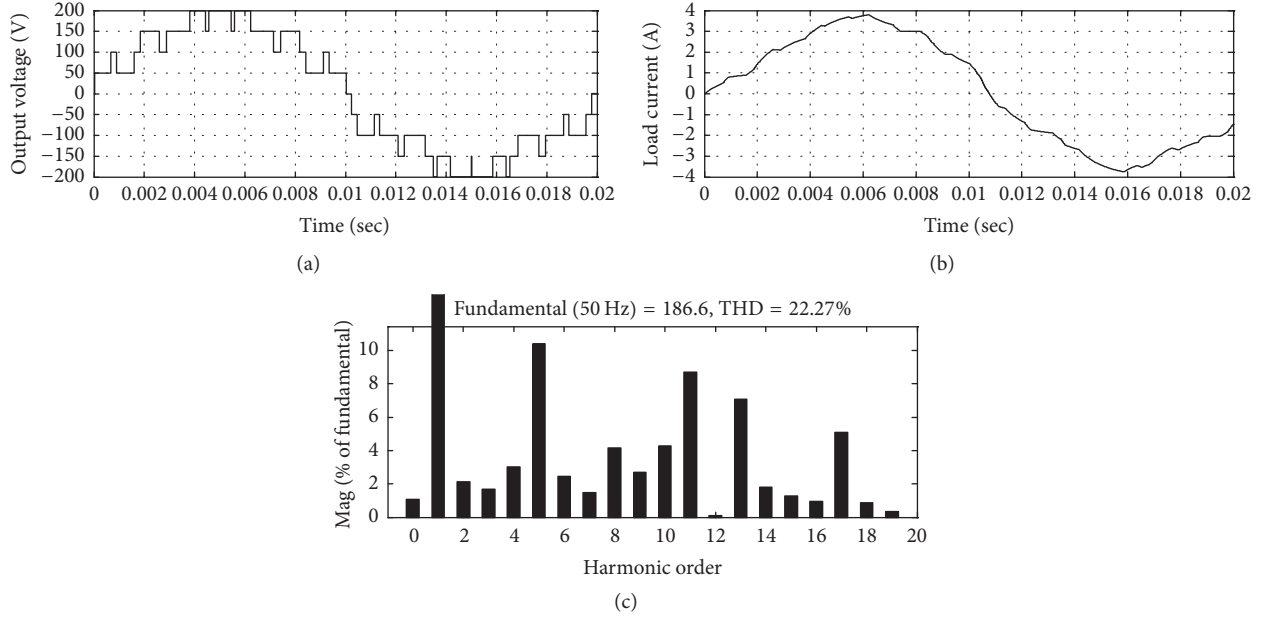


FIGURE 4: Simulation result for nine-level cascaded circuit of multilevel inverter. (a) Output Voltage. (b) Load current. (c) Harmonic contents of output voltage.

In this arrangement four dc sources of equal magnitudes are used. Figure 4 shows that simulation results for the arrangement with  $E$  are equal to 50 V.

3.2. *Second Combination (C2)*. The magnitude of dc voltage sources can be selected as follows for this structure:

$$\begin{aligned} V_{X(k)} &= 2E, \\ V_{Y(k)} &= E. \end{aligned} \quad (6)$$

Other equations are

$$\begin{aligned} V_m^k &= 3E \\ V_m &= 3nE \\ N_l &= 6n + 1, \end{aligned} \quad (7)$$

where  $N_l, n$  represent the number of levels and number of basic blocks connected in series.

To illustrate the structure, two basic blocks are considered for cascaded circuit, which gives the following calculations:

$$\begin{aligned} V_{X(1)} &= V_{X(2)} = 2E; \\ V_{Y(1)} &= V_{Y(2)} = E \\ V_m^1 &= V_m^2 = 3E; \\ V_m &= 6E \\ N_l &= 13. \end{aligned} \quad (8)$$

In this structure four dc sources of two varieties of magnitude and 16 switches generate 13 levels of output

voltage with maximum and minimum level of  $+6E$  and  $-6E$ , respectively. Figure 5 shows simulation results.  $E$  is supposed to be 50 V.

3.3. *Third Combination (C3)*. Proposed values of dc voltage sources in this structure are described with the following equation:

$$\begin{aligned} V_{X(k)} &= 3E, \\ V_{Y(k)} &= E. \end{aligned} \quad (9)$$

It results in

$$\begin{aligned} V_m^k &= 4E \\ V_m &= 4nE \\ N_l &= 8n + 1. \end{aligned} \quad (10)$$

This mode of operation is explained assuming two basic blocks connected in series which gives the following results:

$$\begin{aligned} V_{X(1)} &= V_{X(2)} = 3E; \\ V_{Y(1)} &= V_{Y(2)} = E \\ V_m^1 &= V_m^2 = 4E; \\ V_m &= 8E \\ N_l &= 17. \end{aligned} \quad (11)$$

Output voltage waveform of this 17 level inverter based on this structure is shown in Figure 6.  $E$  is supposed to be 50 V.

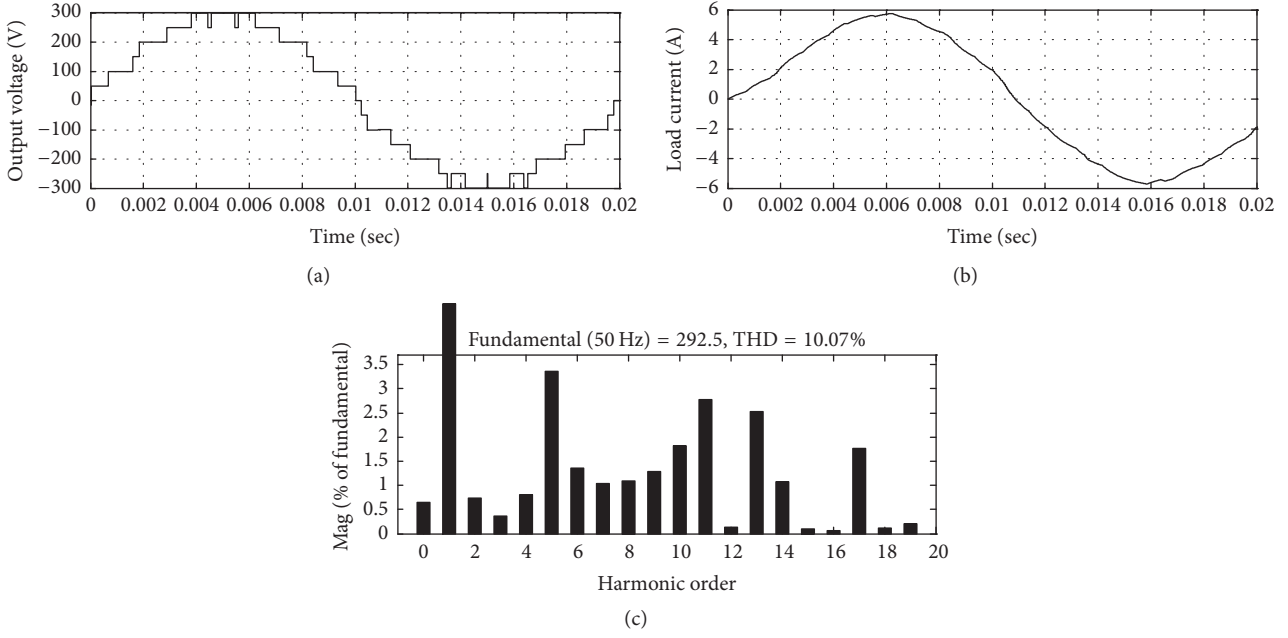


FIGURE 5: Simulation result for thirteen-level cascaded circuit of multilevel inverter. (a) Output voltage. (b) Load current. (c) Harmonic contents of output voltage.

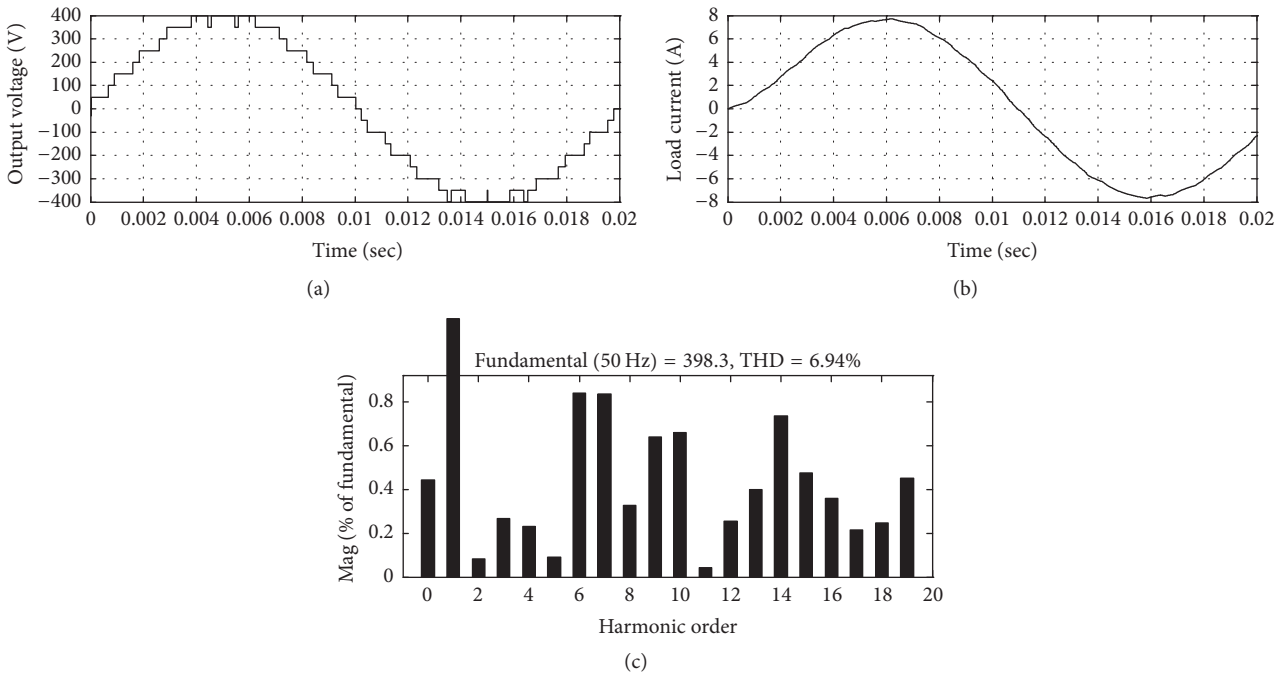


FIGURE 6: Simulation result for seventeen-level cascaded circuit of multilevel inverter. (a) Output voltage. (b) Load current. (c) Harmonic contents of output voltage.

3.4. *Fourth Combination (C4)*. In this combination the values of dc voltage sources are determined according to the following equation:

$$\begin{aligned} V_{X(k)} &= 2V_{Y(k)} \\ V_{Y(k)} &= 2^{(k-1)}E. \end{aligned} \tag{12}$$

For this combination other equations can be written as

$$\begin{aligned} V_m^k &= 3 \times 2^{(k-1)} \times E \\ V_m &= 3 \times (2^n - 1) \times E \\ N_l &= (3 \times 2^{n+1}) - 5. \end{aligned} \tag{13}$$

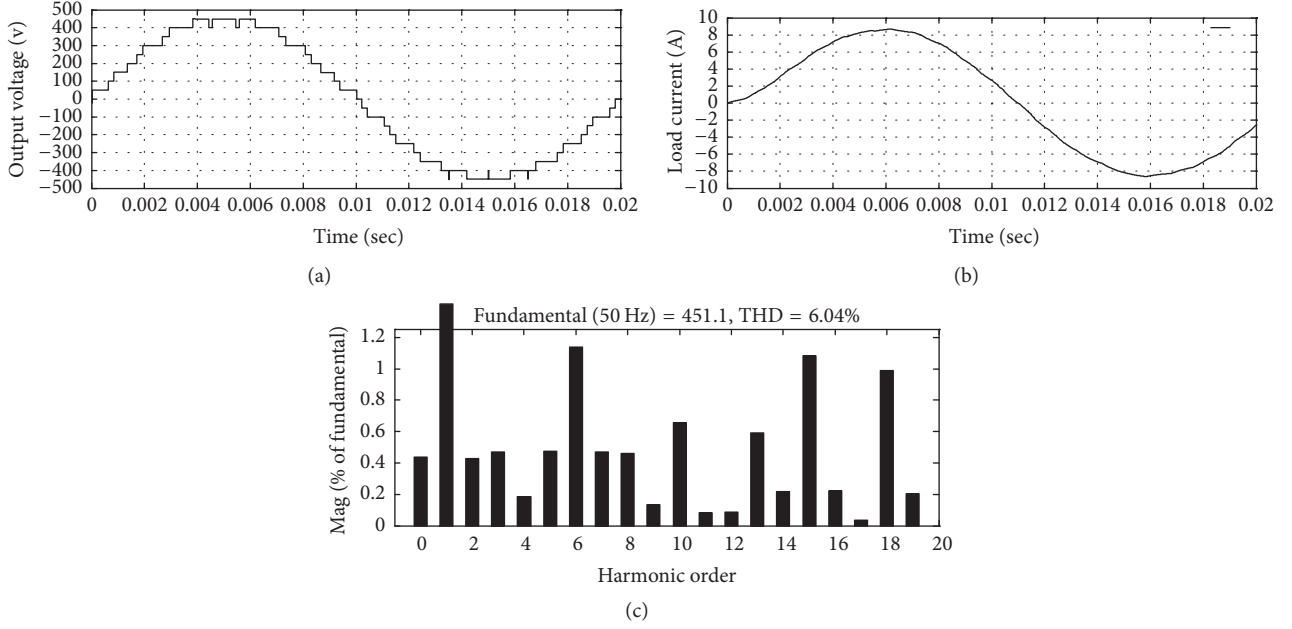


FIGURE 7: Simulation result for nineteen level cascaded circuit of multilevel inverter. (a) Output voltage. (b) Load current. (c) Harmonic contents of output voltage.

In the above equations,  $N_l, n$  represent the number of output voltage levels and number of basic blocks used in series.

To analyse the structure, two fundamental blocks are assumed for cascaded circuit. The values of sources, according to (12), can be calculated as

$$\begin{aligned}
 V_{X(1)} &= 2E, \\
 V_{Y(1)} &= E; \\
 V_{X(2)} &= 4E, \\
 V_{Y(2)} &= 2E \\
 V_m^1 &= 3E, \\
 V_m^2 &= 6E; \\
 V_m &= 9E \\
 N_{\text{level}} &= 19.
 \end{aligned} \tag{14}$$

Considering the above, employing four dc sources with three varieties of magnitude and 16 switches, 19 levels of output voltage are obtainable with maximum and minimum level of  $+9E$  and  $-9E$ , respectively. Figure 7 shows simulation results.  $E$  is assumed to be 50 V.

**3.5. Fifth Combination (C5).** The following equations are used for this combination:

$$\begin{aligned}
 V_{X(k)} &= V_{Y(k)} = 5^{(k-1)}E \\
 V_m^k &= 2 \times 5^{(k-1)} \times E
 \end{aligned}$$

$$V_m = \frac{(5^n - 1)}{2} \times E$$

$$N_l = 5^n.$$

(15)

To illustrate the arrangement, two-block cascaded circuit is assumed, which gives the following calculations:

$$V_{X(1)} = V_{Y(1)} = E;$$

$$V_{X(2)} = V_{Y(2)} = 5E$$

$$V_m^1 = 2E;$$

$$V_m^2 = 10E$$

$$V_m = 12E$$

$$N_l = 25.$$

(16)

In this structure, using 16 switches, 25 levels of output voltage can be generated. Figure 8 shows simulation results.  $E$  is supposed to be 20 V.

**3.6. Sixth Combination (C6).** The following equations are written for this structure. It gives considerable increment in the number of output voltage levels.

$$V_{X(k)} = 3V_{Y(k)}$$

$$V_{Y(k)} = 3^{(k-1)}E$$



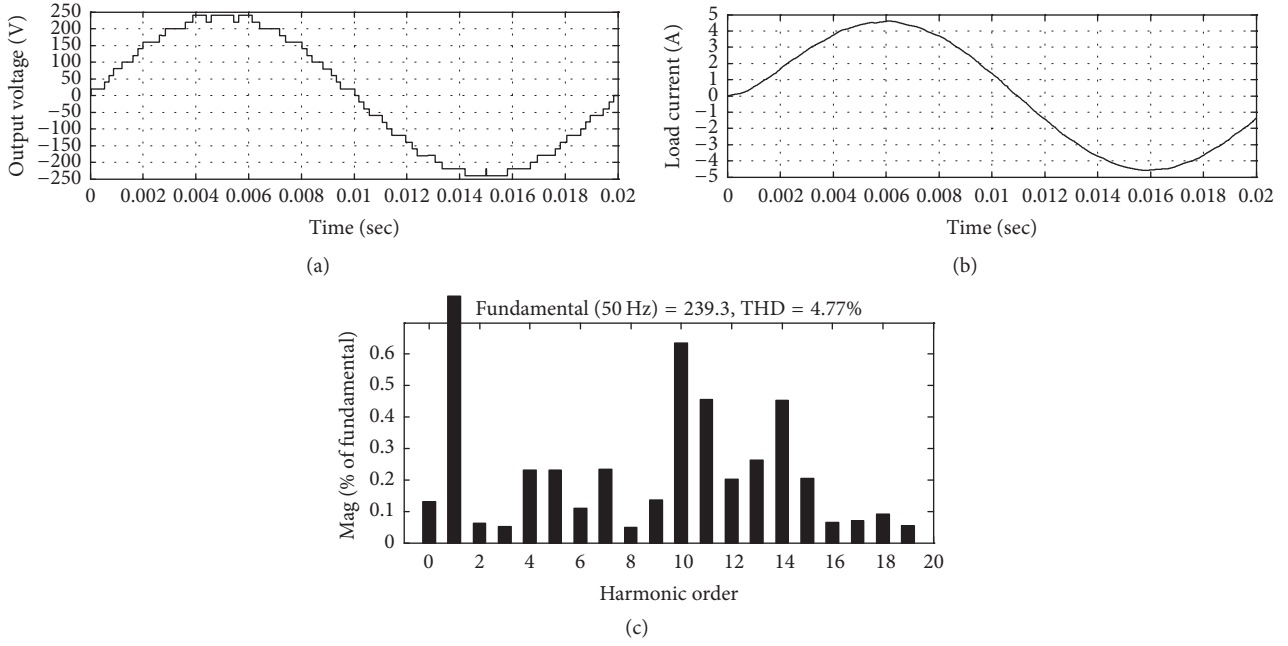


FIGURE 8: Simulation result for twenty-five-level cascaded circuit of multilevel inverter. (a) Output voltage. (b) Load current. (c) Harmonic contents of output voltage.

$$\begin{aligned}
 V_m^k &= 4 \times 3^{(k-1)} \times E \\
 V_m &= 2 \times (3^n - 1) \times E \\
 N_l &= (4 \times 3^n) - 3.
 \end{aligned}
 \tag{17}$$

Here,  $n$  is number of basic blocks connected in series. Illustration is carried out for this arrangement with two-block cascaded circuit, which gives the following results:

$$\begin{aligned}
 V_{X(1)} &= 3E, \\
 V_{Y(1)} &= E; \\
 V_{X(2)} &= 9E, \\
 V_{Y(2)} &= 3E \\
 V_m^1 &= 4E, \\
 V_m^2 &= 12E; \\
 V_m &= 16E \\
 N_l &= 33.
 \end{aligned}
 \tag{18}$$

In this case 33 levels of output voltage can be produced with maximum and minimum level of  $+16E$  and  $-16E$ , respectively. Figure 9 shows simulation results.  $E$  is supposed to be 20 V.

3.7. *Seventh Combination (C7)*. For this case values of sources are determined by the following equations:

$$\begin{aligned}
 V_{X(k)} &= 2 \times 7^{(k-1)} E \\
 V_{Y(k)} &= 7^{(k-1)} E.
 \end{aligned}
 \tag{19}$$

Other equations are

$$\begin{aligned}
 V_m^k &= 3 \times 7^{(k-1)} \times E \\
 V_m &= \frac{(7^n - 1)}{2} \times E \\
 N_l &= 7^n,
 \end{aligned}
 \tag{20}$$

where  $N_l, n$  represent the number of levels and number of basic blocks connected in series.

For example, in cascaded circuit of multilevel inverter with two basic blocks the following calculations are carried out:

$$\begin{aligned}
 V_{X(1)} &= 2E, \\
 V_{Y(1)} &= E \\
 V_{X(2)} &= 14E, \\
 V_{Y(2)} &= 7E \\
 V_m^1 &= 3E; \\
 V_m^2 &= 21E \\
 V_m &= 24E \\
 N_l &= 49.
 \end{aligned}
 \tag{21}$$

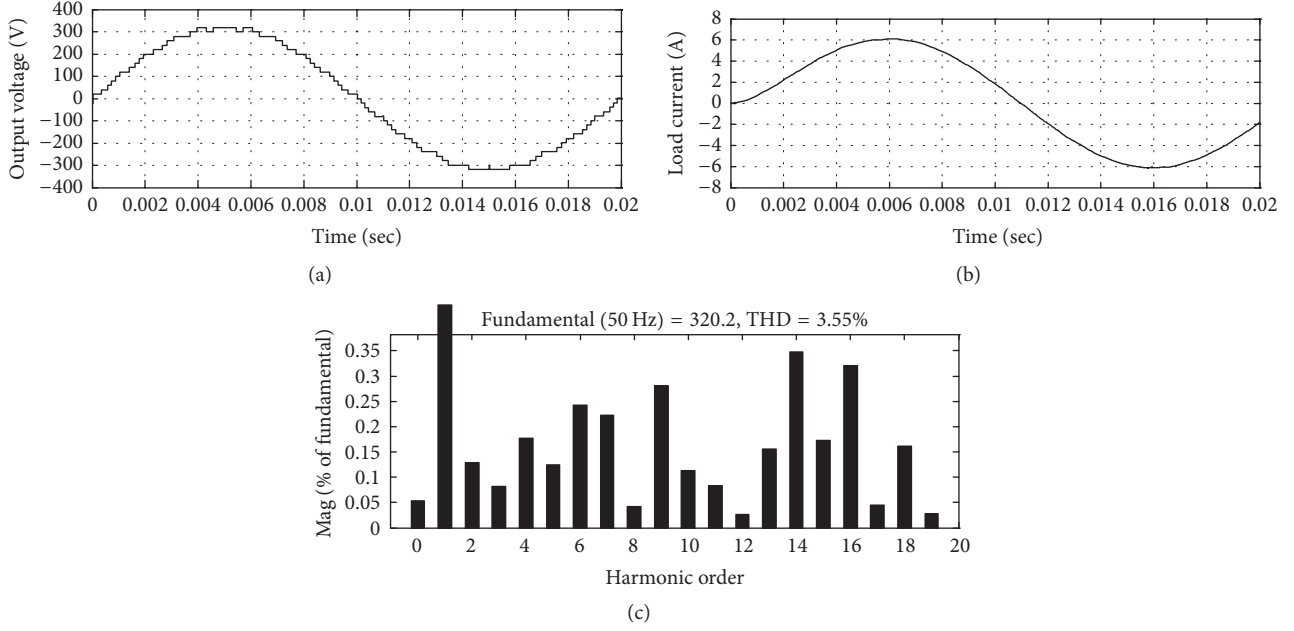


FIGURE 9: Simulation result for thirty-three-level cascaded circuit of multilevel inverter. (a) Output voltage. (b) Load current. (c) Harmonic contents of output voltage.

Simulation results for this 49-level multilevel inverter are shown in Figure 10.  $E$  is supposed to be 20 V for the instance.

Illustration is carried out using two blocks in series for all the above combinations of cascaded multilevel inverter. From simulation results it is seen that, for combinations one to seven, the number of levels of output voltage increases as 9, 13, 17, 19, 25, 33, and 49. And as the number of levels increases harmonic contents decrease improving its quality.

#### 4. Calculation of Standing Voltage of Switches

Standing voltage or blocking voltage of switches is an important parameter. By considering maximum amount of blocked voltage by switches overall cost of inverter can be calculated. The total cost of inverter reduces with reduction in maximum amount of blocked voltage by switches. Therefore it is necessary to consider maximum voltage blocked by each switch. According to basic block shown in Figure 1 standing or blocking voltage of different switches can be expressed as follows:

$$V_{PS,1} = V_{PS,2} = V_{PS,3} = V_{PS,7} = V_X. \quad (22)$$

In (22),  $V_{PS,1}$ ,  $V_{PS,2}$ ,  $V_{PS,3}$ ,  $V_{PS,7}$  represent maximum amount of blocked voltage by switches  $PS_1$ ,  $PS_2$ ,  $PS_3$ , and  $PS_7$ , respectively.

$$V_{PS,5} = V_{PS,6} = V_Y. \quad (23)$$

In (23),  $V_{PS,5}$ ,  $V_{PS,6}$  represent maximum amount of blocked voltage by switches  $PS_5$  and  $PS_6$ , respectively.

$$V_{PS,4} = V_{PS,8} = (V_X + V_Y). \quad (24)$$

In (24),  $V_{PS,4}$ ,  $V_{PS,8}$  represent maximum amount of blocked voltage by switches  $PS_4$  and  $PS_8$ , respectively. Therefore, total amount of blocked voltage by all the switches used in basic block can be expressed as follows:

$$V_b = (6V_X + 4V_Y). \quad (25)$$

Now consider cascaded circuit as shown in Figure 3. The maximum amount of blocked voltage by this circuit having  $n$  blocks connected in series,  $V_{bt}$ , can be expressed as follows:

$$\begin{aligned} V_{bt} &= V_{b1} + V_{b2} + \dots + V_{bn} \\ V_{bt} &= 6(V_{X1} + V_{X2} + \dots + V_{Xn}) \\ &\quad + 4(V_{Y1} + V_{Y2} + \dots + V_{Yn}). \end{aligned} \quad (26)$$

To improve performance of multilevel inverter and to increase number of output voltage levels it is possible to select different combinations of dc voltage sources. To choose magnitudes of dc voltage sources seven different combinations are presented here. For these seven combinations magnitude of dc sources, maximum output voltage generated ( $V_m$ ), number of output voltage levels ( $N_l$ ), variety in values of dc sources ( $N_v$ ), and total maximum voltage blocked by switches ( $V_{bt}$ ) are calculated and shown in Table 3.

#### 5. Comparison

All the seven combinations are compared with each other. Figure 11 compares number of switches required to generate particular number of output voltage levels. It is seen that sixth and seventh combination (C6 and C7) require less number of switches to generate particular number of output voltage levels.

TABLE 3: Different combinations of magnitudes of dc sources and related parameters.

Combination number	DC voltage source magnitudes	$V_m^k$	$V_m$	$N_l$	$N_v$	$V_{bt}$
First (C1)	$V_{X(k)} = V_{Y(k)} = E$ for $k = 1, 2, 3, \dots, n$	$2E$	$2nE$	$4n + 1$	1	$10nE$
Second (C2)	$V_{X(k)} = 2E,$ $V_{Y(k)} = E$ for $k = 1, 2, 3, \dots, n$	$3E$	$3nE$	$6n + 1$	2	$16nE$
Third (C3)	$V_{X(k)} = 3E,$ $V_{Y(k)} = E$ for $k = 1, 2, 3, \dots, n$	$4E$	$4nE$	$8n + 1$	2	$22nE$
Fourth (C4)	$V_{X(k)} = 2V_{Y(k)},$ $V_{Y(k)} = 2^{(k-1)}E$ for $k = 1, 2, 3, \dots, n$	$3 \times 2^{(k-1)} \times E$	$3 \times (2^n - 1) \times E$	$(3 \times 2^{n+1}) - 5$	$n + 1$	$\sum_{k=1}^n 2^{(k+3)}E$
Fifth (C5)	$V_{X(k)} = V_{Y(k)} = 5^{(k-1)}E$ for $k = 1, 2, 3, \dots, n$	$2 \times 5^{(k-1)} \times E$	$((5^n - 1)/2) \times E$	$5^n$	$n$	$2 \sum_{k=1}^n 5^k E$
Sixth (C6)	$V_{X(k)} = 3V_{Y(k)},$ $V_{Y(k)} = 3^{(k-1)}E$ for $k = 1, 2, 3, \dots, n$	$4 \times 3^{(k-1)} \times E$	$2 \times (3^n - 1) \times E$	$(4 \times 3^n) - 3$	$n + 1$	$22 \sum_{k=1}^n 3^{(k-1)}E$
Seventh (C7)	$V_{X(k)} = 2 \times 7^{(k-1)}E$ $V_{Y(k)} = 7^{(k-1)}E$ for $k = 1, 2, 3, \dots, n$	$3 \times 7^{(k-1)} \times E$	$((7^n - 1)/2) \times E$	$7^n$	$2n$	$16 \sum_{k=1}^n 7^{(k-1)}E$

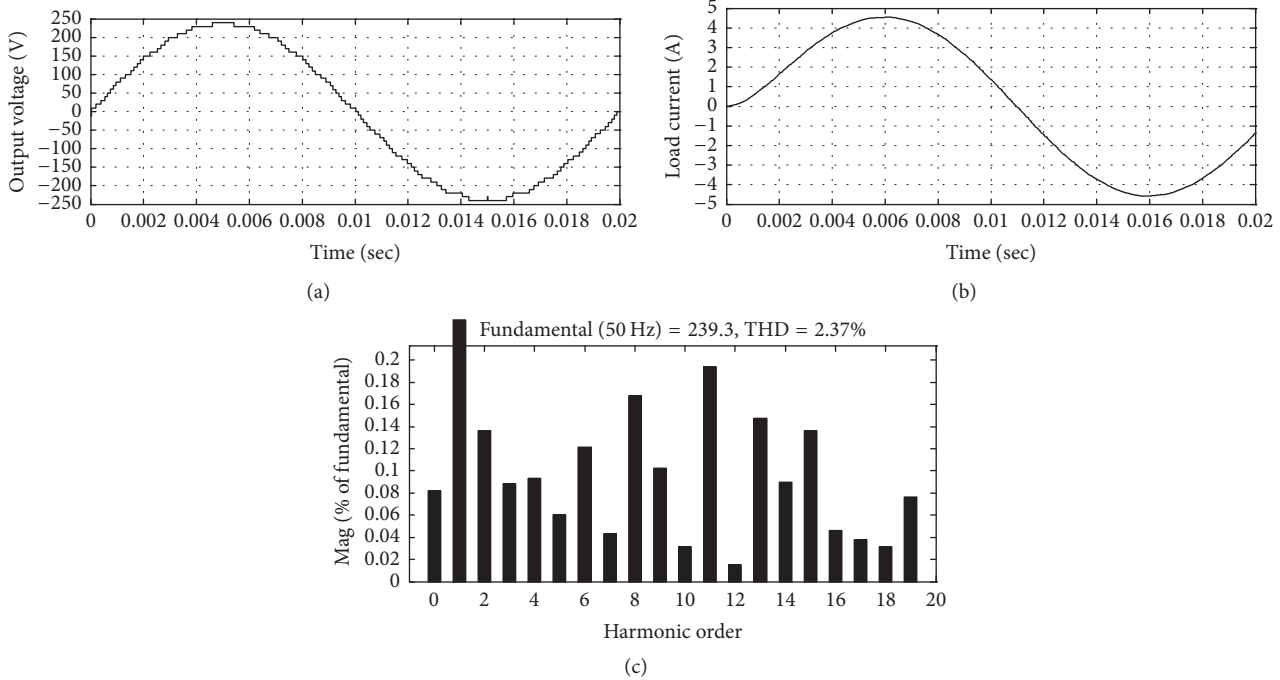


FIGURE 10: Simulation result for forty-nine-level cascaded circuit of multilevel inverter. (a) Output voltage. (b) Load current. (c) Harmonic contents of output voltage.

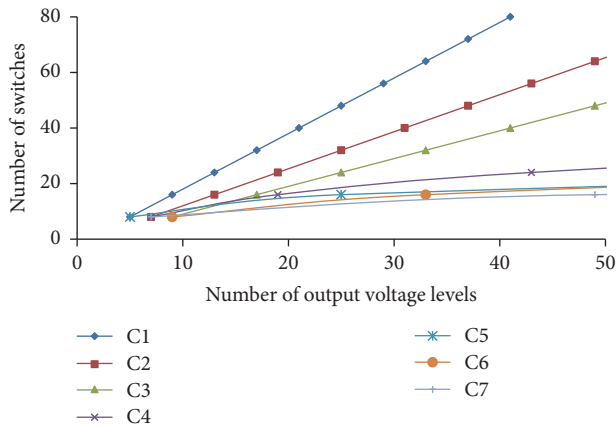


FIGURE 11: Number of switches versus number of output voltage levels in different combinations of proposed topology.

Figure 12 compares number of dc sources required in different combinations. As shown in graph seventh combination (C7) requires minimum number of dc sources and first combination requires maximum number of dc sources to generate particular number of output voltage levels.

Figure 13 shows comparison among proposed and conventional topologies of CHB. First combination C1 which is symmetric proposed topology and seventh combination C7 which gives best performance among seven combinations are considered for comparison. C1 and symmetric CHB generate the same amount of output voltage levels by using particular number of switches. Therefore, both lines overlap each other.

But in C1 to produce suppose 5 levels only 3 switches are conducting at any instant while in symmetric CHB 4 switches are conducting and so on. Means conduction losses are less in C1 as compared to conventional symmetric CHB. C7 requires less number of switches as compared to symmetric CHB and binary asymmetric CHB to generate particular number of output voltage levels. Though the number of switches required in trinary asymmetric CHB is less, the number of conducting switches is more as compared to C7 to generate particular number of output voltage levels. So conduction losses are less in C7.

## 6. Simulation and Experimental Results

To validate proposed topology shown in Figure 1, the experimental and simulation results are presented for basic unit of single phase inverter operating in symmetric mode ( $V_X = E$  and  $V_Y = E$ ) and asymmetric mode ( $V_X = 2E$  and  $V_Y = E$ ,  $V_X = 3E$  and  $V_Y = E$ ). It generates 5-level, 7-level, and 9-level output voltage as mentioned in Table 2. MOSFETs-IRF840 are used as power switches in the prototype. Microchip's PIC-16F877A microcontroller is used to provide pulses for the switches. TLP250 optoisolated gate driver is used to provide amplified gate signals to switches as well as provide isolation between power and control circuit. The block diagram is shown in Figure 14(a) and photograph of hardware setup is shown in Figure 14(b). Components used are given in Table 4. Figures 15, 16, and 17 show simulation and experimental results of single phase inverter. It is seen that both results are in line.

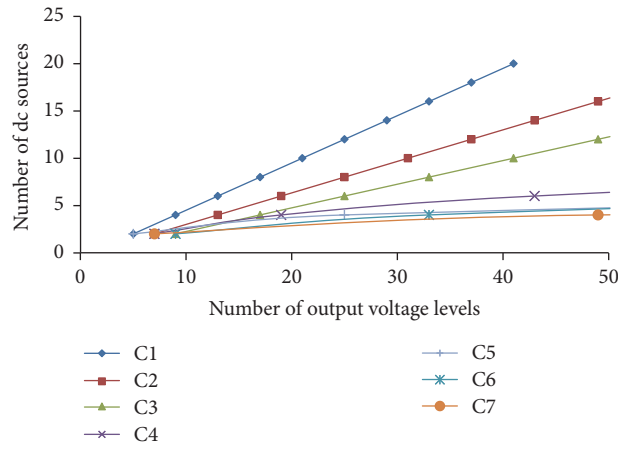


FIGURE 12: Number of dc sources versus number of output voltage levels in different combinations of proposed topology.

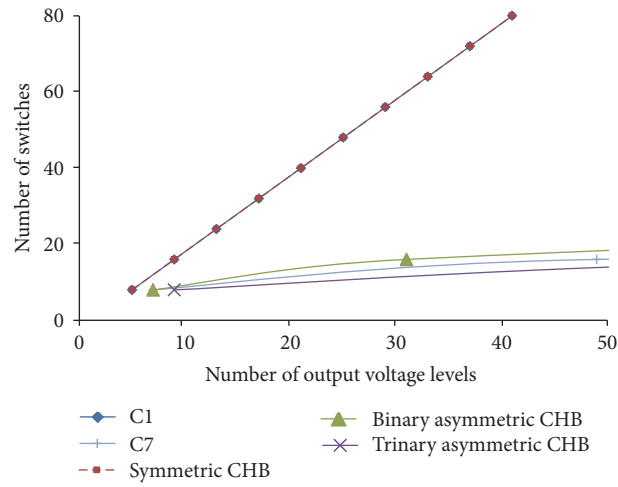


FIGURE 13: Number of switches versus number of output voltage levels in proposed and conventional topologies.

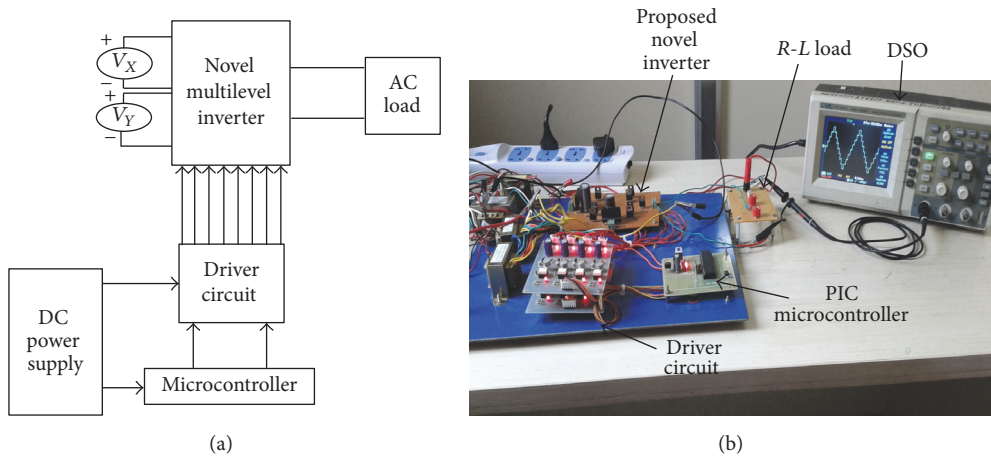


FIGURE 14: (a) Block diagram. (b) Photograph of hardware setup.

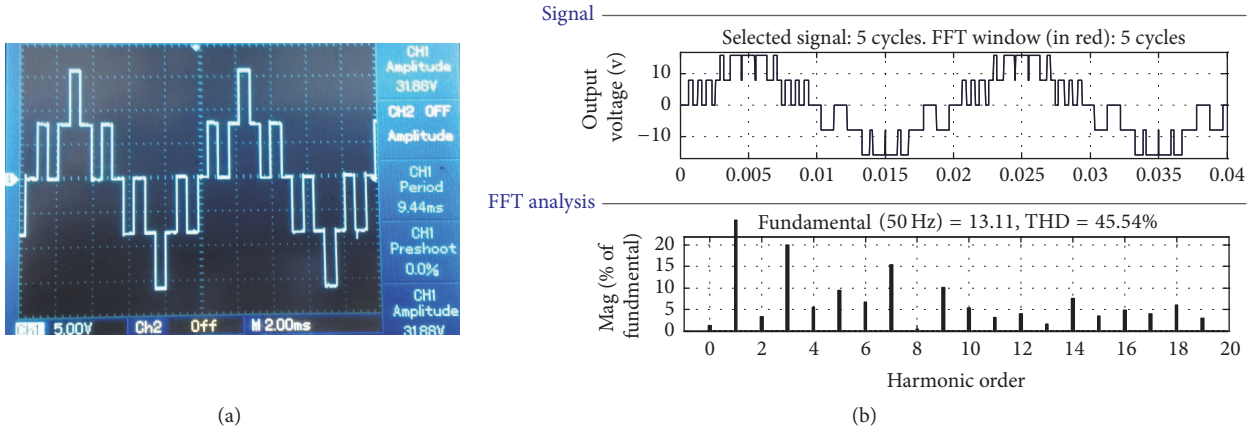


FIGURE 15: Experimental and simulation results for 5-level inverter. (a) Experimental output voltage. (b) Simulation output voltage and harmonic spectrum.

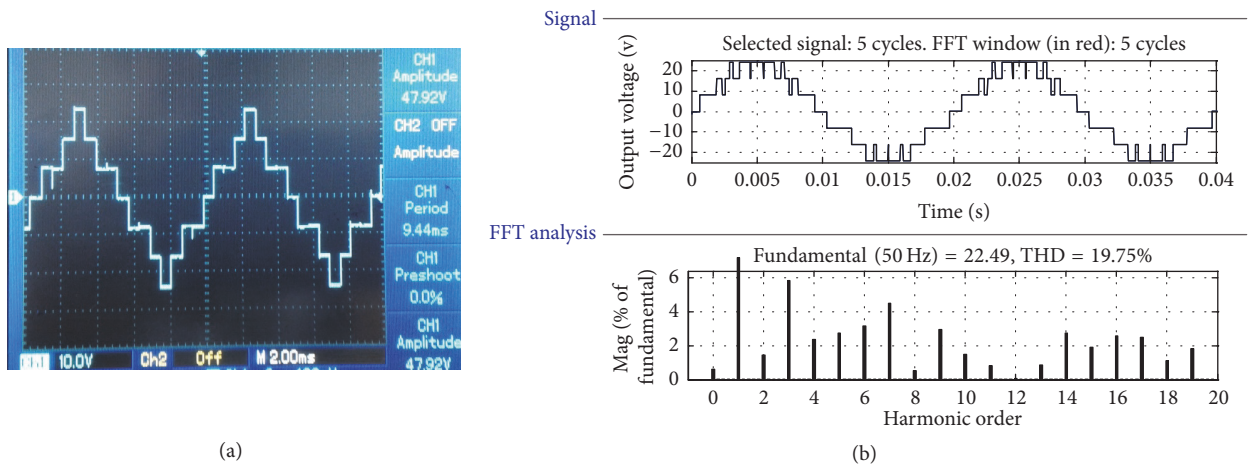


FIGURE 16: Experimental and simulation results for 7-level inverter. (a) Experimental output voltage. (b) Simulation output voltage and harmonic spectrum.

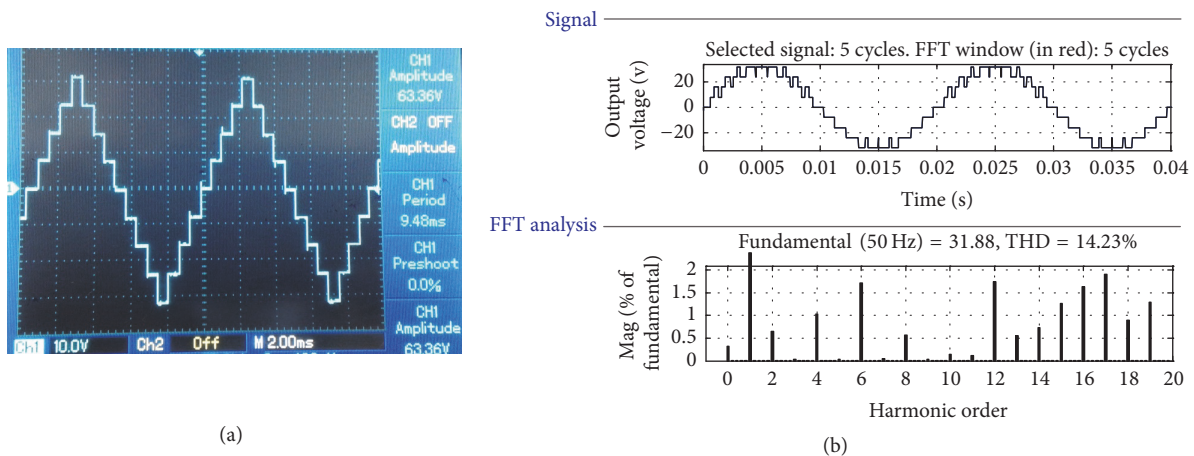


FIGURE 17: Experimental and simulation results for 9-level inverter. (a) Experimental output voltage. (b) Simulation output voltage and harmonic spectrum.



TABLE 4: Components used in prototype.

Sr. number	Component used	Specification
1	$V_X$	8 V, for 5-level output
		16 V, for 7-level output
		24 V, for 9-level output
2	$V_Y$	8 V
3	PIC microcontroller	16F877A
4	Gate driver	TLP250
5	MOSFET	IRF840
6	Load	$R = 50$ ohms
		$L = 100$ mH

## 7. Conclusion

A basic block of novel multilevel inverter topology has been proposed in this paper. Connecting basic blocks in series a cascaded circuit is developed. Seven different combinations to select magnitude of dc voltage sources are introduced. Comparison is carried out among different combinations to find out the best one. From comparison it is seen that C7 requires less number of switches, while C1 needs less variety of magnitude of dc voltage sources.

The main advantage of proposed topology is in increasing as well as getting flexibility in number of output voltage levels by using less number of on-state power switches and dc voltage sources. Simulation results prove the validity of proposed topology and cascaded circuit in producing high voltage containing low value of harmonics. Also, the practicality of basic unit of proposed topology is verified experimentally for the small-scale prototype in the laboratory.

## Conflicts of Interest

The authors declare that they have no conflicts of interest.

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