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Research Article

A Low-Power Voltage Limiter/Regulator IC in Standard Thick-Oxide 130 nm CMOS for Inductive Power Transfer Application

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This paper presents a novel CMOS low-power voltage limiter/regulator circuit with hysteresis for inductive power transfer in an implanted telemetry application. The circuit controls its rail voltage to the maximum value of 3 V DC employing 100 mV of comparator hysteresis. It occupies a silicon area of only 127 μm × 125 μm using the 130 nm IBM CMOS process. In addition, the circuit dissipated less than 1 mW and was designed using thick-oxide 3.6 V NMOS and PMOS devices available in the process library.

1. Introduction and Circuit Description

Wireless inductive transfer of power across air gaps between loosely coupled inductors is of significant interest in remote pickup and telemetry. Voltage control using a limiter/regulator is an essential component of such a system. Also, hysteretic voltage control devices are frequently used in power converters [1, 2]. This paper discusses the design, fabrication, and testing of a hysteretic inductive power limiter/regulator for application in implantable telemetry devices. The schematic diagram of the overall wireless power transfer circuit is shown in Figure 1 with the proposed novel CMOS limiter bounded by the rectangular box. The purpose of the implemented integrated circuit is to control its inductively generated rectified rail-to-rail voltage attained through the wireless power transfer. The current induced on the wireless pickup coil is rectified using the Schottky diode bridge. The rectified current charges a capacitor (power supply capacitor) connected to the load. The voltages on the positive and negative sides of this capacitor are V_{DD} and V_{SS}, respectively, which also forms the rail voltages of the limiter/regulator. The integrated circuit limiter controls the V_{DD} voltage by periodically shorting both sides (terminals) of the pickup coil to the negative terminal of the capacitor (V_{SS} rail) using triode regime MOSFET switches. The MOSFET switches are driven by a novel hysteresis comparator. The maximum value of the controlled voltage is limited to 3 V by employing 100 mV of comparator hysteresis and a suitable reference voltage, V_{ref}. The comparator output is sufficiently buffered to drive the large shorting switches with reasonably small turn-on and turn-off delays. A capacitor is used at the noninverting terminal for shorting any spurious signal pickups. All transistor size values in all the figures are provided in micrometers. The top number and the bottom number adjacent to the transistors, respectively, denote the values for the channel width and the channel length.

Other power circuit components external to the limiter/regulator IC in Figure 1 include inductive power transfer coils, L_S and L_P with 2 : 1 turns ratio, as well as a 22 μF power supply capacitor, C_L, across the variable load (with a nominal value of around 150 Ω). The power transferred depends on the mutual coupling factor, k, between the coils which varies with the air gap separation between the coils. In order to ensure maximum magnetic flux transition, the power

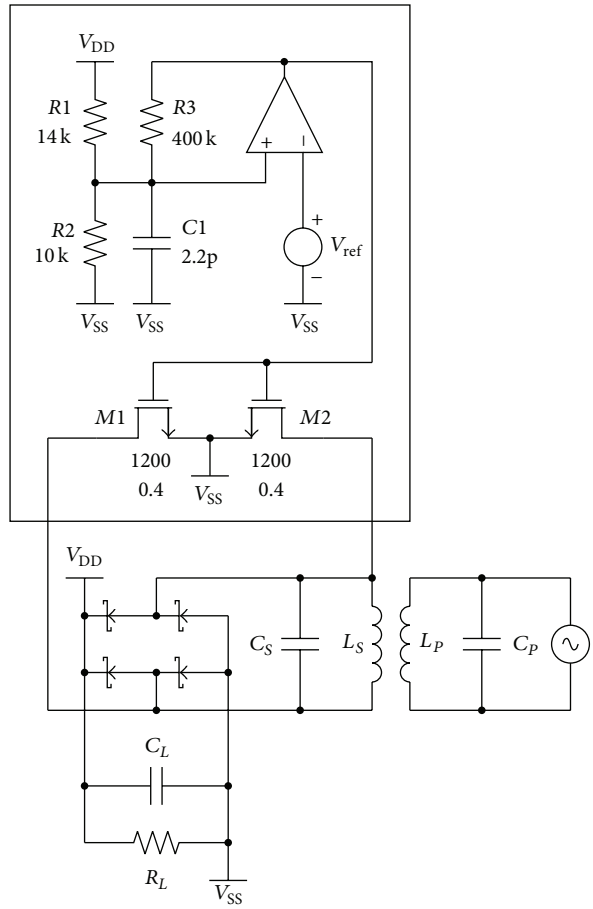

Figure 1: Schematic diagram of the overall circuit. The enclosed schematic is the integrated novel CMOS limiter circuit on a chip.

transfer coils are terminated with parallel capacitors for LC resonance at a specified power transfer line frequency. The line frequency of power transfer was designed to be variable between 40 kHz and 600 kHz for the specific telemetry application. The primary coil is excited by a variable frequency sinusoidal oscillator using a 5 V DC supply. However, the induced input voltage at the secondary power transfer coil can vary considerably due to the possible orders of magnitude variation in the mutual coupling between the coils depending on their separation.

2. IC Design and Simulation

The limiter/regulator IC was designed and simulated on Mentor Graphics platform using the 130 nm IBM CMOS process technology. MOSFET devices with thick gate oxide were used throughout the design. These devices are able to operate with voltages up to 3.6 V. Simulation indicates that the power dissipation of the limiter/regulator IC is less than 1 mW.

2.1. Voltage Reference Circuit. The supply-independent voltage reference circuit as described in [3] was redesigned using the thick-oxide devices available in the 130 nm CMOS process to generate the suitably selected reference voltage V_{ref} = 1.236 V. The schematic diagram of this implemented

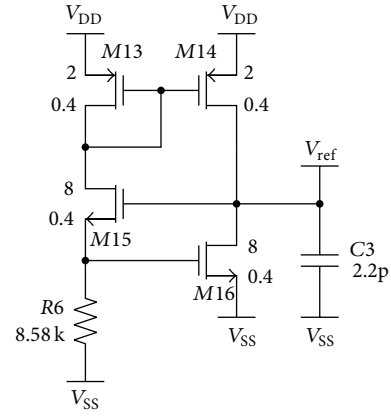

Figure 2: Voltage reference circuit using thick-oxide 3.6 V MOSFET devices.

circuit is shown in Figure 2. Temperature independence is not required in this case, since the device is designed for implanted telemetry application, whereby its temperature will be equal to the body temperature. In addition, no start-up circuit is required for this reference circuit. Initially, the output voltage is equal to 0, which is set by $C3$, and $M15$ is off. The voltage at the gate of $M16$ is also close to 0 and $M16$ is off.

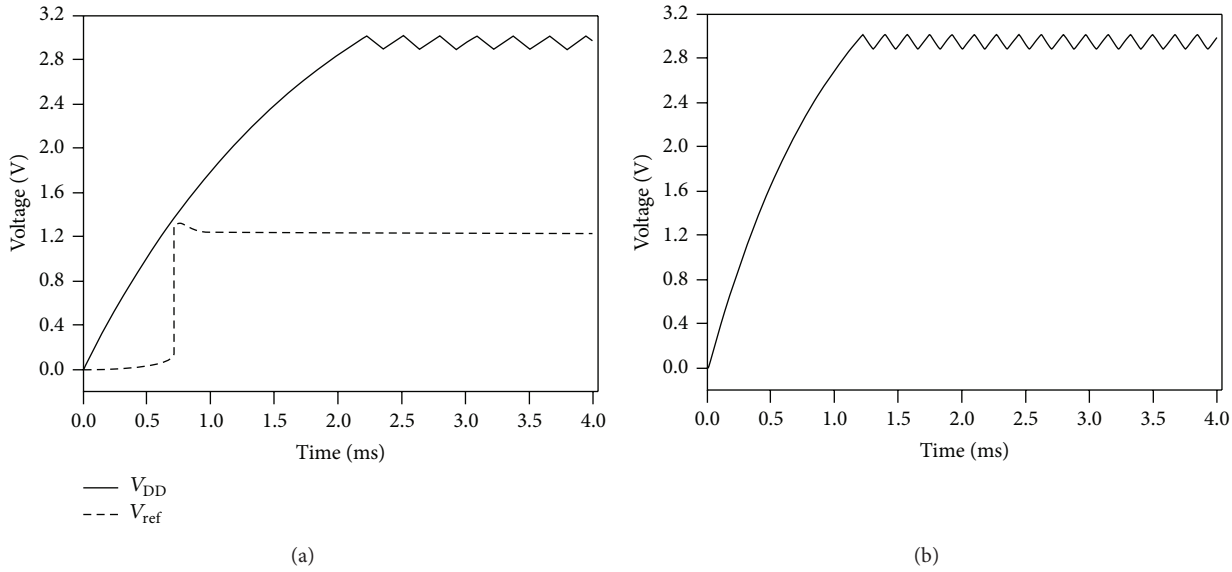

Figure 3: Simulated start-up voltage signals: (a) the comparator input reference voltage V_{ref} and charging-to-rail voltage V_{DD} using a 22 μF power supply capacitor and (b) charging-to-rail voltage V_{DD} using a 12 μF power supply capacitor.

What makes the circuit go out of this state is that the channels of $M15$ and $M13$ act as resistances. Since $M15$ is 4 times wider than $M13$ and the charge-carrier (electron) mobility in NMOS ($M15$) is higher (by around 2.5 times) compared to hole mobility in PMOS ($M13$) [4], the channel of $M15$ has a smaller resistance than that of $M13$. In this way, the voltage at the drain of $M13$ and the gate of $M14$ hovers toward 0 and $M14$ turns on, which starts up the circuit. Figure 3(a) shows the simulated voltage reference signal V_{ref} with respect to the positive rail voltage V_{DD}. Supply-independence of V_{ref} can be clearly noticed after start-up. The charging to the supply rail voltage V_{DD} using a power supply capacitor, C_L, of 22 μF and 12 μF is shown, respectively, in Figures 3(a) and 3(b).

2.2. Comparator Circuit. The comparator is a three-stage single-ended differential amplifier. Its schematic diagram is shown in Figure 4. The first stage is a single-ended differential pair with active current mirror load. The second stage is a PMOS common source amplifier with an NMOS current-source load. The third stage is a push-pull inverter amplifier. The NMOS current-source bias voltage V_{bias} for the tail current of the differential input stage and the NMOS load is generated by the diode-connected device $M8$ and resistor $R4$.

Since there is positive feedback through the 400 K resistor in the overall circuit shown in Figure 1, this is a closed loop amplifier system. Internal frequency compensation was thus employed within the comparator circuit using the series connection of $C2$ and $R5$ as shown in Figure 4 between two high impedance nodes. This arrangement provides enhanced Miller compensation through the use of the series connected resistance $R5$.

2.3. Switching Levels. The negative terminal input to the comparator is the reference voltage V_{ref}, and the positive

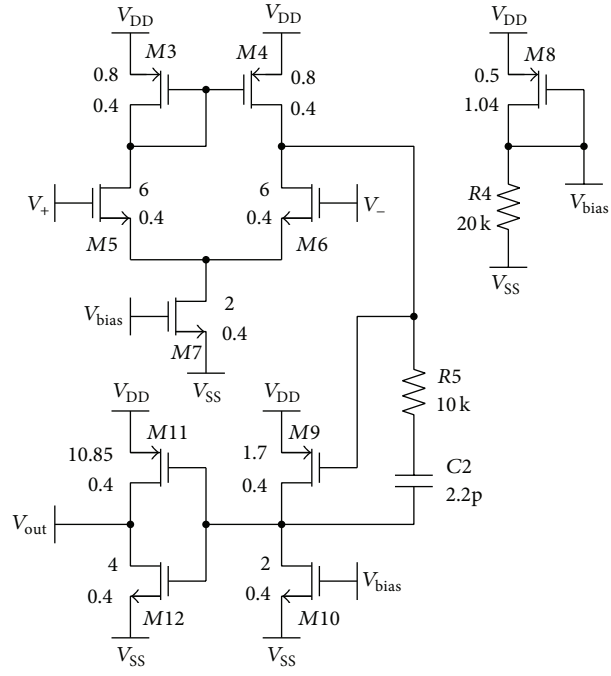

Figure 4: Schematic diagram of the comparator circuit.

terminal input is the output from the composite voltage divider consisting of the resistors $R1$, $R2$, and $R3$ with values of 14 K, 10 K, and 400 K, respectively. The hysteresis is implemented through novel use of the 400 K $R3$ resistor: when the comparator's output voltage is V_{DD}, the 400 K resistor is in parallel with the 14 K resistor, while when it is V_{SS} the 400 K resistor is in parallel with the 10 K resistor. This modifies the overall resistances in the voltage divider. In this way, when the output from the comparator is at V_{SS}, the circuit

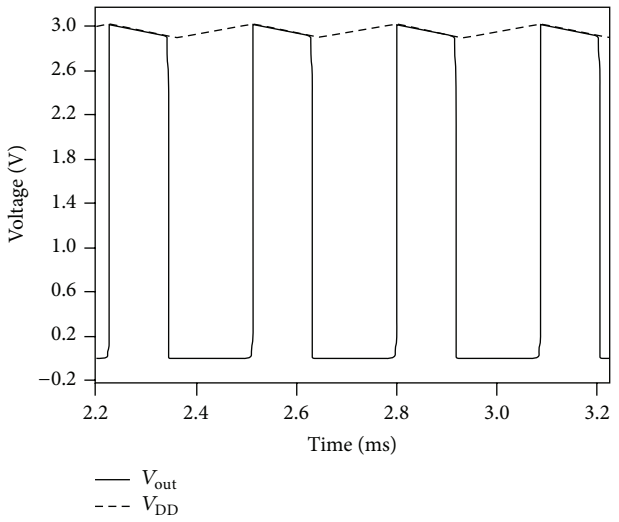

FIGURE 5: Simulated voltage signals: shorting control voltage (V_{out}) and V_{DD}.

will switch on the shorting transistors for a value of V_{DD} given by

$$V_{DD}\,(\text{SHORT}) = V_{ref} \times \frac{(R2 \times R3)\,/\,(R2 + R3) + R1}{(R2 \times R3)\,/\,(R2 + R3)}. \quad (1)$$

Using the values from Figure 1, in this case,

$$V_{DD}\,(\text{SHORT}) \approx 3.01\,\text{V}. \quad (2)$$

While the shorting transistors are on, the comparator output sags downwards along with V_{DD}. The comparator output will change to V_{SS} and switch off these transistors when the value of V_{DD} reaches

$$V_{DD}\,(\text{OPEN}) = V_{ref} \times \frac{(R1 \times R3)\,/\,(R1 + R3) + R2}{R2}. \quad (3)$$

Again, using the values from Figure 1, in this case,

$$V_{DD}\,(\text{OPEN}) \approx 2.91\,\text{V}. \quad (4)$$

Figure 5 shows the simulated output voltage of the comparator for the overall circuit with respect to V_{DD}. The output voltage indicates a comparator switching frequency of around 3.3 kHz in this case. The switching frequency will vary based on the induced voltage and the RC time constant at the output of the rectifier (due to load resistance and value of the power supply capacitor) as well as the set tripping points (switching levels).

3. Fabrication and Testing

The circuit was designed using high-performance MIM capacitors and polysilicon resistors with the largest resistor $R3$ being a high-resistivity RR resistor and others being RP precision resistors [5]. This implementation provided accurate resistor ratios with reduced temperature sensitivity. The core

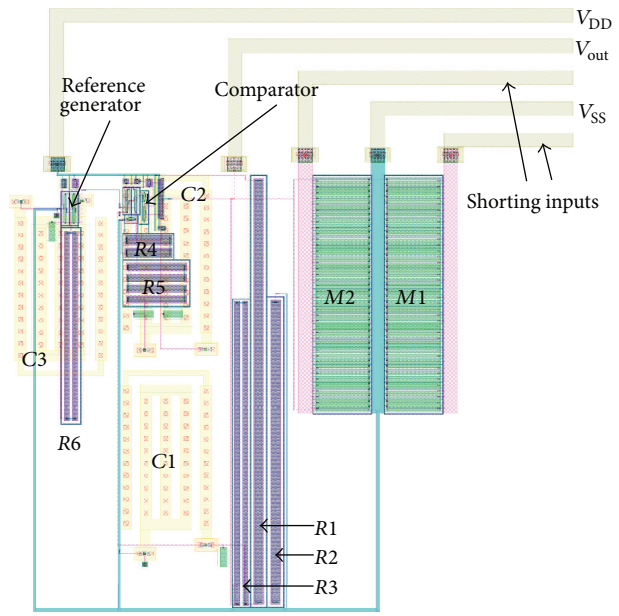

FIGURE 6: Annotated layout of the circuit. Shorting inputs are provided for connection to the secondary coil as indicated in Figure 1.

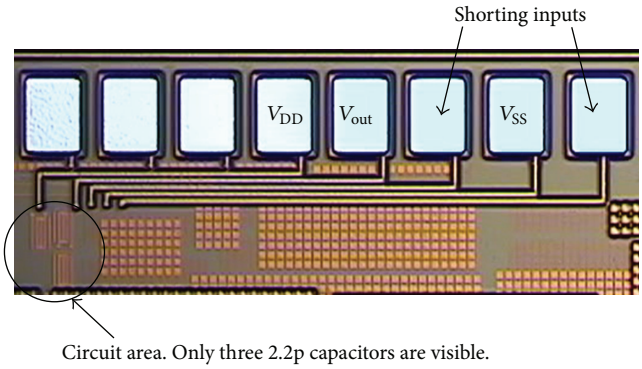

FIGURE 7: Annotated voltage limiter chip photo.

circuit occupied an area of only 127 μm × 125 μm with the active area dominated by the shorting transistors and the passive area dominated by the capacitors. The two shorting NMOSFETS were 1200 μm × 0.4 μm devices, with each laid out in a compact multifinger array of eighty 15 μm × 0.4 μm devices. The threshold voltages for the thick-oxide devices were, respectively, 0.460 ± 0.065 V for the NMOS device and −0.420 ± 0.052 V for the PMOS device. The primary and secondary coils for the inductive power transfer were held at an air gap of several centimeters as intended in the final application.

The inductive power transfer test jig was assembled using the fabricated IC and discrete primary and secondary component assemblies. Figure 6 shows the layout of the circuit while Figure 7 shows the corresponding die photo of the CMOS limiter IC.

Several signals were measured for the inductive power transfer setup shown in Figure 8 through oscilloscope trace

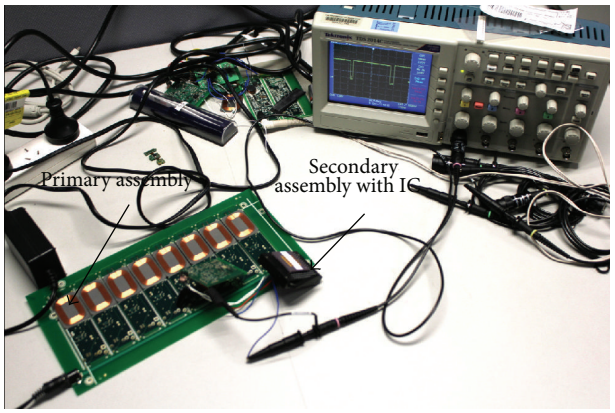

Figure 8: Inductive power transfer test jig with the fabricated regulator IC mounted in the secondary assembly.

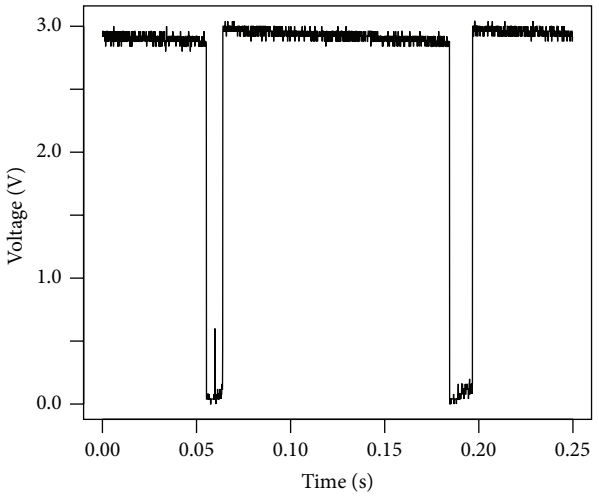

Figure 9: Measured comparator output voltage controlling the shorting transistors.

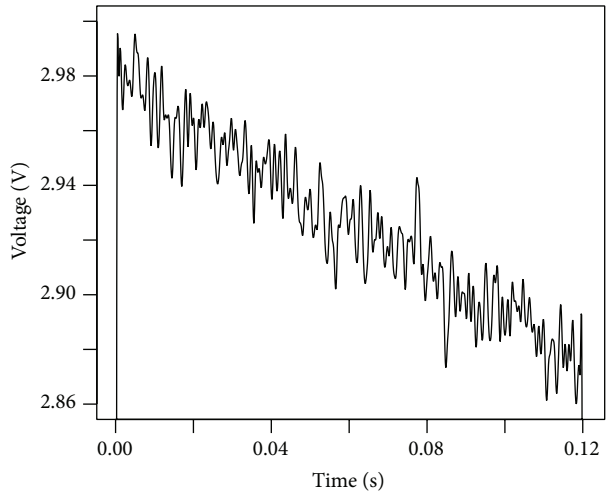

Figure 10: Measured comparator output voltage for one "on" cycle.

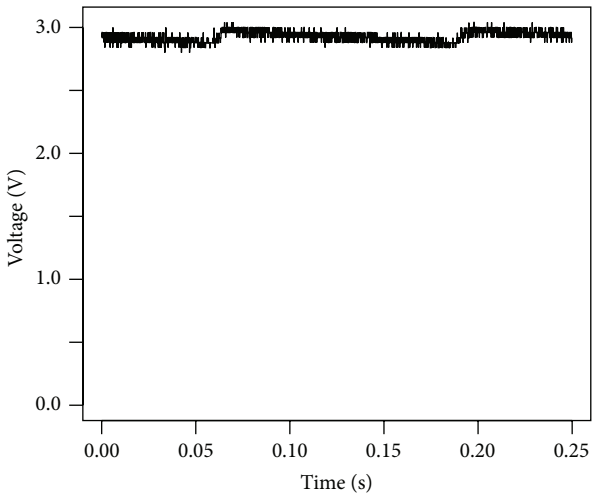

Figure 11: Measured rail voltage V_{DD} with respect to the circuit ground, V_{SS}.

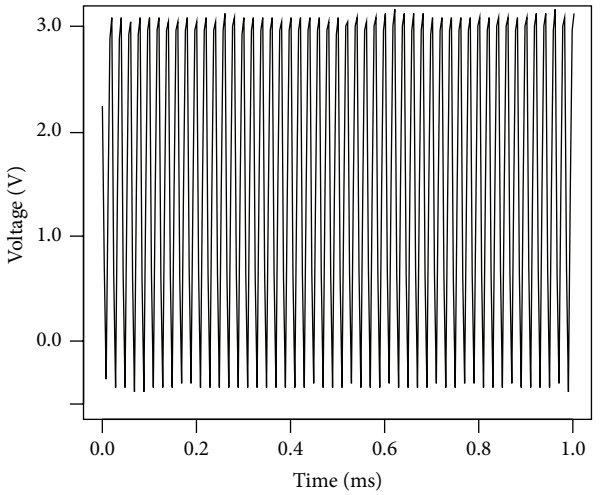

Figure 12: An instance of the measured induced voltage with respect to the circuit ground.

capture. Figure 9 shows the measured shorting control voltage which is the output voltage of the comparator. The magnified version of the same signal for just one "on" cycle is shown in Figure 10. This figure shows that the transistors are switched on (secondary coil shorted) when the supply voltage is about 2.99 V and switched off when it is about 2.88 V. The measured signals are off by less than 1% compared to the desired design specifications. In addition, Figure 11 shows the measured rail voltage V_{DD} with respect to the circuit ground, V_{SS}. This is also the rectified voltage across the load. Also, Figure 12 shows an instance of the measured induced voltage for the circuit.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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References

[1] K. Lee, F. C. Lee, and M. Xu, "A hysteretic control method for multiphase voltage regulator," *IEEE Transactions on Power Electronics*, vol. 24, no. 12, pp. 2726–2734, 2009.

[2] J. Abu-Qahouq, H. Mao, and I. Batarseh, "Multiphase voltage-mode hysteretic controlled dc-dc converter with novel current sharing," *IEEE Transactions on Power Electronics*, vol. 19, no. 6, pp. 1397–1407, 2004.

[3] A. M. Sodagar and K. Najafi, "A wide-range supply-independent CMOS voltage reference for telemetry-powering applications," in *Proceedings of the 9th IEEE International Conference on Electronics, Circuits and Systems (ICECS '02)*, vol. 1, pp. 401–404, September 2002.

[4] P. E. Allen and D. A. Holberg, *CMOS Analog Circuit Design*, Oxford University Press, 2nd edition, 2002.

[5] IBM Microelectronics Division, *CMOS8RF Design Manual, V1.7.0.0, Analog and Mixed Signal Technology Development*, IBM Microelectronics Division, Essex Junction, Vt, USA, 2010.