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Editorial

Clock/Frequency Generation Circuits and Systems

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Clock generation and frequency synthesis systems have played a critical role in modern communication system design. As data rate increases, low-noise and low-power clock/frequency generation is getting more important than ever for high-performance digital communication systems. Timing uncertainty directly affects the overall performance of microprocessors and I/O links. The quality of wireless transceiver systems is often determined by the phase noise performance of frequency synthesizers. Active researches in the areas of clocking, data synchronization, and frequency generation have been performed for broad applications. This special issue focuses on the new and existing clock/frequency generation circuits and systems for wireline and wireless system IC designs with a special emphasis given to advanced technical results.

This special issue consists of nine papers. Four papers focus on wireline applications: a paper on characterizing the jitter tracking performance of the receiver for high-speed source synchronous links, a paper on generating fault-tolerant clock for VLSI circuits, a paper on a wide lock range clock-and-data recovery (CDR) circuit, and a paper on a delay-locked-loop- (DLL-) based clock generation for USB 2.0 applications. Three papers focus on wireless applications: a paper on open-loop phase modulation techniques for wide-bandwidth transmitter design, a paper on high-speed, high-resolution autocalibration techniques for fractional-N phase-locked loops (PLLs), and a paper on a wideband LC-based voltage-controlled oscillator (VCO) design for reconfigurable radio transceivers. Other two subsequent papers present nontraditional ways of generating clock frequency: the one with an all-digital flying-adder-based method and the other with a semidigital PLL-based method.

One of the major factors limiting the maximum achievable I/O data rates occurs from the degradation of system timing margins by clock jitter. The paper by A. Ragab et al. presents a comparative analysis of several jitter tracking architectures employed in source synchronous high-speed links. Tracking the transmit clock jitter in the presence of clock skew and channel loss enables high data rate operation in these links. The paper by G. Fuchs and A. Steininger describes a generation scheme of fault-tolerant clock based on a tick synchronization algorithm. An ASIC chip, implemented in a 0.18-μm CMOS, demonstrates feasibility of this scheme creating a globally synchronized clock, which is tolerant to a configurable number of arbitrary faults.

For high-speed chip-to-chip communication, serial link protocol has been widely adopted in various computer-to-peripheral interfaces. The use of serial links for multi-purpose, however, still presents some challenges which must be overcome by circuit design. The paper by S.-K. Lee et al. presents a 650-Mb/s to 8-Gb/s referenceless CDR with automatic frequency acquisition. By utilizing a novel DLL-based frequency acquisition, the dual-loop CDR shows outstanding performance in terms of lock range, power consumption, and area. The USB 2.0 is one of the most popular wireline standards, but requiring a very small area and low power consumption for portable applications. For low-cost low-power clock generation, a clock generator based on an edge-combiner DLL is presented in the paper by T. Kawamoto et al. The clock generator generates 480-MHz

10-tap output signals from a 12-MHz reference signal and consists of three DLLs to shrink the design area so that it is smaller than the PLL-based one.

The rapid growth of new communication standards like LTE and WiMAX has led to high data rate, wide signal bandwidth and high peak-to-average power ratio. A wide-bandwidth phase modulator is one of the key building blocks for the design of next generation transceivers. The paper by N. Nidhi et al. presents open-loop phase modulation techniques for upcoming 60 GHz wireless communication and software-defined radio. The open-loop modulation technique achieves maximum flexibility with wide-bandwidth operation. In modern wireless transceiver systems, the $\Delta\Sigma$ fractional-N frequency synthesizer is an essential building block. Especially for a wide tuning-range fractional-N frequency synthesizer, high-speed and high-precision automatic calibration is important for shortening the lock time and improving the phase noise. In the paper by J. Shin and H. Shin, an automatic calibration technique for the VCO frequency and the loop gain in the fractional-N PLL design is presented. A simple and efficient autocalibration method based on a high-speed frequency-to-digital converter significantly reduces the calibration time.

Recently, dozens of wireless communication standards have been used for small mobile terminals, for example, GSM, UMTS, LTE, WiMAX, WLAN, Bluetooth, UWB, GPS, DTV, and RFID, and the standards use several frequency bands spreading in a quite wide range such as 800 MHz to 6 GHz. All of these RF front-ends require a wideband-tunable VCO, which is an indispensable component for the multiband radio in common. The paper by Y. Ito et al. presents a wide-band frequency synthesizer with a frequency range from 1 GHz to 6.6 GHz by employing a wide-tuning LC VCO and a tuning-range extension circuit. Such tuning allows to satisfy the requirements of all cellular and WiFi standards, becoming a very interesting solution for multistandard transceiver where the presence of several local oscillator would results in a too expensive design.

The use of advanced CMOS technologies makes the traditional phase-locked loop (PLL) design challenging as on-chip variability and modeling inaccuracy become severe in deep submicron CMOS. Large loop parameter variation makes it difficult to find the optimum bandwidth for phase noise, spur, and settling time. In addition, analog passive devices become a bottleneck for scalability and integrating the loop filter (LPF) has been a challenging task in the conventional PLL design. Therefore, clock generation based on digital or semidigital method has received great attention recently. The paper by P.-L. Chen and C.-C. Tsai describes a flying-adder-based digital frequency synthesizer with an interpolated multiplexer to improve cycle-to-cycle and *rms* jitter performance. This synthesizer, fabricated in a 0.18-μm CMOS, shows a frequency lock range of from 33 MHz to 286 MHz. The paper by N. Xu et al. introduces recent semidigital PLL architectures which relax technology dependency and provide low-cost low-power clock generation. With the absence of the time-to-digital converter (TDC), the semidigital PLL enables low-power linear phase detection and does not necessarily require advanced CMOS technology while maintaining a technology scalability feature.

Lastly, the Guest Editors of this special issue would like to thank all the reviewers for their dedicated efforts in ensuring a high standard for the selected papers. We hope that readers will find this issue interesting.

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