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COMPREHENSIVE SUMMARY OF PERFORMANCE-AFFECTING FACTORS OF CCDS

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This paper considers four factors affecting the functioning of a surface channel CCD. The factors considered are: the interface states, feed forward due to barrier modulation, surface potential fluctuations, and the avalanche multiplication in a CCD. A computer program has also been developed to analyze the performance of a CCD.

INTRODUCTION

In the performance of a CCD the most important factor is the CTI (charge transfer inefficiency), which reflects the ability of the device to maintain the integrity of the charge as they travel through the device. In this paper four factors have been considered and their effect on the functioning of the SCCD has been analyzed. The factors considered here are: the interface states, feed forward due to barrier modulation, surface potential fluctuations, and the avalanche multiplication in a CCD. A computer program has also been developed to analyze the performance of a CCD. The computer program and the result listing is attached at Appx A. The factor analyzed are the CTI due to interface states, edge effect, feed forward, and the variable transfer time. The minimum frequency limit imposed due to dark current is also calculated in the program. The various losses involved with the above phenomena have also been calculated in the program. The reduction of the diffusion constant as a result of surface potential fluctuations is also calculated.

CHARGE TRANSFER INEFFICIENCY DUE TO SURFACE STATES

The free charge transfer model predicts a very small transfer inefficiency for relatively low clock frequencies. In fact, according to the model, an arbitrarily high transfer efficiency can be obtained simply by reducing the clock frequency, thereby allowing enough time for the carriers to transfer to the next electrode. The experimentally-measured values of the transfer efficiency on early devices, however,

showed that transfer efficiency greater than 99.9% were extremely difficult to obtain even at low frequencies. The reason for this limit is the trapping of signal carriers at the surface states. The interaction of the signal carriers with the surface states, therefore, is the most important aspect of charge coupled devices from a practical point of view.

In a CCD such as shown in Fig. 1, the signal electrons are stored at the interface under an electrode. Some of the electrons will then make a transition from the conduction band to the surface states that are lower in energy and will be trapped there. Since the MOS capacitor is in deep depletion, there are no free holes that can recombine with the trapped electrons. When the remainder of the electrons in the conduction band are transferred to the next electrode, the surface states start to emit electrons to the conduction band. If the emission occurs while the surface potential profile is still moving the charge to the next electrode, the emitted electrons will join the remainder of the electrons and will not cause transfer inefficiency. If an electron is emitted from the surface state to the conduction band when the surface potential profile is no longer pushing to the next electrode, the electron cannot join the main charge packet and will cause transfer inefficiency. If no signal charge packet is directly following the main charge packet, the surface state will continue to emit the trapped electrons until a new charge packet comes along. The new charge packet will then fill up all the empty surface states. The number of electrons required to fill the surface states is a monotonically increasing function of the time interval between the two charge packets. These electrons are coming from the new charge packet and some of the trapped electrons cannot join the new charge packet because they are emitted too late. Therefore, the amount of charge lost due to the surface-state trapping depends on the number of empty charge packets even at a constant clock frequency. This property can be used to distinguish the transfer inefficiency due to the surface state trapping from free charge transfer.

Let $N_{ss}(E)$ = surface state density (no. of states $cm^{-2}\ eV^{-1}$)

$\eta_{ss}(E)$ = electron density trapped at the surface states (no. of electrons $cm^{-2}\ eV^{-1}$)

The capture and emission process of electrons can now be described.

Thus $$\frac{dn_{ss}}{dt} = v_{th}\sigma_n(N_{ss} - \eta_{nn})\eta - v_{th}\sigma_n N_c \eta_{ss} \exp\left(\frac{-t}{KT}\right) \qquad (1)$$

where: η is the number of electrons per unit volume in the conduction band (signal electrons)

E = Energy the trapped electron has to jump to make a transition from the surface state to the conduction band edge (E = Ec − Ft)

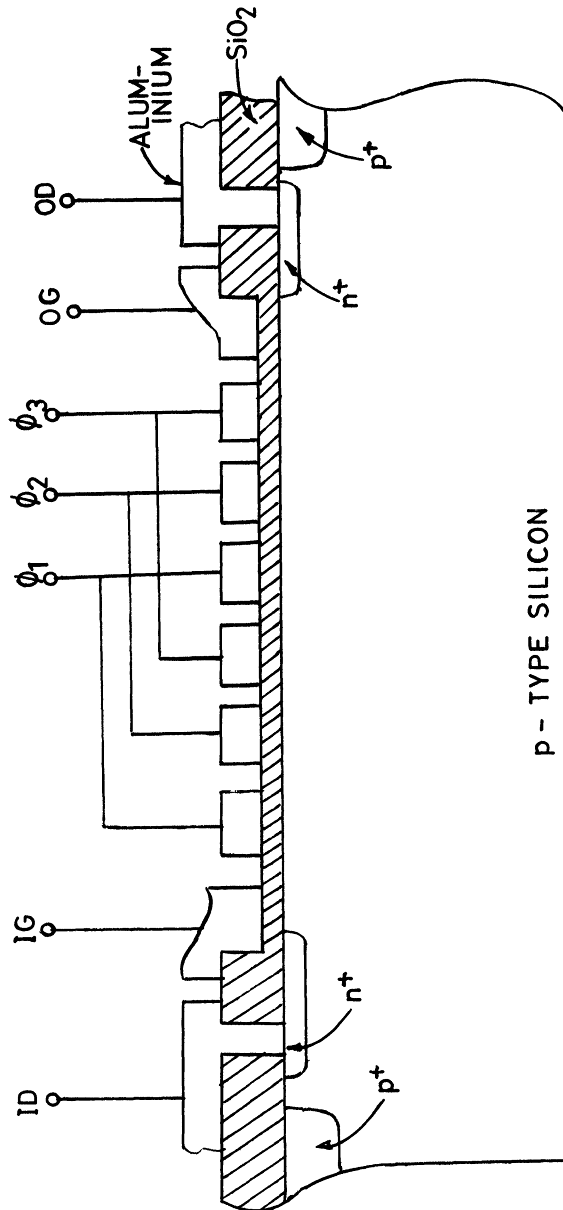

FIGURE 1 A three phase, n channel CCD.

If the signal electrons are stored under an electrode for a long time, a steady state is reached where $dn_{ss}/dt = 0$. In this situation

$$\eta_{ss} = \frac{N_{ss}}{1 + (N_c/\eta)\exp(-E/T)} \tag{2}$$

Suppose now that η_{ss} is altered from the steady state value by δn_{ss}. The variation of δn_{ss} with time is governed by

$$\frac{d\,\delta n_{ss}}{dt} = [v_{th}\sigma_n\eta + v_{th}nN_c(\exp(-E/KT))]\,\delta\eta_{ss} \tag{3}$$

which says that δn_{ss} decreases to zero with a time constant Z_c.

$$Z_c^{-1} = v_{th}\sigma_n\eta + v_{th}\sigma_n N_c(\exp(-E/KT)) \tag{4}$$

when a new charge packet arrives at an empty energy well, the surface states trap electrons and a steady state is reached in a time which is of the order of Z_c. For the surface states near the conduction band edge, the second term is dominant and Z_c is of the order of 1 ps. For those states located deeper in the bandgap, the second term becomes smaller and the time constant is longer. Due to the first term, however, Z_c, in the presence of a signal charge is usually very small (<1 ns), even for the deep surface states. Therefore, one can safely simplify the electron-capture process as being instantaneous.

The energy level up to which electrons are trapped can be found by comparing equation (4) with Fermi-Dirac distribution functions. From the comparison, one notes that an energy level similar to the Formi level can be defined as

$$E_{ff} = KT\ln\left(\frac{N_c}{n}\right) \tag{5}$$

In terms of the energy, equation (5) becomes

$$\eta = \frac{N_{ss}}{1 + \exp[(E_{ff} - E)/kT]} \tag{6}$$

Therefore, the surface states that are located deeper than E_{ff} for normal charge density are very small: one can assume as an approximation that all the surface states are filled in the presence of the signal charge.

As the signal electrons in the conduction band are transferred to the next electrode, the number of electrons under the original electrode decreases and equation (6) becomes

$$\frac{d\eta_{ss}}{dt} = v_{th}\sigma_n N_c\eta_{ss}\exp(-E/KT) \tag{7}$$

which says that the emission of electrons from the surface states to the conduction band is now dominant. The emission time constant is dependent on the energy level of the surface state as

$$Z_c^{-1} = \nu_{th} N_c \sigma n \exp(-E/KT) \tag{8}$$

If we assume that the surface states are completely filled at $t = 0$, the total number of electrons that are emitted in time t, N(t) is

$$N(t) = \int_0^{Eg} N_{ss}(E)\{1 - \exp[-t\nu_{th}\sigma_n N_c(\exp(-E/KT))]\}\, dE \tag{9}$$

This integral can be evaluated approximately for the case where N_{ss} and σ_n are not varying with energy, by noting that the quantity inside the brackets is close to either unity or zero, except around

$$E = KT \ln(tv_{th}\sigma_n N_c) \tag{10}$$

Therefore

$$N(t) \simeq KTN_{ss} \ln(\nu_{th}\sigma_n N_c t) \tag{11}$$

This implies that the filled states at $t = 0$ will empty to an energy level indicated by equation (10) by the emission process during a time period as illustrated by Fig. 2. For silicon, $(v_{th}\sigma_n N_c)$ is about $10'' s^{-1}$. If the surface states are allowed to emit electrons for 1 μs, those surface states within about 0.3eV from the conduction band edge will emit electrons. When a new charge packet arrives, these surface states will be filled again. It is clear therefore, that the states that contribute to the transfer inefficiency in a CCD are those near band edges rather than the midgap states. The distribution of the peak will determine the transfer inefficiency.

Let us now estimate the transfer inefficiency due to the surface states. Suppose signal charge packets of magnitude Q_s separated by Nz empty packets, are being shifted in a 3-phase CCD at a clock frequency f_0. The magnitude Q_s can be expressed as

$$Q_s = A_s C_{0x}\, \Delta V_s \tag{12}$$

where A_s = Area of the signal charge packet under an electrode

C_{0x} = oxide capacitance per unit area

ΔV_s = charge in surface potential due to signal charge

Let us now subdivide one clock period, $T_0 = 1/f_0$, into three time intervals as shown in Fig. (1a) and consider the surface states under one particular electrode of ϕ_1. During T_1 electrons are stored under the electrode: these by lowering the surface potential by V_s. All the surface states are filled except those very close to the conduction band edge. During T_2, most of the electrons are transferred to the next

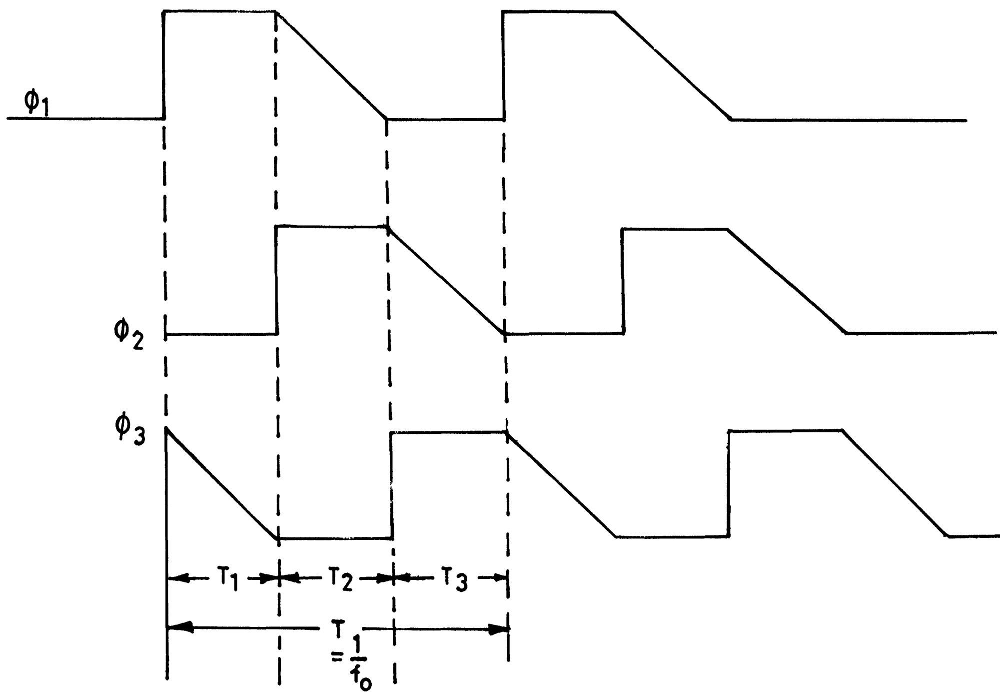

FIGURE 1a Subdivision of clock period.

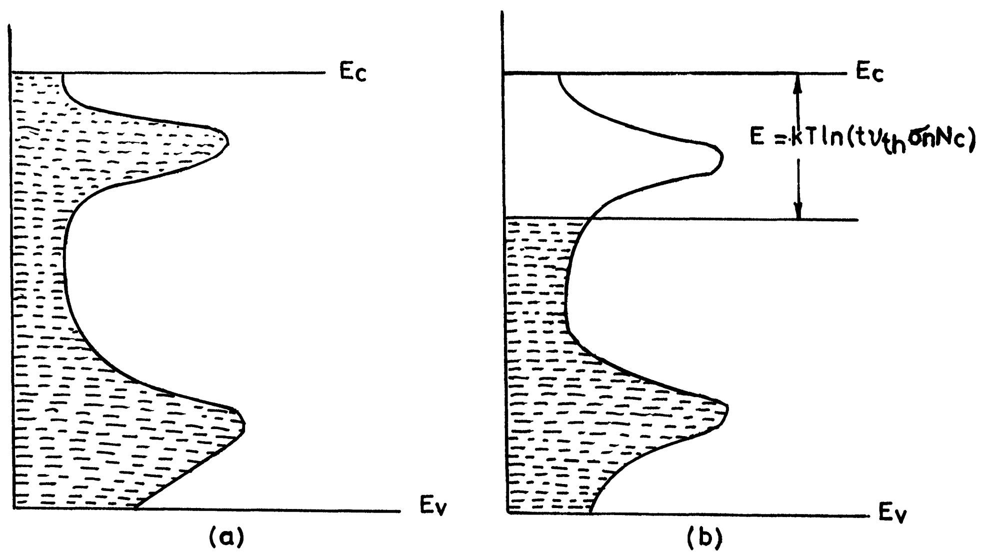

FIGURE 2 Emission of electrons from the surface states. (a) All the surface states are filled. (b) Surface states near conduction band have emitted electrons.

electrode by the free charge transfer model. If the clock frequency is low, one can asume that all the electrons in the conduction band are transferred to the next electrode in a very short time at the beginning of T_2. During the remaining period of T_2, surface states emit electrons and these electrons will be transferred to the next electrode joining the main-charge packet. The number of electrons emitted during this time period will be approximately

$$N(T_2) = A_sN_{ss}KT \ln(T_2 v_{th} \sigma_n N_c) \tag{13}$$

During T_3, emitted electrons can move forward or backward depending on the exact position of surface state − surface potential profile. Here we assume that all the electrons emitted during T_3 do not join the main charge packet. This assumption gives the worst case estimate of the transfer inefficiency. During T_3 and the next N_zT_0 time periods, the surface-states continue to emit electrons. The total number of electrons emitted before the second charge packet arrives is then

$$N(T_2) + N(T_3) + N(N_zT_0) = A_sKTN_{ss} \ln[(T_2 + T_3 + N_zT_0)_s]v_{th}\sigma_n N_c] \tag{14}$$

when the second charge packet arrives, the surface states are filled again. If we neglect those surface states very near the conduction band edge that are not filled, the number of electrons used to fill the surface states is the same as equation (14).

When the second charge packet is transferred to the next electrode, some-trapped electrons are emitted and join the main charge packet; a process similar to that which occurred during T_2 when the first charge packet was transferred. Thus, the net loss for the second charge packet is

$$N_{loss} = A_sKTN_{ss} \ln[(T_2 + T_3 + N_zT_0)v_{th}\sigma_n N_c] - A_sKTN_{ss} \ln[T_2 v_{th} \sigma_n N_c] \tag{15}$$

Since $T_1 = T_2 = T_3 = T_0/3$ for normal operation of a 3-phase C_{CD}

$$N_{loss} = A_sKTN_{ss} \ln[2 + 3N_z] \tag{16}$$

The transfer inefficiency is simply the ratio of qN_{loss} to Q_s.

$$= \frac{qKTN_{ss}}{C_{ox}\, \Delta V_s} \ln[2 + 3N_z] \tag{17}$$

Note here that the transfer inefficiency is independent of the clock frequency. Therefore, when the clock frequency is sufficiently low, the transfer inefficiency is determined not by the free charge transfer but by the surface state trapping. The magnitude of inefficiency for

$$C_{ox} = 3.5 \times 10^{-8}$$

$$v_s = 5V$$

$$N_{ss} = 10'' \text{ cm}^{-2} \text{ eV}^{-1}$$

is about 4×10^{-3} at room temperature for $V_z = 1$. Although the result has been obtained with many assumptions, this value is in reasonable agreement with experimentally measured inefficiency.

In digital applications of CCDs, one and zero can be represented by the presence and absence of signal charge in the energy well. However, one can also represent ZERO by small charge packet rather than the absence of it as long as the output circuit can distinguish it from ONE. The ZERO is called background or FAT ZERO. In the presence of FAT ZERO, all the energy wells in a CCD have signal charge and the surface states are not subjected to a long emission process. Therefore, the transfer inefficiency due to the surface states will be much smaller.

FEED FORWARD DUE TO BARRIER MODULATION IN CHARGE COUPLED DEVICES

Conventionally, the physics of the CCD has been studied by assuming that the signal charge has no influence on the potential distribution in the barrier region. However, Brodersen et al. (1) and Krambeck et al. (2) have considered the effect of signal charge on the barrier potential to some extent and have described its effect on the free charge transfer resulting in charge transfer inefficiency (CTI). All these have shown that there exists a retarding electric field due to the presence of signal charge, which reduces the collection of carriers by the signal packet, and hence results in CTI.

Let us consider the effect of charge induced retarding field, which results in modulation of the barrier potential, on the charges emitted from the interface states. It has been shown that phenomenon of barrier modulation can result in another source of signal degradation called "feed forward of charge" (3) and would also contribute to the CTI.

BASIC CONCEPTS OF BARRIER MODULATION

In a CCD, the charge packets are separated by the barriers, which are either inherent in the structure or are created by suitable clocking of gate electrodes (4). The exact shape of barriers is a function of charges contained in the wells. To illustrate the point, let us consider three different situations for a 3-phase CCD shown in Fig. 3. The instant for which the surface potentials are shown is when two adjacent electrodes are ON and the barrier is provided by the third electrode. The three situations are:

1) The wells on both sides of the barrier contain equal charges as shown in Fig. 3a. The barrier will be symmetrical about the midpoint.

2) The left well contains more charge than the right well as shown in Fig. 3b. The barrier is no longer symmetrical and the location of the peak of the barrier would shift towards the left. This is because the surface potential on the left of the barrier is lower in magnitude than the surface potential on the right.

3) The right well contains more charge than the left well as shown in Fig. 3b. The location of the peak of the barrier would shift towards the right.

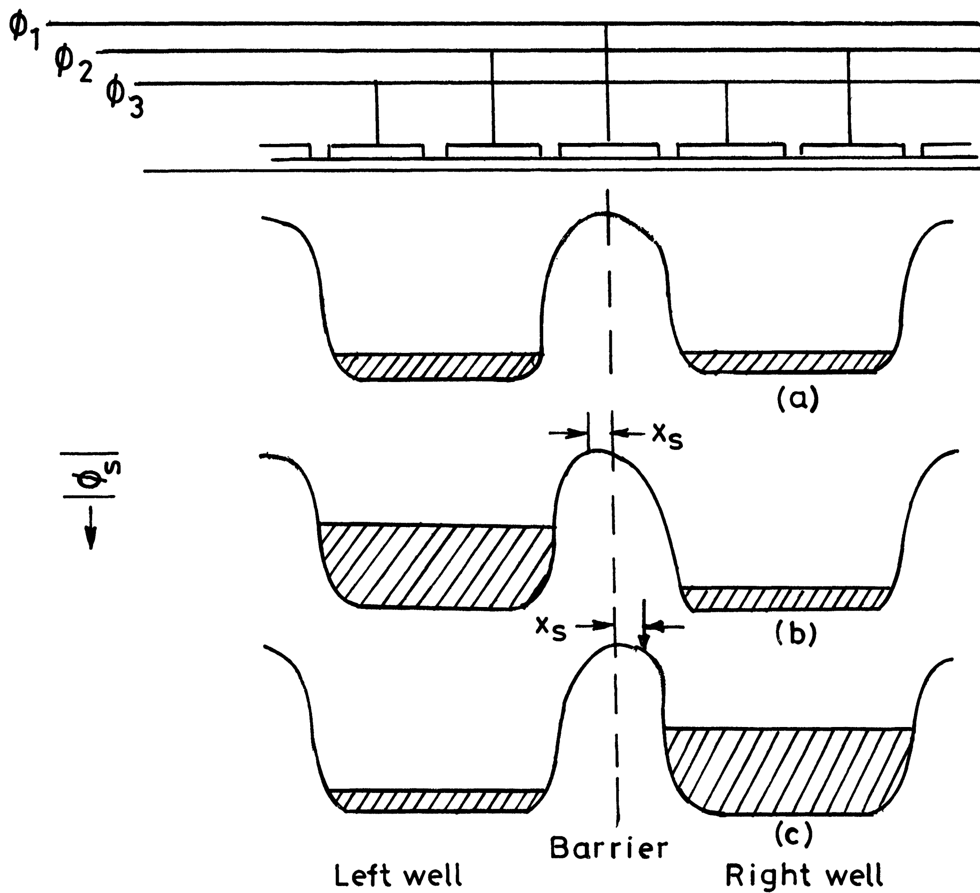

FIGURE 3 Barrier modulation concept.

Let us consider a carrier emitted by an interface state located in the barrier region. If the carrier is emitted from a region away from the peak barrier location, it would drift to the side well because of the large electric field present there. But if it is emitted from near the peak barrier location, where the electric field is small, its motion will be determined by the electric field as well as thermal diffusion. Due to thermal diffusion some of the carriers emitted from the right side of the barrier peak can join the left well and some of those emitted from the left side can join the right well. If the potential is symmetrical near the peak barrier and the emission rates on both sides of the barrier are equal, then we can expect that the number of those carriers emitted from the left side of the peak barrier location that will join the right well will be equal to the number of carriers emitted from the right side that will join the left well. So the net charges that will join each side well will be equal to those emitted from the same side of the peak barrier location.

The above analysis implies that both the wells in situation 1, Fig. 3a will collect equal charges. However, in situation 2 and 3, the asymmetry of the barrier will

result in the collection of more emitted charges by the well, containing lesser charge as compared to situation 1.

To calculate the excess charge collection, the exact shape of barrier potential for the different situations will have to be computed. A comparison of the results will give the shift X_s (Fig. 3) in the location of the peak barrier potential. The amount of shift X_s would give an idea about the excess charge.

Let the peak barrier be at $X = X_0$ when the wells on each side of the barrier contain ZERO (FZ) charges. To a first order approximation, the electric field E(x) near X_0 may be approximated by the first term in the Taylor series expansion.

$$E(x) = E'(x_0)(x - x_0) \tag{18}$$

where $E'(x_0)$ is the electric field gradient at $x = x_0$. Let the signal charge (q_{sig}) plus FZ charge be in the left well while the other well contains only FZ charge. Let the electric field in the barrier region due to this be $E_s(x)$. Then to another first order approximation we assume:

$$E_s(x) = q_{sig}\alpha_e(x) \tag{19}$$

where $\alpha_e(x)$ is the electric field per unit signal charge.

Let the peak barrier location now be at $x = x_m$. This is the location where the net electric field is zero. Assuming that the net electric field is the sum of the electric field given by equations (18) and (19) we get

$$E'(x_0)(x_m - x_0) + q_{sig}\alpha_e(x_m) = 0 \tag{20}$$

$$X_s = x_m - x_0$$

$$= -\frac{q_{sig}\alpha_e(x_m)}{E'(x_0)} \tag{21}$$

The above equation (21) gives a good quantitative picture of the barrier modulation phenomenon and indicates that the shift is inversely proportional to the electric field gradient at the peak of the barrier, and is proportional to the signal charge.

Again from the Fig. 3 we can see that when the shift is towards left (Fig. 3b) it is easier for charge in the left well to spill over to the right well (considering it has a ONE) and this is called the feed forward. For the case of right shift we have a reverse case, i.e., the charge in the right well moves towards the left giving us feed backward. This is confirmed by the calculated percentage shift (X_s/L_b) of the peak barrier location as a function of signal charge in one of the wells, when the adjacent well carries FZ charge corresponding to 5% of full well capacity. The results show that the percentage shift is reduced for larger electrode length. The shift is as much as 20% for the barrier length of 5 μm and signal charge of 80%. This implies that a ZERO which is following a ONE, will collect excess charge from this shift region, compared to the case when it is following a ZERO. Similarly, a ZERO that is followed by a ONE will collect more charge than the case when it is followed by

a ZERO. The former effect will give rise to an effective feed backward and latter will result in feed forward.

CALCULATION OF THE FEED FORWARD CHARGE

Consider the 4-phase push operation of the CCD. The clock-waveforms are shown in Fig. 4. The surface potentials at various instance of time are shown in Fig. 5 in terms of the following parameters:

T_t—is T_c/p, where T_c is the clock period and p is the number of phases.
K_0—is the FZ charge as a fraction of the full well charge.
t_{off}—is the turn off time of any of the phase clocks.
W—width of channel

Let the surface potential beneath ϕ_2 and ϕ_4 in their OFF condition be less than that of ϕ_1 and ϕ_3.

1) At $t = 0^-$ the charge is stored under ϕ_2 and ϕ_3 (Fig. 5a)
2) At $t = 0^+$, ϕ_4 turns on and ϕ_2 starts to turn off. At $t = K_0 t_{off}$, FZ charge leaves ϕ_2 (Fig. 5b).
3) At $t = t_{off}$, ϕ_2 has fully turned off and the barrier peak is under ϕ_2.

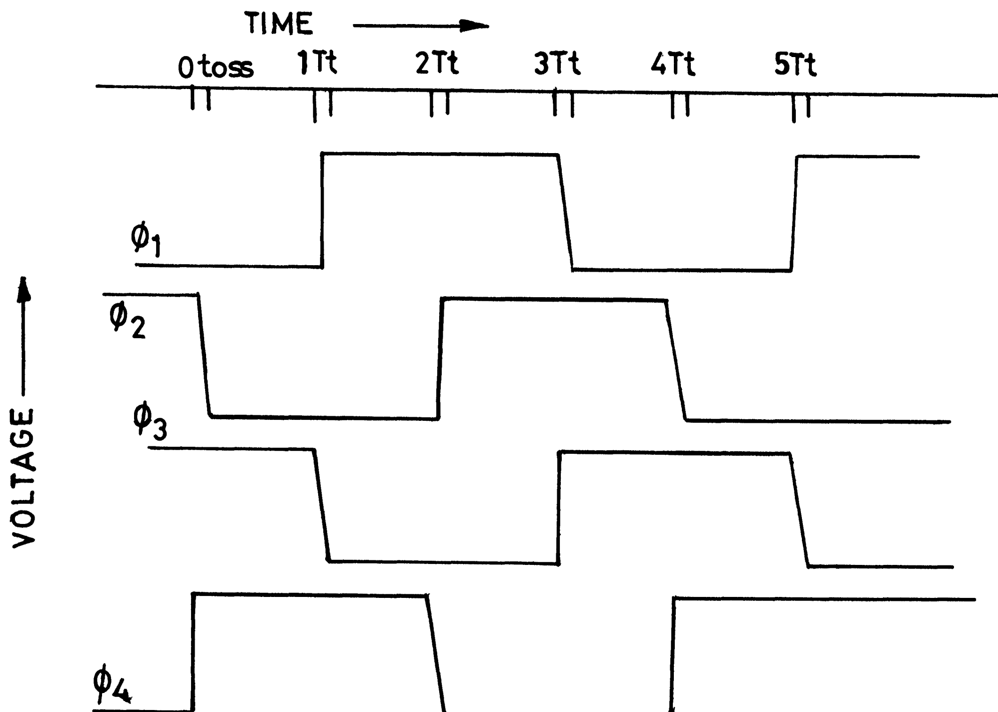

FIGURE 4 Clock waveforms—4 phase.

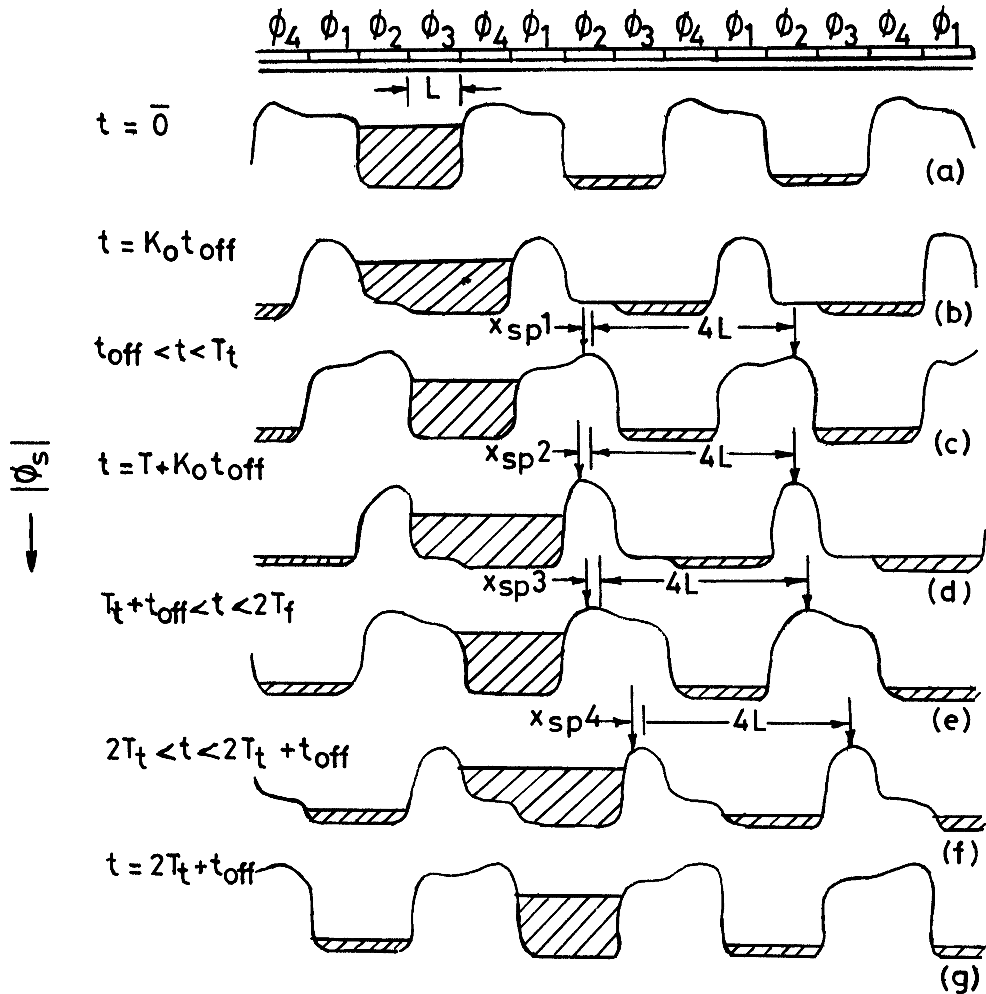

FIGURE 5 Surface potentials for various instants of time for 4-phase push clock.

4) At $t = T_t^+$, ϕ_1 goes on and ϕ_3 starts to turn off. At $t = T_t^+ + K_0 t_{off}$, all the FZ charge leaves ϕ_3 and at $t = T_t + t_{off}$, ϕ_3 has fully turned off (Fig. 5f).
5) At $t = 2T_t^+$, ϕ_2 goes on and ϕ_4 starts to turn off (Fig. 5e).
6) At $t = 2T_t + t_{off}$, ϕ_4 has fully turned off.

Let us consider the feed forward charge Q_{FP} per two transfers i.e. during $t = t_{off}$ to $2T_t + t_{off}$. There are four distinct durations that can be considered:

1) $t = t_{off}$ to T_T, when the peak barrier is under ϕ_2 which is the right barrier electrode (Fig. 5c). Let the shift be X_{sp1}.
2) $t = T_t$ to $T_t + t_{off}$, when the peak barrier is under ϕ_2, and ϕ_2 is the left barrier electrode and ϕ_3 is turning off (Fig. 5d).

3) $t = T_t + t_{off}$ to $2T_t$, when the peak barrier is under ϕ_2 and it is the left barrier electrode (Fig. 5e). Let the shift be X_{sp3}.
4) $t = 2T_t t_0 - 2T_t + t_{off}$, when the peak barrier is under ϕ_3 and it is the left barrier electrode. Let the shift be X_{sp4}. Let q_{fp1}, q_{fp2}, q_{fp3} and q_{fp4} be the feed forward charges during the above mentioned 4 durations, respectively.

The number of charges emitted per $= N(t) = N_{ss}KT1_n(\sigma_n t \nu_{th} N_c)$ per unit Area in time t_v. So the total charges emitted per unit area between times t_1 and t_2, when the free charge leaves the electrode at time t_0, can be derived as:

$$N(t_2, t_1, t_0)N_{ss}KT \ln\left(\frac{t_2 - t_0}{t_1 - t_0}\right) \tag{22}$$

Using the above equation

$$q_{fp1} = X_{sp1}W_qN_{ss}KT \ln\left(\frac{T_t - K_0t_{off}}{t_{off} - K_{0toff}}\right) \tag{23}$$

$$q_{fp2} = x_{sp2}W_qN_{ss}KT \ln\left(\frac{(T_t + t_{off}) - K_0t_{off}}{T_t - K_0t_{off}}\right) \tag{24}$$

$$q_{fp3} = x_{sp3}W_qN_{ss}KT \ln\left(\frac{2T_t - K_0t_{off}}{(T_t + t_{off}) - K_0t_{off}}\right) \tag{25}$$

$$q_{fp4} = x_{sp}4W_qN_{ss}KT \ln\left(\frac{(2T_t + t_{off}) - (T_t + K_0t_{off})}{2T_t - (T_t + K_0t_{off})}\right) \tag{26}$$

Let us assume x_{sp2}, x_{sp3}, x_{sp4}, which are shifts when the barrier peak is under the left barrier electrode, are all equal to x_{spL} and x_{sp1}, which is the shift when the barrier peak is under the right barrier electrode. Then taking $k_0t_{off} \ll t_{off}$ and T_t, we get from eqs. (23) to (26)

$$2_{fp} = x_{spR}W_qN_{ss}KT \ln\left(\frac{T_t}{t_{off}}\right) + x_{spL}W_qN_{ss}KT \ln\left(\frac{2(T_t + t_{off})}{T_t}\right) \tag{27}$$

CTI DUE TO BARRIER MODULATION

Barrier modulation will not only result in feed forward of charge but also would result in CTI. When a 3- or 4-phase CCD is operated with push clock, normally the barrier is provided by two or three adjacent electrodes. There are four types of barriers that are usually encountered in a CCD. These are shown in Fig. 6a,b,c,d. We shall refer to them as case 1, 2, 3 and 4 respectively. Let ϕ_{sL} and ϕ_{sr} be the nominal surface potentials (magnitude) beneath the left and the right barrier electrodes respectively. In cases 1 and 2 (Fig. 6a and 6b), the barriers are asymmetrical about the inter electrode gap. In case 1, $\phi_{sr} < \phi_{sL}$ and the peak barrier

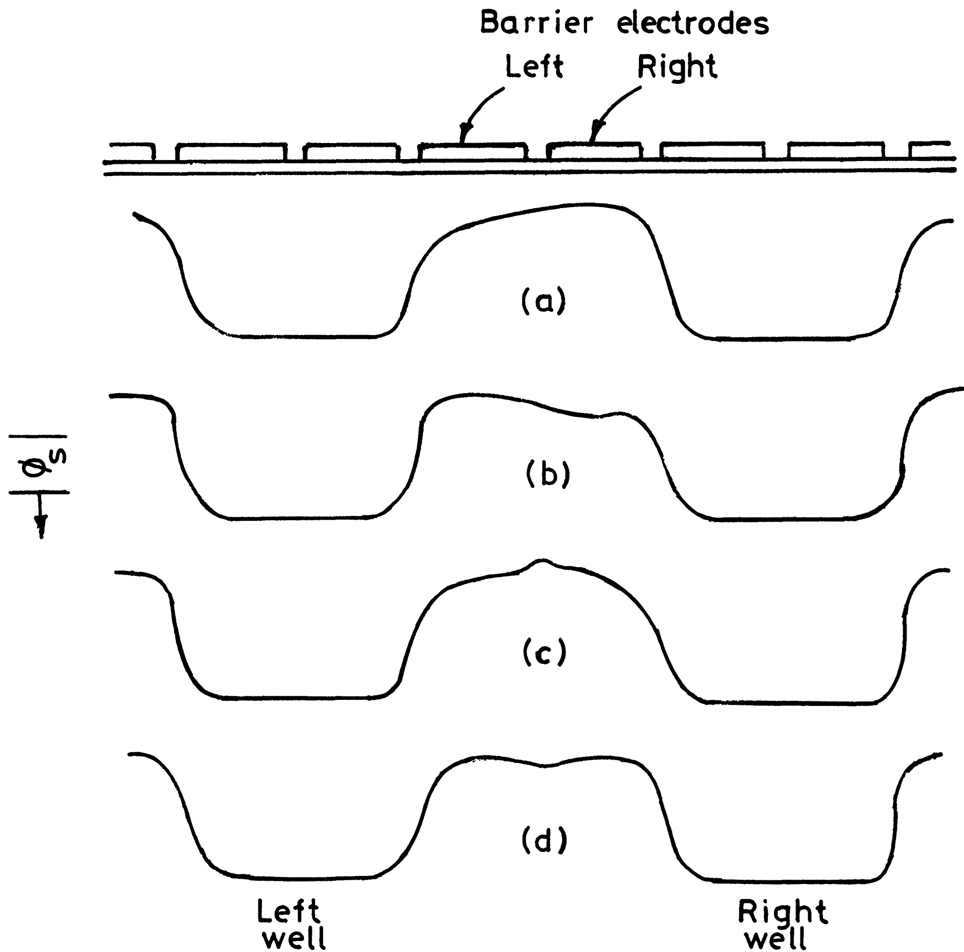

FIGURE 6 Four types of barriers.

location is beneath the right barrier electrode. In case 2, $\phi_{sr} > \phi_{sL}$ and the peak barrier location is beneath the left barrier electrode. In case 3 and 4 (Fig. 6c and 6d), the barriers are symmetrical and $\phi_{sr} = \phi_{sL}$. In case 3, there is a small local barrier beneath the inter-electrode gap region, where as in case 4 there is a small local well beneath the gap region.

Asymmetrical wells are formed when the OFF voltages of the phases have not been compensated for the threshold voltage difference of the electrodes. When the OFF voltages have been compensated for the threshold voltage difference, a symmetrical barrier with a small local barrier beneath the gap region (Fig. 6c) is usually formed for a p-channel device. However, in case of an n channel device with wide inter-electrode gaps, a local well can be formed (Fig. 6d).

Let us consider the barrier modulation for the four different cases mentioned above. Due to barrier modulation, the CTI will arise because of the shift in the

peak barrier due to the presence of signal charge in the well on the right of the barrier (Fig. 6c). This is in contrast to the feed forward, which arises because of the shift in the peak barrier modulation due to signal charge in the well on the left of the barrier.

Case 1

The peak barrier location is under the right barrier electrode as shown in Fig. 7a. Due to the presence of a signal charge (ONE CHARGE) in the well to the right of it, the barrier peak will shift towards the right as shown. Let the shift be x's as shown previously.

$$q_b = x's\ W_q N_{ss} KT \ln \left(\frac{T_t - K_1 t_{off}}{t_{off} - K_1 t_{off}} \right) \tag{28}$$

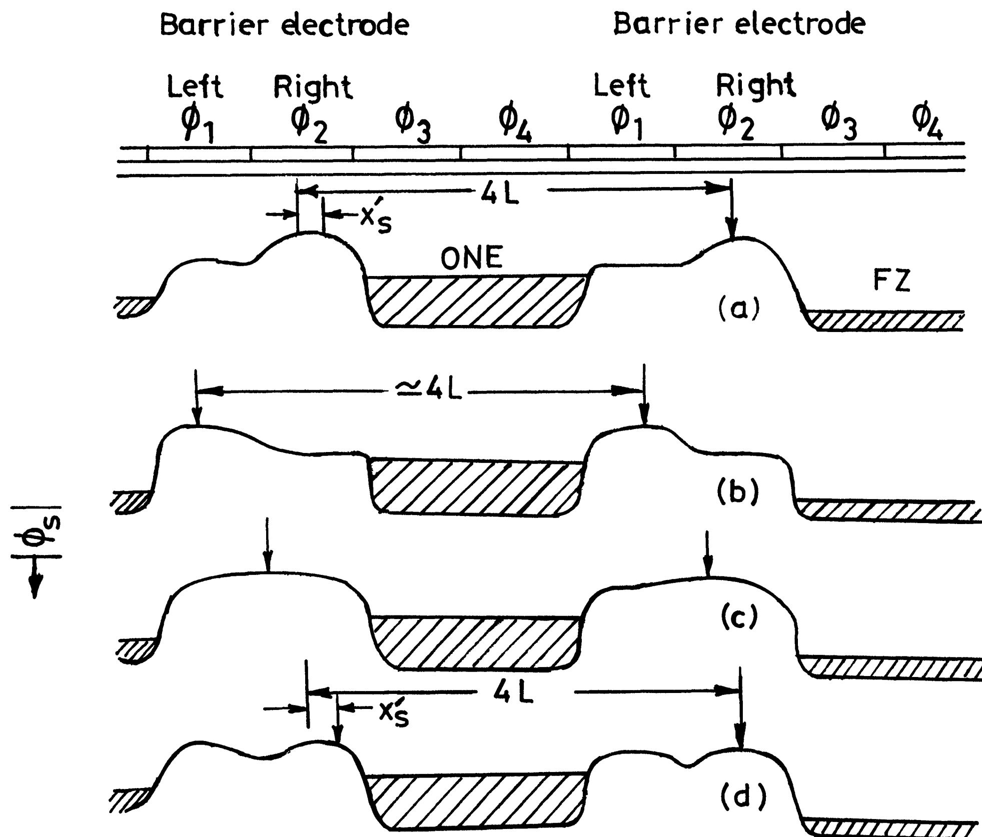

FIGURE 7 CTI due barrier modulation.

where ($t_{off} - K_1 t_{off}$) is the time that the electrode takes to turn off after ONE charge leaves the electrode. For the case $t_{off} < T_t$ this loss can be significant. When $K_1 t_{off} \ll T_t$ and t_{off}, we get

$$q_b = X's\ W_q N_{ss} KT \ln\left(\frac{T_t}{t_{off}}\right) \tag{29}$$

Case 2

The peak barrier location is under the left barrier electrode and is far off from the signal charge (Fig. 7b), and the electric field decreases very rapidly with distance. Thus, the contribution to CTI would also be negligible.

Case 3

The peak barrier is under the inter-electrode gap (Fig. 7c) and the contribution to CTI due to barrier modulation in this case would be similar to the contribution to feed forward, which has been described earlier.

Case 4

This contribution would be similar to Case 1. Although there are two barrier peaks present, the shift in the peak barrier location under the right barrier would be effective in contributions to CTI; since this barrier peak is near the signed charge, the loss would be given by eq. (29).

SURFACE POTENTIAL FLUCTUATIONS

Surface potential fluctuations have been characterized in MOS capacitors by Nicollian and Goetzberger [5] and JR Brews [6]. These fluctuations arise mainly due to the random distribution of fixed and interface charges and they result in an electric field over and above the normally calculated value, which does not take into consideration these fluctuations

In the patch work model proposed by Nicollian and Goetzberger [5], the surface potetnail is assumed to be constant under each patch of a characteristic Area A_c. The r.m.s. value of the surface potential fluctuation, σ_s, is proportional to $(N_{ox})^{1/2}$, where N_{ox} is the number of charges per cm^2 at the interface [6].

The measured value of σ_s has been found to lie between 40 to 67 mV for N_{ox} in the range of 3×10^{10} to 2×10^{11} cm^{-2} [7]. In the model proposed by Nicollian and Goetzberger, the surface potentials beneath various patches are also assumed to be uncorrelated and this would mean that the surface potential can change significantly over a distance of $(A_c)^{1/2}$. Nicollian and Goetzberger also found the values of A_c to be about 2.5×10^{-10} cm^2. Thus, $(A_c)^{1/2} = 1.5 \times 10^{-5}$ cm. Let a potential variation of 45 mV take place over this distance. This would mean that there would exist an electric field whose average magnitude value is about 3×10^3V/cm larger due to these fluctuations: this is much larger than the electric fields

encountered near the barrier peak. The existence of these large electric fields due to the surface potential fluctuations would obviously affect the charge movement. These fluctuations would also result in small potential wells and barriers to be formed under the electrodes, and charge movement would mainly be determined by the diffusion charges over the small barriers: primarily it would be the average electric field profile obtained by ignoring these fluctuations, which would determine the sharing of the charges omitted from the barrier region between the two wells. So it would be reasonable to assume that the charges emitted from the left of the barrier peak (determined by the average electric field) would move towards the left well and those emitted from the right will join the right well.

CTI DUE TO SURFACE POTENTIAL FLUCTUATIONS

Due to the trapping of charges in the wells formed because of surface-potential fluctuations, CTI is increased. This possibility has been briefly mentioned by Taylor and Chaterjee [8]. Let us consider this in detail.

Due to the formation of small wells under an electrode because of surface potential fluctuation (Fig. 8), the free charges would get trapped and they will have to cross small barriers to join the signal packet. This will slow down the charge transfer process. These fluctuations can be characterized by a simple first order model.

MODEL

Let the surface potential fluctuations be represented by small wells of constant depth ϕ_d. Consider a one-dimensional model where the width of the wells is equal to the width of the channel. The length of the well and the barriers are L_{sw} and L_{sb} respectively (Fig. 9). Let q_{an} and ϕ_{nn} represent the charge concentration per cm^2 and the barrier height for the nth well under an electrode, respectively. Since no electric field is assumed to be present in the barrier region, only diffusion current

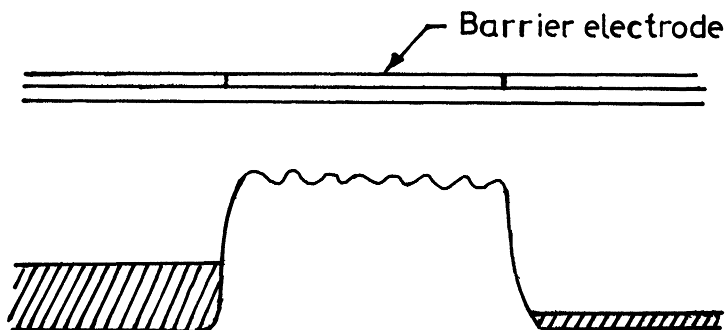

FIGURE 8 Small wells formed due to surface potential fluctuations.

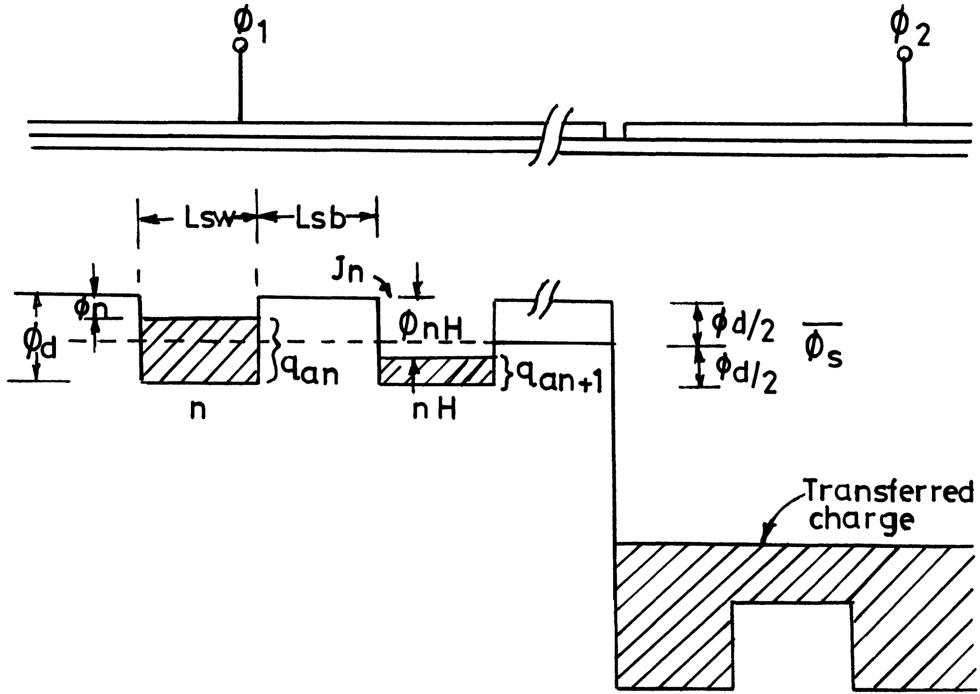

FIGURE 9 Surface potential fluctuation model.

would flow. The current J_n per unit width between n^{th} and $(n + 1)^{th}$ well would be [9, 10].

$$J_n = \frac{D}{L_{sb}} [q_{an} \exp(-\phi_n) - q_{an+1} \exp(-\phi_{n+1}\beta)] \tag{30}$$

where $\beta = q/KT$ and D = Diffusion coefficient of carriers. (31)

and

$$\Delta\phi_n = \phi_{n+1} - \phi_n \tag{32}$$

Thus, we get

$$J_n = \frac{D}{L_{sb}} \{q_{an} \exp(-\phi_n\beta)\{1 - \exp(-\phi_n\beta)\} - \Delta q_{an} \exp(-\phi_n\beta) \exp(-\Delta\phi_n\beta)\} \tag{33}$$

Assuming $\Delta\phi_n \ll 1/\beta$ and since

$$\phi_n = \phi_d - \frac{q_{an}}{C_{ox}} \tag{34}$$

We get

$$\Delta\phi_n = -\frac{\Delta q_n}{C_{ox}} \tag{35}$$

and

$$J_n - \frac{D}{L_{sb}} \Delta q_{an} \left(1 + \frac{q_{an}\beta}{C_{ox}}\right) \exp(-\phi_n\beta) \tag{36}$$

For the case $q_{an}/C_{ox} \ll q/\beta$, which holds for the last pattern of the charge, we get from equation (34)

$$\phi_n \cong \phi_d \tag{37}$$

and so

$$J_n = -\frac{D\ \Delta q_{an} \exp(-\phi_d\beta)}{L_{sb}} \tag{38}$$

Equating

$$\frac{\Delta q_{an}}{L_{sw}} + L_{sb} = \frac{dq_a(x)}{d_x} \tag{39}$$

and letting $L_{sw} = L_{sb}$ we get

$$J_n = -D_{eff} \frac{dq_aZ(x)}{d_x} \tag{40}$$

where $D_{eff} = -2D \exp(-\phi_d\beta)$ (41)

This equation indicates that in the presence of surface potential fluctuations the effective diffusion coefficient, D_{eff}, would reduce significantly when $\phi_d \gg 1/\beta$. The way this model has been described, the value of ϕ_d would be 2 σ_s where σ_s is the rms value of surface potential fluctuations. This is derived below:

σ_s is defined as

$$\sigma_s^2 = \frac{1}{L_f} \int_0^{L_f} (\phi_s(x) - \phi_s)^2\, dx \tag{42}$$

where L_f = Any large length

$\phi_s(x)$ = Surface potential at x.

$\phi_s(x)$ = Average value of surface potential at x.

The dash-dot line in Fig. 9 represents the average value $\phi_s = \phi_d/2$ below the barriers. The potential at barriers $\phi_s - \phi_{d/s}$ and at the bottom of the wells is $\phi_s + \phi_d/2$. Using equation (42) we get

$$\sigma_s^2 = \phi_d^2/4$$

or

$$\sigma_s = \phi_d/2 \quad \text{or} \quad \phi_d = 2\sigma_s \tag{43}$$

For the reported values of σ_s in the range of 40–67 mV, the effective diffusion coefficient D_{eff} for the last portion of the charge to be transferred would be reduced by a factor of about 10–100 over the normally assumed value. This indicates that the charge transfer process would slow down considerably and can result in CTI.

AVALANCHE MULTIPLICATION IN CHARGE COUPLED DEVICE

Avalanche multiplication in semiconductor devices is a well known phenomena [11, 12]. This occurs when carriers pass through an electric field of the order of 10^5 V/cm. Due to the high electric field, the carriers attain sufficient energy to generate hole-electron pairs. The high energy carriers are called hot carriers. The generated carriers add to the signal charge, and hence give rise to effective carrier multiplication.

In charge coupled devices, application of a voltage of the order of 10V between the-closely-spaced electrodes results in a maximum electric field of the order of 10^5 to 2×10^5 V/cm beneath the interelectrode gaps. This high electric field can result in a number of phenomena in CCD, such as carrier velocity saturation, [11–13], lower probability for a carrier to get trapped in an empty interface state and high emission probability for the trapped charges [11], reduced charge handling capacity [14], and avalanche multiplication (impact ionization) [11, 12].

Hess & Sah [11, 12] have pointed out the theoretical possibility of avalanche multiplication. Let us consider this in detail.

THEORETICAL POSSIBILITY OF AVALANCHE MULTIPLICATION IN CCDS

Consider a 2-phase CCD. In such a CCD, there is a barrier to give directionality to charge transfer as shown in Fig. 10. This barrier could be achieved by suitably

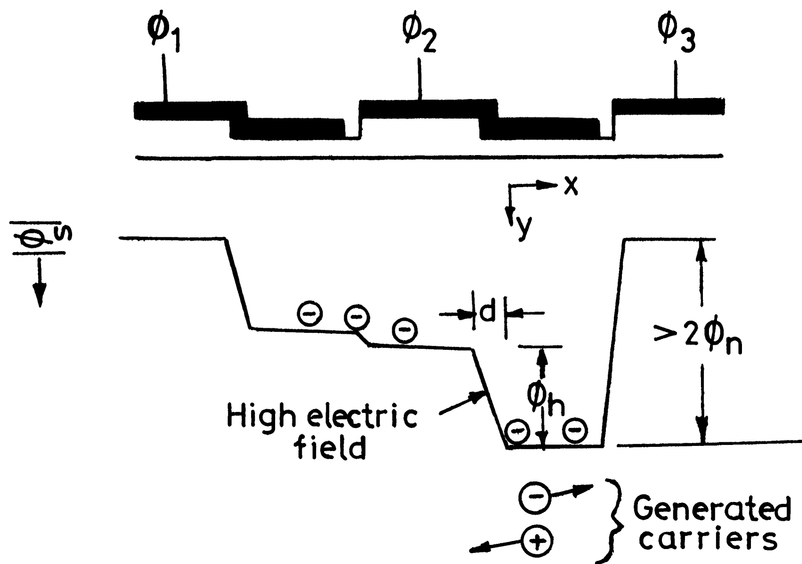

FIGURE 10 2ϕ CCD with surface potential diagram.

clocking a 4-phase CCD [4]. The presence of a barrier gives rise to a large electric field, which is typically concentrated within about 1 μm around the inter-electrode gap [15]. For a sufficiently larger barrier height ϕ_h (Fig. 1c), a large electric field of the order of 10^5 V/cm may be present over a distance 'd' of 1 μm, and this can cause generation of hole-electron pairs due to impact ionization when a carrier falls down this barrier and becomes hot. In an n-channel device, the generated electrons will add to the signal packet and the generated holes will tend to drift towards the bulk semiconductor and contribute to the substrate current. The generated electrons and the signal electrons can again acquire sufficient energy and generate more hole-electron pairs, thereby causing an effective multiplication of the signal charge. The generated holes will be subjected to two electric fields: the field along the surface will tend to move them towards the barrier ($-$x direction) and the field in the y direction will result in their drifting towards the bulk semiconductor (see Fig. 1c). If the electric field in the x direction is large compared to that in the y direction, the holes will tend to remain in the high electric field region for a longer duration and can also cause further ionization. However, we will neglect the effect of generated holes since the ionization rate of holes is typically less than that of electrons by a factor of 5 to 10. So we assume that the multiplication is due to electrons only.

It has been observed experimentally that Avalanche multiplication results in an increase of charge at the output, and this has been measured. In an overlapping gate CCD, it has been observed to occur at 8 V, which is not very high. Because of the fact that avalanche multiplication has been observed to occur at a much lower voltage than the oxide breakdown voltage, the upper limit to the amplitude of clock voltages that can be applied to a CCD is likely to be determined by this

avalanche multiplication mechanism rather than oxide breakdown criterion. For CCD structures that have wide gaps, the avalanche multiplication is expected to occur at higher amplitude levels because the peak value of electric field present in the interelectrode gap region is lower than that for an overlapping gate structure. Generally in a 3- or 4-phase CCD operated with push clocks, the rise and fall times of the clock pulses are not less than a few tens of a nanosecond. Under these conditions, the bulk of the free charge can quickly equilibrate, and no avalanche multiplication is expected in the initial stage of charge transfer. But the last fraction of free charge and charge emitted from the interface states can get multiplied due to a high electric field that they would encounter near the inter-electrode gaps when the transferring electrode has been turned off.

In 2-phase operation, the free charge can experience avalanche multiplication even for small ϕ_h of the order of 4–5 V.

Consider Fig. 10 and 11. Let us now calculate the increase in the output charge due to avalanche multiplication. For the sake of simplicity in the analysis, we neglect the depletion layer charge. For a gate voltage V_g the surface potential V_s is given by

$$\phi_s = V_g - \frac{q_n}{C_e} - V_{FB} \tag{44}$$

where q_n = magnitude of the minority carrier

C_e = Electrode capacitance of ϕ_2 & ϕ_4 gates

V_{FB} = Flatband voltage

Let ϕ = Difference between the surface potential beneath ϕ_4 and beneath ϕ_3 (Refer to Fig. 11) and let $\Delta\phi = \Delta\phi_0$ when ϕ_4 does not contain any charge.

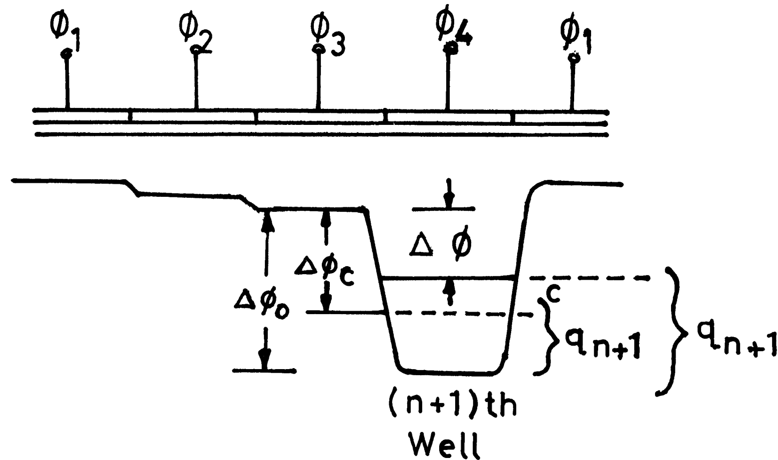

FIGURE 11 Surface potential diagram for different levels of charges in a CCD well.

Let V_{T_d} = Threshold voltage difference between ϕ_2 and ϕ_1 as well as between ϕ_4 and ϕ_3. Now when ϕ_4 contains charge q_n,

$$\phi = (V_{n_2} - V_{n_1} - V_{T_d}) - \frac{q_n}{C_e} \tag{45}$$

In a CCD, the avalanche multiplication basically depends upon the profile of electric field beneath the interelectrode gap region. These are various clocking and device parameters that affect this electric field profile. The most important parameters are the clock voltages, charges contained in the well,and the oxide thickness [15]. However, to make the calculations simpler we assume that the electric field only depends upon the surface potential difference between the two adjacent electrodes. Hence, the gain factor g will be a function of $\Delta\phi$. For input charge q_n into the $(n + 1)^{th}$ well, the output charge q_{n+1} after one transfer will be

$$Q_{n+1} = q_n(1 + g(\Delta\phi)) \tag{46}$$

This equation is valid only for small values of input charge q_n, because for large values of q_n, the $\Delta\phi$ will itself vary during the charge transfer process and output charge may not be linearly related to the input charge.

For an input charge q_0 into the CCD, the output charge q_N after N number of transfers would be

$$q_N = q_0(1 + g(\Delta\phi)^N) \tag{47}$$

and the gain in the output charge q_N will be

$$q_N = q_N - q_0(1 + g(\Delta\phi)^N) - 1 \tag{48}$$

It has been found that the gain factor is negligible for small ϕ and then increases rapidly. Let

$\Delta\phi_c$ = Critical value below which $g(\Delta\phi)$ is assumed to be zero.

Let us consider the charge transfer process when charge enters ϕ_4 from ϕ_2 across ϕ_3 electrode (Fig. 11).

$\Delta\phi_0$ is the barrier height for no charge in ϕ_4. With charge entering ϕ_4, the surface potential difference $\Delta\phi$ decreases, leading to a reduction in the gain factor $g(\Delta\phi)$. If sufficient charge enters ϕ_4, making $\Delta\phi$ less than $\Delta\phi_c$, no further avalanche multiplication will take place. This indicates that the avalanche multiplication is a highly nonlinear process.

If the amount of charge entering ϕ_4 is such that at the end of the transfer process, $\Delta\phi$ becomes less than $\Delta\phi_c$, then a constant amount of charge generation per transfer will take place for any given input charge. From eq. (46) we have

$$dq_{n+1} = (1 + g(\Delta\phi)\ dq_n \tag{49}$$

So that q_{n+1}

$$\int_0 \frac{dq'_{n+1}}{(1 + g(\Delta\phi)} = \int_0^{q_n} dq'_n \tag{50}$$

Let q^c_{n+1} be the critical charge in the well (Fig. 10) beyond which no avalanche multiplication takes place and q^c_n be the corresponding input charge which enters the well.

From eq. (45)

$$\Delta\phi = \Delta\phi_0 - q_{n+1/C_e} \tag{51}$$

So that

$$q^c_{n+1} = (\Delta\phi_0 - \Delta\phi_c)C_e \tag{52}$$

From eqs. (50–52)

$$\int_0^{q_{n+1}} \frac{dq_{n+1}}{1 + g(\phi)} = q^c_n \tag{53}$$

$$\int_{\phi_c}^{q_0} \frac{C_e d(\phi)}{1 + g(\phi)} = q^c_n \tag{54}$$

The net maximum gain incharge at each transfer ΔQ_{n+1} for sufficiently large input $q_n \gg q^c_n$ is given by

$$\Delta q_m = q^c_{n+1} - q^c_n \tag{55}$$

from eqs. (52), (54), and (55)

$$\Delta q_m = C_e \int_{\phi_c}^{\phi_0} \frac{g(\phi)}{1 + g(\phi)} d(\Delta\phi) \tag{56}$$

Under the condition $q_n \gg q^c_n$ the maximum excess charge q_{N_m} at the CCD output after N transfer will be

$$Q_{N_m} = q_m N \tag{57}$$

EFFECTS OF AVALANCHE MULTIPLICATION

The effects of avalanche multiplication will vary according to the clock waveform used and the structure of the device.

Since maximum clock voltage is expected to be determined by the avalanche multiplication, it would limit the minimum obtainable value of CTI due to interface

states, because the CTI decreases with increasing clock amplitude [16]. In p-channel devices, since the hole ionization rates are much smaller, higher clock voltage amplitudes should be possible and it should be possible to achieve lower values of CTI (at least at low frequencies) for equal values of all other device and interface state parameters, compared to the case. In the CCD structures with wider gaps, the avalanche multiplication is expected to occur at higher clock voltages [12], because peak value of electric field present in the inter-electrode gap region is lower than in an overlapping gae structure. This implies that much lower values of CTI due to edge effect may be possible.

The other important consequences are:

1) Maximum signal handling capacity for the strucutres with wider gaps will be more than that of overlapping gate structures because of higher possible clock amplitudes. Similarly, for a p-channel device it will be higher than that of an n-channel device.
2) Maximum charge handling capacity of the devices would decrease at lower temperatures, since the ionization rate increases at lower temperatures [17].
3) Since avalanche multiplication is a highly non-linear mechanism (in CCDs), devices operated even under weak avalanche conditions can result in a significant amount of harmonic distortion.
4) The phenomenon of avalanche multiplication could be ultilized when small signal charges are to be estimated. The charge can be multiplied by pasing it through the CCD driven by clocks.

COMPUTER ANALYSIS

A detailed analysis of the effect of the interface states, edge effect, the barrier modulation, and the variable transfer time of electrons on the CTI has been done through the computer program in Appendix A. The results show that the effect of interface states creates the highest amount of CTI, followed by the edge effect, then the CTI caused by the barrier modulation. The least amount of CTI among the four is caused by the variable transfer time effect.

The losses created by these have also been calculated and can be seen in Appendix B. The low frequency limit imposed by the dark current has also been calculated for different fractions of 'alpha' and the ratio of Q_{dark} and Q_{sat}.

CONCLUSIONS

A detailed study of the performance-affecting factors have been made and an analysis of these factors and their effect on CTI have been calculated. It shows that the losses due to interface states have the most considerable effect on the functioning of the CCD. The effect of barrier modulation and the feed-forward has also been shown.

REFERENCES

1. Q.W. Broderson, D.D. Buss and A.F. Tasch, Jr. "Experimental Characterization of Transfer Inefficiency in CCD's," IEEE Trans Electron Devices, ED-22, pp 40–46, Feb. 1975.
2. R.H. Krambeck, T.F. Ratajczyk, Jr. and L.D. Yau, "Low Frequency Transfer Efficiency of E-Beam Faricated Conductively Connected Charge Coupled Device," IEEE J. Solid-State Circuits, SC-11, pp 171–179, Feb. 1976.
3. S.K. Madan, B. Mathur and J. Vasi, "Feed Forward due to Barrier Modulation in Charge Coupled Devices," IEEE Trans. Electron Devices, Vol. ED-29, pp 1269–1276, Aug. 1982.
4. C.H. Sequin and M.F. Tompsett, Charge Transfer Devices, Academic Press, Inc. New York, London, 1975.
5. E.H. Nicollian and A. Goetzberger, "The Si-SiO_2 Interface Electrical, Properties as Determined by MIS Conductance Technique," Bell Syst. Tech. J., Vol. 46, pp 1055–1133, July 1967.
6. J.R. Brews, "Surface Potential Fluctuations Generated by Interface Charge Inhomogenities in MOS Devices," J. Appl. Phys., Vol. 43, pp 2306–2313, May 1972.
7. G. Declerck, R. Van Overstraeten and G. Proux, "Discussion of the Surface Potential Fluctuations Caused by Oxide-Charge Fluctuations," J. Appl. Phys., Vol. 45, pp 2593–2595, June 1974.
8. G.W. Taylor and P.K. Chaterjee, "An Evaluation of Submicrometer Potential Barriers Using Charge Transfer Devices," IEEE Trans. Electron Devices, Vol. ED-27, pp 1579–1598, Aug. 1980.
9. P.K. Chaterjee, G.E. Taylor, A.F. Tasch Jr., "Charge Couple Device Structures for VLSI Memories," IEEE Trans. Electron Devices, Vol. ED-26, pp 871–881, 1979.
10. S.M. Sze, Physics of Semiconductor Devices, 2nd Ed., Wiley.
11. K. Hess and C.T. Sah, "Hot Electrons in Short-Gate CCDs," IEEE Trans. Electron Devices, Vol. ED-25, pp 1399–1405, Dec. 1978.
12. K. Hess and C.T. Sah, "The Ultimate Limits of CCD Performance Imposed by Hot Electron Effects," Solid State Electronics, Vol. 22, pp 1025–1033, Dec. 1979.
13. M.H. Elsaid, S.G. Chamberlain and L.A.K. Watt, "Computer Model and Charge Coupled Devices, Solid State Electronics, Vol. 22, pp 61–69, Jan. 1977.
14. K. Hess and H. Shichijo, "The Charge Handling Capacity of Buried Channel Structure Under Hot Electron Conditions," IEEE Trans Electron Devices, Vol. ED-27, pp 503–504, Feb. 1980.
15. J. McKenna and N.L. Schryer, "The Potential in a Charge Coupled Devices With No Mobile Minority Carriers and Zero Plate Separation," Bell Syst. Tech. J., Vol. 52, pp 669–696, May–June 1973.
16. W.J. Bertram, A.M. Mohsen, F.J. Morris et al., "A Three Level Metallization Three Phase CCD," IEEE Trans. Electron Devices, Vol. ED-21, pp 70–72, Jan. 1974.
17. CCD and Their Applications: J.D.E. Beynon and D.R. Lamb, McGraw Hill Publication.

APPENDIX–A

```
 1  C       PROG PERFORMANCE ANALYSIS SCCD
 2          DIMENSION X(10),Y(10),Z(10),V(10),W1(10),Z1(10),Y1(10)
 3          REAL NI,NA,NZ
 4          DATA AS/2.CE-6/,TK/.026/,RHO/1.0E-11/,NZ/1/,SK/.005/,
 5        1 DV/5/,DVS/5/,DN/35/,NI/1.4E10/,NA/1.0E15/,DLN/6.0E-2/,
 6        2 TT/3.33E-7/TOFF/3.0E-8/,TOU0/1.0E-6/,S/1.0/,XD/1.CE-3/,
 7        3 T/1.0E-04/,N/1OCO/,COX/3.5E-8/,
 8        4 AE/2.CE-4/,Q/1.6E-19/,EK/.003/,W/25.0E-5/
 9          READ(5,*)SIGMA1,SIGMA2,T2,T3,TO,AD,XS,NIN
10          DO10I=1,NIN
11          READ(5,5C)SSN,ALPHA
12  50      FORMAT(F15.0,F15.12)
13          A=AS*SN*TK
```

```
14            B=Q*TK*SSN
15   C        ELECTRONS  EMITTED
16            TN2=A*ALOG(T2*RHO)
17            TOT=A*ALOG((T2+T3+NZ+T()*RHO)
18   C        TOTAL  LOSS
19            CLOSS=TOT—TN2
20            EFF=CLOSS*G/(AS*COX*DV)
21   C        FOR 3 PHASE  CCD
22            EFF3=B*ALOG(2+3*NZ)/(CCX*DV)
23            EFFED=EFF3*AD
24            EFFT=E*(SK—BK)/(COX*DV)
25            DFJ=(Q*DN*NI*NI)/(NA*DLN)
26            GJ=(Q*XD*NI)/(2*TOU0)
27            GSJ=(Q*S*NI)/2
28            DARKJ=DFJ+GJ+GSJ
29            PDARK=AE*GSJ*N*T
30            CCAP=CCX*DVS
31            FMIN=DARKJ*N/(CCAP*ALPHA)
32   C        FEED FORWARD
33            BLOSS=XS*SSN*Q*W*TK*ALCG(TT/TOFF)
34            EFFB=BLOSS/(AS*COX*DV)
35            DD=—2/TK
36            DEF1=2*DN*EXP(DD*SIGMA1)
37            DEF2=2*DN*EXP(DD*SIGMA2)
38            X(I)=SSN
39            W1(I)=EFF3
40            Z(I)=EFFED
41            V(I)=EFFT
42            Z1(I)=ALPHA
43            Y1(I)=FMIN
44            Y(I)=EFFB
45       1C   CONTINUE
46            WRITE(6,21)((X(I),W1(I)),I=1,NIN)
47     21      FORMAT(1X,'NSS='E13.3,2X,'EFF3=',E13.3)
48             WRITE(6,22)((X(I),Z(I)),I=1,NIN)
49     22      FORMAT(1X,'NSS=',E13.3,2X,'EFFED=',E13.3)
50             WRITE(6,23)((X(I),V(I)),I=1,NIN)
51     23      FORMAT(1X,'NSS=',E13.3,2X,'EFFT=',E13.3)
52             WRITE(6,24)((Z1(I),Y1(I)),I=1,NIN)
53      24     FORMAT(1X,'ALPHA=',E13.3,2X,'FREQ0=',E13.3)
54             WRITE(6,25)((X(I),Y(I)),I=1,NIN)
55      25     FORMAT(1X,'NSS=',E13.3,2X,'EFFB=',E13.3)
56             WRITE(6,26)BLOSS,DARKJ,PDARK,CLOSS
57     26      FORMAT(1X,'BLOS=',E13.3,1X,'DAKJ=',E13.3,1X,
              'PDAK=,E13.3,
58       1     1X,'CLOS=',E13.3)
59             WRITE(6,27)SIGMA1,SIGMA2,DEF1,DEF2
```

```
60    27     FORMAT(1X,'SIGMA1=',E13.3,'DEF1='E9.3,'SIGMA2='E13.3,
61        1  4X,'DEF2='E9.3)
62
63
64
65
66
67
68
69
70
71
72           STOP
73           END
```

APPENDIX–B

```
 1  NSS=   0.100E+12  EFF3=    0.383E-02
 2  NSS=   0.200E+12  EFF3=    0.765E-02
 3  NSS=   0.300E+12  EFF3=    0.115E-01
 4  NSS=   0.400E+12  EFF3=    0.153E-01
 5  NSS=   0.500E+12  EFF3=    0.191E-01
 6  NSS=   0.600E+12  EFF3=    0.230E-01
 7  NSS=   0.700E+12  EFF3=    0.268E-01
 8  NSS=   0.100E+13  EFF3=    0.383E-01
 9  NSS=   0.200E+13  EFF3=    0.765E-01
10  NSS=   0.300E+14  EFF3=    0.115E+01
11  NSS=   0.100E+12  EFFED=     0.803E-03
12  NSS=   0.200E+12  EFFED=     0.161E-02
13  NSS=   0.300E+12  EFFED=     0.241E-02
14  NSS=   0.400E+12  EFFED=     0.321E-02
15  NSS=   0.500E+12  EFFED=     0.402E-02
16  NSS=   0.600E+12  EFFED=     0.482E-02
17  NSS=   0.700E+12  EFFED=     0.562E-02
18  NSS=   0.100E+13  EFFED=     0.803E-02
19  NSS=   0.200E+13  EFFED=     0.161E-01
20  NSS=   0.300E+14  EFFED=     0.241E+00
21  NSS=   0.100E+12  EFFT=    0.475E-05
22  NSS=   0.200E+12  EFFT=    0.951E-05
23  NSS=   0.300E+12  EFFT=    0.143E-04
24  NSS=   0.400E+12  EFFT=    0.190E-04
```

```
25  NSS=    0.500E+12  EFFT=    0.238E-04
26  NSS=    0.600E+12  EFFT=    0.285E-04
27  NSS=    0.700E+12  EFFT=    0.333E-04
28  NSS=    0.100E+13  EFFT=    0.4753-04
29  NSS=    0.200E+13  EFFT=    0.951E-04
30  NSS=    0.300E+14  EFFT=    0.143E-02
31  ALPHA=    0.100E-02  FREQ0=    0.641E+07
32  ALPHA=    0.200E-03  FREQ0=    0.320E+08
33  ALPHA=    0.300E-04  FREQ0=    0.214E+09
34  ALPHA=    0.400E-05  FREQ0=    0.160E+10
35  ALPHA=    0.500E-06  FREQ0=    0.128E+11
36  ALPHA=    0.600E-07  FREQ0=    0.107E+12
37  ALPHA=    0.700E-08  FREQ0=    0.915E+12
38  ALPHA=    0.800E-09  FREQ0=    0.801E+13
39  ALPHA=    0.900E-10  FREQ0=    0.712E+14
40  ALPHA=    0.100E-10  FREQ0=    0.641E+15
41  NSS=    0.100E+12  EFFB=    0.572E-04
42  NSS=    0.200E+12  EFFB=    0.114E-03
43  NSS=    0.300E+12  EFFB=    0.172E-03
44  NSS=    0.400E+12  EFFB=    0.229E-03
45  NSS=    0.500E+12  EFFB=    0.286E-03
46  NSS=    0.600E+12  EFFB=    0.343E-03
47  NSS=    0.700E+12  EFFB=    0.401E-03
48  NSS=    0.100E+13  EFFB=    0.572E-03
49  NSS=    0.200E+13  EFFB=    0.114E-02
50  NSS=    0.300E+14  EFFB=    0.172E-01
51  BLOS=   0.601E-14  DAKJ=    0.112E-05 PDAK=    0.224E-13
CLOS=  0.000E+00
52  SIGMA1= 0.400E-01DEF1=0.670E-01SIGMA2=    0.323E+01
DEF2=0.404E+00
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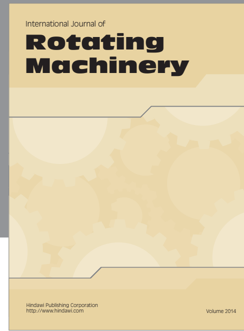
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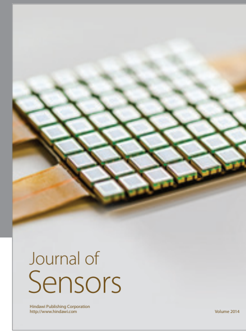
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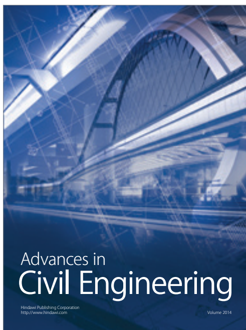
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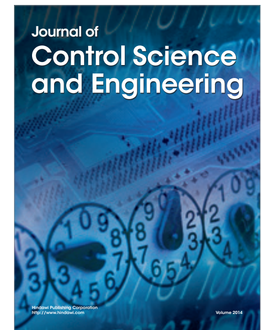
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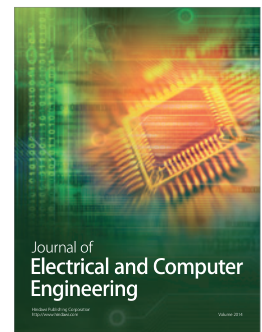
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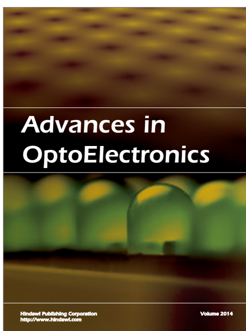
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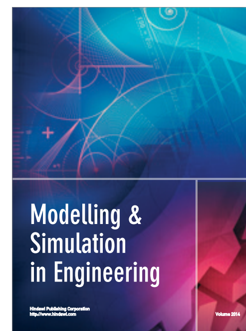
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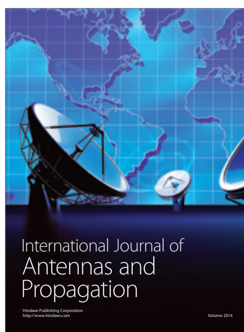
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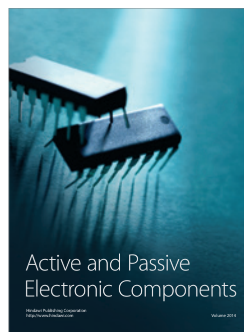
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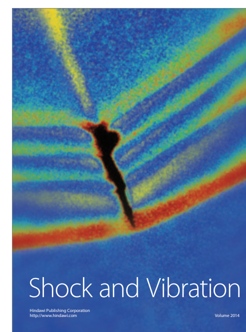
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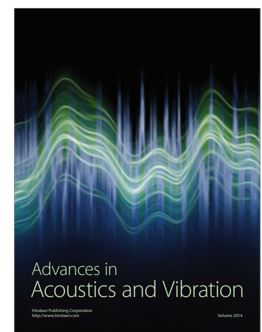
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