A New Universal Second-Order Filter using Configurable Analog Building Blocks (CABs) for Filed-Programmable Analogue Arrays

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تصميم جديد لمرشح شامل ثنائي الدرجة باستخدام تشكيلات المنظومات التماثلية القابلة للبرمجة

محمد طاهر عبدالمعطي *أ و أسامة أوغلا فارس ب

الخلاصة: تقدم هذه الورقة تصميما لمرشح شامل ثنائي الدرجة باستخدام تشكيلات المنظومات التماثلية القابلة للبرمجة. هذه التشكيلات يمكنها اجراء عمليات التكامل والتفاضل والتكبير واللوغاريتم والاس والجمع وكذلك قلب الاشارة. ومن اجل تمكين المرشح من معالجة الذبذبات عالية التردد فان برمجة وتشكيل مكوناته تتم عن طريق التحكم في تيارات التهيئة(الانحياز) بالطرق الرقمية. وتوضح هذه الورقة انه يمكن باستخدام اربعة فقط من التشكيلات التماثلية بناء مرشح يحقق العمليات الخمسة القياسية وهي: مرشح تمرير الذبذات المنخفضة ومرشح تمرير الذبذبات العالية ومرشح تمرير حزمة من الذبذبات ومرشح منع حزمة من الذبذبات ومرشح تمرير جميع الذبذات. وقد استخدم برنامج المحاكاة سبايس من اجل التحقق من فاعلية المرشح المقترح باستخدام الخصائئ العملية للترانسستورات ثنائية القطبية.

المفاتيح: المرشحات الفعالة– المنظومات التمثالية القابلة للبرمجة

Abstract: In this paper, the design of a universal second-order filter using configurable analog blocks (CABs) for field programmable analog arrays is presented. The configurable blocks are capable of performing integration, differentiation, amplification, log, anti-log, add and negate functions. To maintain high frequency operation, the programmability and configurability of the blocks are achieved by digitally modifying the block's biasing conditions. Using at most four CABs, this article shows that it is possible to design a versatile second-order filter realizing all the standard five filter functions; lowpass, highpass, bandpass, notch and allpass. SPICE simulation results using practical bipolar junction transistor (BJT) parameters confirm the feasibility of using the CABs in designing second-order filters.

Keywords: Active filters, Field programmable analog arrays

1. Introduction

At present, research in Field Programmable Analog Arrays (FPAAs), the analog counterpart of the FPGAs, is attracting the attention of many researchers; see for example references (Znamirowski, *et al*. 2002 and Pankiewicz, *et al*. 2002) and the references cited therein. Over the years various designs for Configurable Analog Blocks (CABs) and FPAAs have been develped and reported using operational ampli-

fiers, operational transconductance amplifiers and current conveyors. In most of these designs, the programmability and tenability were achieved using banks of programmable resistors and capacitors resulting in limited bandwidth and large silicon area.

The ever-presented demand on high frequency operation and lower supply voltages is the main requirement that affect the design of the CABs of any FPAA. The existing FPAAs, except that reported in (Kutuk and Kang, 1998), can not satisfy these require-

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ments. In general, voltage-mode circuits will always suffer from the need of higher power supply voltages to maintain reasonable dynamic ranges. Voltage-mode operational amplifier-based CABs will also suffer from the limited upper frequency range.

In a recent publication (Fares and Abuelma'attiu, 2008), the authors presented a bipolar junction transistor (BJT)-based current-mode configurable analog building blocks (CABs) for field programmable analog arrays. A single CAB comprises three different circuits: a current mode differential integrator circuit, a current-mode differentiator/exponential/pass circuit and a current-mode circuit for realizing a logarithmic operation. In fact this set of functions is the same as the one adopted by the commercially available TRAC FPAA (Buzton 2000). However, unlike the TRAC FPAA which uses operational amplifiers in realizing these functions, the proposed CABs use transistor-based current-mode continuous-time approach utilizing the bipolar-junction-transistor (BJT) translinear-principle (TLP). To maintain high frequency operation, the programmability and configurability of the CABs are achieved by digitally modifying the CABs biasing currents to switch on (or off) specific BJTs to enable the CAB to perform integration, differentiation, exponentiation, logarithmic or pass function. This avoids the use of capacitor- and/or resistor-banks and the relatively large number of switches needed for programming the CABs. Thus, reducing the required silicon area for integration and achieving higher frequencies of operation. Moreover, current-mode transistor-based circuits avoids the limitations of the operational amplifiers; for example the limited gain-bandwidth product and the slew-rate, and does not require large values of DC supply voltages to maintain reasonable dynamic ranges.

This paper presents the application of the CABs presented in (Fares and Abuelma'attiu, 2008) in realizing a second-order universal filter. The realized universal filter is capable of performing lowpass filter (LPF), bandpass filter (BPF), highpass filter (HPF), Notch filter, and allpass filter (APF) transfer functions.

2. Background of Configurable Analog Building Blocks (CABs)

In order to make this paper complete, this section presents a brief background of the CABs presented in (Fares and Abuelma'attiu, 2008). This would give readers not familiar with some clue (Fares and Abuelma'attiu, 2008). The transfer function of the current-mode integrator circuit proposed in the CAB reported in (Fares and Abuelma'attiu, 2008) can be expressed in the s-domain as

$$\frac{I_o}{I_{in}} = \frac{I_A^2 /(I_B C V_T)}{s + I_X /(C V_T)} = \frac{a}{s+b} \tag{1}$$

In Eq. (1), $I_{in} = I_{in1} - I_{in2}$ is the differential input current, $I_o = I_{o1} - I_{o2}$ is the differential output current, I_A, I_B and I_X are constant current sources, C is the capacitance of the two externally connected capacitors and V_T is the thermal voltage. As Eq. (1) suggests, the values of both constants a and b of the proposed integrator can be independently tuned via constant current sources I_A, I_B and I_X.

The transfer function of the current-mode differentiator circuit proposed in the CAB reported in (Fares and Abuelma'attiu, 2008) can be expressed in the s-domain as

$$I_o = I_B \cdot C \cdot V_T \cdot s \cdot I_{in} /(I_A I_C) \tag{2}$$

In Eq. (2) I_{in} is the differential input current defined as the difference between the two input currents I_{in1} and I_{in2}, and the differential output current I_o is the difference between the two output currents I_{o1} and I_{o2}. Equation (2) suggests that the gain can be controlled by the constant current sources I_A, I_B, and I_C.

The transfer function of the current-mode exponential circuit proposed in the CAB reported in (Fares and Abuelma'attiu, 2008) can be expressed as

$$I_o = I_{o1} - I_{o2} = I_{A1} I_k x \, exp(R I_{in} / V_T)/ I_A \tag{3}$$

In Eq. (3), $I_o = I_{o1} - I_{o2}$ is the differential output current, is the input current, is the resistance of an the externally connected resistor, I_{a1}, I_k and I_A are constant current sources, and x is a scaling factor.

The transfer function of the current-mode pass circuit proposed in the CAB reported in (Fares and Abuelma'attiu, 2008) can be expressed as

$$I_o = I_{o1} - I_{o2} = I_B \left(I_{in1} - I_{in2} \right)/ I_A = I_B I_{in} / I_A \tag{4}$$

In Eq. (4), $I_{in} = I_{in1} - I_{in2}$ is the differential input current, $I_o = I_{o1} - I_{o2}$ is the differential output current, I_A and I_B are constant current sources. Equation (4) indicates that this cell can not only operate as a Pass cell, but also as a linear current amplifier with an amplification factor dependant on the ratio of I_B to I_A.

3. Realization of Second-Order Universal Filter Using CABs

Basically there are two possible topologies in which the CABs can be connected to each other to form a universal filter; the string-like topology and the matrix-like topology. In this paper CABs will be used to design a universal filter using the string-like topology.

Figure 1 shows the block diagram of four CABs connected in a two string-like topology. Depending on the values of the biasing currents of each CAB, the overall circuit can be programmed to work as a second-order lowpass filter (LPF), highpass filter (HPF), bandpass filter (BPF), Notch and allpass filter (APF). The standard transfer functions of these filters can be lumped together in one biquadratic form written as
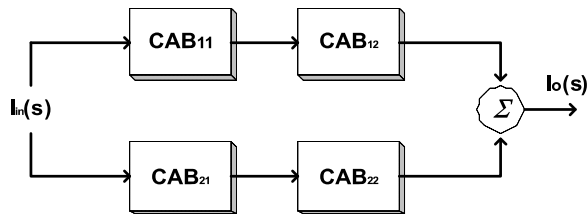

Figure 1. Block diagram of the string-like universal filter

$$\frac{I_o(s)}{I_{in}(s)} = \frac{\alpha_1 s^2 + \beta_1 s + \gamma_1}{s^2 + \beta_2 s + \gamma_2} \tag{5}$$

where α_1, β_1, β_2, γ_1, and γ_2 are all programmable constants depending on the biasing currents of the CABs and $I_o(s)$ and $I_{in}(s)$ are the output and input currents of the circuit respectively.

To implement the transfer function of Eq. (5) using string like CABs, connected as shown in Fig. 1, this transfer function must be factorized into two terms. Each of these terms can then be implemented using one of the strings and the results added to give the required operation. However, factorizing this transfer function imposes a very strict limit on the values of β_2 and γ_2 and thus on the possible values of the Q-factor of the implemented filters. This limitation comes from the fact that all currents are of real values and thus the following inequality must be satisfied

$$\sqrt{\beta_2^2 - 4\gamma_2} > 0 \tag{6}$$

The center frequency and the Q-factor are related to β_2 and γ_2 as follows

$$w_o = \sqrt{\gamma_2} \tag{7}$$

and

$$Q = \frac{\sqrt{\gamma_2}}{\beta_2} \tag{8}$$

Substituting Eqs. (7) and (8) in Eq. (6), it can be seen that the Q-factor must be less than 0.5.

3.1. Highpass Filter (HPF)

The transfer function of a HPF is given as

$$\frac{i_o}{i_{in}} = \frac{\alpha_1 s^2}{s^2 + \beta_2 s + \gamma_2} \tag{9}$$

where both β_1, and γ_1 of Eq. (5) are set to zero. This transfer function can be factorized as follows

$$\frac{i_o}{i_{in}} = \frac{a_1 s}{s + b_1} - \frac{a_2 s}{s + b_2} \tag{10}$$

where

$$a_1 = 2a_2 = 2\alpha_1 \tag{11}$$

$$b_2 = \frac{1}{3}\beta_2 \tag{12}$$

$$b_2 = \frac{1}{2}b_1 = \sqrt{\frac{\gamma_2}{2}} \tag{13}$$

In realizing the transfer function of Eq. (10) using the block diagram of Fig. 1, CAB11 will be configured as an integrator and CAB12 will be configured as a differentiator. Similarly, CAB21 and AB22 will be configured as integrator and differentiator respectively. The parameters a_1, a_2, b_1 and b_2 will be given by

$$a_{1,2} = \frac{I_{A1,2}^2 I_{BD1,2}}{I_{B1,2} I_{AD1,2} I_{CD1,2}} \tag{14}$$

and

$$b_{1,2} = \frac{I_{X1,2}}{CV_T} \tag{15}$$

In Eqs. (14) and (15), the subscripts D indicate a biasing currents related to a differentiator block. Figure 2 shows a possible realization for the HPF transfer function of equation (9) using the string-like structure of Fig. 1. Figure 2 comprises two CABs configured as integrators and two CABs configured as differentiators. Each CAB is biased by currents I_A, I_B, I_C, I_x and I_{Ei}, $i = 0,1,2,....,6$. The current sources I_{Ei}, $i = 0,1,2,....,6$ are switched on or off depending on the required CAB configuration. This switching process is controlled by the output of the decoders with a 3-bit digital input $b_2 b_1 b_o$.

As an example, the circuit was simulated for a centre frequency $f_o = 50$MHz with $Q = 0.47$ and a gain = 0dB. Figure 3 shows the gain-frequency characteristic of the realized HPF. To examine the effect of transistor parameters on the performance of the HPF, the simulations were performed for three cases; two of them assuming default parameters for the transistors with $\beta = 100$ and 1000 and the third one using the parameters of the BFP640 Infineon transistors shown in Appendix A where $\beta = 450$. Due to the fact that the gain of the HPF, and all other filters, can be easily adjusted to the required value via the biasing currents and by using other gain-stages, it is the simulated centre frequency that is important to be compared with the expected theoretical values. Inspection of Fig. 3 shows that for
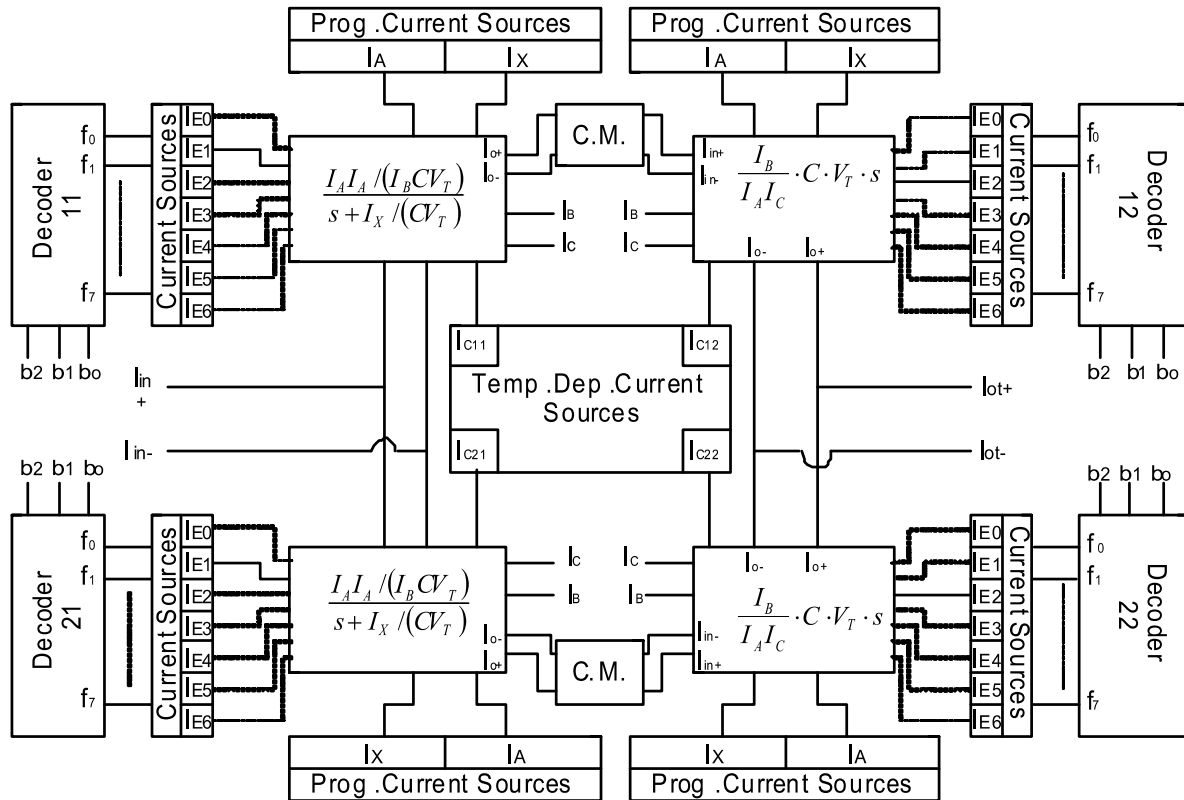
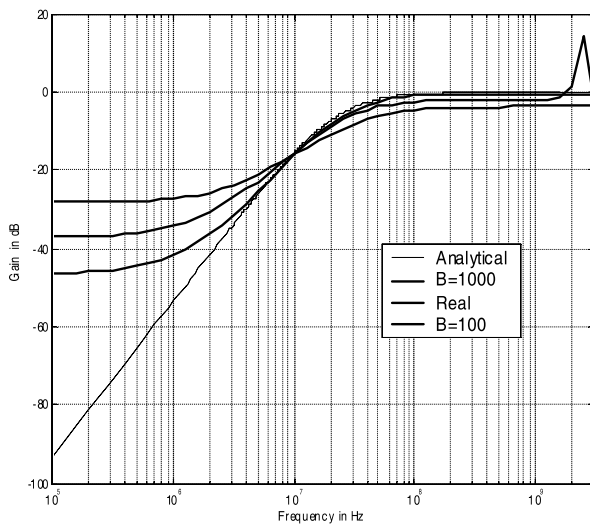**Figure 2. Detailed blocks of the CABs of Figure 1 when configured as a HPF**

Figure 3. Gain-frequency characteristic of the simulated HPF obtained from Fig. 2 with $I_{AI} = I^{BI} = ImA$, $I_{XI} = 100uA$, $I_{ADI} = ImA$, $I_{BDI} = 2mA$, $I_{CDI} = I_{A2} = I_{B2} = ImA$, $I_{X2} = 50\ \mu A$, $I_{AD2} = ImA$, $I_{BD2} = ImA$ and $I_{CD2} = ImA$

real transistor parameters or default parameters with β = 1000, the simulated and analytical gain-frequency characteristics are almost identical with a percentage error of less than 2% in the pass band.

.2. *Lowpass filter (LPF)*

The transfer function of a LPF is given as

$$\frac{i_o}{i_{in}} = \frac{\gamma 1}{s^2 + \beta_2 s + \gamma_2} \tag{16}$$

here both α_1 and β_1 of Eq. (5) are set to zero. This ansfer function can be factorized as follows

$$\frac{i_o}{i_{in}} = \frac{a_1}{s + b_1} \frac{a_2}{s + b_2} \tag{17}$$

here

$$\gamma 1 = a_1 a_2 \tag{18}$$

$$\gamma_2 = b_1 b_2 \tag{19}$$

and

$$\beta_2 = b_1 + b_2 \tag{20}$$

In realizing the transfer function of Eq. (17) using the block diagram of Fig.3, CAB11 and CAB12 will be configured as integrators and CAB21 and CAB22 will be in their OFF mode. After some mathematical manipulations, the parameters a_1, a_2, b_1 and b_2 can be mapped into the biasing currents and will be given by

$$a = a_1 = a_2 = \frac{I_{A1,2}^2}{CV_T I_{B1,2}} \qquad (21)$$

and

$$b_{1,2} = \frac{I_{X1,2}}{CV_T} \qquad (22)$$

In Eqs. (21) and (22), the subscripts 1 and 2 refer to the integrator blocks CAB11 and CAB12 respectively. The circuit was simulated for a centre frequency $f_o = 3$ MHz with $Q = 0.47$ and a DC gain of 33 dB. Figure 4 shows the gain-frequency characteristics of the realized LPF. Inspection of Fig. 4 shows that for real transistor parameters or default parameters with β = 1000, the simulated and analytical gain-frequency characteristics are almost identical with a percentage error in the pass band of less than 3% for the default parameters and 6% for the real parameters.
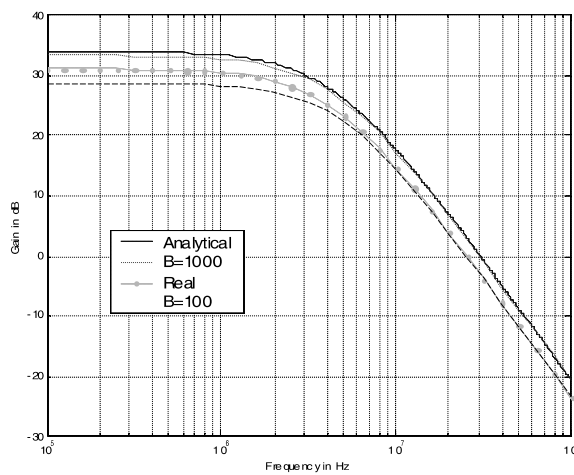

Figure 4. Gain-frequency characteristics of the simulated LPF. The following values of the biasing currents are used; $I_{A1,2}$ = 0.1mA, $I_{B1,2} = I_{XI}$ = 10μA and I_{X2} = 20uA

3.3. Bandpass Filter

The transfer function of a BPF can be represented as

$$\frac{i_o}{i_{in}} = \frac{\beta_1 s}{s^2 + \beta_2 s + \gamma_2} \qquad (23)$$

where both α_1 and γ_1 of Eq. (5) are set to zero. This transfer function can be factorized as follows

$$\frac{i_o}{i_{in}} = \frac{a_1}{s + b_1} - \frac{a_2}{s + b_2} \qquad (24)$$

where

$$\beta_1 = a_1 - a_2 \qquad (25)$$

$$\beta_2 = b_1 + b_2 \qquad (26)$$

$$\gamma_2 = b_1 \cdot b_2 \qquad (27)$$

and

$$b_1 = \frac{a_1}{a_2} b_2 \qquad (28)$$

In realizing the transfer function of Eq. (24) using the block diagram of Fig. 1, CAB11 and CAB21 will be configured as integrators and CAB12 and CAB22 will be configured either as amplifiers or pass cells. The parameters a_i and b_i are directly mapped into currents as shown in Eqs. (29) and (30).

$$a_{1,2} = \frac{I_{A1,2}^2}{CV_T I_{B1,2}} \qquad (29)$$

and

$$b_{1,2} = \frac{I_{X1,2}}{CV_T} \qquad (30)$$

The circuit was simulated for a centre frequency $f_o = 8.7$MHz with $Q = 0.47$ and a gain = 19dB. Figure 5 shows the gain-frequency characteristic of the simulated BPF. Inspection of Fig. 5 shows that the centre
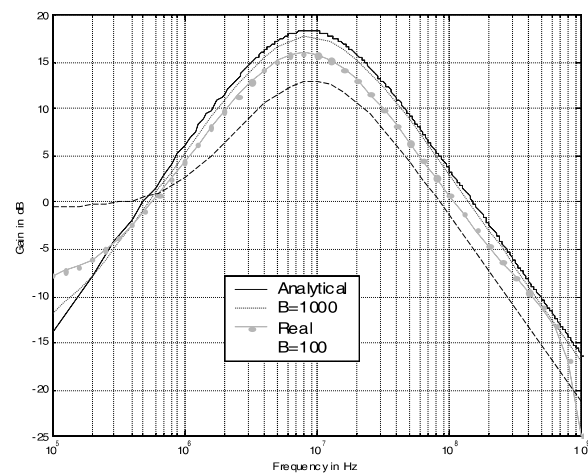

Figure 5. Gain-frequency characteristics of the simulated BPF. The following values of the biasing currents were used; I_{AI} = 0.1mA, I_{BI} = 0.1mA, I_{XI} = 40μA, I_{A2} = 0, ImA, I_{B2} = 0.2mA and I_{X2} = 20μA

frequency is almost independent of the transistor parameters whereas the gain of the BPF does depend on it. The centre frequency of the simulated BPF shows a very good matching with the expected value

with a percentage error of about 2% when using real transistor parameters.

3.4. Notch Filter

The transfer function of a notch filter can be represented as

$$\frac{i_o}{i_{in}} = \frac{s^2 + \gamma_1}{s^2 + \beta_2 s + \gamma_2} \tag{31}$$

where α_1 and β_1 and of Eq. (5) are set to one and zero respectively. Utilizing the long division, the transfer function of Eq. (31) can be rewritten as

$$\frac{i_o}{i_{in}} = 1 - \frac{\beta_2 s + (\gamma_2 - \gamma_1)}{s^2 + \beta_2 s + \gamma_2} \tag{32}$$

Equation (32) can be factorized as in Eq. (24) and thus can be implemented using the block diagram of Fig. 1 with CAB11 and CAB21 configured as integrators and CAB21 and CAB22 configured as amplifier or pass cells. Obviously a DC current component with appropriate value must be added (or subtracted) to obtain the desired transfer function. Factorizing Eq. (32) as in Eq. (24) yields

$$\beta_2 = b_1 + b_2 = a_1 - a_2 \tag{33}$$

$$\gamma_2 = b_1 \cdot b_2 \tag{34}$$

and

$$\gamma_2 - \gamma_1 = a_1 b_2 - a_2 b_1 \tag{35}$$

where a_1, a_2, b_1 and b_2 are as defined in Eqs. (29) and (30).

The circuit was simulated for a centre frequency f_o = 1.27MHz with Q = 0.3 and a gain = 0dB. Figure 6 shows the gain-frequency characteristic of the realized notch filter. Inspection of Fig. 6 shows that the simulation results depend heavily on the transistor parameters with the best results obtained using transistors with default parameters and β = 1000.

3.5. Allpass filter

The transfer function of an APF can be represented as

$$\frac{i_o}{i_{in}} = \frac{s^2 - \beta s + \gamma}{s^2 + \beta s + \gamma} \tag{36}$$

This transfer function can be simplified utilizing the long division yielding,

$$\frac{i_o}{i_{in}} = 1 - \frac{2\beta s}{s^2 + \beta s + \gamma} \tag{37}$$
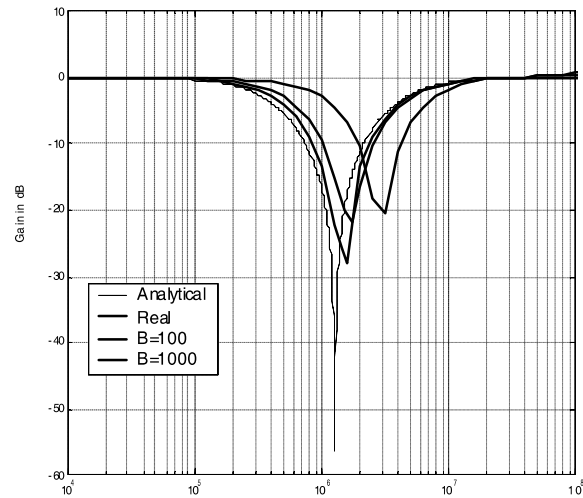
Figure 6. **Gain-frequency characterstic curves of the simulated notch filer. The following values of the biasing currents are used; I_{A1} = 39.5μA, I_{B1} = 39.5 A, I_{B1} = .1mA, I_{X1} = 124.8 20uA, I_{A2} = 13.2μ A, I_{B2} = .1mA and I_{X2} = 1.36μA**

Equation (37) can be factorized as in equation (24) and thus can be implemented using the block diagram of Fig. 1 with CAB11 and CAB21 configured as integrators and CAB21 and CAB22 configured as amplifiers or pass cells. Obviously a DC current component with appropriate value must be added (or subtracted) to obtain the desired transfer function. Factorizing Eq. (37) as in Eq. (24) yields

$$\beta = (b_1 + b_2) = \frac{1}{2}(a_1 - a_2) \tag{38}$$
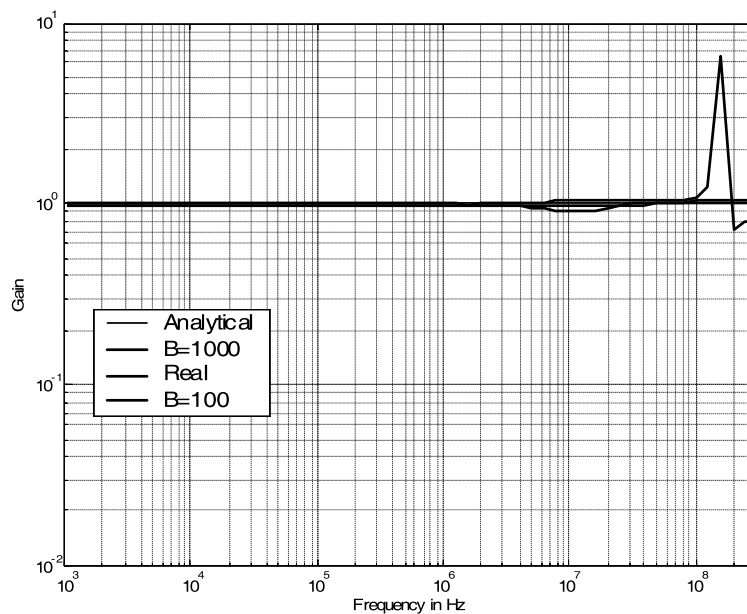
$$b_2 = a_2 b_1 / a_1 \tag{39}$$

and

$$\gamma = b_1 \cdot b_2 \tag{40}$$

where the parameters and are as defined in Eq. (29) and (30).

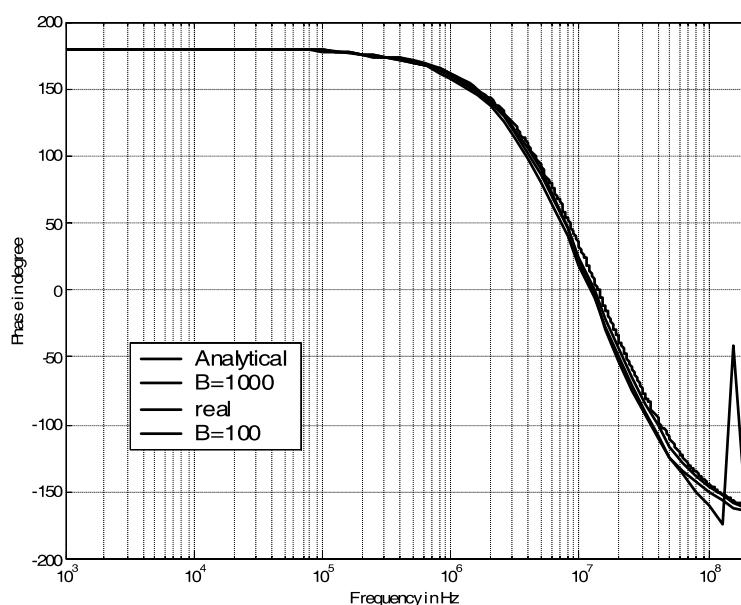The circuit was simulated for a centre frequency f_o = 13.0MHz with Q = 0.43 and a gain = 0dB. Figure 7 shows the gain- and phase-frequency characteristics of the realized APF. The gain response of the filter shows expected characteristics up to nearly 50 MHz with maximum phase error less than 5o and up to 100 MHz for a maximum phase error of about 20o.

3.6. Filter Programmability

Configuration of the proposed universal filter is car-

(a)

(b)

Figure 7. (a) Gain-frequency and (b) Phase-frequency characteristics of the simulated APF. The following values of the biasing currents are   used; I_{A1} = 0.1766mA, I_{B1} = 0.1mA, I_{X1} = 73μA, I_{A2} = 0.096mA, I_{B2} = 0.1mA, and I_{X2} = 24μA

ried out by programmable current sources. Assuming that the CABs are going to be built as a part of a mixed-mode system, the programmable current sources are realized using MOSFETs (Fares and Abuelma'attiu, 2008). Each current source is assumed to consist of two programmable cells, one for coarse tuning and the other for fine tuning.   The value of the

output current depends on a controlling binary code word that is generated by a user interface program, designed using Visual Basic. Depending on the filtering function and the specifications of the required filter, *ie*. the *Q*-factor, gain, and the centre frequency, the user interface program generates the required controlling word. This controlling word is stored in latches

that control the gate voltages of the MOSFETs of the programmable current sources and thus giving the required values of the biasing currents needed. The programmable current sources used in this application use 7-bits for each tuning part, fine and coarse. Of course, increasing the number of bits used will increase the accuracy and the tuning range of these current sources. This has direct influence on the resulting accuracy and tuning range of the overall system.

Conclusions

In this paper, the use of CABs for FPAA reported in (Fares and Abuelma'attiu, 2008) in designing universal second-order filters has been presented. These CABs are capable of performing Integration, Differentiation, Pass with gain and exponential functions, in addition to summing and subtraction, which can be easily implemented in current-mode operation.

As the proposed circuits are based on the TLP with BJTs in the active mode, one main factor affecting the accuracy and bandwidth of these circuits is the base currents. In order to partially solve this problem, BJTs with larger dc current gain can be used. However this may not be possible when using transistors with higher cutoff frequency. Alternatively, compensation current sources can be used to reduce the effect of these base currents.

The main enhancement achieved in this paper over the CABs of the TRAC FPAA and the other CABs found either in the literature or in the market is in terms of both the frequency ranges and the power supply voltages. The maximum upper frequency achieved here was in the case of the LPF realization and it was around 100 MHz and the minimum was around 10 MHz in the case of the APF. However, these circuits face problems when used for low frequency applications, the minimum possible frequency is 50 KHz for the BPF. One reason for this problem is the need for all capacitors to be on-chip. This implies serious limitations on the maximum possible value of these capacitors. It is assumed in all circuits that the capacitor value is 20 pF. Because the current-mode technique is used in all the designs, no high gain nodes exist in the circuits and thus Miller theorem cannot be applied to enhance the effective value of the used capacitors. One possible solution to this problem is to use biasing currents with smaller ranges. Although this will impose a reduction in the transistors cutoff frequency, this will not affect the results since we are assuming low frequency signals.

All proposed analog CABs used in this paper are assumed to operate using ±1.5 V power supply. Depending on the set of functions the CABs can perform, it is believed that having sufficient number of these blocks integrated on one chip allows the designer to carry out almost any analog task. For example, extending the proposed second-order universal filter into orders above two can be easily done by cascading several stages to it.

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Appendix A

A-1 Default Transistor Parameters
IS=100.0E-18 BF=100 NF=1 BR=1 NR=1 CN=2.42 D=.87

A-2 Practical (Real) Transistor Parameters (BFP640 Infineon)
IS=.22F VAF=1000 NE=2 VAR=2 NC=1.8 RBM=2.707 CJE=227.6F TF=1.8P ITF=0.4 VJC=0.6 TR=.2N
MJS=.27 XTI=3 AF=2 BF=450 IKF=.15 BR=55 IKR=3.8M RB=3.129 RE=.6 VJE=.8 XTF=10 MJC=.5
CJS=93.4F NK=-1.42 FC=.8 KF=72.91P NF=1.025 ISE=21F NR=1 ISC=400F IRB=1.522M RC=3.061
MJE=0.3 VTF=1.5 CJC=67.43F XCJC=1 VJS=.6 EG=1.078