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SHORT PAPER

A Method for Finding Multiple DC Operating Points of Short Channel CMOS Circuits

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Abstract This paper is devoted to the analysis of CMOS transistor circuits, fabricated in nanometer technology, having multiple DC operating points. The MOS transistors are characterised by the intricate PSP 103.1.1 model elected by the CMC as a standard. To find the operating points an approach is proposed based on a mathematical concept called a deflation. According to this concept the equations describing the circuit are deformed to avoid the solutions earlier determined and retain the remaining solutions. A new efficient deflation technique is developed and combined with the homotopy method and the discrete circuit equivalent of the Newton–Raphson nodal analysis. An algorithm has been worked out for finding multiple DC operating points of CMOS circuits encountered in practical applications. To illustrate the proposed approach three numerical examples are given.

Keywords CMOS circuits · DC analysis · Deflation technique · Multiple operating points

1 Introduction

Finding multiple DC operating points of nonlinear circuits is a basic question of the analysis and design and a difficult task in circuit simulation. The methods which guarantee finding all the DC operating points are very time consuming, capable of analysing only small size circuits. They employ different mathematical concepts and computation techniques, e.g. linear programming [14], interval analysis [11], the idea

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of successive contraction, division and elimination of some hyperrectangular regions where the solutions are sought [17, 18, 20], the theory of monotonic operators [19], and the simplex method [25].

Recently several methods have been published which are capable of finding multiple DC operating points but do not guarantee finding all of them [5, 7, 10, 13, 15, 21–24]. They are less time consuming and do not require a high computing power. Consequently, more complex circuits can be analysed. In reference [21] the deflation concept is used to analyse circuits containing diodes and bipolar transistors having multiple DC operating points. In this paper the deflation technique is extended to CMOS circuits manufactured in nanometer technology.

CMOS electronic circuits fabricated in nanometer technology contain transistors characterised by very complicated DC models, PSP or BSIM 4. Each of the models is described by several hundred nonlinear equations. Consequently, the analysis of these circuits, even when there is a unique solution, is very time consuming and uncertain. This is why the programs based on the SPICE simulator offer sets of different methods rather than one method for DC analysis, enabling us to choose a new one when a tried method fails. For example, MicroCap 10 offers five basic methods: standard Newton–Raphson, source stepping, diagonal Gmin stepping, junction Gmin stepping, and pseudo transient. The methods and the order in which they are tried are user controllable. The program IsSPICE 4 offers three methods: standard Newton–Raphson, source stepping, and Gmin stepping. DC analysis is much more difficult and time consuming in the case of circuits having multiple operating points. Consequently, no simulator offers a systematic method in this area, and the problem is open.

The approach proposed in this paper employs a concept known in mathematics under the name deflation [3, 9]. The main idea of deflation is as follows. To find succeeding solution of an equation having multiple solutions, the equation is deformed in such a way that the earlier determined solutions are deflated out and a method capable of finding one solution is applied. To explain this technique we consider a nonlinear equation

$$\mathbf{f}(\mathbf{x}) = \mathbf{0}, \quad (1)$$

where $\mathbf{x} = [x_1 \cdots x_n]^T$, $\mathbf{f}(\mathbf{x}) = [f_1(\mathbf{x}) \cdots f_n(\mathbf{x})]^T$, $\mathbf{0} = [0 \cdots 0]^T$, where T denotes transpose.

Suppose that (1) has several solutions and one of them, labelled $\mathbf{r}^{(1)}$, has already been found. To determine other solution, (1) is deformed so that it retains the remaining solutions but avoids $\mathbf{r}^{(1)}$. In Ref. [3] the following deformation is proposed. Let $\mathbf{M}(\mathbf{x}, \mathbf{r}^{(1)})$ be an $n \times n$ matrix, called a deflation matrix, such that

$$\lim_{i \rightarrow \infty} \inf \|\mathbf{M}(\mathbf{x}^{(i)}, \mathbf{r}^{(1)})\mathbf{f}(\mathbf{x}^{(i)})\| > 0 \quad (2)$$

for any sequence $\mathbf{x}^{(i)}$ which tends to $\mathbf{r}^{(1)}$. We form the function

$$\mathbf{g}_1(\mathbf{x}) = \mathbf{M}(\mathbf{x}, \mathbf{r}^{(1)})\mathbf{f}(\mathbf{x}) \quad (3)$$

and solve the equation $\mathbf{g}_1(\mathbf{x}) = \mathbf{0}$ using an appropriate method for finding one solution. Certainly, $\mathbf{r}^{(1)}$ is not a solution of this equation and the sequence generated by

the method will converge to other solution. A simple deflation matrix [3] is

$$\mathbf{M}(\mathbf{x}, \mathbf{r}) = \frac{1}{\|\mathbf{x} - \mathbf{r}\|} \mathbf{C}, \tag{4}$$

where \mathbf{C} is an $n \times n$ nonsingular matrix. To deflate out several solutions $\mathbf{r}^{(1)}, \dots, \mathbf{r}^{(l)}$ the function

$$\mathbf{g}_l(\mathbf{x}) = \mathbf{M}(\mathbf{x}, \mathbf{r}^{(1)}) \cdots \mathbf{M}(\mathbf{x}, \mathbf{r}^{(l)}) \mathbf{f}(\mathbf{x}) \tag{5}$$

is created and equation $\mathbf{g}_l(\mathbf{x}) = \mathbf{0}$ solved.

Unfortunately, the described approach is not effective in DC analysis of electronic circuits. In this paper a new deflation technique is proposed and combined with the homotopy approach and the discrete circuit equivalent of the Newton–Raphson nodal analysis.

2 Preliminaries

Let us consider a DC circuit containing short channel MOS transistors, characterised by a PSP model [6, 8, 12, 16, 28]. Each power supply source is represented by a current source and a resistor connected in parallel; thus we will be able to apply the standard nodal method for the circuit description. To keep some matrices which will arise during the analysis well conditioned, we insert in the circuit the junction and the node-to-ground resistors having small conductances equal to 10^{-12}S . This is a standard approach commonly used in DC analysis of nonlinear circuits.

Let us consider an n -channel MOS transistor fabricated in nanometer technology. To characterise the transistor we use the PSP 103.1.1 model [8]. This model was chosen by the Compact Model Council, a gathering of more than 30 of the largest integrated manufacturers and electronic design automation vendors, as the standard. The PSP model is the most advanced MOSFET model incorporating the surface-potential-based approach and has been verified and used in circuit design for technology nodes from 250 to 32 nm [6]. We replace the transistor by three nonlinear voltage-controlled current sources as shown in Fig. 1.

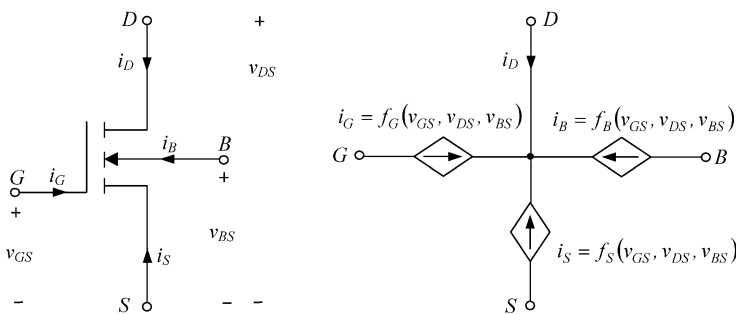


Fig. 1 A circuit model of NMOS transistor

Unfortunately, the functions f_G , f_B , and f_S are not given in any explicit analytical form. However, for given values of v_{GS} , v_{DS} , v_{BS} we can find i_G , i_B , and i_S handling several hundred nonlinear equations describing the PSP model. Also, the derivatives of these functions with respect to v_{GS} , v_{DS} , and v_{BS} can be calculated in a numerical way.

We replace all the MOS transistors by the model depicted in Fig. 1 and describe the circuit using the nodal method,

$$\mathbf{g}(\mathbf{v}) = \mathbf{0}, \quad (6)$$

where $\mathbf{v} = [v_1 \cdots v_n]^T$ is a vector consisting of the node voltages and $\mathbf{g}(\mathbf{v}) = [g_1(\mathbf{v}) \cdots g_n(\mathbf{v})]^T$ includes the functions $f_G(v_{GS}, v_{DS}, v_{BS})$, $f_B(v_{GS}, v_{DS}, v_{BS})$, and $f_S(v_{GS}, v_{DS}, v_{BS})$ of all the transistors, where voltages v_{GS} , v_{DS} , v_{BS} are expressed in terms of the node voltages. The fact that these functions are not given in explicit analytical form considerably complicates the analysis.

The first step of the proposed method for finding multiple DC operating points is finding one of them, which will be considered as the first operating point. For this purpose we use the Newton homotopy method [27] combined with the concept of the discrete circuit equivalent of the Newton–Raphson nodal analysis [4]. The Newton homotopy method sets up the equation with an additional variable λ , called a homotopy parameter,

$$\mathbf{h}(\mathbf{v}, \lambda) = \mathbf{g}(\mathbf{v}) + (\lambda - 1)\mathbf{g}(\mathbf{v}^{(0)}) = \mathbf{0}, \quad (7)$$

where $\mathbf{v}^{(0)} = [v_1^{(0)}, \dots, v_n^{(0)}]^T$ is an arbitrary point, and $\mathbf{h}(\mathbf{v}, \lambda) = [h_1(\mathbf{v}, \lambda) \cdots h_n(\mathbf{v}, \lambda)]^T$, where

$$h_i(\mathbf{v}, \lambda) = g_i(\mathbf{v}) + (\lambda - 1)g_i(\mathbf{v}^{(0)}), \quad i = 1, \dots, n. \quad (8)$$

The function $h_i(\mathbf{v}, \lambda)$ is interpreted as the algebraic sum of the currents flowing through all branches meeting at the i -th node and an additional current specified by the term $(\lambda - 1)g_i(\mathbf{v}^{(0)})$. This additional current can be represented by a current source connected between the i -th node and the reference node (ground).

The Newton–Raphson method for solving (7) at a given value of λ will exploit the associated linear resistive circuit at each iteration, called the Newton–Raphson discrete equivalent circuit [4], as follows. The nonlinear elements of the MOS transistor circuit are the voltage-controlled current sources shown in Fig. 1. Let us take into account one of them specified by $i_S = f_S(v_{GS}, v_{DS}, v_{BS})$. Using the main idea of the Newton–Raphson method, we form the equation which describes this element at the $(j + 1)$ -st iteration,

$$i_S^{(j+1)} = F_S + \Delta_{GS}^S v_{GS}^{(j+1)} + \Delta_{DS}^S v_{DS}^{(j+1)} + \Delta_{BS}^S v_{BS}^{(j+1)}, \quad (9)$$

where

$$\begin{aligned} \Delta_{GS}^S &= \frac{\partial f_S}{\partial v_{GS}}(v_{GS}^{(j)}, v_{DS}^{(j)}, v_{BS}^{(j)}), & \Delta_{DS}^S &= \frac{\partial f_S}{\partial v_{DS}}(v_{GS}^{(j)}, v_{DS}^{(j)}, v_{BS}^{(j)}), \\ \Delta_{BS}^S &= \frac{\partial f_S}{\partial v_{BS}}(v_{GS}^{(j)}, v_{DS}^{(j)}, v_{BS}^{(j)}), \end{aligned}$$

$$F_S = f_S(v_{GS}^{(j)}, v_{DS}^{(j)}, v_{BS}^{(j)}) - \Delta_{GS}^S v_{GS}^{(j)} - \Delta_{DS}^S v_{DS}^{(j)} - \Delta_{BS}^S v_{BS}^{(j)}.$$

Although the function $i_S = f_S(v_{GS}, v_{DS}, v_{BS})$ is not given in explicit analytical form, its value can be found for given values $v_{GS} = v_{GS}^{(j)}$, $v_{DS} = v_{DS}^{(j)}$, and $v_{BS} = v_{BS}^{(j)}$ using the PSP model with equations (4.1)–(4.219) presented in Sect. 4 of the PSP 103.1 documentation issued 04/2009 [8] as well as the equations given in Sect. 4 of the JUNCAP 2 documentation issued 04/2009 [8]. The derivatives $\partial f_S / \partial v_{GS}$, $\partial f_S / \partial v_{DS}$, and $\partial f_S / \partial v_{BS}$ at $v_{GS} = v_{GS}^{(j)}$, $v_{DS} = v_{DS}^{(j)}$, and $v_{BS} = v_{BS}^{(j)}$ can be found using a numerical approach.

Equation (9) describes a circuit, called a discrete model of the nonlinear voltage-controlled current source at the $(j + 1)$ -st iteration, associated with the Newton–Raphson method. Similarly we create discrete models at the $(j + 1)$ -st iteration of the nonlinear voltage-controlled current sources $i_G = f_G(v_{GS}, v_{DS}, v_{BS})$ and $i_B = f_B(v_{GS}, v_{DS}, v_{BS})$. In this way we form a discrete model of each of the transistors associated with the Newton–Raphson method at the $(j + 1)$ -st iteration and perform the iteration process to find a solution. Next we increase the parameter λ and repeat this approach until $\lambda = 1$. The solution at $\lambda = 1$, labelled $\mathbf{r}^{(1)}$, is the first operating point of the circuit.

3 Finding Multiple DC Operating Points

To determine other solutions of (6) (operating point) we propose a deflation technique, whose main idea will be explained using a simple example. Let us consider a single equation with a single variable $w(x) = 0$ having two solutions labelled $r^{(1)}$ and $r^{(2)}$. Suppose that the solution $r^{(1)}$ has already been found and we wish to find the solution $r^{(2)}$. For this purpose we propose a deflation technique which deforms the Newton–Raphson iteration formula rather than the equation as follows:

$$x^{(j+1)} = x^{(j)} - \frac{w(x^{(j)})}{p(|x^{(j)} - r^{(1)}|)w'(x^{(j)})}, \quad (10)$$

where $w' = dw/dx$, $|x^{(j)} - r^{(1)}| = \Delta_j$ is a distance between x at the j -th iteration and the solution $r^{(1)}$ which must be deflated out, $p(\Delta_j)$ is a nonlinear function

$$p(\Delta_j) = \begin{cases} \sin^N(\Omega \Delta_j), & \Delta_j < \delta, \\ 1, & \Delta_j \geq \delta, \end{cases} \quad (11)$$

where $\Omega = \frac{\pi}{2\delta}$ and δ is a preset constant, whereas $N = 4$.

Let the graph of the function $w(x)$ be as depicted in Fig. 2, where the initial guess $x^{(0)}$ and the assumed δ are also indicated. Since the distance Δ_0 between $x^{(0)}$ and $r^{(1)}$ is larger than δ , $p(\Delta_0) = 1$ and the iteration formula (10) becomes the standard Newton–Raphson formula. Consequently, we perform the standard Newton–Raphson iteration to find $x^{(1)}$. Similarly we find $x^{(2)}$. Figure 2 shows that $\Delta_2 = |x^{(2)} - r^{(1)}| < \delta$, hence, $p(\Delta_2) < 1$ and $p(|x^{(2)} - r^{(1)}|)w'(x^{(2)}) < w'(x^{(2)})$. Consequently, in order to perform the third iteration, at $x^{(2)}$ we do not use the tangent but the straight line having the slope smaller than $w'(x^{(2)})$, leading to $x^{(3)}$ as illustrated in Fig. 2. Since

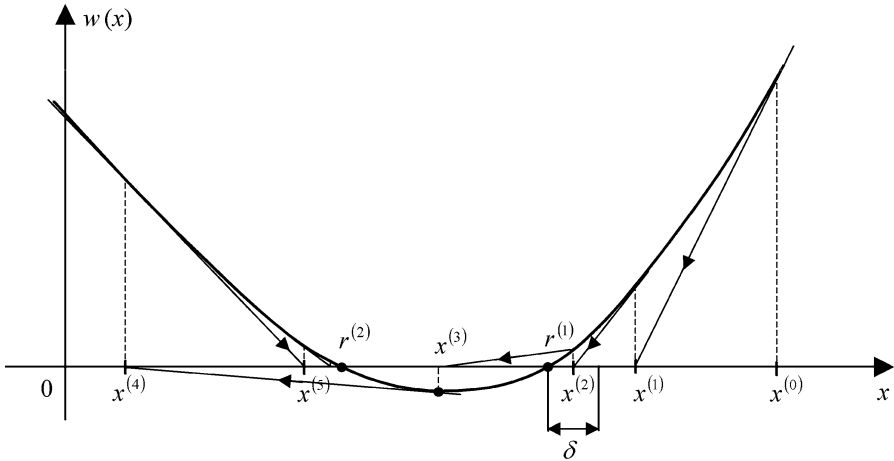


Fig. 2 Illustration of the proposed deflation technique

$\Delta_3 = |x^{(3)} - r^{(1)}| > \delta$, $p(\Delta_3) = 1$, and we carry out the standard Newton–Raphson iteration finding $x^{(4)}$ and then $x^{(5)}, x^{(6)}, \dots$, converging to $r^{(2)}$.

In a general case of the MOS circuits specified by (6) we apply the deflation technique, which deforms the Newton–Raphson method, to the discrete models of all voltage-controlled current sources associated with this method. As a result (9) is modified as follows:

$$i_S^{(j+1)} = F_S + p(\|\mathbf{v}^{(j)} - \mathbf{r}^{(1)}\|_2)(\Delta_{GS}^S v_{GS}^{(j+1)} + \Delta_{DS}^S v_{DS}^{(j+1)} + \Delta_{BS}^S v_{BS}^{(j+1)}), \quad (12)$$

$$F_S = f_S(v_{GS}^{(j)}, v_{DS}^{(j)}, v_{BS}^{(j)}) - p(\|\mathbf{v}^{(j)} - \mathbf{r}^{(1)}\|_2)(\Delta_{GS}^S v_{GS}^{(j)} + \Delta_{DS}^S v_{DS}^{(j)} + \Delta_{BS}^S v_{BS}^{(j)}), \quad (13)$$

where $\|\cdot\|_2$ is the Euclidean norm. Equations (12) and (13) describe a deflation discrete model that has the same structure as the model discussed in Sect. 2, but different parameters. All other discrete models are modified similarly. In this way the operating point $\mathbf{r}^{(1)}$ is deflated out and another operating point, labelled $\mathbf{r}^{(2)}$, is obtained. To deflate out several earlier determined solutions $\mathbf{r}^{(1)}, \mathbf{r}^{(2)}, \dots, \mathbf{r}^{(l)}$ we modify (9) in the following way:

$$i_S^{(j+1)} = F_S + (\min\{p(\|\mathbf{v}^{(j)} - \mathbf{r}^{(1)}\|_2), p(\|\mathbf{v}^{(j)} - \mathbf{r}^{(2)}\|_2), \dots, p(\|\mathbf{v}^{(j)} - \mathbf{r}^{(l)}\|_2)\}) \times (\Delta_{GS}^S v_{GS}^{(j+1)} + \Delta_{DS}^S v_{DS}^{(j+1)} + \Delta_{BS}^S v_{BS}^{(j+1)}), \quad (14)$$

$$F_S = f_S(v_{GS}^{(j)}, v_{DS}^{(j)}, v_{BS}^{(j)}) - (\min\{p(\|\mathbf{v}^{(j)} - \mathbf{r}^{(1)}\|_2), p(\|\mathbf{v}^{(j)} - \mathbf{r}^{(2)}\|_2), \dots, p(\|\mathbf{v}^{(j)} - \mathbf{r}^{(l)}\|_2)\}) \times (\Delta_{GS}^S v_{GS}^{(j)} + \Delta_{DS}^S v_{DS}^{(j)} + \Delta_{BS}^S v_{BS}^{(j)}) \quad (15)$$

and create the corresponding deflation discrete model.

Sketch of the Algorithm

1. Replace all MOS transistors by the circuit model shown in Fig. 1 and write the nodal equations. Set the required accuracy.
2. Find a DC operating point.
 - 2.1. Choose zero initial guess $\mathbf{v}^{(0)} = \mathbf{0}$ and $\lambda = \lambda_1 \in (0, 1)$, next create the current sources $(\lambda - 1)g_i(\mathbf{v}^{(0)})$ $i = 1, \dots, n$ and connect them between the nodes and the ground.
 - 2.2. Create the linear discrete models of the nonlinear controlled sources associated with the Newton–Raphson method for $j = 0$ and solve the linear circuit. Continue this process every time updating the model parameters until a convergent criterion is satisfied. In this way we obtain a solution labelled $\mathbf{z}^{(1)}$ of the homotopy equation at $\lambda = \lambda_1$.
 - 2.3. Choose $\lambda = \lambda_2 > \lambda_1$, update the sources $(\lambda - 1)g_i(\mathbf{v}^{(0)})$, assume the initial guess $\mathbf{z}^{(1)}$ and perform step 2.2. This procedure is repeated until $\lambda = 1$. The corresponding solution is the first operating point $\mathbf{r}^{(1)}$.
3. Find another operating point $\mathbf{r}^{(2)}$ by repeating step 2, using the deflation discrete models specified by (12)–(13) for i_S and similar formulas for the other controlled sources.
4. Repeat step 3 using the deflation discrete models specified by (14)–(15) with $l = 2$, enabling us to deflate out $\mathbf{r}^{(1)}$ and $\mathbf{r}^{(2)}$ and find operating point $\mathbf{r}^{(3)}$.
5. Perform step 4 for $l = 3, 4, \dots$ until no new solution is found in the preset number of iterations.

Note The parameters N and δ of function (11) were picked up on the basis of many numerical experiments. During these experiments different combinations of the numbers belonging to the sets $\tilde{N} = \{2, 3, 4, 5\}$ and $\tilde{\delta} = \{0.05, 0.1, 0.2\}$ were considered and 10 circuits of the class discussed in this paper were analysed. In any case the difference between the numbers of found and expected solutions as well as the CPU time were taken into account. Using the criterion of minimising the number of missed solutions and CPU time, the parameters $N = 4$ and $\delta = 0.1$ were selected and implemented in the computer program. For a fixed value of N , increasing δ may cause a solution to be missed, whereas decreasing δ makes the algorithm more time consuming.

4 Numerical Examples

The proposed algorithm has been implemented in Delphi and tested using numerous MOS circuits fabricated in nanometer technology. The calculations were executed using a PC with an Intel® Core (TM) i7-2600 processor. To illustrate the effectiveness of the algorithm, we consider three numerical examples. The results presented below are correct to three decimal places. To increase the accuracy more iterations of the Newton–Raphson method must be carried out.

Example 1 Let us consider the circuit shown in Fig. 3, based on the structures proposed in [2], containing 45 MOS transistors. The W and L values of the transistors

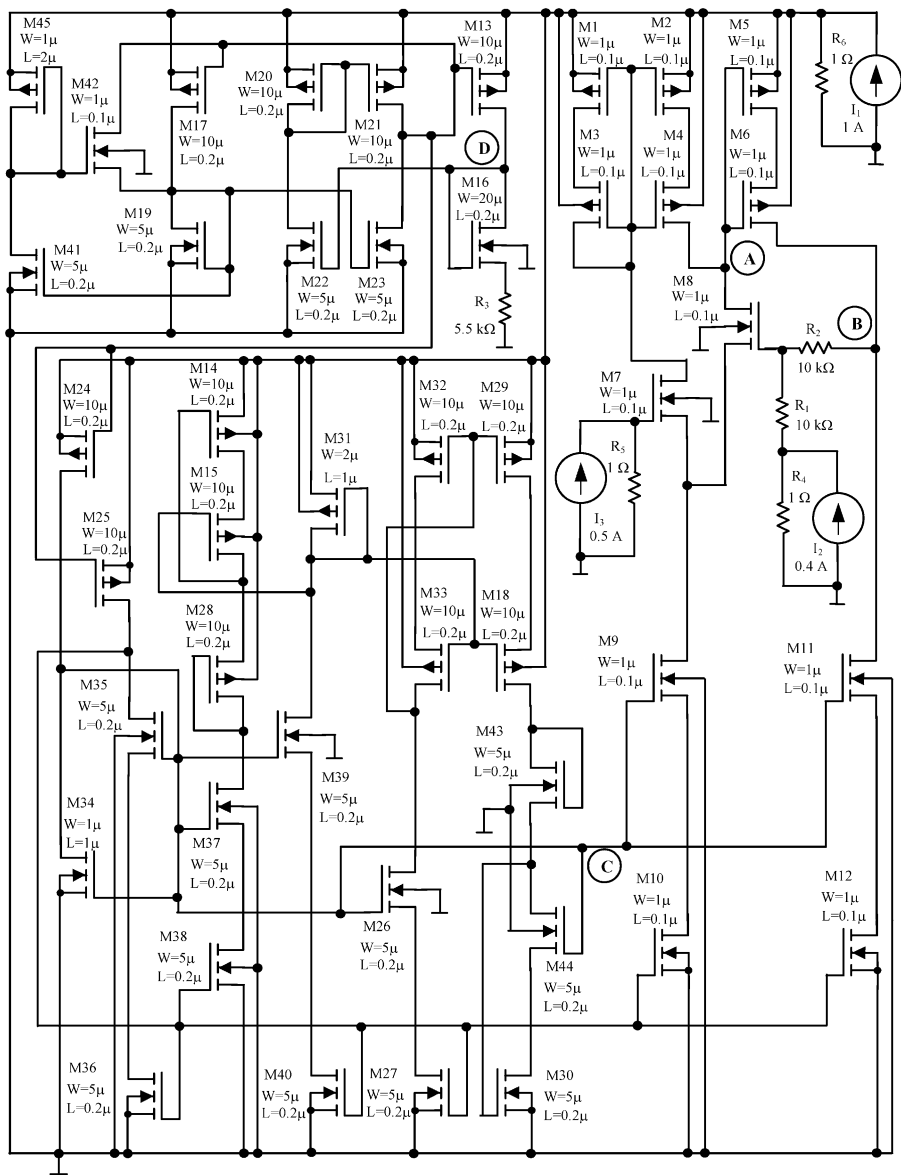


Fig. 3 Circuit containing 45 MOS transistors

are indicated in the figure. The proposed method leads to 3 operating points, as expected. The voltages corresponding to these operating points at four selected nodes (A, B, C, D) indicated in Fig. 3 are listed below:

$$\begin{aligned}
 v_A^{(1)} &= 0.300 \text{ V}, & v_A^{(2)} &= 0.996 \text{ V}, & v_A^{(3)} &= 0.525 \text{ V}, \\
 v_B^{(1)} &= 0.906 \text{ V}, & v_B^{(2)} &= 0.376 \text{ V}, & v_B^{(3)} &= 0.637 \text{ V},
 \end{aligned}$$

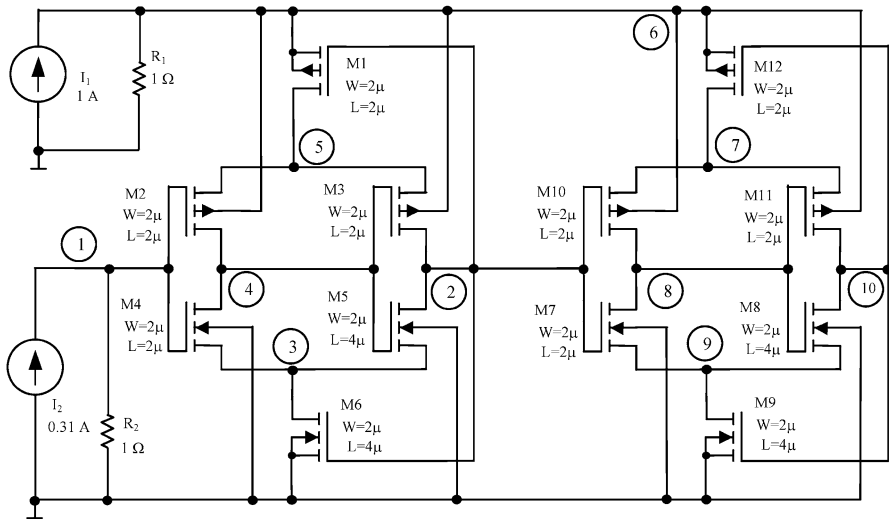


Fig. 4 Circuit containing 12 MOS transistors

$$\begin{aligned}
 v_C^{(1)} &= 0.339 \text{ V}, & v_C^{(2)} &= 0.339 \text{ V}, & v_C^{(3)} &= 0.339 \text{ V}, \\
 v_D^{(1)} &= 0.760 \text{ V}, & v_D^{(2)} &= 0.760 \text{ V}, & v_D^{(3)} &= 0.760 \text{ V}.
 \end{aligned}$$

The time consumed by the method is 27 s. During the computation process the algorithm exploits the deflation models specified by (12)–(13) or (14)–(15) 1056 times with $p(\|\cdot\|) < 1$.

Example 2 Let us consider the circuit shown in Fig. 4, which is a connection of two Schmitt’s triggers based on the structure proposed in [1], containing 12 MOS transistors. The W and L values of the transistors are indicated in the figure. The proposed method leads to 5 operating points, as expected. They are as follows:

$$\begin{aligned}
 v^{(1)} &= [0.310 \ 0.671 \ 0.014 \ 0.045 \ 0.671 \ 1.000 \ 0.841 \ 0.001 \ 0.000 \ 0.841]^T, \\
 v^{(2)} &= [0.310 \ 0.554 \ 0.052 \ 0.320 \ 0.713 \ 1.000 \ 0.786 \ 0.003 \ 0.002 \ 0.786]^T, \\
 v^{(3)} &= [0.310 \ 0.152 \ 0.152 \ 0.993 \ 0.997 \ 1.000 \ 1.000 \ 0.999 \ 0.076 \ 0.076]^T, \\
 v^{(4)} &= [0.310 \ 0.554 \ 0.052 \ 0.320 \ 0.713 \ 1.000 \ 0.968 \ 0.868 \ 0.280 \ 0.280]^T, \\
 v^{(5)} &= [0.310 \ 0.554 \ 0.052 \ 0.320 \ 0.713 \ 1.000 \ 0.934 \ 0.598 \ 0.272 \ 0.336]^T,
 \end{aligned}$$

where the elements of the vectors are the node voltages in volts.

The time consumed by the method is 8.47 s. During the computation process the algorithm exploits the deflation models 424 times.

Example 3 Let us consider the circuit shown in Fig. 5, based on the one proposed in [26], containing 15 MOS transistors. The W and L values of the transistors are

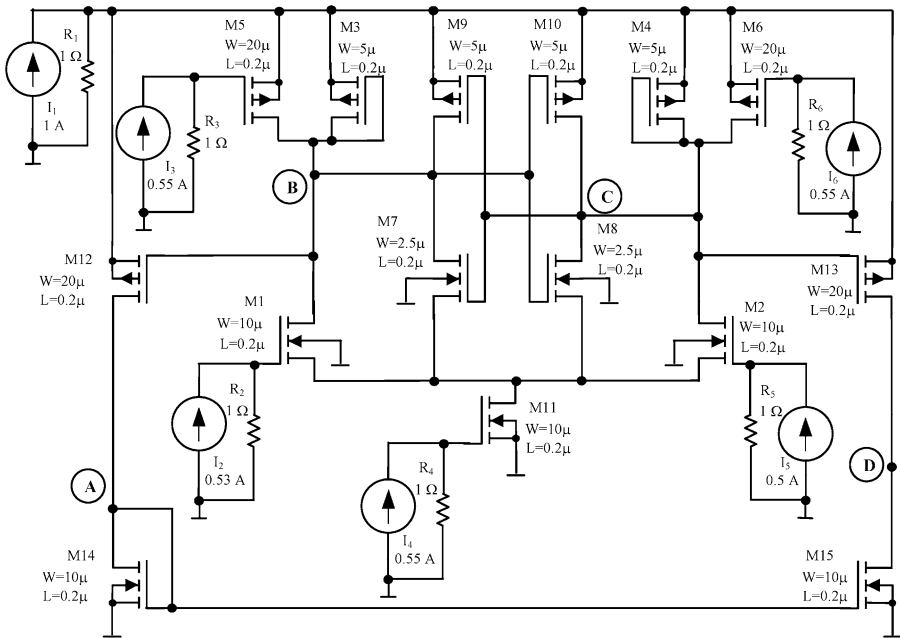


Fig. 5 Circuit containing 15 MOS transistors

indicated in the figure. The proposed method leads to 3 operating points, as expected. Voltages at four selected nodes (A, B, C, D) indicated in Fig. 5 are listed below:

$$\begin{aligned}
 v_A^{(1)} &= 0.545 \text{ V}, & v_A^{(2)} &= 0.050 \text{ V}, & v_A^{(3)} &= 0.288 \text{ V}, \\
 v_B^{(1)} &= 0.335 \text{ V}, & v_B^{(2)} &= 0.925 \text{ V}, & v_B^{(3)} &= 0.667 \text{ V}, \\
 v_C^{(1)} &= 0.948 \text{ V}, & v_C^{(2)} &= 0.376 \text{ V}, & v_C^{(3)} &= 0.547 \text{ V}, \\
 v_D^{(1)} &= 0.000 \text{ V}, & v_D^{(2)} &= 0.999 \text{ V}, & v_D^{(3)} &= 0.953 \text{ V}.
 \end{aligned}$$

The time consumed by the method is 7.96 s. During the computation process the algorithm exploits the deflation models 2423 times.

The CPU time and the circuit behaviour strongly depend on the applied MOS transistor model and also on the number of nodes and the number of solutions. For the intricate PSP model specified by more than 200 nonlinear equations the time of handling these equations during the computation process dominates the remaining time consumed by the algorithm. For example, the total time consumed by the method in Example 1 is 27 s, whereas the time of handling with the equations which describe the transistors is 26.12 s.

5 Discussion and Concluding Remarks

The proposed algorithm enables us to find multiple DC operating points of MOS circuits, fabricated in nanometer technology, using an intricate PSP transistor model. The following properties of the algorithm show its efficiency.

- (i) The developed method automatically searches for multiple operating points with no user intervention.
- (ii) Unlike many other algorithms for finding multiple DC operating points, the proposed one does not ask for the hybrid representation of the circuit.
- (iii) The algorithm works with original nonlinearities and does not require any piecewise linear approximation.
- (iv) The proposed algorithm does not guarantee finding all the DC operating points, although in 13 out of 14 analysed circuits the number of obtained operating points agrees with the expectation. However, since no existing method is capable of finding all the DC operating points in the discussed circuits or even evaluating their number, we are not clear about whether they can have some additional operating points. In just 1 out of 14 analysed circuits the proposed algorithm leads to 3 DC operating points, whereas the expected number is 5.
- (v) The proposed method can be directly adapted to the circuits including MOS transistors characterised by the BSIM 4.6 model.

Alternative methods, e.g. [5, 7, 24], which are potentially capable of finding multiple operating points using the PSP model need some preliminary manipulations or require specific user knowledge. These properties make them difficult to implement. The above-mentioned advantages of the proposed method show that it is a useful tool for finding multiple DC operating points of medium size, short channel CMOS circuits.

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